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# Sputter-etching of Heterogeneous Surfaces

Abstract: In conventional sputter etching, heterogeneous surfaces are eroded at generally unpredictable rates. The reasons for this are discussed and a solution to the problem is given: Based on control of redeposition, the technique involves the use of a device called a "catcher," which is placed near the target of the sputtering chamber to trap re-emitted particles. Experiments are described which confirm the effectiveness of the approach.

#### Introduction

The technique of rf sputter-etching[1] is now widely used. Its chief attraction is that it will cause the erosion of materials without regard to whether they are insulating or conducting. The rf sputter-etch rates for a wide range of different materials are relatively close (within a factor of 10) so that many of the restrictions associated with chemical etching are not apparent. Furthermore, the sharpness of the edge that is eroded away is limited only by the sharpness of the mask since no undercutting can take place. Masks of several conventional photoresist materials have been successfully used for this purpose.

To implement the technique, the substrate that is to be sputter-etched is made a part of the target of an rf sputtering system. Then, when the rf glow discharge is initiated, the entire target (including the substrate assembly) is eroded away at some rate dependent on a number of parameters such as rf power, gas pressure, etc. Most workers have found that it is good practice to make the body that is to be etched and the target on which it is placed of the same material, if possible, and relative rates for the sputter-etching of various materials have been measured [1] for such an arrangement.

Several workers have noted that when the surface to be sputter-etched consists of more than one material, particularly if each has a markedly different sputtering rate, the resultant rate for the erosion of the entire surface cannot be readily predicted[2]. Thus, to construct a hypothetical situation, if material A is known to sputter at a different rate from material B, and a pattern is prepared that consists of alternating lines of A and B, it will be found that neither A nor B etches at the relative

rates determined using surfaces of pure A and pure B. Further investigation would show that the actual rates observed depend on the type of pattern used as well as on the various sputtering parameters employed. The purpose of this paper is to present an explanation of this phenomenon and to indicate how it can be avoided.

### Discussion

It is now firmly established that during rf sputtering a significant fraction of the deposited material is re-emitted during the entire sputtering cycle[3]. The exact amount of this re-emission is a complex function of the relative areas of the target, the substrate assembly, and the chamber walls as well as of the rf and dc coupling between these respective surfaces[4]. This re-emission can have several causes, the principal ones being:

- Resputtering of the deposited material as the result of bombardment by energetic ions from the discharge [4];
- 2) resputtering due to bombardment by energetic neutrals present in the sputtering gas[3-5];
- resputtering due to energetic negative ions which originate at the target surface and are accelerated across the Crookes dark space[4]; and
- 4) thermal re-emission[6].

It has been found that even if re-emission due to mechanism 1 is largely eliminated (by seeing to it that no significant potential difference exists between the depositing film and the rf plasma), re-emission due to the other three causes is still generally around 30%[3]. Thus, in any rf sputter-etching system, it is possible that as much as 30%

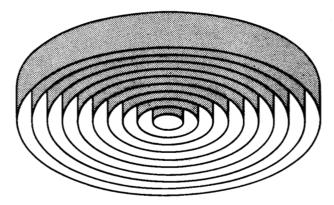
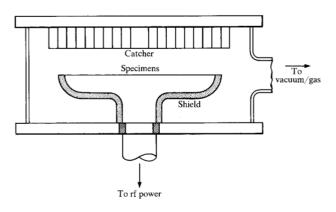


Figure 1 Sketch of the catcher. The backside is a flat plate.

Figure 2 Sketch of sputtering chamber showing position and relative size of catcher.



of the material that leaves the surface being etched eventually returns to it. This cannot be prevented by sputtering at high pressure since any back-diffusion which is sufficient to hinder the return of material from the walls will be even more effective in causing the return of material to the target itself.

Thus, if a surface of low sputtering yield is present in the midst of a sea of material of relatively high sputtering yield, zero net removal of this surface may occur since, in an extreme case, material B will be depositing onto A at a greater rate than A can be removed. The exact net removal rate of regions A and B will be a complicated function of a number of factors including the relative areas of A and B and the relative sputtering yields of A and B. This is further complicated by the fact that a layer of a high sputtering yield material deposited onto one of low sputtering yield tends to have an even higher sputtering yield than normal, the converse also being true [7]. Additional factors that may play a role include the effects of simple back diffusion at relatively high pressure (in excess of about 20  $\mu$ m)[8] and possible focusing effects.

For example, if the chamber bell-jar is curved it may act as a concave mirror, concentrating material towards the center of the target.

#### Suppression of re-emission

To eliminate the effects described above, it was necessary to develop a method for completely suppressing reemission. This was done by the adaptation of a technique used for the measurement of the re-emission coefficient[6]. Essentially, the method consisted of measuring the impingement rate (as opposed to the deposition rate) through the modification of an approach first developed by Devienne[9]. It was found that a cylindrical receptacle of relatively deep aspect ratio acts towards the sputtered particles in a manner analogous to that of a black body in that any material entering it has a low probability of escaping from it again, independent of whatever reemission processes may be operating.

To suppress re-emission on a large scale, a "catcher" plate was developed which consisted of a series of concentric cylinders. The walls of the latter were as thin as possible and a ratio of at least 3:1 between the height of the rings and separation between successive rings was maintained. This is illustrated diagramatically in Fig. 1, and relative size and location of the device are shown in Fig. 2. By placing such a catcher plate relatively close to the surface that was being sputter-etched (so as to block off potential contamination by material from the walls of the chamber) and by sputtering at as low a pressure as is possible (so as to minimize return of material through back diffusion), the amount of redeposition during sputter-etching was greatly reduced.

## Confirmation of catcher effectiveness

Even if the material or surface being etched is of uniform composition, it may contain contaminants whose continuous return to the surface being etched would be highly undesirable. For example, consider the sputter-etching of the oxide surfaces of a semiconductor device. It is well known that such an oxide may be contaminated by sodium ions that will subsequently induce instabilities in a semiconductor device protected in this fashion. Removal of the sodium ions through sputter-etching of the oxide would thus be desirable. However, if a fraction of the sodium ions is always returned to the oxide surface that is being etched, it will not be possible to remove entirely this source of contamination.

The useful properties of the catcher element were demonstrated in an experiment that employed a very sensitive parameter (the surface potential of silicon) to detect improvements associated with its presence. Four silicon wafers of 8  $\Omega$ -cm resistivity were oxidized at 1000°C in a furnace containing pure oxygen at one atmosphere pressure; a coating of SiO<sub>2</sub> having a thickness of 1000Å

Table 1 Effect of catcher on flat-band charge density.

Sample	Initial $N_{\rm FB}$ (× $10^{11}/cm^2$ )	$N_{\rm FB}$ after stress* $(\times 10^{11}/cm^2)$	$( imes 10^{11}/cm^2)$	Comments
$1) \operatorname{SiO}_2 + \operatorname{Si}_3 \mathbf{N}_4$	1.4	4.0	2.6	No PSG, no catcher
$2) \operatorname{SiO}_{2}(+\operatorname{PSG}) + \operatorname{Si}_{3}\operatorname{N}_{4}$	2.0	3.9	1.9	No catcher
3) $SiO_2(+PSG) + Si_3N_4$	0.8	1.6	0.8	Catcher
4) $SiO_2(+PSG) + Si_3N_4$	0.8	1.7	0.9	Catcher

was formed. Sample 1 was used as a control. Samples 2, 3 and 4 received 250Å of phosphosilicate glass (PSG) which was deposited by exposing the wafers to POCl<sub>3</sub> heated to 850°C. The resultant phosphosilicate glass was then removed from wafer 2 by sputter-etching in a conventional sputter-etching apparatus (no catcher). The phosphosilicate glass on wafers 3 and 4 was removed in a sputter-etching apparatus provided with a catcher. Immediately following the removal of the glass layer, silicon nitride was deposited by reactive sputtering of a silicon target in nitrogen. Aluminum electrodes were then evaporated onto the surface of the resulting silicon nitride layer by means of an electron beam.

The capacitance of such a metal-insulator-silicon (MIS) structure is a function of the dc voltage across the insulator. The capacitance-voltage curve goes through a minimum value when the silicon forms a depletion layer whose capacitance is in series with that of the insulator. This occurs when the sum of the applied dc voltage and any charge in the insulator  $Q_{\rm ins}$  is just sufficient to deplete the silicon of majority carriers near the silicon-insulator interface. Closely associated with this minimum is the "flat-band" condition[10]; the dc voltage at which this occurs is called the flat-band voltage  $V_{\rm FB}$ . Since  $V_{\rm FB}$  is a function of the charge, if any, in the insulator, any changes in the amount of that charge  $Q_{\rm ins}$  causes a change in  $V_{\rm FB}$ , To determine the "flat-band charge density"  $N_{\rm FB}$  associated with  $V_{\rm FB}$ , one uses the equation

$$qN_{\rm FB} = C_{\rm ins} V_{\rm FB}$$

where  $C_{\rm ins}$  is the capacitance of the insulator and q is the electronic charge. A measure of the stability of an MIS structure is given by the magnitude of  $\Delta N_{\rm FB}$ , the change in  $N_{\rm FB}$  due to electrical/thermal stress. This change can be due to the drift of ionic charge in the insulator, polarization, charge trapping at the Si-insulator interface etc. A common cause is alkali ion drift[11]. For the experiment described above, the results are given in Table 1.

The instability of the semiconductor surface potential in this series of runs is directly related to the amount of contamination reintroduced during the sputter etching of the phosphosilicate glass layers in runs 2, 3 and 4. Wafer 2 shows the effect of gettering Na<sup>+</sup> with PSG, which was removed by sputter etching without a catcher element. The improvement, i.e., the decrement in  $\Delta N_{\rm FB}$ , is evident. Wafers 3 and 4 show the improvement after sputter etching the PSG with the catcher in place.

Table 1 shows very clearly the effect of including a catcher element in the sputter etching apparatus. The reduction in  $\Delta N_{\rm FB}$  in wafers 3 and 4 as compared to wafer 2 is due to a permanent reduction in contaminant deposition occurring when the PSG layer was removed by sputter etching.

Another experiment was performed to demonstrate the validity of the catcher concept. A film of Cr was sputtered off a substrate and the amount of Cr deposited on a blank substrate positioned nearby in the same run was determined. Cr was chosen because of the sensitivity of detection by x-ray fluorescence. The experiment consisted of evaporating 500 Å of Cr onto glass substrates  $(8 \times 3 \text{ cm})$ . Two such substrates were placed on the pedestal, alternating with two blank substrates from the same package. The Cr was then removed by sputter etching at 300 watts rf power and 6  $\mu$ m Ar gas for 15 minutes, long enough to remove all the Cr. The blank substrates were then examined by x-ray fluorescence to determine the amount of Cr transferred to them. This experiment, performed with and without the catcher, gave the results shown in Table 2. The concentration of Cr is expressed as the equivalent thickness of a uniform layer. The reproducability of measurements on a substrate was  $\pm 1$  Å, and counts were obtained at a number of areas on each substrate. The results indicate that less Cr is transferred from the original to the blank substrates when the catcher is installed. Also, the outer blanks (numbered 1) pick up less Cr than the inner ones (numbered 3). The small amount of material that is transferred, even in the

Table 2 Effect of catcher on redeposition of sputter-etched Cr.

Sample	Cr thickness (Å)
Blank 1:	
with catcher	4
no catcher	$7 \pm 1$
Blank 3:	
with catcher	5
no catcher	$17 \pm 1$
Average:	
with catcher	4.5
no catcher	12
Control	$1 \pm 1$

presence of a catcher, is accounted for by back-diffusion of material to the target plane[8].

# Acknowledgments

The authors thank D. Stenabaugh and R. G. Simmons for designing and building the catcher plate and related rf etching equipment, as well as A. R. Baker, Jr. who performed the evaluation of the MIS structures.

#### References

- 1. P. D. Davidse, J. Electrochem. Soc. 116, 100 (1969).
- 2. J. D. Vossen and J. J. O'Neill, Jr., RCA Review 29, 149 (1968).
- 3. R. E. Jones, C. L. Standley and L. I. Maissel, J. Appl. Phys. 38, 4656 (1967).
- 4. H. R. Koenig and L. I. Maissel, IBM J. Res. Develop. 14, 168 (1970).
- 5. H. F. Winters and E. Kay, J. Appl. Phys. 38, 3928 (1967).
- 6. L. I. Maissel, R. E. Jones and C. L. Standley, IBM J. Res. Develop. 14, 176 (1970).
- G. K. Wehner, private communication.
  J. L. Vossen, J. J. O'Neill, K. M. Finlayson and L. J. Royer, RCA Review 31, 293 (1970).
- 9. C. R. Devienne, Compt. Rend. 234, 80 (1952).
- 10. A. S. Grove, B. E. Deal, E. H. Snow and C. T. Sah, Solid State Electronics 8, 145 (1965).
- 11. W. A. Pliskin, D. R. Kerr and J. A. Perri; "Thin Glass Films", *Physics of Thin Films*, *Vol. IV*, Academic Press, New York 1967.

Received December 10, 1970 Revised August 6, 1971

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