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Cross-coupled Thyristor Storage Cell

Abstract: A symmetrical, cross-coupled, two-thyristor storage cell with 1 μW stand-by power dissipation and 60 nsec switching time is described. When integrated in silicon planar technology each thyristor consists of a vertical npn transistor and a lateral pnp transistor.

Symbols

α_0	dc transistor current gain
α_{npn}	npn-transistor current gain
α_{npnI}	Inverse npn-transistor current gain
α_{pnp}	pnp-transistor current gain
α_{pnpI}	Inverse pnp-transistor current gain
α_{sub_1}, α_{sub_2}	Current gain substrate transistor $p_1n_1p_{sub}$, $p_2n_1p_{sub}$
C_1, C_2, C_3	Capacitance related to junction J_1, J_2, J_3
C_j	Junction capacitance
C_{j0}	Zero-volt junction capacitance
C_d	Diffusion capacitance
D_p, D_n	Diffusion constants
I	Emitter current (ac plus dc)
I_A	Cell anode current
I_B	Bit line current
I_c	Effective current charging C_2
I_d	Effective current discharging C_2
I_E	dc emitter current
I_s	Junction saturation current
I_{sub}	Cell substrate current
I_w	Word line current
J_1, J_2, J_3, J_{sub}	Thyristor junctions
K	Ratio of base diffusion impurity concentration of emitter to that of collector
n_1, n_2, p_1, p_2	Thyristor semiconductor regions
R_i	Word-driver impedance
r_b	Thyristor base resistance effective in cell
s	Laplace operator
t_c	Cell center junction charging time
t_d	Cell center junction discharging time
t_s	Cell switching time
t_r	Cell READ delay time
τ_B	Transistor base transient time
τ_d	Diffusion capacitance time constant
τ_α	Current source delay
U_A	Anode voltage
U_D	Junction contact voltage
U_1, U_2, U_3	Thyristor junction voltage
$\lvert\hat{U}_2\rvert$	Center junction stand-by steady-state voltage
U_T	Temperature voltage kT/e
U_w	Word-driver voltage
W	Transistor base width

Introduction

Semiconductor cells for monolithic memories are generally characterized by small size, small power dissipation and simple structure suitable for integration with conventional techniques. The silicon planar technology for bipolar transistors is well established and offers the advantage of low-impedance, high-current READ/WRITE operation.

The conventional bistable cell consists basically of two cross-coupled vertical npn transistors and two load resistors, usually with high standby power dissipation. Bistable circuits with a single pair of complementary bipolar transistors have also been described [1, 2]. One characteristic of these circuits is the thyristor-like ON-OFF characteristic. Unfortunately thyristor-like circuits can be switched by voltage spikes on the power supply lines. Proposals have been made to solve this rate-effect problem, for example, by coupling two thyristors at the anode and cathode [3].

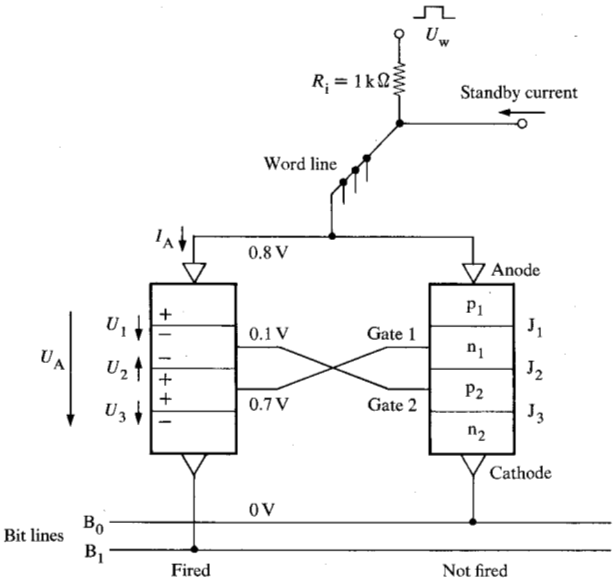


Figure 1 Cross-coupled thyristor cell schematic.

In this paper a new kind of coupling between two thyristors forming one cell [4] is described. It is a cross-coupling of the two inner layers of each thyristor resulting in stable *and* fast operation. Moreover, it is shown how the standby power dissipation can be kept extremely small. Structure and operation of an integrated cell are described.

Cell structure and basic function

The cell as shown schematically in Fig. 1 consists of two thyristors [5, 6, 7], one of which is in the ON state, the other in the OFF state. Since the gates of the thyristors are cross-coupled, the junction voltages of the conducting thyristor block off the nonconducting thyristor. The voltages in Fig. 1 are given as an example to explain the cell operation.

When integrated into a storage array the cell is located at the intersection of a word line with two complementary bit lines. A severe problem with normal single-thyristor operation is the rate effect, by which the device in the OFF state can be fired by a steep anode voltage slope. This rate effect is caused by capacitive currents flowing through the device junctions which bias the two emitter junctions p_1n_1 and p_2n_2 in forward direction (Fig. 1). These junctions emit minority carriers and thus start the firing mechanism.

With the cross-coupled cell the emitter junctions p_1n_1 and p_2n_2 of the OFF thyristor are back-biased by the junctions of the ON thyristor and therefore heavily blocked. Moreover, the ON device practically clamps the cell voltage (i.e., the OFF device anode voltage). Therefore the cell is considerably less sensitive to voltage slopes or spikes than is a single thyristor [3, 8].

Another advantage of the cross-coupling is that during cell switching the thyristor that was previously on is switched off very quickly by the active discharge of its junctions (not by carrier recombination, as with single-thyristor operation) [2, 9].

Each thyristor consists of an npn transistor and a pnp transistor [10, 11]. The minimum current for cell bistability is approximately given by the condition that the sum of current gains of the pnp and npn transistors is $\alpha_{pnp} + \alpha_{npn} > 1$ (see Appendix A), implying that the cell standby current, then, must exceed the thyristor holding current. Both current gains, α_{npn} and α_{pnp}, decrease with decreasing current [12, 13], so the holding current cannot be infinitely small. Furthermore, in practical semiconductor fabrication the current gains strongly depend on the quality of the semiconductor processing. However, holding currents below 10 nA can well be obtained and therefore the cell can be operated with a standby current in the 1-μA range.

With higher junction temperature the current gains increase and the cell stability is thus increased. The temperature dependence of the thyristor *U–I* characteristic is uncritical since the cell current is stabilized by an external current source.

The cell is selected in a storage array by driving a word line and a pair of bit lines. As an example, a voltage U_w is applied to the word line via an impedance R_i = 1 kΩ (Fig. 1). Simultaneously the standby current of the total chip is switched off. The unselected cells hold their switching states capacitively during the selection interval. This capacitive information storage is inherent to the two-thyristor cell since there is no external ohmic conductance for discharging the junction capacitances. After the actual selection phase the cell information is regenerated.

Control of the selected pair of bit lines is different for READ and WRITE. During READ operation both bit lines of the selected pair (and *only* of the selected pair) are switched to ground potential by the sense amplifier/bit driver. Consequently a current can flow from the word line through the selected cell into one of the bit lines according to the stored information. The sense current is in the order of 1 mA. No other cell yields a substantial current because the unselected word lines are switched off and the unselected pairs of bit lines are at higher potential.

For a WRITE operation, i.e., for cell switching, one of the bit lines of the selected pair is grounded. To the other bit line a positive pulse of 1 V is applied. Now again a current of about 1 mA can flow from the word line through the selected cell into the grounded bit line.

The grounded thyristor is fired and the ungrounded thyristor is switched off.

The cell operates at two power levels, a low level in the standby state and a higher level for fast READ or WRITE. The standby current is common to the whole word or even to the whole array. The standby currents of the individual cells are unequal, since a separate load resistor inside each cell is eliminated to reduce cell size. The current-sharing factor depends on the thyristor *U–I* characteristic and its tracking at the chip level (provided there is a stable current source at the chip level). Analysis shows that the tracking of the thyristor *U–I* curve will be within 59 mV (Appendix C). Since the thyristor *U–I* curve is similar to a normal diode characteristic the current sharing will be up to a factor of 7.2. Thus with a nominal cell standby current of 1 μA the cell current may vary between 0.37 μA and 2.7 μA.

The standby state is stable when the cell current exceeds a thyristor holding current of less than 10 nA. There is then a sufficient noise tolerance.

Process technology

The thyristor cell is fabricated by the conventional silicon planar technology with n-epitaxy and double diffusion [10, 14]. The pnpn layer sequence consists of a normal npn transistor and an additional laterally structured p-layer.

Figure 2(a) shows the thyristor semiconductor cross-section with the lateral $p_1n_1p_2$ transistor and the normal vertical $n_2p_2n_1$ transistor. The p_1 and p_2 layers are diffused simultaneously by a single base diffusion step. The cell layout shown in Fig. 2(b) is designed for integration in a storage array. The photograph Fig. 2(c) shows the fabricated cell array after metal etching.

Table 1 presents some data on the npn and pnp transistors obtained with the semiconductor geometry and impurity concentrations given in Fig. 2, with

$$\tau_{B_{pnp}} = \frac{W^2}{2D_p} \qquad D_p = 6.6 \text{ cm sec}^{-2} \qquad (1)$$

$$\tau_{B_{npn}} = \frac{W^2}{2D_n} \qquad D_n = 10 \text{ cm sec}^{-2} \qquad (2)$$

The values D_p and D_n are the diffusion constants determined by the actual carrier concentration.

The base transient times are calculated with the simplifying assumption of a uniformly doped base. The current gains are measured figures.

The lateral current gain α_{pnp} is one of the key thyristor parameters. It can be increased considerably by a circular geometry and by a lower epitaxial impurity concentration [12, 13].

Since the recombination rate in the pnp transistor base should be small, no gold doping is applied. Thereby the

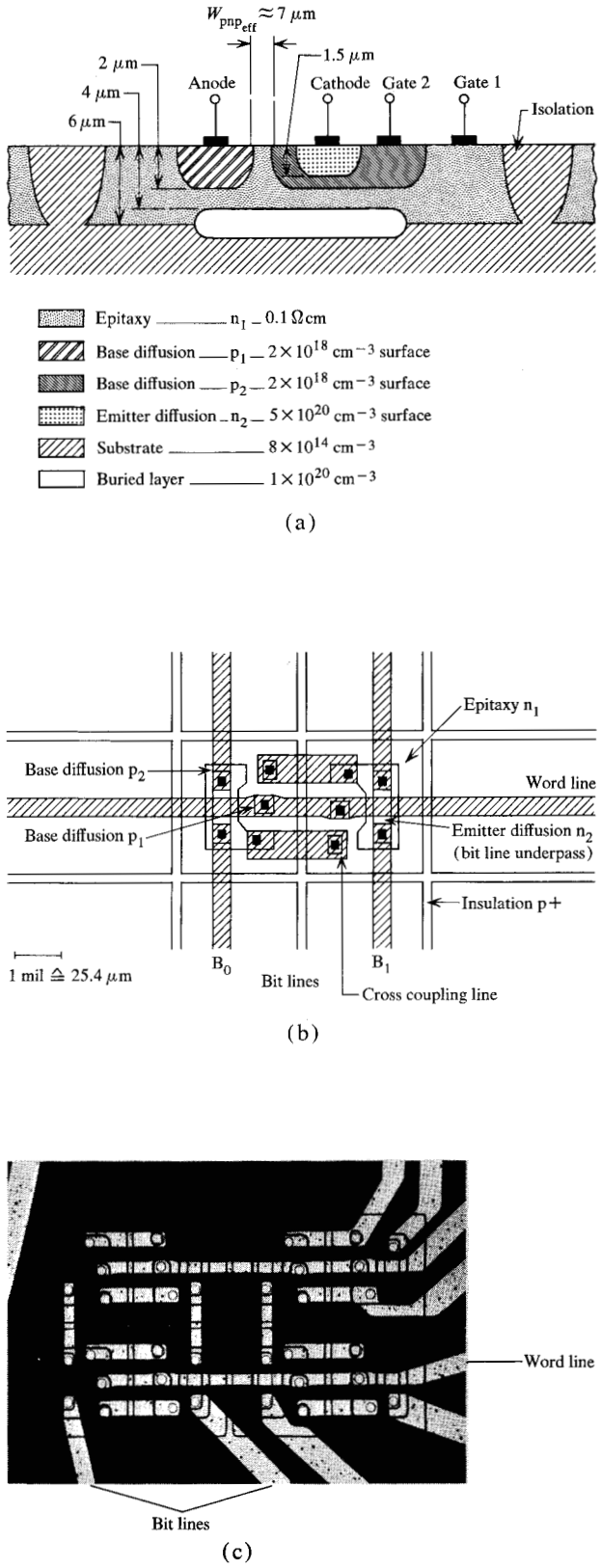
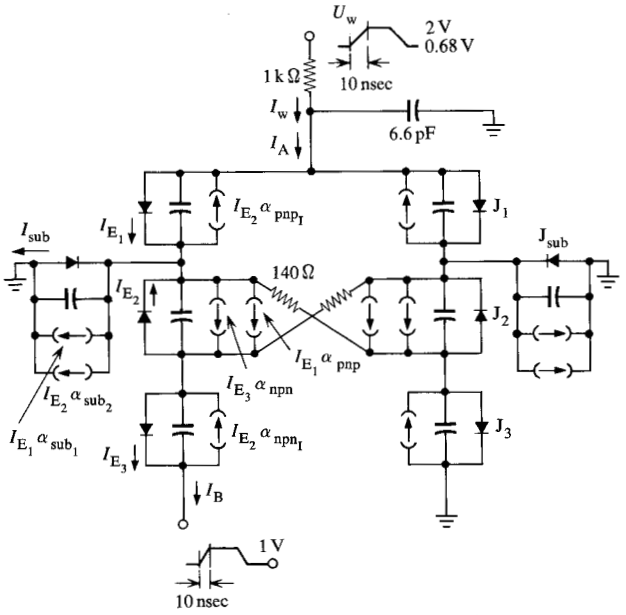


Figure 2 The thyristor cell. (a) Thyristor semiconductor cross section; (b) cell layout; (c) photograph of fabricated 4-cell array.

Table 1 Comparative data for W, α, and τ_B for npn and pnp transistors [Fig. 2(a)].

Parameter	*npn transistor*	*pnp transistor*
Effective base width W	0.5 μm	7 μm
Current gain α	0.96 to 0.99	0.33 to 0.42
Base transient time τ_B	0.13 nsec	37 nsec

Figure 3 Thyristor cell equivalent circuit.



current gains α_{sub} of the parasitic substrate transistors $p_1n_1p_{sub}$ and $p_2n_1p_{sub}$ remain large, in the order of 0.4 and 0.2. The buried layer [14] prevents α_{sub} from being even higher. About 60% of the dc thyristor anode current goes into the substrate. With the dimensions used here, the substrate transistor is mainly lateral and is formed by the p-insulation frames. The vertical substrate transistor effect is nearly eliminated by the buried layer.

Transient behavior

The thyristor cell is operated dynamically during WRITE, READ and half-selection disturb. During the WRITE operation the cell switches into the other stable state. With both READ and WRITE operations the cell current is increased from about 1 μA to about 1 mA to obtain a good performance. The transients are evaluated with an appropriate large signal equivalent circuit and compared with measurements. Since all voltages remain sufficiently small the carrier multiplication effect [15, 16] is negligible.

Lumped-cell equivalent circuit

The equivalent circuit used matches the specifications of the so-called TLCAP program (Transmission Line and Circuit Analysis Program). The program has a topological input of lumped element networks. Nonlinear elements as functions of time, voltage or currents are inserted in the form of tables or analytic functions. The three-dimensional and distributed nature of the semiconductor structure is simulated by a crude one-dimensional model of lumped elements.

The thyristor consists basically of the three junctions J_1, J_2, J_3. An additional junction which, however, is always negative-biased, is the substrate junction J_{sub}. The dc junction currents are obtained by superposition of all junction emitter currents and collector currents [6]. Extending this model to the transient behavior, we get the thyristor cell equivalent circuit in Fig. 3. So each junction is represented by a diode, a capacitance C and one or two current sources in parallel [17, 18]:

a) The diode is equivalent to the dc characteristic of the junction emitter current:

$$I_E = I_s\left[\exp\left(\frac{U}{U_T}\right) - 1\right], \tag{3}$$

where I_E is the junction dc emitter current, I_s is the saturation current and U_T the temperature voltage. The parameters in Eq. (3) and in the following equations are measured or calculated and listed in Table 2 and Table 3.

b) The capacitance C consists of a junction capacitance and a diffusion capacitance,

$$C = C_j + C_d. \tag{4}$$

Both capacitances are voltage dependent. Simplifying the voltage dependence of the junction capacitance to that of the step junction we get for $U < 1/2\,|U_D|$:

$$C_j = C_{j0}\left(\frac{|U_D|}{|U_D| - U}\right)^{\frac{1}{2}} \tag{5}$$

where U_D is the contact potential.

c) The current sources represent the collector currents injected from adjacent junctions.

The diffusion capacitance represents the minority carrier charge. As there are several collectors belonging to one emitter the corresponding different diffusion capacitances must be summed:

$$C_d = \sum \tau_{di}\frac{I_{Ei}}{U_T}. \tag{6}$$

Splitting of the emitter currents at the junctions J_1 and J_2 is sketched in Fig. 9. In the case of a uniform base the transient times τ_{di} are approximated [17]:

$$\tau_d = \tfrac{2}{3}\tau_B = \frac{W^2}{3D} \tag{7}$$

The inserted numerical figures are given in Appendix B.

The current sources in Fig. 3 are defined as αI_E, where:

α_{pnp}	:	J_1 emits, J_2 collects
α_{pnpI}	:	J_2 emits, J_1 collects
α_{npn}	:	J_3 emits, J_2 collects
α_{npnI}	:	J_2 emits, J_3 collects
α_{sub_1}	:	J_1 emits, J_{sub} collects
α_{sub_2}	:	J_2 emits, J_{sub} collects.

The current gains α are measured and plotted vs corresponding emitter currents in Fig. 4.

Since the base width of the pnp transistor is large the delay of the current gains α_{pnp} must be taken into account. Roughly it is

$$\alpha \approx \alpha_0 \frac{1}{(1 + s\tau_\alpha)}, \tag{8}$$

where s is the Laplace operator, α_0 is the dc current gain and τ_α the current source delay of the equivalent circuit. For uniform base we have [14, 17]:

$$\tau_\alpha = \frac{1}{6}\frac{W^2}{D} \tag{9a}$$

$$\tau_B = \tau_\alpha + \tau_d . \tag{9b}$$

Note that with Eq. (8), and according to the equivalent circuit in Fig. 3, the current gain α is related to the dc emitter current.

The resistor $r_b = 140\ \Omega$ in Fig. 3 represents the sum of the pnp and npn transistor base resistors.

The capacitance 6.6 pF at the anode is the word line capacitance due to the experimental set.

Measurement of transients

For verification of the computed cell transients, oscillograms of the READ and WRITE operation are taken on the actually fabricated device. The parameter measurements previously mentioned are also taken on this device, which is part of the integrated array shown in Fig. 2(c).

WRITE operation

The cell state is characterized by the charges in the cell junction capacitances, in particular by the charge or voltage polarity of the center capacitances C_2. Cell switching changes the polarity of the voltage U_2 at C_2.

Switching is performed with a positive word pulse at the anode and a coincident positive bit pulse at the cathode of the left thyristor, which is assumed to be in the ON state. Thus the left thyristor current is interrupted. The switching time is defined to lie between the 10% point of the drive pulse voltage U_w and the 90% point of the word line current I_w as illustrated in Fig. 6(a). This definition yields about the same switching time as the polarity change of voltage U_2 but simplifies measurements.

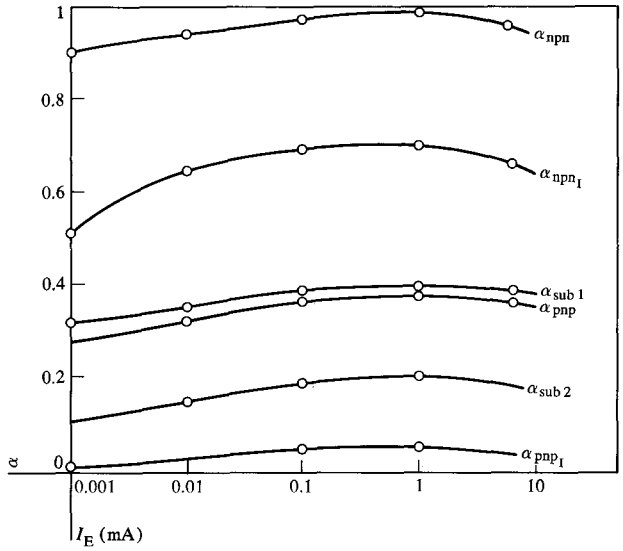
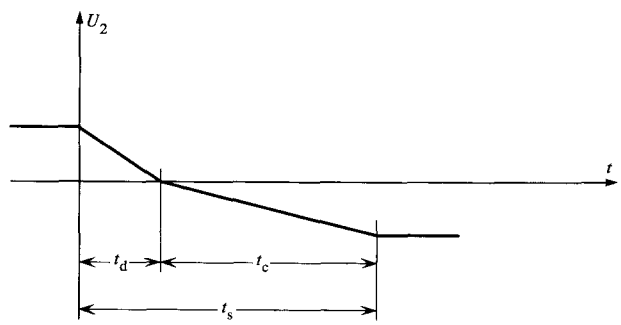


Figure 4 DC current gain vs emitter current I_E.

Figure 5 Center voltage U_2 during switching.

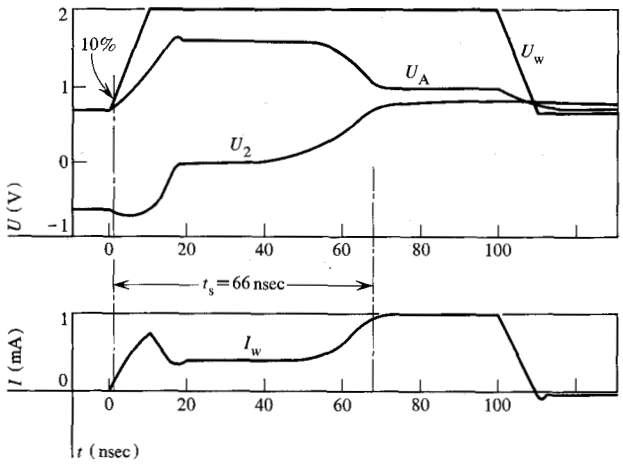


Switching can be explained by dividing the switching time t_s into a discharging time t_d and a charging time t_c, as sketched in Fig. 5. During t_d, the cell current transverses the left p_1n_1 junction of the initially conducting thyristor, the cross-connection and the right p_2n_2 junction. The current discharging the capacitance C_2 of both thyristors is the difference between the current of the left and right current sources:

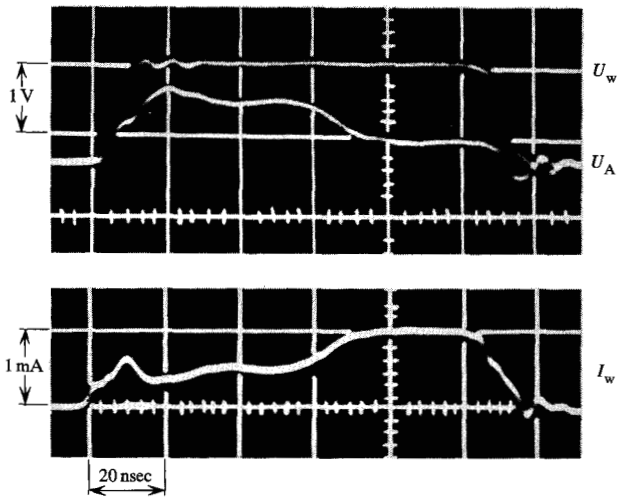
$$I_d = I_E(\alpha_{npn} - \alpha_{pnp}). \tag{10}$$

α_{npn} and α_{pnp} are, as represented by Eq. (8) and Fig. 4, functions of time and current. The capacitance C_2 is a function of current or of voltage, respectively. For a rough estimate of t_d a simple relation can be found when neglecting the rest of the capacitances and inverse and substrate transistor currents and setting $I_E = I_A$:

$$t_d \approx \frac{2C_2\,|\hat{U}_2|}{I_A(\alpha_{npn} - \alpha_{pnp})}. \tag{11}$$



(a)



(b)

Figure 6 The WRITE transients. (a) Computed cell WRITE transients with parameters in Table 2 and Table 3; (b) measured cell WRITE transients.

$\hat{U}_2$ is the steady standby state center junction voltage. The capacitance C_2 in Eq. (11) can be approximated by the small junction capacitance. The value t_d is relatively small since α_{pnp} is much smaller than α_{npn} and since α_{pnp} starts with a large delay.

As the voltage across the center junction decreases to zero, the cell current is gradually taken over by the right p_1n_1 junction. When $U_2 = 0$ the dc emitter currents through both upper junctions are equal.

The charging time t_c is determined by the thyristor current feedback mechanism. The current difference

$$I_c = I_E(\alpha_{npn} + \alpha_{pnp} - 1) \tag{12}$$

charges the center junction capacitances. The value t_c can be estimated by an approximation similar to Eq. (11):

$$t_c \approx \frac{2C_2\,|\hat{U}_2|}{I_A(\alpha_{npn} + \alpha_{pnp} - 1)}. \tag{13}$$

The value t_c is relatively large (Fig. 6) since the effective charging current I_c is very small during the delay time of the current source $\alpha_{pnp}I_A$.

Equations (11) and (13) are useful for estimating the basic influence of parameters on the switching time t_s. More accurate evaluations, however, are based on TLCAP computations. The computed transients are plotted in Figs. 6(a) and 8(a), with the input parameters as presented in Table 2, Table 3 and in Fig. 4. U_w is the driving word pulse, U_A the cell voltage and I_w the word line current (cell current I_A plus current through word line capacitance of 6.6 pF). As shown in Fig. 1 and Fig. 3,

$$U_A = U_1 - U_2 + U_3 \tag{14}$$

and

$$I_A = \frac{U_w - U_A}{R_i}, \tag{15}$$

where U_1, U_2, U_3 are the voltages across the junctions of the ON thyristor. The word-driver parameters $U_w = 2$ V and $R_i = 1$ kΩ are chosen to operate similarly to normal storage array application. If I_w were supplied by a current source and therefore were constant at 1 mA, the switching time would, of course, be much smaller.

In Fig. 6(a) the first spike of I_w is due to the capacitances. The cell voltage U_A has a maximum according to Eq. (14) when the center voltage U_2 runs through zero. Figure 6(b) shows the measured transients of the experimental cell, of which the data and the driving conditions are equal to the computed cell. The center voltage U_2 could not be measured adequately, but the measured and computed transients U_A and I_w are in good agreement. The measured switching time is $t_s = 67$ nsec.

The switching time is computed for a more careful investigation of parameter influence than that of Eqs. (11) and (13). The most critical parameters varied are α_{sub_1}, α_{sub_2}, α_{pnp} and the delay parameters of the lateral transistors. All other parameters, according to Tables 2 and 3, are the same for all computer runs. The computed switching time is plotted in Fig. 7 versus the normalized lateral delay parameters $(\tau/\tau_n)_{lat}$. The ratios $(\tau/\tau_n)_{lat} = \frac{2}{3}$ and $\frac{1}{3}$ respectively in Fig. 7 represent the reduction of the actual figures listed in Table 2 and Table 3 of all lateral delays τ_{d_1}, τ_{d_2}, $\tau_{\alpha_{pnp}}$ and $\tau_{\alpha_{sub}}$ to $\frac{2}{3}$ and $\frac{1}{3}$ respectively. The switching time t_s increases considerably with the lateral delays, as expected. Moreover, t_s decreases with increasing α_{pnp}, since t_c decreases and since the increasing t_d remains sufficiently smaller than t_c. The influence of α_{sub} on t_s is small for a given α_{pnp}, because during the

discharging time t_d the dc substrate current is very small owing to the current source delay and because during the charging time t_c the effect of α_{sub} on the effective charging current is also small. This is analogous to the effect of α_{sub} on the dc current I_{E_2}, as is explained in Appendix A.

The temperature dependence of the WRITE time is estimated to be relatively small. Strongly temperature-dependent factors, α_{pnp} and α_{sub}, partly neutralize each other (Fig. 7). However, more detailed analysis should be applied to this question.

READ operation

During the READ operation a word pulse increases the cell current from nominally 1 μA to 1 mA. The current flows from the word line to one of the common bit sense lines. The bit line current I_B is the cell current I_A minus the substrate current I_{sub}.

In Fig. 8(a) the computed transients of the READ operation are plotted versus time. Note that the center junction voltage U_2 first decreases below its standby value and then increases to the powered value, owing to the delay of the α_{pn}-current source. Even when U_2 decreases to almost zero (under conditions which far exceed normal operation) no loss of information could be observed. The READ operation is nondestructive and regenerates the state of the cell.

Figure 8(a) shows that the pseudo-steady-state is not reached before about 100 nsec after word pulse rise. However, the access time of information is very much shorter.

The substrate current has the largest delay. As long as I_{sub} is zero or small, the bit line current I_B is nearly equal to the cell current I_A, so that I_B can quickly rise. The READ delay t_r, defined to be between the 50% point of the word pulse U_w and 50% of the maximum bit line current, is as short as if α_{sub} were zero. The value $t_r = 5$ nsec is computed. Figure 8(b) shows the corresponding oscillograms with $t_r \approx 5$ nsec. Measured and computed transients are in fair agreement.

The computed READ delay t_r changes only within a few percent, if the parameters are varied as in Fig. 7.

Half-selection disturb

In the storage array the cell is switched by a coincident bit- and word-pulse. The cells half-selected by the bit line pulse are disturbed. However, the center-junction capacitances are discharged only slightly by the capacitive currents caused by the bit pulse, as TLCAP simulations demonstrate. Between two consecutive half-selection operations the cell regenerates. After many consecutive half-selection disturbs, the characteristic center junction voltage decreases to a saturated value which, however, is uncritical for cell stability.

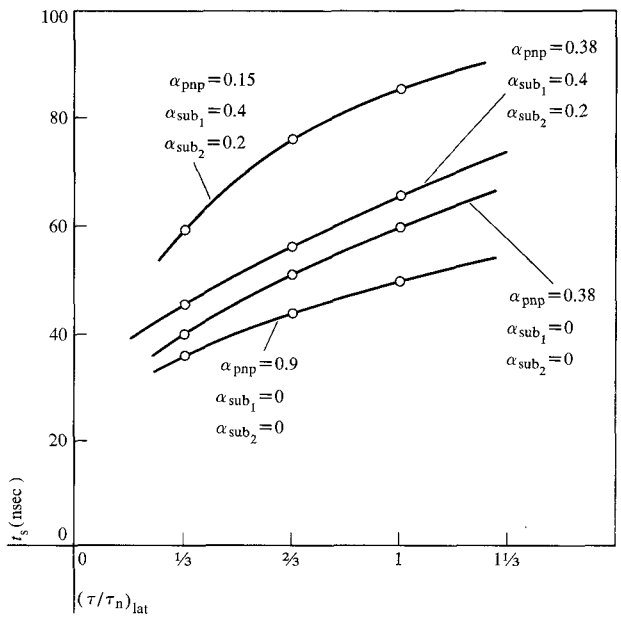
Table 2 Parameters, Eqs. (3) to (8).

	I_s *in* 10^{-15} *A*	U_T *in mV*	U_D *in V*	C_{j0} *in pF*	τ_d *in nsec*
Junction J_1	4.6	30	0.94	0.09	26
J_2	13.5	30	0.94	0.57	12.5
J_3	13.5	30	1.02	0.60	0.04
J_{sub}		30	0.70	0.81	

Table 3 Parameters, Eq. (8) and Fig. 4.

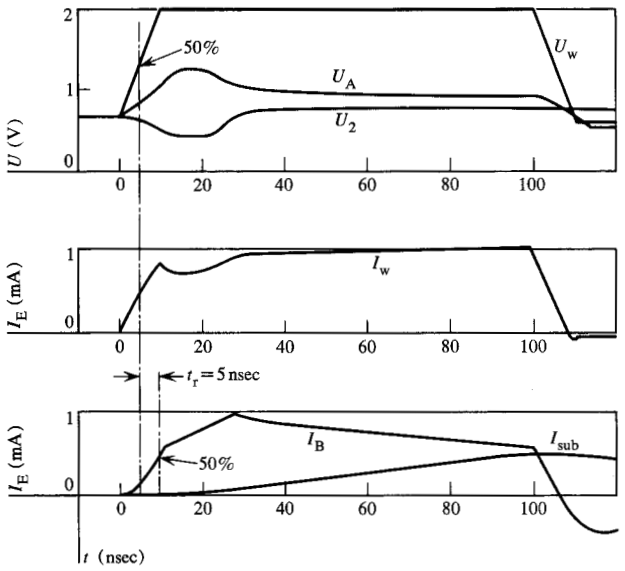
	α *at 1 mA*	τ_α *in nsec*
α_{pnp}	0.38	12.3
α_{pnpI}	0.04	12.3
α_{npn}	0.98	0.04
α_{npnI}	0.68	0.04
α_{sub1}	0.40	18.5
α_{sub2}	0.20	18.5

Figure 7 Computed switching time vs normalized delays $(\tau/\tau_n)_{lat}$ of the lateral transistors.



Conclusion

The flipflop with two cross-coupled thyristors is very suitable for integration in a monolithic storage because of small semiconductor area of 16 mil^2 (0.01 mm^2), simple structure with single-layer metallization, low standby power dissipation of 1 μW, lack of rate effect, and reasonable WRITE time of 60 nsec and short READ delay time of 5 nsec.



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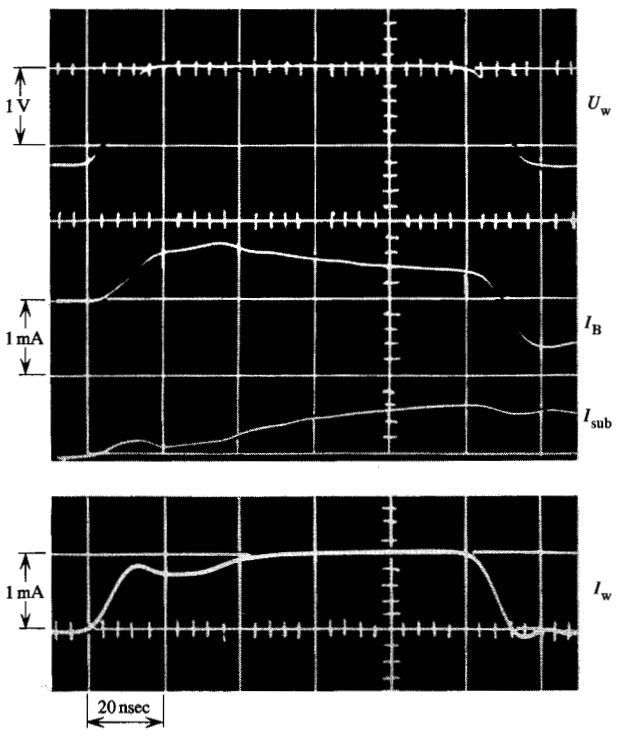

(b)

Figure 8 The READ transients. (a) Computed cell READ transients; (b) measured cell READ transients.

The performance can be improved by decreasing the semiconductor dimensions. The cell simulation used for computation is rather crude but yields a good insight into cell switching behavior and fair agreement with measurements.

Acknowledgments

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Appendix A. Calculation of I_{E_2}

The dc current I_{E_2} through the center junction is calculated based on the equivalent circuit Fig. 3:

$$I_{E_1} - I_{E_2}\alpha_{pnp_1} = I_A \tag{A1}$$

$$I_{E_1}(\alpha_{pnp} + \alpha_{sub_1}) - I_{E_2}(1 - \alpha_{sub_2}) + I_{E_3}\alpha_{npn} = I_A \tag{A2}$$

$$I_{E_1}\alpha_{pnp} - I_{E_2}(1 - \alpha_{npn_1}) - I_{E_3}(1 - \alpha_{npn}) = 0. \tag{A3}$$

This system of algebraic equations results in:

$$I_{E_2} = I_A[\alpha_{pnp} + \alpha_{npn} - 1 + \alpha_{sub_1}(1 - \alpha_{npn})] / [1 + \alpha_{pnpI}(\alpha_{npn}\alpha_{sub_1} - \alpha_{pnp} - \alpha_{sub_1}) - \alpha_{sub_2}(1 - \alpha_{npn}) - \alpha_{npn}\alpha_{npnI}]. \tag{A4}$$

The condition for the thyristor holding current ($I_{E_2} \geq 0$) is

$$\alpha_{pnp} + \alpha_{npn} + \alpha_{sub_1}(1 - \alpha_{npn}) \geq 1. \tag{A5}$$

The value α_{sub_1} increases the holding current slightly. I_{E_2} and therewith the substrate current $I_{sub} = I_{E_1}\alpha_{sub_1} + I_{E_2}\alpha_{sub_2}$ are strongly increased by α_{npnI}.

Appendix B. Calculation of effective diffusion capacitances

The diffusion capacitance generally is

$$C_d = \tau_d \frac{J_E}{U_T}, \tag{B1}$$

where the delay parameter τ are calculated according to Ref. 14, p. 73. Since with junctions J_1 and J_2 we have to split up the diffusion capacitance C_d into partial capacitances, the diffusion capacitance is:

$$C_d = \sum C_{di} = \frac{1}{U_T} \sum \tau_{di} I_{Ei}. \tag{B2}$$

The diffusion capacitances represent the charge of minority carriers in regions I to IV, Fig. 9. The emitter currents I_E of junctions J_1, J_2 and J_3 consist of holes and electrons that contribute as minority carriers to the total charge. The emitter current splitting factors are measured and indicated in Fig. 9. For instance, the emitter current I_E in junction J_1 consists of

47% holes emitted from p_1 area towards isolation (into region I),
38% holes emitted from p_1 area towards p_2 layer (into region II),

15% electrons emitted from n_1 layer into p_2 layer (into region III).

The emitter current of junction J_3 is practically an electron current and can be considered quite conventionally without splitting.

For a uniform base there is, according to Ref. 14,

$$\tau_d = \frac{W^2}{3D}. \tag{B3}$$

For a graded p-diffused base with the impurity concentration decreasing towards the collecting junction the approximation in Ref. 14, p. 73 is in a simplified form:

$$\tau_d = \frac{W^2}{[3 + (\frac{1}{2}\ln K)^2 + \frac{3}{2}\ln K]D_n}, \tag{B4}$$

where K is the ratio of the base impurity concentration of emitter to that of collector.

For a graded p-diffused base with the impurity concentration increasing towards the collecting junction the corresponding approximation of Ref. 14 is in a simplified form:

$$\tau_d = \frac{W^2[1 + \frac{3}{2}(L_p/W)]}{[3 + (\frac{1}{2}\ln K)^2 - \frac{3}{2}\ln K + 3(W/L_p)]D_n}, \tag{B5}$$

where L_p is the diffusion length of holes.

Thus the diffusion capacitance of the p_1n_1 junction J_1 is:

$$C_{d_1} = \frac{I_E}{U_T}\left[0.47\frac{W_I^2}{3D_p} + 0.38\frac{W_{II}^2}{3D_p} + 0.15\frac{W_{III}^2}{3D_n}\right]. \tag{B6}$$

With $W_I \approx 8.5\ \mu m$, $W_{II} \approx 7\ \mu m$, $W_{III} \approx 2\ \mu m$, $D_p \approx 6.6\ cm^2/sec$, $D_n \approx 10\ cm^2/sec$, Eq. (B6) yields:

$$C_{d_1} = \frac{I_E}{U_T}\tau_{d_1}; \qquad \tau_{d_1} = 26\ \text{nsec}.$$

The diffusion capacitance of the p_2n_1-junction J_2 is:

$$C_{d_2} = \frac{I_{E_2}}{U_T}\left[0.28\frac{W_I^2}{3D_p} + 0.04\frac{W_{II}^2}{3D_p} + 0.68\frac{W_{IV}^2[1 + \frac{3}{2}(L_p/W_{IV})]}{[3 + (\frac{1}{2}\ln K)^2 - \frac{3}{2}\ln K + 3(W_{IV}/L_p)]D_n}\right]. \tag{B7}$$

The diffusion length L_p of the holes which are emitted from the p_2 area towards the buried layer area can be estimated by the assumption that most of the holes recombine within the most heavily doped part of the buried layer. In Eq. (B7) $L_p \approx 4\ \mu m$ is inserted. With $K \approx 5$ and $W_{IV} \approx 0.5\ \mu m$, the above equation yields

$$C_{D_2} = \frac{I_E}{U_T}\tau_{d_2}; \qquad \tau_{d_2} = 12.5\ \text{nsec}.$$

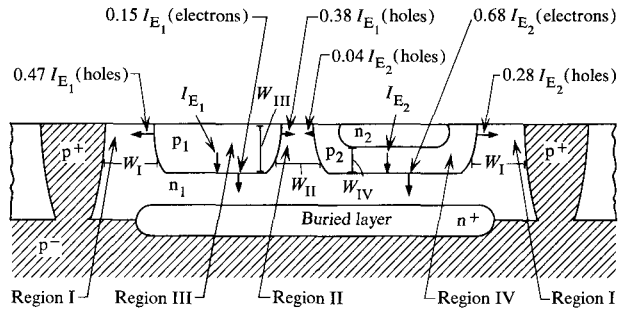

Figure 9 Scheme of current components in the thyristor cross-section.

The diffusion capacitance of the p_2n_2-junction J_3 is:

$$C_{d_3} = \frac{I_{E_3}}{U_T}\frac{W_{IV}^2}{[3 + (\frac{1}{2}\ln K)^2 + \frac{3}{2}\ln K]D_n} = \frac{I_{E_3}}{U_T}\tau_{d_3} \quad \text{with} \quad \tau_{d_3} = 0.04\ \text{nsec}. \tag{B8}$$

The calculation of τ_α, the delay of the current gains, is performed in a similar manner based on Ref. 14, p. 73.

Appendix C. Analysis of thyristor ON-voltage

In this simplified analysis the spread of the thyristor ON-voltage U_A on chip level for standby operation is shown.

Simplifying assumptions (symbols according to Fig. 3):

npn-transistor current gain $\alpha_{npn} \approx 1$;
Inverse pnp-transistor current gain $\alpha_{pnpI} \approx 0$.

Then the three junction dc emitter currents are:

$$I_{E_1} \approx I_A, \tag{C1}$$

$$I_{E_2} \approx I_A\frac{\alpha_{pnp}}{1 - \alpha_{npnI}}, \tag{C2}$$

$$I_{E_3} \approx I_A(1 - \alpha_{pnp} - \alpha_{sub_1}) + I_{E_2}(\alpha_{npnI} - \alpha_{sub_2}). \tag{C3}$$

The voltage U_A is, according to Fig. 1,

$$U_A = U_1 - U_2 + U_3 = f(I_{E_1}) - f(I_{E_2}) + f(I_{E_3}). \tag{C4}$$

For analysis of the spread of U_A on chip level the following assumptions are made:

Spread (tracking) of junction voltages U_1, U_2, U_3: ± 5 mV,
Spread (tracking) of current gains β_{pnp}, β_{npn}, β_{npnI}, β_{sub_1}, β_{sub_2}: $\pm 20\%$.

The spread of U_A is, with $U_T = 30$ mV,

$$\Delta U_A = U_{A\,max} - U_{A\,min} = 3 \times 10\text{mV} + U_T \ln\frac{(I_{E_2}I_{E_3})_{max}}{(I_{E_2}I_{E_3})_{min}} = 59.1\text{mV}. \tag{C5}$$

Assuming a normal diode characteristic for $U_A = f(I_A)$ (with $U_T = 30$ mV), the current sharing factor $I_{A\,max}/I_{A\,min}$ of the different cell standby currents on an array chip is 7.2.

References and notes

1. M. A. Nicolet, "Complementary Transistor Flipflop Circuits," *IEEE Trans. Circuit Theory* **CT-10,** 534–537 (1963).
2. R. Greiller, "Steuerbare Vierschicht-Halbleiter und ihre Verwendung als Binärspeicher," *Elektronische Rechenanlagen* **7,** H.6, 293 (1965).
3. R. A. Stasior, "How to Suppress Rate Effect in PNPN-Devices," *Electronics,* **37,** No. 2, 30 (1964).
4. W. Jutzi and C. Schuenemann, "Ein symmetrisches bistabiles Thyristor-Flip Flop," Tagungsbericht der 3. *Mikroelektronik-Tagung* (INEA), Munich, R. Oldenbourg, Munich 1968, p. 278.
5. M. C. Gantry, et al., *Semiconductor Controlled Rectifiers,* Prentice-Hall, Inc., Englewood Cliffs, N. J., 1964.
6. J. L. Moll, M. Tanenbaum, J. M. Goldey and N. Holonyak, "P-N-P-N. Transistor Switches," *Proceedings of the IRE* **44,** 1174 (1965).
7. W. Gerlach and F. Seid, "Wirkungsweise der steuerbaren Siliziumzelle," *Electrotechnische Zeitschrift-A* **8,** 270 (1962).
8. L. L. Rosier, C. Turrel and W. K. Liebmann, "Semiconductor Crosspoints," *IBM J. Res. and Develop.* **13,** No. 4, 439 (1969).
9. R. Shively, "A Silicon Monolithic Memory Utilizing a New Storage Element," *AFIPS Conference Proceedings,* **27,** Part I, 637 (1965).
10. W. Kapallo, E. Rocher, "The ON-Characteristics of Planar-SCR's with Regard to the Use of these Devices in Monolithic Circuits," *Solid State Electronics,* **11,** 437 (1968).
11. E. Y. Rocher and R. E. Reynier, "Response Time of Thyristors: Theoretical Study and Application to Electronic Switching Networks," *IBM J. Res. and Develop.,* **13,** No. 4, 447 (July 1969).
12. E. S. Yang and N. C. Voulgaris, "On the Variation of Small Signal Alphas of a PNPN Device with Current," *Solid State Electronics,* **10,** 641–648, Pergamon Press, London, 1967.
13. D. E. Fulkerson, "A Two-Dimensional Model for the Calculation of Common-Emitter Current Gains of Lateral PNP-Transistors," *Solid State Electronics,* **11,** 821 (1968).
14. C. S. Meyer, O. K. Lynn, et al., "Integrated Circuits" and "Analysis and Design of Integrated Circuits," *Motorola Series in Solid State Electronics,* McGraw-Hill Book Company, New York, 1965.
15. A. A. Lebedev and A. I. Uvarov, "Theory of the Switching Process in a PNPN-Structure," *Soviet Physics-Semiconductors,* **1,** No. 2, 167 (1967).
16. R. L. Davies and S. Petruzella, "PNPN Charge Dynamics," *Proc. IEEE,* **55,** No. 8, 1318–1330 (August 1967).
17. Hauri Bachmann, *Grundlagen und Anwendungen der Transistoren,* Generaldirektion PTT, Abteilung Forschung, Bern 1962.
18. R. Paul, *Transistoren, physikalische Grundlagen und Eigenschaften,* Friedrich Vieweg und Sohn, 1965.

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