H. N. Ghosh
A. S. Oberai
J. J. Chang
M. B. Vora

An Arsenic Emitter Structure for High-Performance Silicon Transistors

Abstract: Arsenic-doped emitters have been shown to produce high performance in bipolar silicon transistors. In comparison with phosphorus, the emitter dopant commonly used in the industry, the use of arsenic results in a steeper gradient (10^{24}/cm^4), less compensation of the base region, no "emitter dip" effect, and a flatter profile with higher sheet conductivity. Since arsenic atoms are a better match to Si than are phosphorus atoms and the arsenic process requires lower surface concentration for a particular diffusion depth and sheet conductivity, fewer crystal defects are generated. As a result the arsenic emitter process results in a higher device yield and is much more reproducible, even for shallow diffusion depths. Arsenic-emitter transistors, both with and without gold doping, are found to be superior in performance, with 1.6 to 2 times higher gain bandwidth, f_T and current gain, β, than those with phosphorus emitters with similar geometry. Also the ability of the arsenic emitter to sustain large current densities, exceeding 30,000 A-cm^{-2}, makes it extremely desirable for high density, small geometry, and high-performance silicon devices.

Introduction

Progress in photolithography in the last decade has brought about higher component density on semiconductor chips by permitting smaller dimensions in the geometry of transistors and diodes. Reaching the goal of high density and high performance in circuits has been assisted by the companion development of thin epitaxial growth and shallow diffusions. In such technology, phosphorus has been commonly used as the dopant for the emitter region of the npn transistor. However, the demand for increasingly high density, high performance, and high yield places continually increasing importance on the following requirements:

1) Small geometry, which implies that the device will carry a high current density at operating current levels. It has been shown [1] that to prevent performance degradation, such as fall-off of current gain β or gain bandwidth f_T at high injection density, sharp emitter impurity profiles with a high gradient at the junction will be required.
2) Narrow basewidth with high total integrated base doping to provide a high collector-to-emitter punch-through voltage and low base resistance.
3) Control of basewidth within very narrow dimensions.
4) Reasonably long diffusion time so that the emitter process will be reproducible. A companion requirement on diffusion temperature is that solid solubility at that temperature be higher than the required surface concentration.
5) A low density of diffusion-induced defects, such as dislocations, precipitation, etc., which occur at very high concentration and produce yield losses due to junction leakage and collector-to-emitter breakdown.

In this and other papers in this issue, we shall attempt to demonstrate that the phosphorus emitter has some undesirable limitations when the requirements above are stringently imposed. Such objectives are much better realized by forming the emitter region by arsenic diffusion. The arsenic emitter process, by which the devices under discussion in this paper have been fabricated, is a closed-tube capsule diffusion process. However, the same conclusions will apply to other methods of diffusion such as from a doped-oxide source [2] or similar open-tube process.

Arsenic vs phosphorus emitter

Diffusivity

At a given temperature, arsenic diffusivity has been found to be much more concentration-dependent than phosphorus. As shown in the paper by Chiu and Ghosh [3], over a temperature range of 950 to 1200°C and a concentration range of 10^{19} to 3×10^{20} cm^{-3}, arsenic diffu-

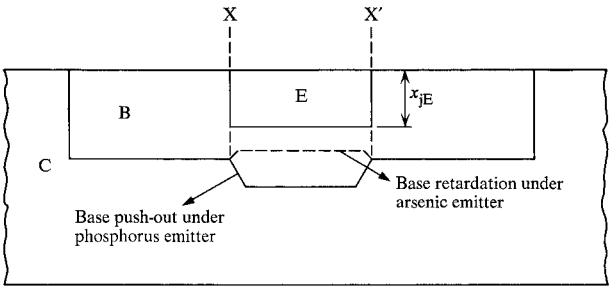


Figure 1 Collector-base junction of a transistor under the influence of phosphorus and arsenic emitters.

sivity increases with concentration by a factor of 20 to 40, which is at least five times higher than the corresponding increase in diffusivity for phosphorus impurities. As a result, a complementary error function (constant diffusivity) fit to phosphorus diffusion to match sheet resistivity ρ_s and junction depth x_j results in a small inaccuracy in the surface concentration C_0 thus determined as compared with the C_0 value determined by neutron activation analysis. However, a similar fit to an arsenic impurity profile results in an erfc C_0 that is larger than the actual value by a factor of about 30. Such discrepancies are even greater if one tries to fit the erfc profile to the impurity gradient of a typical arsenic emitter profile near the junction (on a p-type substrate); the resultant erfc C_0 then becomes larger than the density of silicon atoms ($> 5 \times 10^{22}$ cm^{-3})!

Hence it is imperative that any accurate simulation of the arsenic impurity profile include a strong nonlinear dependency of diffusivity on concentration. The impurity profile predicted by the diffusion model [3] indicates a flat profile extending from the surface with a sharp impurity gradient near the emitter junction x_{jE} (Fig. 1) for arsenic impurities. Yet the surface concentration required for arsenic profiles will be lower than that of the phosphorus profile for comparable sheet resistivity and junction depth, as shown in Table 1.

• *Process reproducibility*

Note from Table 1 that for comparable junction depth and sheet resistivity in the diffused layer, the emitter diffusion process can be conducted at a higher temperature and over a longer time for arsenic than for phosphorus. The diffusion temperature of phosphorus is sufficiently low that solid solubility becomes a limitation and severe precipitation lowers the impurity content available for conduction purposes (electrically ionized impurities). Thus, run-to-run reproducibility is much better for the arsenic process.

• *Ability to support high current density*

As shown in Fig. 2(a), the net charge distribution based on a typical phosphorus impurity profile indicates that neutralization of the emitter junction becomes severe even at 4000 A-cm^{-2} for state-of-the-art diffusion depths. This results in base widening [1] and an increase in neutral capacitance [4, 5], leading to a fall-off in β and f_T. (Note that both devices had a collector doping level of 10^{17} cm^{-3}, and hence base widening due to the "Kirk effect" [6] was negligible.) To prevent such degradation of device parameters, phosphorus emitters have to be very shallow, as in Fig. 2(b). Figure 3 indicates that current densities in fabricated transistors with a 0.1×0.5 mil^2 emitter are about an order of magnitude higher than the current density in Fig. 2(a). To support such current densities, phosphorus diffusion has to be even shallower than in Fig. 2(b) and/or the surface concentration has to be higher to provide large impurity gradients near the junction. Such high gradients are needed to prevent neutralization of the junction by the injected carrier densities.

The arsenic emitter, on the other hand, will produce a sharp impurity gradient even for relatively deep diffusion (1 μm or more), while producing a much higher impurity gradient at shallow depths (Table 1) to sustain β and f_T even at much larger current densities.

• *Yield*

The preceding requirements lead to a severe process control problem for shallow phosphorus diffusion, since warmup and purge cycles consume nearly as much time as the actual diffusion. High surface concentration is not desirable either. Because of the mismatch between P and Si atoms, high-concentration diffusion leads to precipitation, dislocation, and ragged junctions in the

Table 1 Process conditions for P and As diffusion.

	C_0 (cm^{-3})	x_j (μm)	a_E (cm^{-4})	ρ_s (ohms)	T (°C)	t (min)
Phosphorus:						
$POCl_3$	8×10^{20}	0.483	2×10^{23}	22	900	5-30-5
PH_3	10^{21}	0.584	3×10^{23}	17	885	5-33-5
Arsenic:						
Capsule	5×10^{20}	0.533	10^{24}	15	1000	85

phosphorus emitter region. Such defects put a serious limitation on the ability of narrow basewidth devices to avoid yield loss due to degradation of expected current gain by increased leakage current and lower junction breakdown voltage.

With arsenic, the ability to produce an efficient emitter with lower surface concentration holds even for deeper diffusion, as will be shown below. The lower limit of the surface concentration is determined only by the metal-to-Si contact resistance. Here again, the spreading resistance in the bulk is small because of the square nature of the arsenic profile.

• *Basewidth control*

High β and f_T require a narrow basewidth in the intrinsic region (XX′ in Fig. 1) directly beneath the emitter. However, if the total number of base impurities is not sufficient in this region, the device will suffer from low punch-through (breakdown) voltage and high base resistance. In the phosphorus emitter device, the heat treatment during emitter diffusion drives the base impurities farther under the emitter region. Because of this phenomenon, called the "base push-out" or "emitter dip" effect [7], and the fact that the emitter junction itself becomes ragged with high-concentration phosphorus diffusion, manufacturable basewidth has been restricted to 0.5 μm or more. Since the emitter has to be driven further in to catch up with the pushed-out base region, a significant portion of the diffused base region will be compensated, as shown in Fig. 4. Thus, for a narrow basewidth, the total number of base impurities in the basewidth will be small. Any variation in base or emitter diffusion depths across a wafer or from wafer to wafer will produce variability in the device characteristics, and yield loss due to collector-to-emitter punch-through. In contrast, the arsenic emitter does not produce any base push-out effect. For a boron or gallium doped base, the arsenic emitter will in fact produce "base retardation" [8], a "pull-in" effect on the base-collector junction under the influence of the electric field produced by the steep impurity gradient during arsenic diffusion. (Figure 5 compares this with the push-out effect.) Further, with the arsenic emitter the sharper falloff near the junction causes less compensation of the base region and achieves a larger total base doping than that for a comparable basewidth in a phosphorus-emitter device, as shown in Fig. 4. Thus, a narrow-basewidth device with reproducible characteristics can be manufactured with the arsenic emitter.

• *Effect on gold doped devices*

One particular application for the arsenic emitter is in devices that employ gold doping. The gold is used to reduce the saturation time constant in silicon devices intended for saturated-mode operation, but it has the un-

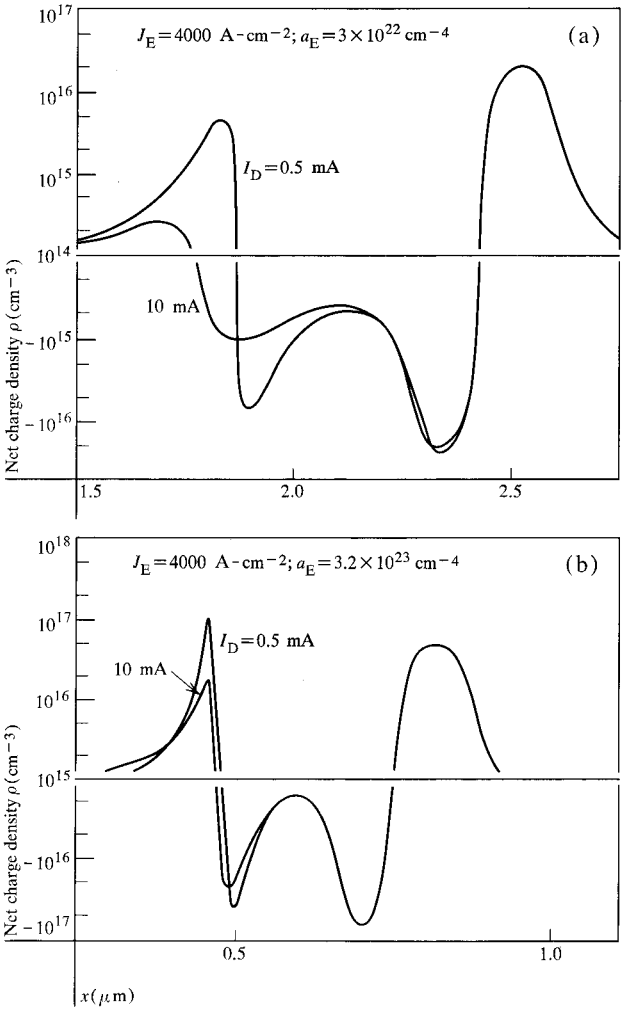
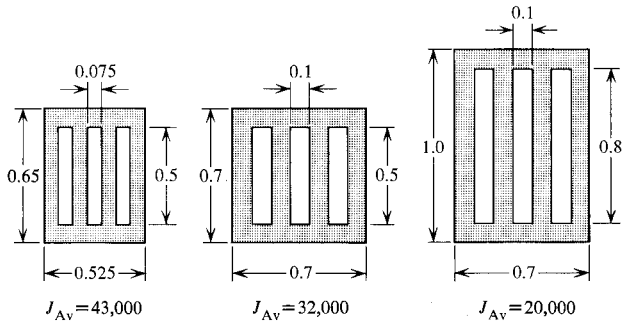


Figure 2 Comparison of base widening due to neutralization of the emitter junction by injected carrier density. (J_E is the emitter current density, a_E the emitter impurity gradient at the junction, and I_D the diode current.)

Figure 3 Increase in current density with decreasing device size.



J_{Av} in A−cm^{-2} at 10 mA
All dimensions are in mils (inches × 10^{-3})

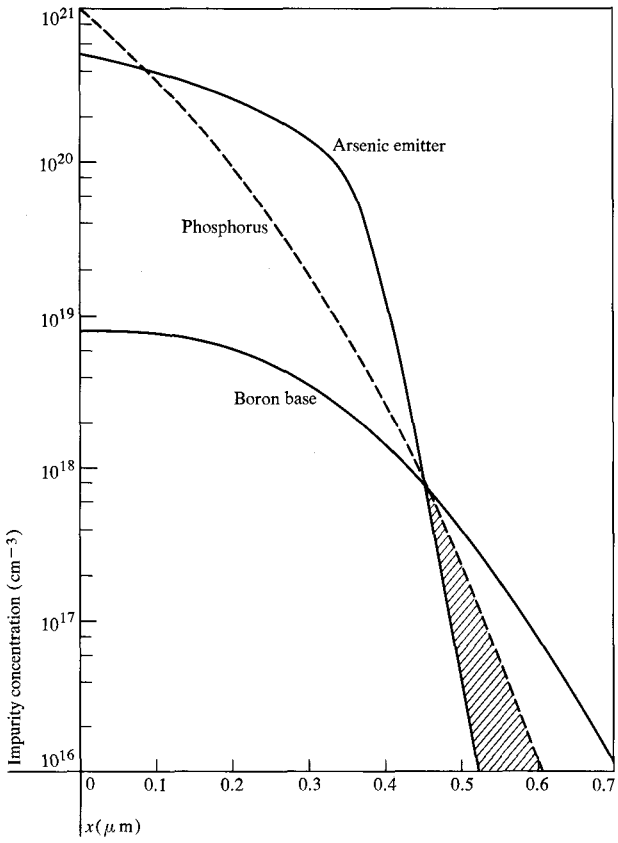


Figure 4 Effect of phosphorus and arsenic emitter profiles on the total base doping of a transistor.

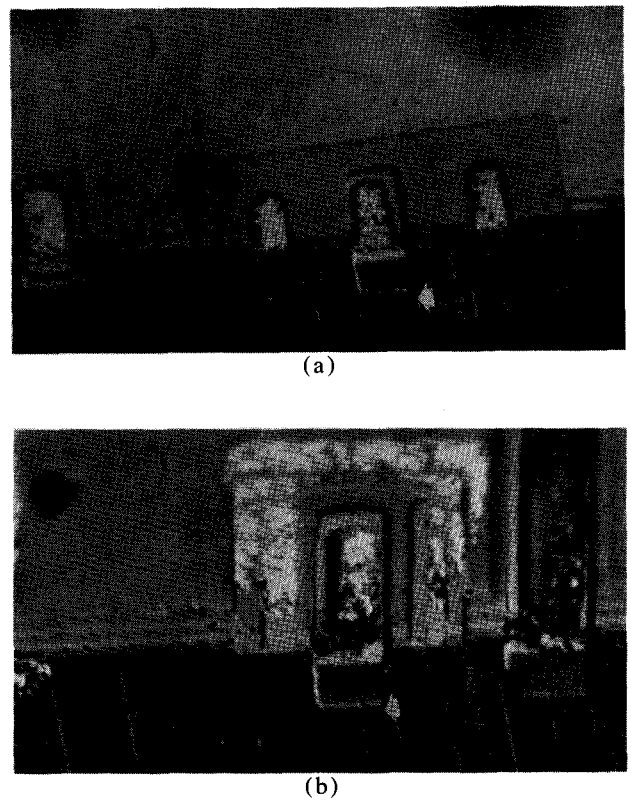


Figure 5 Cross sections of (a) phosphorus-emitter, boron-base transistor showing "base push-out," and (b) arsenic-emitter, boron-base transistor showing "base retardation."

desirable effect of also reducing current gain. Also, because of the high temperature required for gold diffusion, shallow phosphorus emitter junctions are not feasible. On the other hand, deep phosphorus emitter junctions require greater basewidth, with the disadvantages discussed above. The resulting lower f_T leads to increased rise and fall times during switching.

The arsenic emitter, however, with its increased emitter efficiency and narrower basewidth, offers not only the required high f_T but also higher current gain, even in the presence of gold. The process described next below demonstrates the effect of such improvements on devices with deeper diffusion.

Process for gold-doped devices with arsenic emitter

1) Collector epitaxy

Orientation:	⟨100⟩
Resistivity:	4 Ω-cm
Type:	n

2) Base diffusion deposition

Method:	Sealed tube diffusion with boron source
Sheet resistance:	7 Ω/□
Junction depth:	0.56 μm
Surface concentration:	1.4×10^{20} cm^{-3}, assuming complementary error function

3) Base diffusion drive-in and reoxidation

Sheet resistance:	208 Ω/□
Junction depth:	0.63 μm
Surface concentration:	2.7×10^{19} cm^{-3}, assuming Gaussian distribution

4) Emitter diffusion

Method:	Sealed tube diffusion with arsenic source
Temperature:	1000° C
Time:	90 minutes
Junction depth:	0.46 μm
Sheet resistance:	22 Ω/□

5) Emitter reoxidation

Temperature:	900° C

Time:	90 min in steam
SiO_2 thickness:	3000 Å

6) Phosphosilicate glass (PSG) formation by phosphorus diffusion

Temperature:	900° C
Time:	70 min
PSG thickness:	1000 Å
Diffusion source:	$POCl_3$

7) Introduction of gold

Source of gold:	Sand-blast back of wafer and then evaporate 500 Å of gold on wafer.
Diffusion temperature:	1000° C
Diffusion atmosphere:	Dry N_2
Diffusion time:	2 hr

The time-temperature cycle of the gold diffusion process that actually determines the final impurity profile of the transistor should be noted. The final vertical dimensions of the transistor are shown in Fig. 6.

A beveled cross-sectional view of this device is depicted in Fig. 5(b). The effect of the gold on the junction depth is expected to be small. Passivation or stabilization of the device is accomplished by the formation of the phosphosilicate glass (PSG) [9,10] after emitter diffusion and reoxidation. The PSG also serves as a getter for positive ions (e.g. sodium) to prevent inversion of the base region. Leaky junctions, presumably caused by base region surface inversion, and surface contamination discouraged many earlier workers in the development of the arsenic emitter transistor. With the introduction of a PSG formation step into the process, however, junction quality comparable to that of the phosphorus emitter device can be obtained. The process has proved that arsenic emitter transistors are far superior than their phosphorus counterparts. The observed characteristics of the arsenic emitter transistor with gold doping are given in the next section.

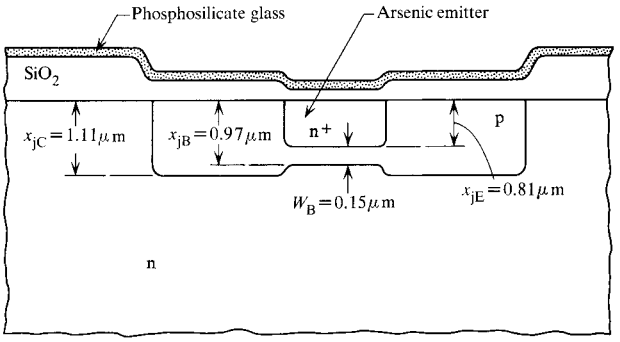
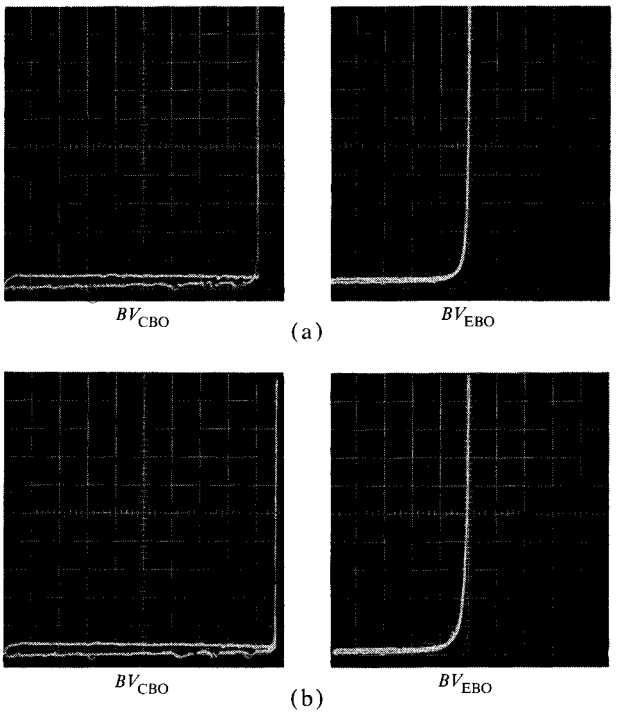


Figure 6 Final vertical dimensions of gold doped arsenic-emitter transistor (after all high-temperature processing steps).

Figure 7 Collector and emitter junction characteristics: (a) with PH_3 gettering cycle 5-15-5; (b) without gettering cycle. Vertical scale 10 μA/div. Horizontal scale 2V/div for BV_{CBO} and 1V/div for BV_{EBO}.



Experimental results

• *Devices without gold doping*

Transistors of various geometries have been processed with similar epitaxial-layer thickness and the same base diffusion process to permit comparison of the characteristics of phosphorus- and arsenic-emitter transistors. The phosphorus emitter was formed in a boron-diffused wafer through open-tube PH_3 diffusion under the conditions shown in Table 1. The arsenic emitter was formed by a capsule diffusion using a powdered source, as described by Sandhu and Reuter [11].

The arsenic emitter by itself lacks the gettering effect of the P_2O_5 glass that is formed during open-tube phosphorus emitter diffusion. Hence, softer breakdown characteristics are expected in the absence of a gettering cycle with the arsenic emitter process. However, if a phosphorus cycle exists prior to emitter diffusion, enough gettering action will be provided to produce "hard" junction characteristics. Such phosphorus diffusion is normally used to provide a reach-through diffused region for lower collector resistance or for resistor diffusion. Figure 7 indicates that for such a process, an additional gettering cycle after emitter diffusion does not make any significant difference in device characteristics.

Total base doping in the intrinsic region of the transistor has been monitored by a test structure and is indicated

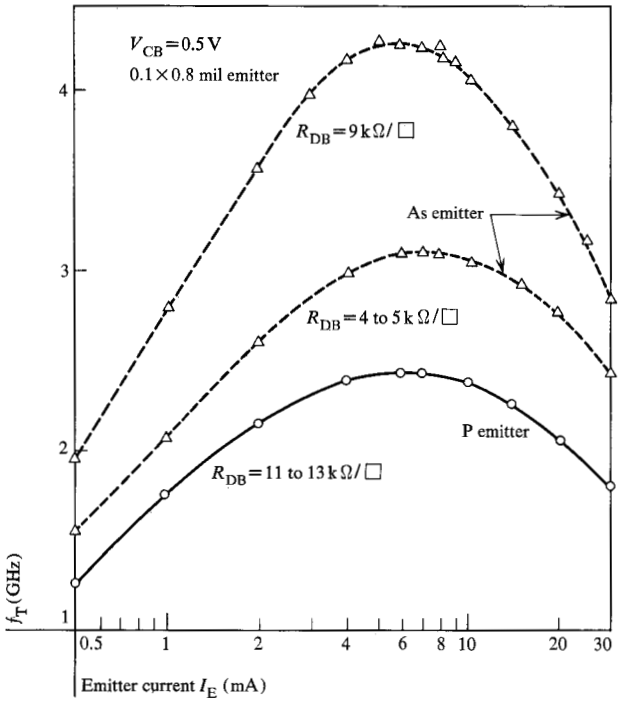


Figure 8 Comparison of f_T for phosphorus and arsenic emitter transistors with 0.1 × 0.5 mil emitter area.

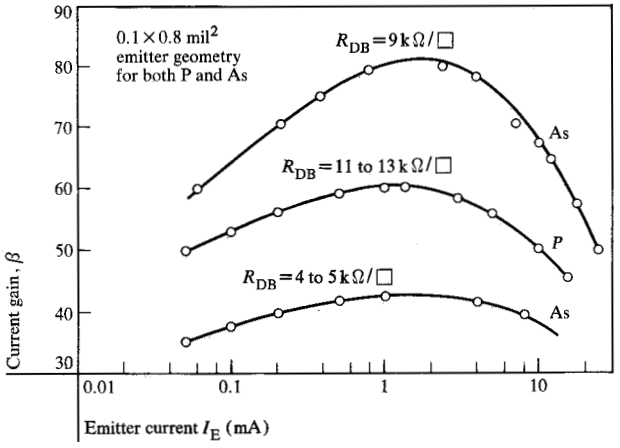


Figure 9 β vs I_E for arsenic and phosphorus emitters.

by the parameter R_{DB} in Fig. 8. This parameter is inversely proportional to the total base doping and is measured after emitter diffusion. Note from Fig. 8 that about 60 to 100% improvement in gain bandwidth f_T can be achieved by an arsenic emitter as compared with a phosphorus emitter for comparable R_{DB}. Both transistors have similar dimensions (0.1 × 0.8) and breakdown characteristics as follows:

BV_{CBO} = 15 V;
BV_{CEO} = 4.6 V;
BV_{CES} = 10 to 11 V;
BV_{EBO} = 4.8 V (5.4 V for phosphorus).

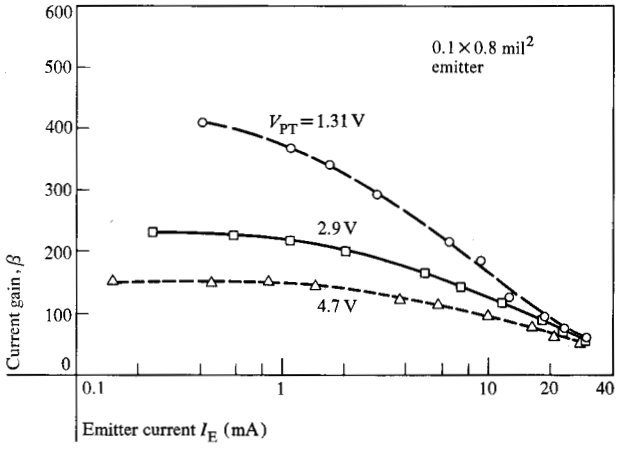
A 60% increase in dc current gain β at comparable R_{DB} has been observed for the arsenic emitter device. Typical dc current gain curves are shown in Fig. 9. The absence of a ragged junction and base push-out (both of which occur for the phosphorus emitter) allows further reduction of basewidth without severe yield loss. Arsenic emitter devices can be fabricated more reproducibly and with higher yield in the V_{PT} range of 10 to 3 V, than with the phosphorus emitter. Thus, an arsenic-emitter transistor having very high gain is feasible, as shown in Fig. 10.

The arsenic emitter's ability to sustain higher current densities offers the possibility that device dimensions can be reduced to a point where performance improvement is again limited by photolithography technology

Table 2 Parameters and dimensions for gold doped arsenic-emitter transistor.

Parameter or dimension	*Measured value*
Emitter geometry	0.5 × 2 mil
Base width W_B	0.15 μm
Common emitter current gain h_{FE}	
Gain-bandwidth f_T	85
Base resistance r'_B	3200 MHz
Base sheet resistance R_{DB}	200 Ω
Integrated base doping	9600 Ω/□ 3 × 10^{12} cm^{-2}

Figure 10 Current gain β vs emitter current I_E.



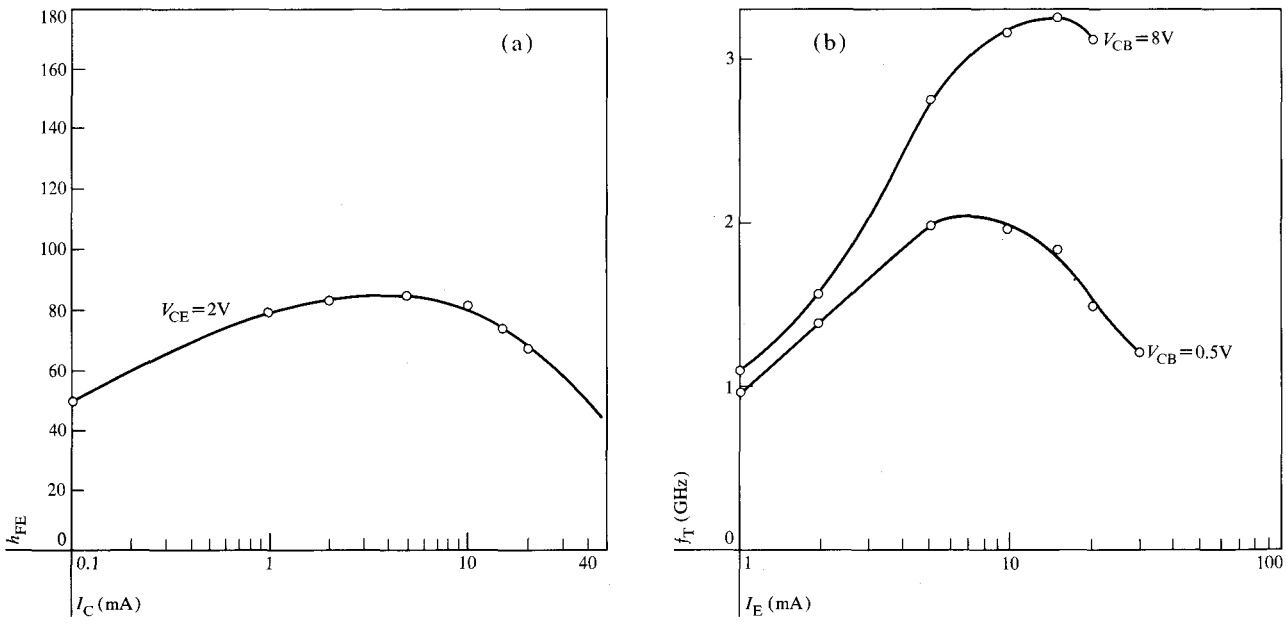


Figure 11 (a) Common emitter current gain vs collector current and (b) gain-bandwidth vs emitter current for gold doped arsenic-emitter transistor.

and interconnection metallization. Performance improvement [12] in this direction is discussed in another paper [13].

• *Devices with gold doping*

The dimensions and typical parameters for the experimental gold-doped device described above are shown in Table 2, and some results from the measurement of common-emitter current gain h_{FE} and gain bandwidth f_T for this device are given in Fig. 11. As can be seen from the Figure, both parameters are superior to those of state-of-the-art phosphorus devices of comparable geometry.

Conclusions

The arsenic emitter has been shown to offer improved performance, yield, and reproducibility in silicon technology. Over-all performance improvement by a factor of 1.6 to 2 has been achieved over the state-of-the-art phosphorus emitter generally used in the industry. For devices that employ gold doping, the improvement is expected to be somewhat higher. A further increase in component density is achievable as a result of this improved process, which uses a smaller geometry with consequent decreases in junction and parasitic capacitance and improved ac performance.

Acknowledgments

The authors thank W. Rosenberg, P. Melzer, J. Sandhu, J. Reuter and A. Platt for their contributions to the development of the arsenic diffusion technology used in fabricating the transistors discussed in this paper.

References

1. H. N. Ghosh, F. H. Delamoneda and N. R. Dono, *Proc. IEEE* **55,** 1897 (1967).
2. K. Fujinuma et al., 'Silicon Microwave Transistors made by New Techniques", *Proc. 1st Conference on Solid State Devices*, Tokyo 1969. Supplement to *J. Japan Society of Applied Physics* **39,** (1970).
3. T. L. Chiu and H. N. Ghosh, *IBM J. Res. Develop.* **15,** 472 (1971, this issue).
4. S. P. Morgan and F. M. Smits, *Bell System Tech. J.* **39,** 1573 (1960).
5. C. T. Sah, *Proc. IRE* **49,** 603 (1961).
6. C. T. Kirk, *IEEE Trans. Electron Devices* **ED-9,** 164 (1962).
7. R. Gereth et al., *J. Electrochem. Soc.* **112,** 323 (1965).
8. T. Klein and J. R. A. Beale, *Solid State Electronics* **9,** 59 (1966).
9. D. R. Kerr, J. S. Logan, P. J. Burkhardt and W. A. Pliskin, *IBM J. Res. Develop.* **8,** 376 (1964).
10. P. Balk and J. M. Eldridge, *Proc. IEEE* **57,** 1558 (1969).
11. J. S. Sandhu and J. L. Reuter, *IBM J. Res. Develop.* **15,** 464 (1971, this issue).
12. A. S. Oberai and V. A. Dhaka, "Ultrahigh-Speed Current Switch Using 12.6 GHz Silicon Transistor," presented at IEEE International Electron Devices Conference, October 1968.
13. H. N. Ghosh, K. G. Ashar, A. S. Oberai and D. DeWitt, *IBM J. Res. Develop.* **15,** 436 (1971, this issue).

Received April 16, 1971
Revised July 26, 1971

H. N. Ghosh, A. S. Oberai and M. B. Vora are located at the IBM Components Division Laboratory, East Fishkill (Hopewell Junction), New York 12533. J. J. Chang is located at the IBM Components Division Laboratory, Burlington (Essex Junction), Vermont 05452.