

Experimental Evaluation of High Energy Ion Implantation Gradients for Possible Fabrication of a Transistor Pedestal Collector

Abstract: The use of ion accelerators to implant impurities in crystals has become the subject of widespread research. Such studies have been limited mainly to low energies with acceleration voltages of 50 to 500 kilovolts. In this energy range, impurities are implanted into the upper micron or less of the surface.

The present work describes certain characteristics of high energy ion implantation. The ions used were boron and phosphorus. They were implanted into silicon with energies of 2 to 4 megavolts. In this energy range, the impurities have a useful positive impurity concentration gradient from the surface. The surface concentration is about $4 \times 10^{16} \text{ cm}^{-3}$, and the peak concentration exceeds 10^{19} cm^{-3} depending on dosage. The peak concentration occurs about $2.5 \mu\text{m}$ deep. After annealing the radiation damage introduced into the semiconductor, it was determined that the surface silicon recovered over 90% of its expected maximum conductivity and mobility.

A discussion is given of the concentration gradients required to fabricate a collector pedestal for a high-speed switching transistor, and it is shown that such gradients can be obtained by using high energy ion-implantation. The pedestal may be implanted after the base and emitter diffusions, and annealed at a low temperature, thus keeping a sharp impurity gradient. Also, since it is put into the final epitaxial layer, its vertical position relative to the emitter-base junction will be independent of epitaxial undulations.

Introduction

There have been only two published works which concern implanting electrically active impurities into silicon using MeV energies. Davies [1] has determined the mean range (i.e. the depth of the concentration peak) of boron, phosphorus, and arsenic in silicon for energies in the range 500 keV to 1.7 MeV. Roosild et al [2] utilized junction staining techniques to obtain rough profiles of boron and phosphorus implanted into silicon at energies of 1 to 2.5 MeV. In this work, experiments were conducted to obtain a more detailed knowledge of the concentration gradients in silicon that had been ion implanted with impurities at MeV energies. The goal was to demonstrate that ion implantation is a feasible process for producing a pedestal collector.

The pedestal-collector transistor [3] is a planar bipolar silicon transistor whose cross section is shown in Fig. 1 for a typical configuration. The purpose of the pedestal collector structure is to provide a wide separation between the base region and the high conductivity subcollector except in the "active" transistor region directly under the emitter. This reduces the parasitic base-to-collector capacitance to a minimum, which substantially increases the transistor's performance when used in a switching circuit.

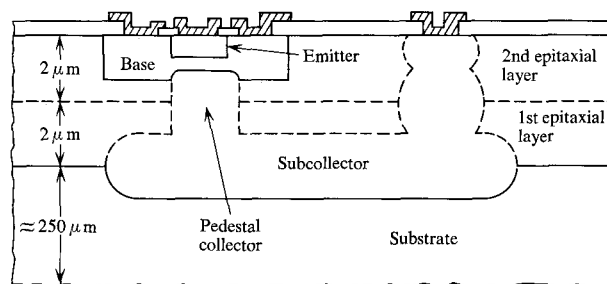


Figure 1 Cross section of a pedestal-collector transistor. The first epitaxial layer contains the pedestal diffusion and a reach-through diffusion to the buried collector. After the second epitaxial layer is grown, the base and emitter are diffused into the top surface.

The pedestal collector device is difficult to produce with high yield by conventional techniques of integrated circuit manufacture. It is necessary to grow two epitaxial layers, one to a high precision. The first epitaxial layer is grown to accommodate the pedestal collector, while the second contains the base and emitter. As shown in Fig. 1, the second epitaxial layer must be grown to an accuracy of a fraction of the basewidth. If this layer is

too thick, the performance falls off rapidly, while if the layer is too thin, an emitter-to-collector short or low emitter collector breakdown voltage can result. In practice, it is difficult to grow an epitaxial layer to the required tolerance over a whole silicon wafer, and thus a low yield results. However, if the pedestal region could be ion-implanted, undulations in the epitaxial layer would have no effect on the position of the base-collector junction. This type of device could be fabricated by ion implantation as shown in Fig. 2. In this case, all impurities that form the active device regions are introduced through the top layer; the critical difference is that the vertical registration is independent of the epitaxial layer thickness. As an additional benefit attributable to the low processing temperature required for ion implanted layers ($<800^{\circ}\text{C}$), the pedestal diffusion could have a sharper concentration gradient and be more accurately aligned with the emitter structure.

In the fabrication of a transistor pedestal, the implantation profile between the surface and the peak is most important. Figure 3 is an example of the impurity profiles of a high-performance pedestal-transistor fabricated using thermal diffusions and two epitaxial layers as shown in Fig. 1. The important aspects of these profiles, which must be duplicated by an ion implantation process, are that 1) the base-pedestal junction must be sufficiently deep to provide for the emitter diffusion (e.g. $\approx 0.6\text{ }\mu\text{m}$ in the current process) and 2) the net gradient of the pedestal concentration at the collector junction should be greater than approximately 10^{22} cm^{-4} .

In the following sections some initial experiments are described which answer the following questions:

- a) Can the ion-implanted impurities be made to duplicate the necessary concentration gradients and conductivities for a pedestal-collector?
- b) Can the semiconductor above the ion-implanted layer be recovered to its original electrical state?

The results of these initial experiments indicate that both objectives are feasible.

Experimental procedure

• Implantations

The implantations were made using a High Voltage Engineering Co. accelerator. They supplied beams of boron at $0.1\text{ }\mu\text{A}$ and phosphorus at $0.3\text{ }\mu\text{A}$. The beam was monitored visually by a frosted quartz disk which could be rotated into the sample position. The image of the unswept beam showed a diameter of approximately 1 mm. Electrostatic sweeping was utilized to raster the beam across a one centimeter square area on the target wafer in order to produce a uniform implantation. The target chamber was kept at less than 1×10^{-5} Torr during implantations.

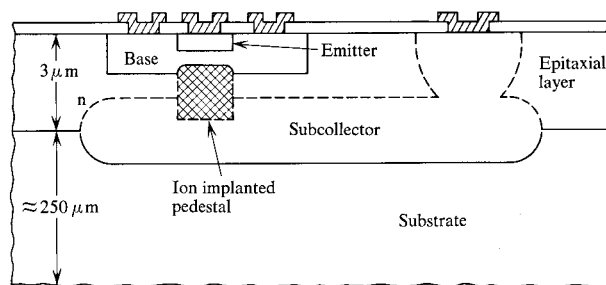
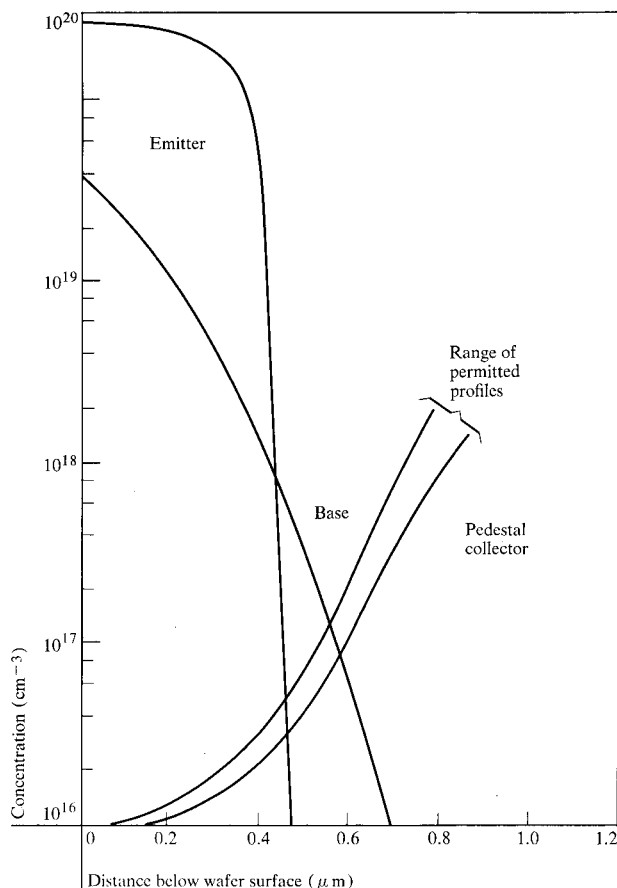


Figure 2 The pedestal collector is shown as fabricated by high energy ion implantation. Since all three active regions (emitter, base and pedestal) are put in through the top surface, they will have a constant relative vertical position even if the epitaxial layer undulates.

Figure 3 Typical experimental impurity profiles for a pedestal-collector transistor, obtained using the double-epitaxial-layer fabrication technique shown in Fig. 1. The pedestal was diffused into the first epitaxial layer. After the second epitaxy was grown, the base and emitter were introduced.



The wafers were held by four beryllium-copper clips to heat sinks of brass. The substrate temperature during implantation was estimated to be less than 100°C . The beam current was measured and integrated by direct reading of the implanted wafer. No provision was made

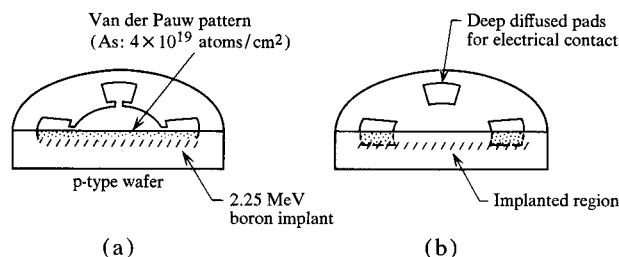


Figure 4 Test patterns used to determine the electrical characteristics of the ion-implanted wafers. (a) Van der Pauw pattern used to electrically test the semiconductor near the surface, above the implant. Tests were made before and after the implantation as described in the text. (b) Wafer prepared for electrical tests of the ion-implantation region. After the implant the wafer was etched leaving a four-armed mesa containing the four contacts and a central region containing the implant in a van der Pauw pattern similar to that in (a).

Table 1 Electrical Characteristics above the Implanted Region.

	Sheet resistivity ($\Omega/\square$)	Mobility ($\text{cm}^2/\text{V-sec}$)
Boron implant at room temperature:		
Initial	364	465
After implant and anneal (900°C, 1/2 hr)	420 $\pm$ 40	410 $\pm$ 41
Boron Implant at 625°C:		
Initial	328	465
After implant	340 $\pm$ 34	440 $\pm$ 44

for minimizing electron sputtering from the wafer, and the actual ion current was estimated by comparing the current reading from the test wafer to that obtained from a standard Faraday cup biased at -180 V.

The background radiation level of the implantation room during these MeV implantations is of interest. No increase of energetic electrons or energetic photons was detected outside the 0.5 in. aluminum target chamber during the implantations.

• Electrical evaluation of implanted layers

The electrical evaluation of ion-implanted layers was accomplished by Hall effect and sheet resistivity measurements on van der Pauw configurations. Depth profiles of carrier concentration and carrier mobility were accomplished by using these measurements in conjunction with anodic oxidation and HF layer removal techniques as outlined[4] by Mayer et al. The details of the experimental procedure have been reported[5]. Annealing was conducted in a nitrogen atmosphere.

Experimental results and discussion

• Electrical characteristics of silicon above the implanted region

The majority carrier resistivity and mobility within the upper $1 \mu\text{m}$ of the semiconductor were tested before implantation, after implantation, and after an annealing cycle. The test pattern used is shown in Fig. 4(a). A four-pad van der Pauw pattern was diffused into the p-type silicon wafer to a depth of $1 \mu\text{m}$ with a concentration of about $4 \times 10^{19} \text{ cm}^{-3}$. Arsenic was used to obtain a relatively sharp cut-off at the junction. The sheet resistivity of the diffused layer was 300 to $500 \Omega/\square$.

After the initial resistivity and mobility were determined, a boron dose of $1 \times 10^{15} \text{ ions/cm}^2$ was implanted through this layer at an energy of 2.25 MeV. At this energy, the implanted boron contaminating the surface van der Pauw pattern was less than 10^{17} cm^{-3} . The peak boron concentration should occur at $2.8 \mu\text{m}$ [1]. The results of the tests, before and after, are indicated by the typical results in Table 1.

It was found that surface states affected the tests just described to about 10%, depending on how the bare wafer was cleaned after implantation. From these experimental results, only a slight degradation of sheet resistivity and mobility resulting from the boron implantation was noted.

• Profiles of high energy implantations

The wafers used for profiling studies had prediffused contact pads to facilitate electrical contact to the buried implanted region, as shown in Fig. 4(b). These wafers were 1 ohm-cm , $\langle 100 \rangle$ silicon. During implantation, the wafer was tilted 5° from the beam to minimize channeling effects. After implantation and annealing, the van der Pauw configuration was produced by etching a mesa as described in Ref.[5]. Implantations were made with the energies and doses shown in Table 2. Column 5 of Table 2 lists the percent of the implanted ions which are electrically active and uncompensated as determined from the measured total dose and the integrated number of carriers obtained from the profiling experiments. It should be noted that the measured total dose is somewhat uncertain because the beam current from the wafer included a large contribution from the scattered electrons, as previously mentioned.

The concentration profiles obtained from differential sheet resistivity and sheet Hall measurements are presented in Fig. 5 for boron and Fig. 6 for phosphorus. Figure 5 represents only a portion of the profile (experimental difficulties precluded obtaining the rest of this profile, but for the purposes of pedestal fabrication, the initial positive gradient portion of the profile is of most interest). It should be noted that all depth measurements have an experimental error of 10%; e.g., for 2.5 MeV

Table 2 Implantation energies and doses.

Impurity	Energy (MeV)	Dosage (cm ⁻²)	Post-implantation anneal (°C-Min)	% Electrically active	Final sheet resistivity (Ω/□)
Boron	2.25	5.0×10^{15}	900-45	40	57
Phosphorus	2.50	1.2×10^{15}	850-30	50	77
Phosphorus	2.50	5.8×10^{15}	850-30	51	23
Phosphorus	4.00	1.0×10^{15}	850-30	43	63

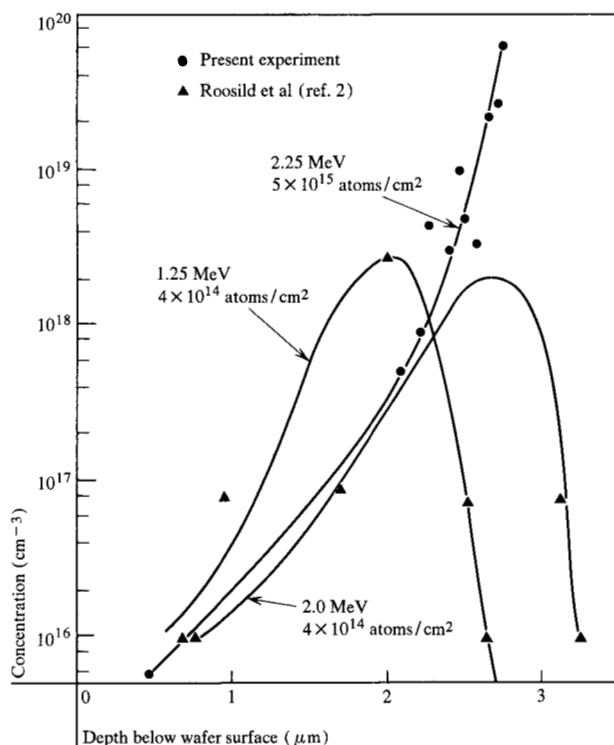


Figure 5 High-energy ion implantation of boron. The solid circles represent the upper edge of the impurity profile as determined by electrical measurements of a 2.25 MeV boron implantation. The leftmost circle came from a separate measurement of junction-staining to obtain the concentration near the surface. The other two profiles are from Ref.[2] and are only approximate profiles.

phosphorus implantations, the peak concentration occurs at a depth of $2.2 \pm 0.2 \mu\text{m}$. It should also be emphasized that the profiling procedure is a differential technique and is less reliable near the surface (e.g., below $2 \mu\text{m}$ for the boron profile and $1 \mu\text{m}$ for the phosphorus profile).

With respect to boron implantation at room temperature, it is known that higher annealing temperatures are required in order to render a large fraction of the implanted boron electrically active and uncompensated than are required for the conventional n-type dopants in silicon (e.g. P or As)[6]. Roosild et al.[2] indicated that,

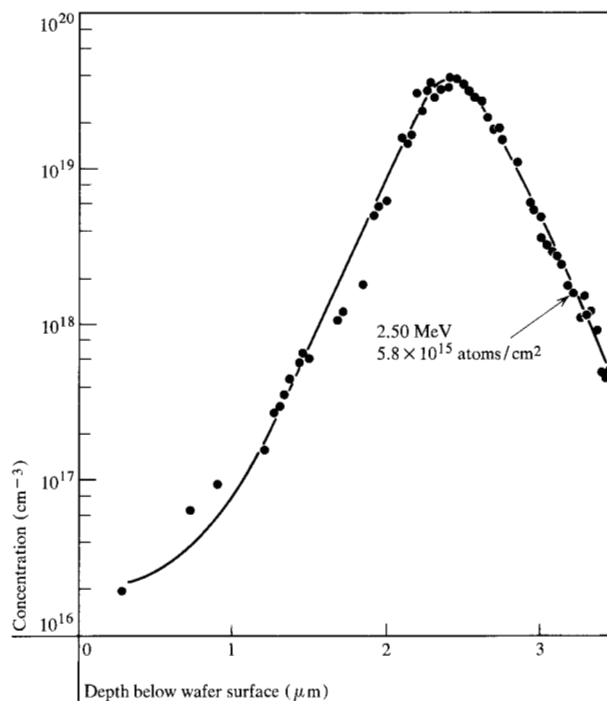


Figure 6 High-energy ion implantation of phosphorus. The solid circles are the results of electrical profiling techniques as described in the text. Several other profiles were taken, but this illustrates their general character.

for doses greater than 10^{14} cm^{-2} , an annealing temperature of 1000°C (1 hour) is required to make most of the boron electrically active, and uncompensated, for MeV implantation energies. Their data[2] for implants annealed at 1000°C for 1 hour are reproduced for convenience in Table 3. Thus, boron implantation with sheet resistivities of less than $10 \Omega/\square$ can be obtained. The profile data of Roosild et al[2], given in Fig. 5 for comparison with our data, were obtained after only a 700°C anneal. It is evident from our data that the boron profile after adequate annealing is much steeper than

Table 3 Data from Roosild et al[2].

Boron dose (ions/cm ²)	Sheet resistivity ($\Omega/\square$)
2×10^{13}	1300
2×10^{14}	230
2×10^{15}	30
2×10^{16}	6

Table 4 Device comparison.

	Conventional pedestal transistor	Phosphorus ion implantation
Base-pedestal junction	$>0.5 \mu\text{m}$	$>0.9 \mu\text{m}$
Pedestal concentration gradient	$4 \times 10^{22} \text{ cm}^{-4}$	$2.5 \times 10^{22} \text{ cm}^{-4}$
Sheet resistivity of pedestal	$8 \Omega/\square$	$28 \Omega/\square$

indicated by the results in[2] and thus should be useful for pedestal fabrication in pnp transistors (e.g., if one wished to have complementary devices on the same chip). Of course, a lower energy implantation could be used if a base-collector junction closer to the surface were desired (e.g. as in Fig. 3 for the npn structure).

The profile obtained for 2.5 MeV phosphorus ions (Fig. 6) is suitable for fabricating a pedestal in an npn bipolar transistor. Table 4 lists the relevant parameters one would obtain for a device made with such an implant as compared with a conventional pedestal transistor. For a base-collector junction nearer the surface, an energy somewhat lower than 2.5 MeV could be employed, which should also result in an improved concentration gradient.

The fact that the phosphorus implantations were not totally electrically active after the 850°C anneal (Table 2) is somewhat surprising and may be an indication that the total dose measurement was in error. This point could be

verified by using neutron activation profiling of the implanted phosphorus.

Conclusions

It has been demonstrated that a buried n-type layer with a concentration gradient suitable for a pedestal collector can be produced by implantation of phosphorus at energies near 2.5 MeV. Boron profiles adequate for a pedestal pnp transistor can also be obtained. Although a very low sheet resistivity is not required for the application shown in Fig. 2, in which ion implantation is used in conjunction with a sub-collector diffusion, it should be noted that buried layers with sheet resistivities of less than $10 \Omega/\square$ can be produced by ion implantation.

It has been shown that, within the accuracy of our electrical measurements, a transistor emitter should not be electrically affected by such implantation. It has not been shown whether the base minority carrier mobility might be affected.

These initial experiments indicate that the use of high energy ion implantation to construct deep electrically-active layers should be further investigated.

References

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