

## Electron Beam Fabrication of Micron Transistors

**Abstract:** For high-speed performance as well as high packing density, it is desirable to make the components in integrated circuits as small as possible. One of the fundamental problems in making smaller components is that of limitations in the optical technology. This paper describes an experimental process and the results obtained by using an electron-optical system to fabricate small transistors. Planar bipolar transistors with emitter and base contact windows one micron wide have been fabricated, with the electron beam exposure system used to open all the diffusion windows as well as to expose the metallization patterns.

Conventional etching techniques are unable to provide 1- $\mu\text{m}$  wide metal paths in half-to one-micron thick metal layers; therefore the lift-off process is used. The dc and ac characteristics presented compare favorably, for the first time using this fabrication process, with the best bipolar transistors produced by optical masking processes. These characteristics provide a guide for refinement in future micron transistor design.

### Introduction

The present trend of integrated circuit technology is toward large-scale integration. This requires making the components as small as possible and packing more circuits on a silicon chip. Smaller components give higher packing density, higher speed due to their low capacitance, and higher yield due to their small active area. One of the fundamental problems in making smaller components is that of limitations in the optical masking technology. Electron-optical systems represent the most promising alternative to the optical masking process.

The electron-optical system has many advantages over the conventional masking techniques used in integrated circuit fabrication. The electron beam system with its deflection and blanking capabilities can be readily automated. This would provide a turn-around time from computer programmed circuit layout to exposed wafer of a few minutes, rather than several weeks as in the ordinary masking process. Discretionary wiring on the silicon wafer can be readily achieved with the electron beam system, providing the foundation for extremely large-scale integration. By eliminating the masks and their associated defects, the yield of complex integrated circuit chips should also improve with direct electron beam exposure. For future applications, the electron-optical system is the most promising method for fabricating sub-micron devices. In fact the resolution capability of the electron-optical system is so good that for practical purposes it is limited only by registration and

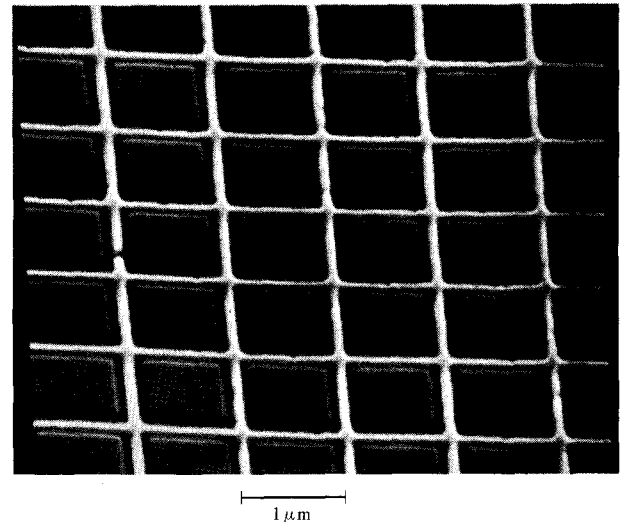


Figure 1 1000 Å metal lines on 1- $\mu\text{m}$  centers.

etching capabilities in the device fabrication process. To illustrate the high resolution capability of the scanning electron beam exposure system, Fig. 1 shows an electron micrograph of a set of metal grid lines approximately 1000 Å wide on 1- $\mu\text{m}$  centers. These lines were made by exposing an electron resist to the electron beam and then depositing metal on the wafer in the developed resist pattern.

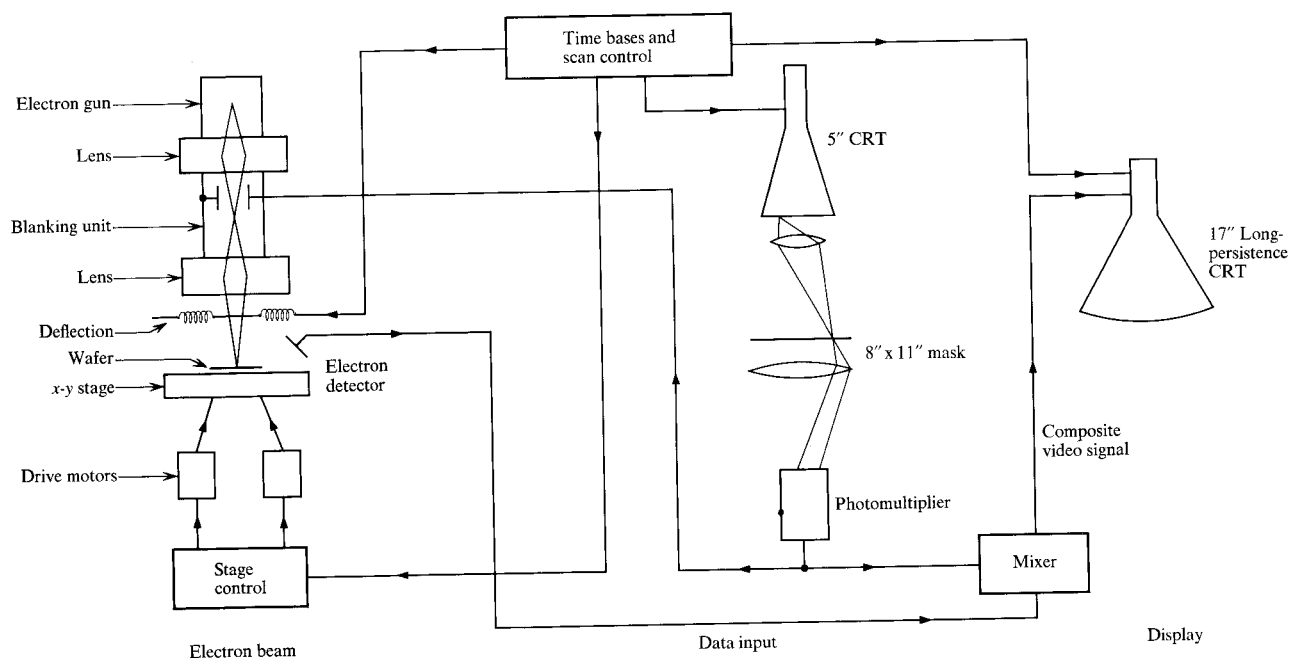


Figure 2 Schematic of electron beam exposure system.

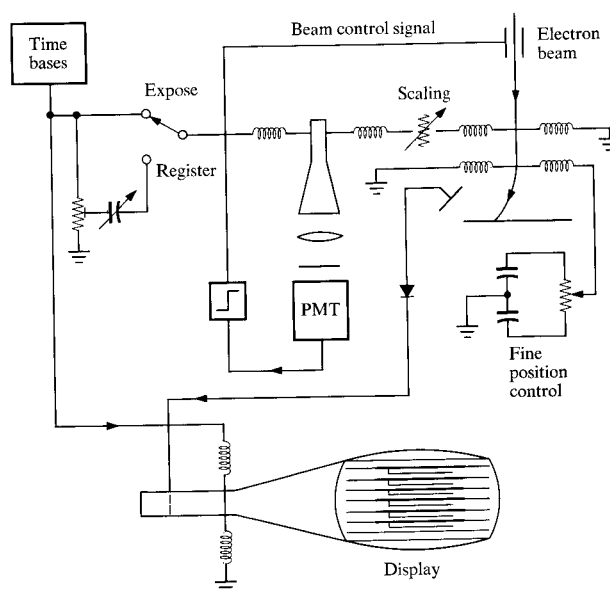
### Electron beam system

The exposure system used in fabricating micron transistors has been described elsewhere[1]. A schematic of the system is shown in Fig. 2. The electron beam is produced by a conventional tungsten hairpin cathode and two demagnifying lenses. The main beam is scanned in synchronism with a flying-spot scanner pattern generator. The scanner consists of a 5-in., high-resolution CRT, generating a 1000-line raster which is projected through a lens onto an  $8.5 \times 11$  in. mask. Light transmitted through the clear areas of the mask falls on a photomultiplier; the resulting signal is used for blanking the electron beam. A 17-in., long-persistence CRT, in synchronism with the scanner, serves as a viewing monitor. The signals from the flying-spot scanner and the secondary electron signal from the sample surface are used to modulate the brightness of the monitor.

### Registration process

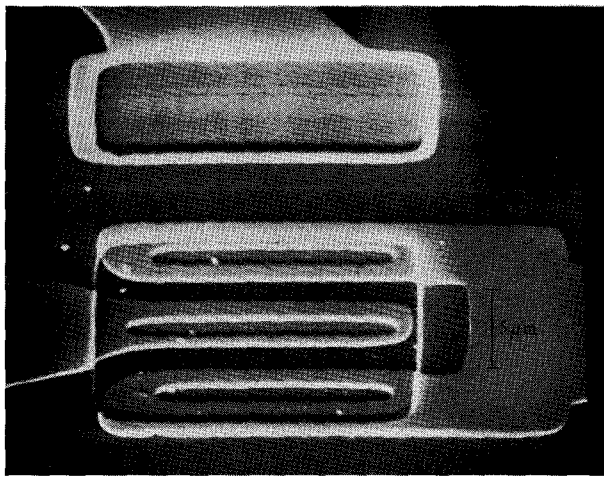
Figure 1 shows a pattern with the extremely small dimensions which can be generated by the system. Patterns of several levels are required to make up the transistor; these must be aligned with respect to each other. The alignment operation is carried out before pattern exposure by scanning only a small area near the edge of the field, where registration marks are located. The registration marks are simply etched steps in the silicon dioxide layer. The secondary emission signal from the registration scan is used to modulate the brightness of the viewing CRT. Misregistration is represented by a deviation

Figure 3 Schematic of registration system.



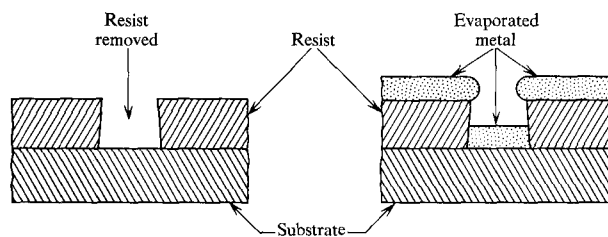
of the etched mark from the center of the scanning window and can be corrected by a small dc bias current in the  $x$  and  $y$  scan coils of the main electron beam. Figure 3 is a schematic of the registration system.

Besides the  $x$  and  $y$  positions, the angle of rotation  $\theta$  and the field size also must be adjusted for proper alignment. After the wafer is mounted on the  $x$ - $y$  stage, rotational alignment is achieved by mechanically aligning the

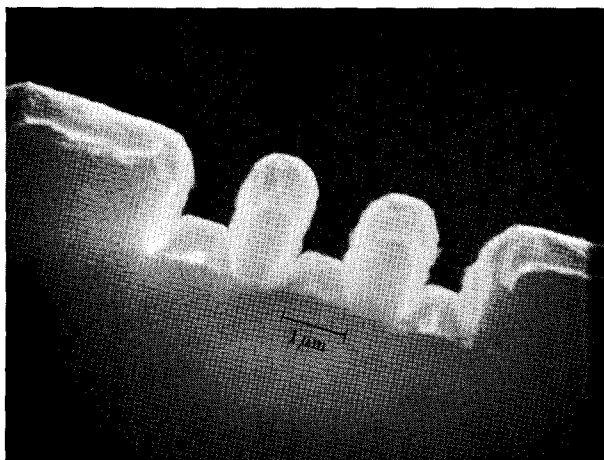


**Figure 4** Scanning electron micrograph of a 1- $\mu$ m linewidth transistor.

**Figure 5** Lift-off process using electron beam resist.



**Figure 6** Scanning electron micrograph of  $1 \times 1 \mu$ m metal lines evaporated through resist.



fields with the scan axis of the electron beam for successive levels, with the aid of a high-power microscope. For field size adjustment, multiple registration marks must be displayed simultaneously on the CRT so the  $x$  and  $y$  scan amplitudes can be adjusted until all the registration

marks fall into perfect alignment. Changes in field size are generally due to the instability of the scan generator. However, silicon wafer thickness variations also require field size adjustment.

Complete alignment is carried out on the first chip to be exposed. A mechanical stage is used to move from one chip area to the next. Some minor adjustment in  $x$  and  $y$  positioning is usually required before the exposure of each chip, due to the mechanical limitations of the stage. With properly etched registration marks and careful work, good registration accuracy can be achieved. Registration accuracy of approximately  $0.1 \mu$ m is obtained. Figure 4 is an electron micrograph of one of the completed micron transistors.

### Electron resist

A suitable resist is needed to take advantage of the resolution capability of the exposure system. Standard negative resists such as KTFR give sloping edges after exposure; thus they are unsuitable for high-resolution work. A special electron resist, poly-methyl-methacrylate, is used for its high resolution, etch resistance and insensitivity to light[2]. This is a positive resist; the exposed area dissolves much faster in developer than does the unexposed area. The developer is a mixture of isopropyl alcohol and methyl-isobutyl ketone. A development time of one minute is found to be adequate for an exposure density of  $8 \times 10^{-5} \text{ C/cm}^2$ . The resist thickness used is usually 2000 to 4000 Å for silicon dioxide etching, and over 10,000 Å for the metallization process.

### Metallization

In fabricating micron transistors it is also necessary to make micron size metallization patterns. As linewidth decreases, thickness must be increased for a given current density. If the maximum allowable current density is  $10^6 \text{ A/cm}^2$ , for a  $1\text{-}\mu\text{m}$  wide metal path the thickness required is also  $1 \mu\text{m}$  to carry a 10-mA current.

Conventional etching cannot provide the required  $1 \times 1 \mu\text{m}$  metallization pattern, because this technique gives rather large edge slope and irregularity. Therefore, the lift-off process (Fig. 5) is used, which is compatible with the high resolution capability of the electron beam exposure. By comparison, Fig. 6 is an electron micrograph showing the actual profile of the developed resist and evaporated metal. The metal thickness is  $1 \mu\text{m}$  and the opening is also approximately  $1 \mu\text{m}$ . In this process, metal is deposited onto the wafer after the metallization pattern is exposed and developed in the resist layer. Electron beam exposure gives an undercut in the developed resist; this provides a discontinuity between the metal deposited on the substrate and that on top of the resist. This discontinuity allows the solvent to penetrate to the unexposed resist and lift off the metal on top of the resist

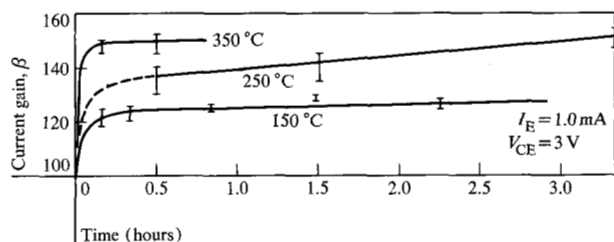


Figure 7 Current gain vs annealing time.

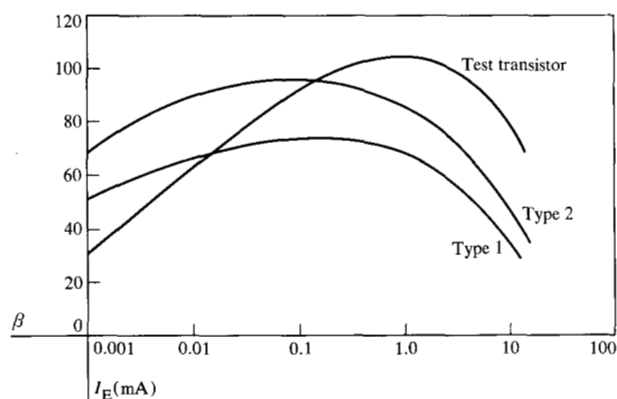


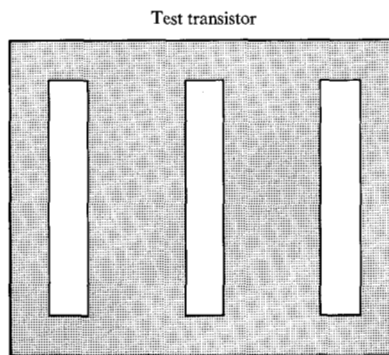
Figure 8 Current gain vs emitter current.

layer by dissolving the resist. Hot trichloroethylene is used as the solvent.

Problems encountered using the lift-off process were poor adhesion and large contact resistance. Poor adhesion results in metal peeling off during probing; excessive contact resistance detrimentally affects transistor performance. To avoid these problems, after developing the resist the wafers are thoroughly rinsed in alcohol and deionized water, and then blown dry. Immediately before the metal evaporation the wafers are etched in buffered HF to remove any possible contamination layers that might have grown in the room atmosphere.

### Annealing

It is well known that electron beams in the 10 to 20 kV energy range will not generate lattice defects in silicon[3]. Trapped charge and other surface defects, however, will form as a result of electron beam exposure[4]. These surface defects will detrimentally influence current gain, especially for small transistors which have a high perimeter-to-area ratio for the emitter junction. Fortunately the surface defects generated by electron beam bombardment can be annealed out by a simple heat cycle[5] such as the diffusion process. Since there is no heat cycle following metallization, an annealing process is required to bring up the current gain, which was reduced by electron beam processing.



Scale:  
→ ← 1 μm

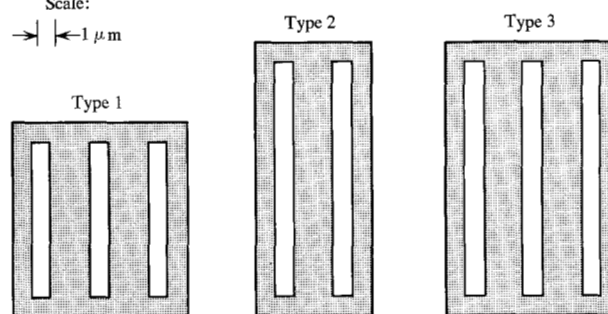


Figure 9 Experimental transistor geometries.

It is found that heat treatment either for 3 hours at 250°C or 15 minutes at 350°C in nitrogen is sufficient for the recovery of current gain. Typical results are summarized in Fig. 7. The current gain,  $\beta$ , measured after annealing for two different micron transistors and for the test transistor is shown in Fig. 8 as a function of the emitter current. It can be seen that good current gains are obtained for values as low as 1  $\mu$ A. This further indicates that most surface defects were removed by annealing.

### Fabrication process

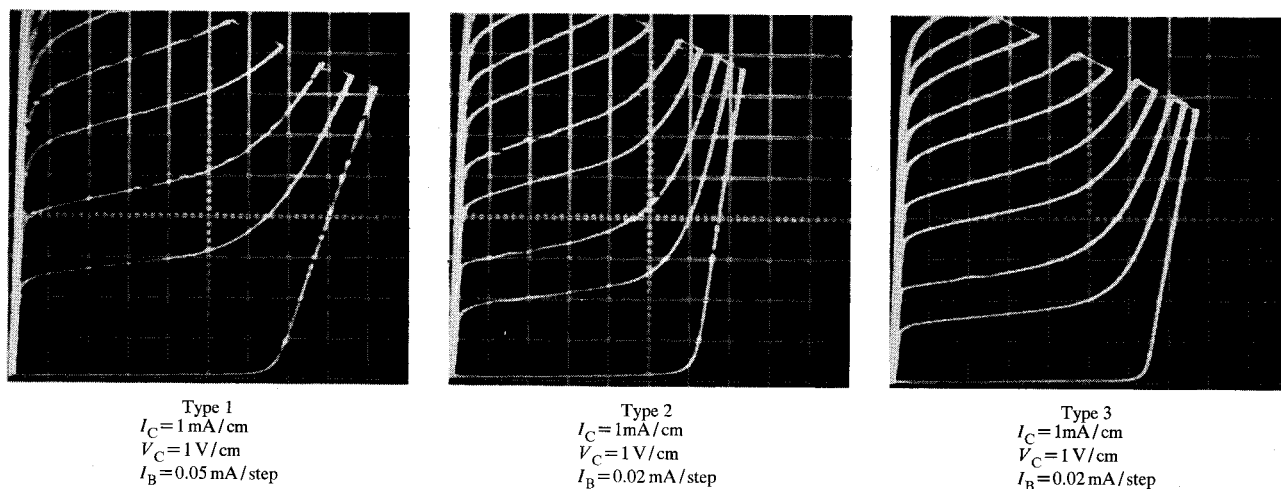
Four transistor geometries were included in the layout of the experimental chip. The geometries of the active areas are shown in Fig. 9. An 0.1-mil linewidth test transistor was used so the performance of the electron beam-fabricated devices could be compared with devices produced by a standard masking process. After annealing,  $\beta$  for the electron-beam processed test device compared favorably with that for an optically processed device of identical geometry. Starting with the  $p^-$  substrate, the process steps are:

- 1)  $n^+$  subcollector diffusion
- 2)  $n^-$  epitaxial deposition
- 3)  $n^+$  collector reach-through diffusion
- 4)  $p$  base diffusion

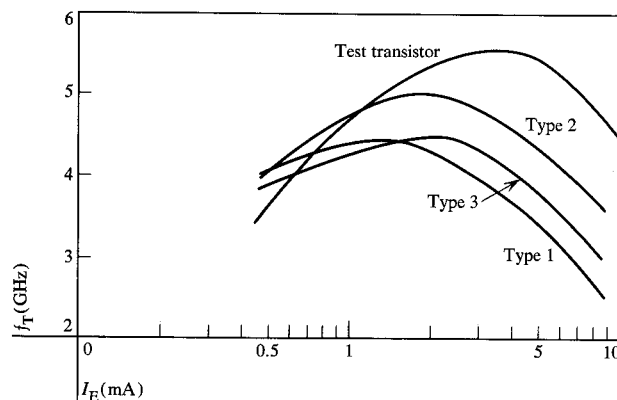
**Table 1** Typical dc characteristics.

| Transistor<br>type (Fig. 9) | $BV_{EBO}$<br>(V) | $BV_{CBO}$<br>(V) | $FV_{EBS}$<br>at 0.5 mA<br>(mV) | $FV_{EBS}$<br>at 10 mA<br>(mV) | $V_{EBS}$<br>(mV) | $\beta$<br>at 1 mA | $\beta$<br>at 10 mA |
|-----------------------------|-------------------|-------------------|---------------------------------|--------------------------------|-------------------|--------------------|---------------------|
| 1                           | 5.7               | 24                | 816                             | 948                            | 132               | 88                 | 35                  |
| 2                           | 5.7               | 24                | 800                             | 930                            | 132               | 110                | 50                  |
| 3                           | 5.7               | 24                | 799                             | 919                            | 120               | 110                | 60                  |
| Test                        | 5.7               | 24                | 785                             | 901                            | 116               | 145                | 85                  |

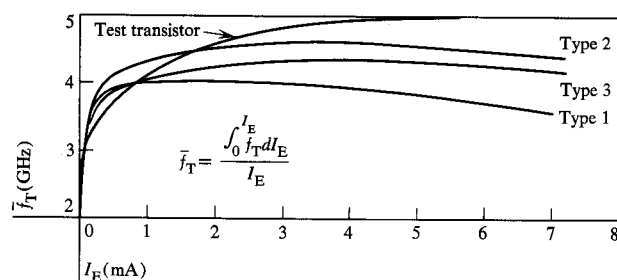
**Figure 10** Collector  $I$ - $V$  characteristics.



**Figure 11**  $f_T$  vs emitter current.



**Figure 12**  $\bar{f}_T$  vs emitter current



- 5) Pyrolytic silicon dioxide deposition
- 6)  $n^+$  emitter diffusion
- 7) Base contact
- 8) Metallization

These semiconductor processing steps are quite conventional, except for As emitter diffusion to improve device performance. The As emitter characteristics are discussed elsewhere[6], and the problems associated with metallization have already been discussed.

#### Device characteristics

The dc characteristics of the micron transistors are summarized in Table 1. These values were obtained on bonded devices after proper annealing. Both the emitter-base junction and the collector-base junction have a sharp breakdown and low leakage current. The values of  $\Delta V_{BE}$  are rather low, even for the Type 1 transistors, indicating that the contact resistances are quite small. The lower current gain values (Table 1) of the micron transistor are due to its higher emitter perimeter-to-area ratio and emitter side wall-to-area ratio. Figure 10 shows the common-emitter characteristics of these devices.

For the ac characteristics, Fig. 11 shows the gain-bandwidth product  $f_T$  as a function of emitter current. The peak value of  $f_T$  is approximately 5 GHz. In switch-

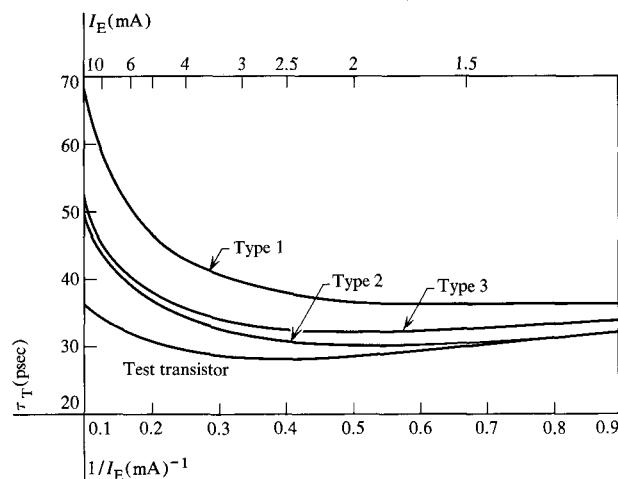


Figure 13 Transit time vs emitter current.

ing circuits it is important to know the average value of  $f_T$  over the range of operating current. The average value,  $\bar{f}_T$ , can be obtained by integration:

$$\bar{f}_T = \frac{\int_0^{I_E} f_T(I_E) dI_E}{I_E}.$$

The values of  $\bar{f}_T$  are shown in Fig. 12. Accurate measurement of very high values of  $f_T$  is rather difficult due to various parasitic effects. As a check of the measurement validity, the transit time  $\tau_T$  is also measured as a function of emitter current (Fig. 13). The agreement between the values of  $\tau_T$  and  $1/2\pi f_T$  is quite good.

Another important parameter for high speed operation is junction capacitance. The base-collector junction capacitance  $C_{BC}$  was measured as a function of reverse bias. The stray capacitances due to the header and metal lands are subtracted from the measured values; the results are shown in Fig. 14. As expected, the junction capacitance is lower for the smaller devices. The correlation between measured capacitances and calculated base area is quite good. The base resistance-collector capacitance time constant,  $R_B C_C$ , measured as a function of emitter current, is shown in Fig. 15. This time constant is very small for the micron devices, but the spread in the measured values is quite large.

## Conclusions

A practical method of making micron-size transistors utilizing an electron beam exposure system has been presented. The micron transistors display dc and ac characteristics comparing favorably with the best optically processed devices. The advantage of the small geometry appears as very low  $R_B C_C$  values. Practical use of the lift-off process provides narrow-linewidth, thick conductors. These results indicate that it is indeed possible

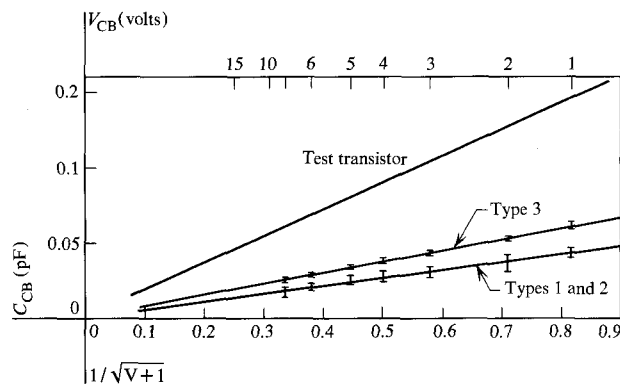
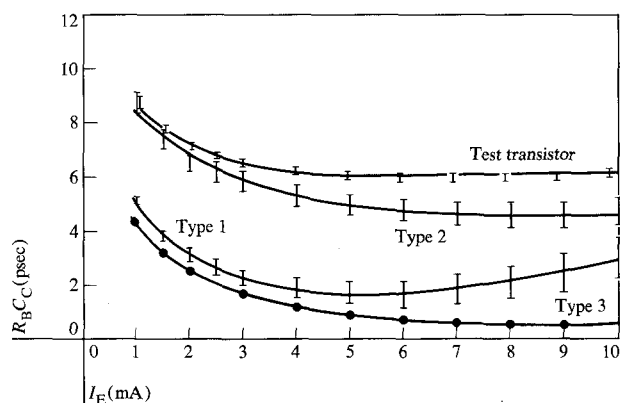


Figure 14 Base-collector junction capacitance vs reverse bias voltage.

Figure 15  $R_B C_C$  time constant vs emitter current.



to fabricate high performance devices utilizing the high resolution capability of the electron beam exposure system.

## References

1. R. F. M. Thornley and M. Hatzakis, "Electron-Optical Fabrication of Solid-State Devices," *Proc. 9th Annual IEEE Symposium on Electron, Ion and Laser Beam Technology*, San Francisco Press 1967, p. 94.
2. M. Hatzakis, "Electron Resist for Microcircuit and Mask Production," *J. Electrochem. Soc.* **116**, 1033 (1969).
3. J. J. Loferski and P. Rappaport, "Displacement Thresholds in Semiconductors," *J. Appl. Phys.* **31**, 1296 (1959).
4. N. C. MacDonald and T. E. Everhart, "Selective Electron-Beam Irradiation of Metal-Oxide Semiconductor Structures," *J. Appl. Phys.* **39**, 2433 (1968).
5. D. Green et al, *Appl. Phys. Letters* **6**, 3 (1965).
6. Papers on arsenic-emitter transistors, *IBM J. Res. Develop.* **15**, 457-477 (1971, this issue).

Received March 15, 1971

M. Hatzakis is located at the IBM Thomas J. Watson Research Center, Yorktown Heights, New York 10598; S. Magdo and C. H. Ting are located at the IBM Components Division Laboratory, E. Fishkill (Hopewell Junction), New York 12533.