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Planar Mesa Schottky Barrier Diode

Abstract: Planar silicon technology has been used to fabricate mesa Schottky barrier diodes with high breakdown voltages. This method proves to be superior to alternate methods used to increase the breakdown voltage of Schottky diodes. The processing techniques and characteristics of mesa Schottky diodes are described in this paper.

Introduction

A Schottky barrier diode is formed when a metal is brought into intimate contact with a semiconductor. The barrier depends on the work function difference between the metal and the semiconductor and the interface states at the metal-semiconductor interface. The current-voltage characteristic of a Schottky barrier can be explained[1] in terms of either the "diode" theory or the "diffusion" theory. When the usual approximations are made, both derivations result in essentially the same current-voltage dependence given by[1]

$$J = J_s[\exp(qV/nkT) - 1], \tag{1}$$

where J_s is the saturation current density given by

$$J_s = A^* T^2 \exp(-q\phi_b/kT); \tag{2}$$

A^* is the modified Richardson constant, T is the temperature in absolute scale, ϕ_b is the barrier height in volts, and n is the ideality factor ($n = 1$ for ideal diodes).

The usual method of fabricating Schottky barrier diodes is to start with a heavily doped n-type substrate and to deposit between 2 and 4 μm of high-resistivity (0.1 to 2 Ω-cm) n-type silicon. A thick oxide (6000 to 10,000 Å) is either grown or deposited on these wafers. Contact areas are made by opening "windows" in the oxide by the usual photo-resist techniques. After cleaning the window, a metal is sputtered or evaporated onto the wafer in a good vacuum and then metal patterns are etched.

The reverse breakdown of a Schottky barrier diode fabricated by using the technique above is lower than that of a p^+-n junction with the same n doping. This is due to the high electrostatic field at the edge of the metal-semiconductor contact[2] and is similar to the curvature effect in p-n junctions.

The high electrostatic field at the periphery [Fig. 1(a)], which causes premature breakdown, can be removed by using a p^+ guard ring surrounding the metal[2], as shown in Fig. 1(b). This method introduces a p^+-n junction in parallel with the Schottky barrier diode, accompanied by an increase in total capacitance of the junction. The resulting structure will have higher breakdown voltage and reduced switching speed. Another method that has been suggested[3] is to extend the metal layer over the thin oxide surrounding the contact [Fig. 1(c)]. This extends the reverse-biased depletion region and lowers the high electrostatic fringing field. The oxide should be thin (less than 1000 Å) for effectively increasing the breakdown voltage. This calls for a two-step etching process and also increases the capacitance of the junction.

Proposed structure and method of fabrication

Another method for increasing the breakdown voltage of the Schottky barrier diode is proposed here. This method does not increase the capacitance of the struc-

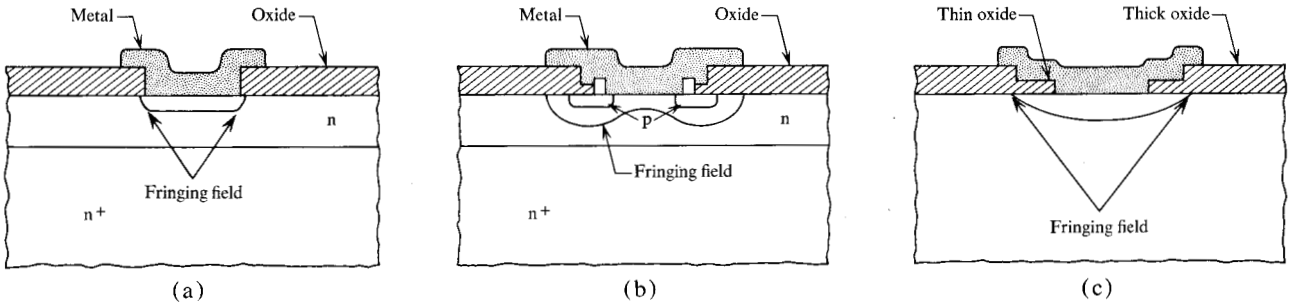


Figure 1 Reverse breakdown voltage of Schottky diode. (a) High electrostatic field at periphery; (b) p-n junction guard ring; (c) extended metal overlap.

ture and is compatible with planar technology. The proposed structure is a mesa Schottky barrier diode. Since the mesa is surrounded by thermally grown oxide on all sides, the peripheral fringing field is reduced, resulting in high breakdown voltage.

The process steps for fabricating mesa Schottky diodes are shown in Fig. 2. First, a lightly doped (0.2 to 1 Ω-cm) n-type epitaxial layer of 3 to 5 μm is deposited on a heavily doped n-type substrate [0.002 Ω-cm, Fig. 2(a)]. Silicon nitride is deposited on top of the epitaxial layer to a thickness of 1000 Å, and approximately 3000Å of pyrolitic oxide is deposited over the nitride [Fig. 2(b)]. Photolithographic techniques are used to etch the oxide everywhere except in the device area [Fig. 2(c)]. Next the oxide is used as a mask to etch the nitride everywhere except the device area [Fig. 2(d)], and then the oxide over the device area is removed [Fig. 2(e)]. This is followed by high-temperature oxidation of the wafers in an oxygen atmosphere. Since nitride is a good barrier for oxygen, no oxide grows under the silicon nitride. The oxide surrounding the silicon nitride creates a mesa structure [Fig. 2(f)]. The next step is removal of the nitride [Fig. 2(g)], followed by metallization and the final photolithographic process to etch the metal patterns [Fig. 2(h)].

Molybdenum-silicon and PtSi-Si Schottky diodes have been fabricated by using the technique described above. Small-area diodes are 1 mil in diameter and the large-area diodes (capable of carrying 1 A in the forward direction) are 20 mil in diameter (2×10^{-3} cm^2). Figure 3 compares the breakdown voltage of a small-area (1-mil dia.) PtSi-Si mesa Schottky diode with a regular diode of the same size fabricated with the same epitaxial resistivity (0.2 Ω-cm) and the same metal. The reverse breakdown obtained for the mesa diode is approximately the same as the breakdown for a Schottky diode with a p^+ guard ring. The forward characteristics of the diodes are nearly equal. Curve 1 of Fig. 4 shows the characteristics of a regular large-area PtSi-Si Schottky barrier diode. Curves 2 and 3 show the characteristics of a p^+ guard-ring diode

Figure 2 Processing steps for mesa Schottky diode.

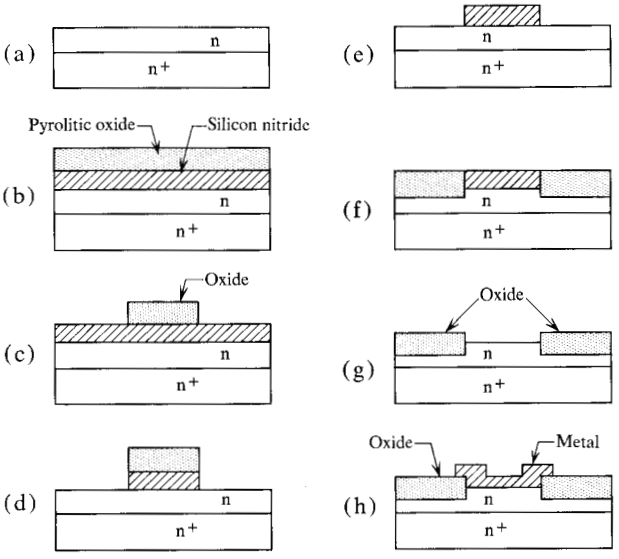
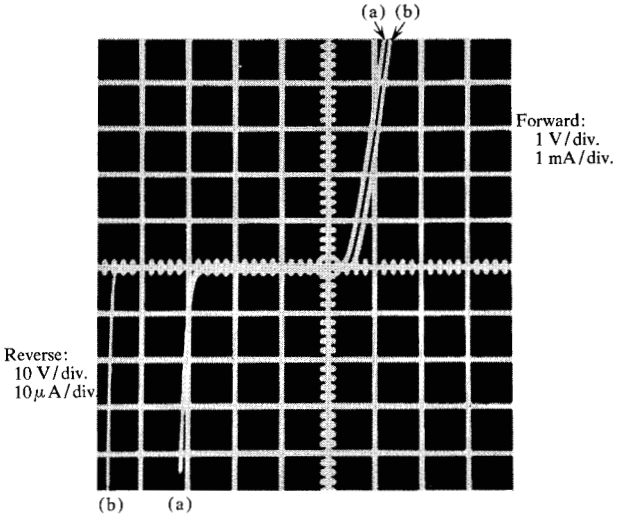


Figure 3 *I-V* characteristics of small-area Schottky diode (1-mil dia.). (a) Regular diode; (b) mesa diode.



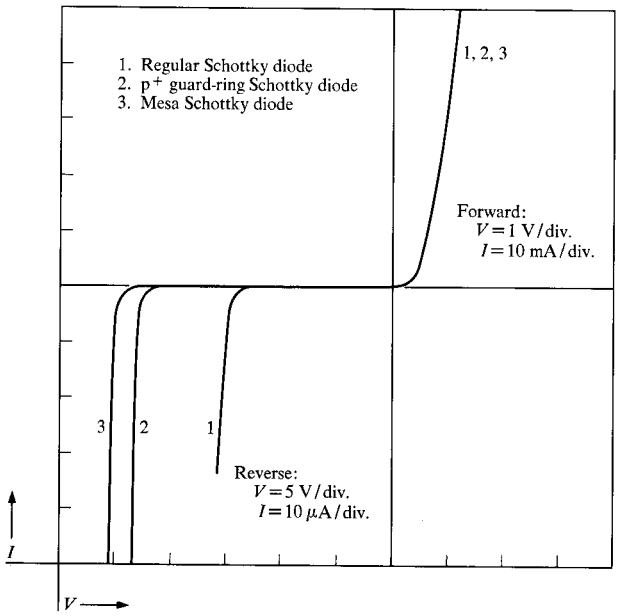
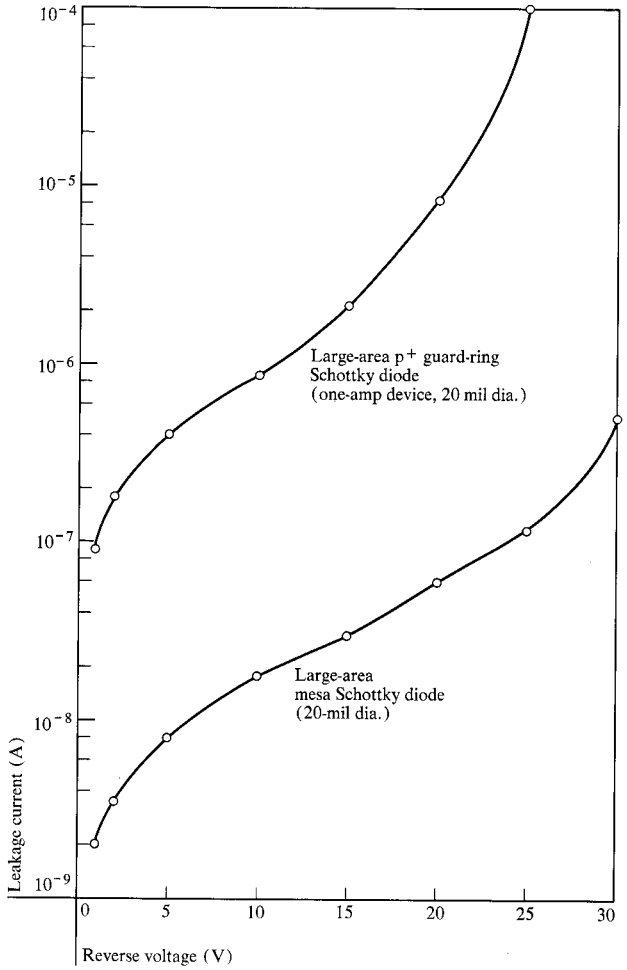


Figure 4 *I-V* characteristics of large-area Schottky diodes.

Figure 5 Leakage current vs reverse voltage of PtSi-Si diodes.



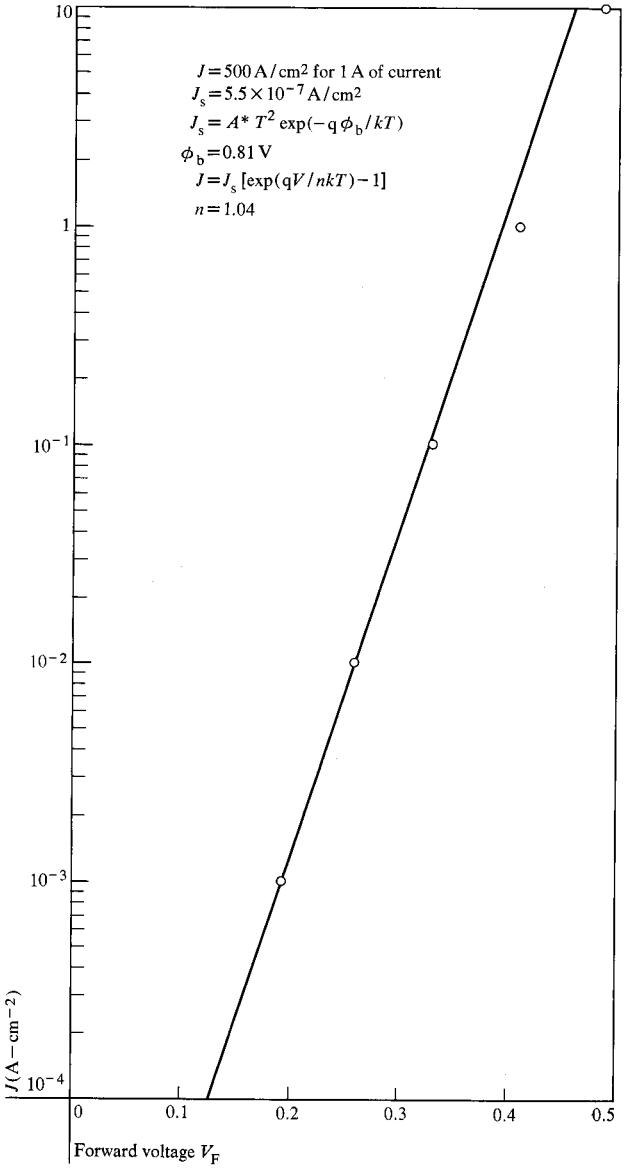


Figure 6 *I-V* characteristics of 1-ampere PtSi-Si diode.

and of a mesa Schottky diode, respectively. All the diodes in Fig. 4 were fabricated with the same epitaxial-layer resistivity and the same metal. The reverse breakdown voltage of the mesa diode is higher than that obtained with the p^+ guard-ring technique. This indicates that the mesa structure is more efficient in reducing the fringing field at the edge of the contact than a p^+ guard ring. No appreciable difference in breakdown voltage between a mesa structure and p^+ guard-ring structure was observed when the area of the diode was small (1-mil dia.).

The reverse leakage of a PtSi-Si large-area mesa Schottky diode is compared with a p^+ guard-ring diode of the same size in Fig. 5. We see that the leakage current

of the mesa diode is significantly lower than that of the p^+ guard-ring diode. The forward current vs voltage of the large-area mesa Schottky diode is shown in Fig. 6. The saturation current density was determined by extrapolating the *I-V* characteristic to zero voltage. The barrier height calculated from the saturation current J_s and Eq. (2) is 0.81 eV. The capacitance-voltage relation of the large-area mesa Schottky diode is shown in Fig. 7, where $1/C^2$ is plotted against reverse bias.

The barrier height ϕ_b is calculated by using the relation[4]

$$\phi_b = V_i + \phi_F + \frac{kT}{q} - \Delta\phi, \tag{3}$$

where V_i is the intercept of the $1/C^2$ vs voltage line on the x axis, ϕ_F is the Fermi potential calculated from the knowledge of doping concentration, and $\Delta\phi$ is the image force lowering of the barrier height. The barrier height calculated from the capacitance-voltage relation is 0.834 eV. This compares well with the value of 0.83 to 0.85 eV reported by other investigators[2,5].

Conclusions

The planar mesa Schottky diode structure has been fabricated. The process of fabrication is conventional and compatible with integrated circuit techniques. It has been shown that the breakdown voltage of these diodes can be increased without increasing the capacitance, thus allowing higher switching speed and improved microwave performance.

The results indicate that the mesa planar structure is preferable to the p^+ guard ring method for obtaining high break-down voltage for large-area diodes.

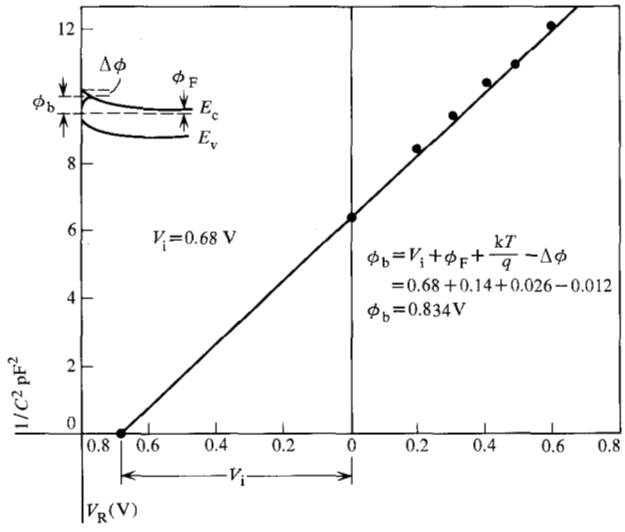


Figure 7 Plot of $1/C^2$ vs voltage of PtSi-Si diode.

References

1. For example, see S. M. Sze, *Physics of Semiconductor Devices*, Wiley-Interscience Publishers, New York 1969.
2. M. P. Lepselter and S. M. Sze, *Bell System Tech. J.* **47,** 195 (1968).
3. A. Y. C. Yu and C. A. Mead, *Solid State Electron.* **13,** 97 (1970).
4. S. M. Sze, *op. cit.* p. 404.
5. H. Jäger and W. Kosak, *Solid State Electron.* **12,** 511 (1969).

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