H. N. Ghosh
K. G. Ashar
A. S. Oberai
D. DeWitt

# Design and Development of an Ultralow-Capacitance, High-Performance Pedestal Transistor

**Abstract:** High-performance transistors with small geometries require a highly doped collector region to produce a large impurity gradient at the collector-base junction. This allows the structure to sustain high current densities and to attain low collector series resistance. However, the resulting increase in collector transition capacitance degrades the ac characteristics of the transistors. A structure is proposed and experimental results are presented in this paper to demonstrate that the conflicting requirements above, which limit the high-performance characteristics of transistors, can be resolved by the planar IC process.

## Introduction

Analysis of transistor switching circuits to determine the sensitivity of circuit speed to device parameters has established[1] that collector-to-base capacitance, base resistance, and gain bandwidth $f_T$ are important in that order. Base resistance and emitter capacitance have been decreased by decreasing emitter width. However, inherent in modern planar technology is the fact that much of the collector-base junction lies outside the active region of the transistor and the resulting parasitic capacitance does not scale down with the decrease in emitter width. This parasitic capacitor is further enhanced by increasing the effective doping in the collector to permit the transistor to operate at the increased current densities required for small, high-performance devices. The purpose of this paper is to suggest a structure that provides a high doping in the active collector region but a low doping in the parasitic region, thus providing a high current density capability on the one hand, with minimal base-to-collector parasitic capacitance on the other.

Integrated circuit technology has introduced still another important parameter: collector-to-isolation capacitance. A low doping in the collector epitaxial layer will reduce this capacitance. Oberai and Dhaka[2] have studied the trade-offs among these various design parameters for a three input emitter-follower current switch. A lumped model (Fig. 1) of the transistor, including high-level effects such as emitter crowding, was used for this study. Intrinsic base resistance has been modeled by a parallel RC network equivalent to the distributed effects derived in Ref. 3. The gain bandwidth product $f_T$ in the model is similar to the arsenic emitter ($0.1 \times 0.8$ mil) device[4]. Note from Fig. 2 that collector-to-base capacitance and collector-to-isolation capacitance play a dominant role in limiting further reduction of circuit propagation delays.

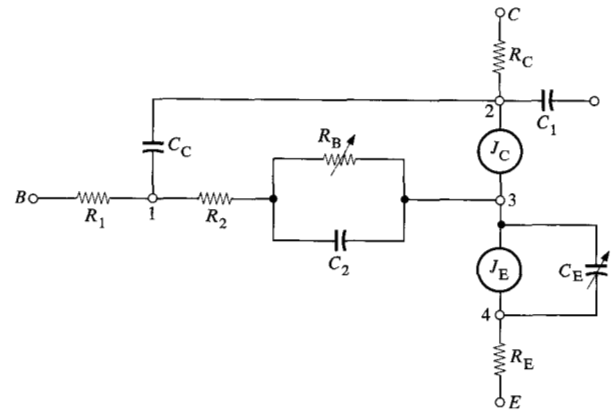



**Figure 1** Model of the transistor used for speed computations.

The idea of a limited-base transistor to reduce collector capacitance by the etching process was proposed earlier

by S. L. Miller[5]; and a limited-base structure made by the epitaxial refill method, by H. N. Yu[6]. The present process achieves similar results by conventional diffusion and epitaxial growth as applied in the conventional IC process. Thus both of the performance limitations mentioned above have been reduced drastically in this structure, which has been called the pedestal transistor. Use of the arsenic emitter permits a further reduction in the device dimensions because of the inherent superiority of arsenic over phosphorus. Consequently, significant improvement in over-all circuit performance results, as demonstrated[2] later in this paper.

### Description of the structure

The pedestal transistor derives its name from having a pedestal-like, highly-doped collector region in the intrinsic active transistor area. [Compare the vertical region XX′ in Fig. 3(a) with that of 3(b).] Unlike the conventional transistor in Fig. 3(a), the pedestal transistor, Fig. 3(b), is made of two epitaxial layers, both of which are grown without any added dopant except for what is added through auto-doping. The process starts with the diffusion of an arsenic buried layer into a p-type substrate, followed by growth of the first epitaxial layer ($\approx 2\ \mu$m), as in a conventional process. The buried layer has the dimensions needed to bring a collector contact to the surface. After the first epitaxial growth, an extra arsenic buried-layer diffusion is made. It has the same dimensions as the emitter and is located below it. Boron is then diffused into the isolation area, and the second epitaxial layer ($\approx 2\ \mu$m) is grown. The base diffusion into the second epitaxy runs into the upper buried layer, giving a high capacitance per unit area (0.6 pF/mil$^2$) but only over the small area of the emitter. However, the actual base diffusion area is an order of magnitude greater than the active emitter area in a typical double-base stripe, single-emitter stripe design. Since the epitaxy is very lightly doped (1 to 4 Ω-cm), the collector-to-base capacitance per unit area outside the active region is reduced to about one-fourth that within the region. Thus, total collector-to-base capacitance $C_{CB}$ is expected to be reduced by a factor of 2 to 3 by the pedestal transistor process.

The isolation is completed by outdiffusion of boron during the second epitaxial growth and heat treatment in subsequent processing. This mid-isolation scheme, in contrast to conventional isolation diffusion from the top, allows a shorter diffusion heat cycle and increased packing density resulting from the narrower lateral diffusion. In spite of a slightly larger collector isolation junction area than in the conventional non-pedestal process, the collector-to-isolation capacitance is also reduced because of the high-resistivity epitaxial layers in the pedestal transistor. Note that if such lower doping (2 to 5 × $10^{15}$ cm$^{-3}$) in the epitaxial layer is used in the conventional transistor, severe base widening at current densities above 5000 A/cm$^2$ will result in a sharp fall of current gain and gain bandwidth $f_T$. Hence, very small emitter geometries cannot be used with high-resistivity epitaxy. However, in the pedestal transistor, high doping ($10^{17}$ to

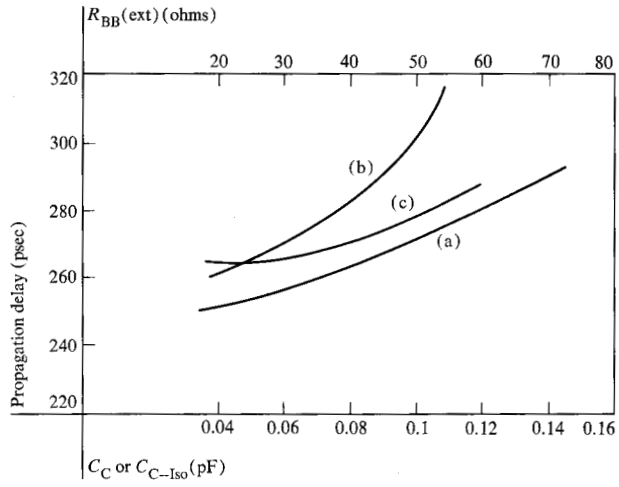
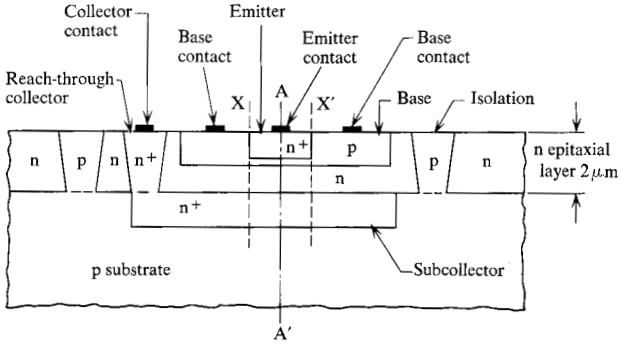
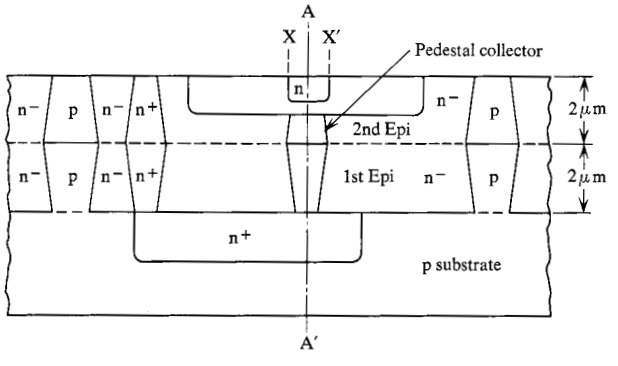



**Figure 2** Circuit delay (3-input gate) vs (a) base resistance $R_{bb}$ (extrinsic) for $C_C = 0.07$ pF and $C_{C\text{-}Iso} = 0.09$ pF; (b) collector-to-base capacitance $C_C$ for $R_{bb}$ (ext) = 36 Ω and $C_{C\text{-}Iso}$ = 0.09 pF; (c) collector-to-isolation capacitance $C_{C\text{-}Iso}$ for $R_{bb}$ (ext) = 36 Ω and $C_C = 0.07$ pF.

**Figure 3** (a) Typical planar transistor; (b) pedestal transistor.




(a)




(b)

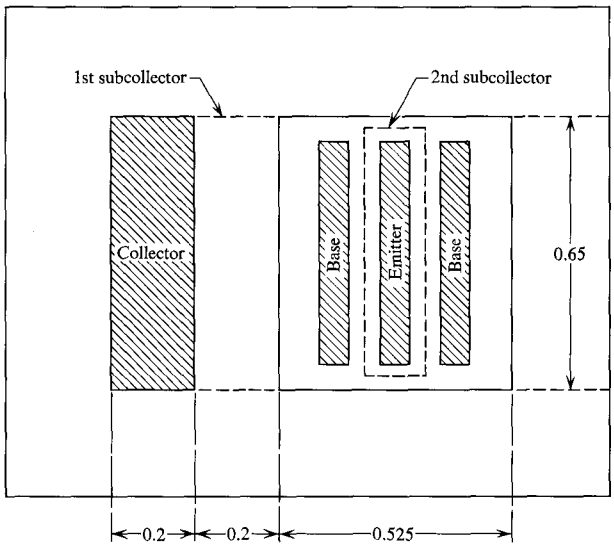
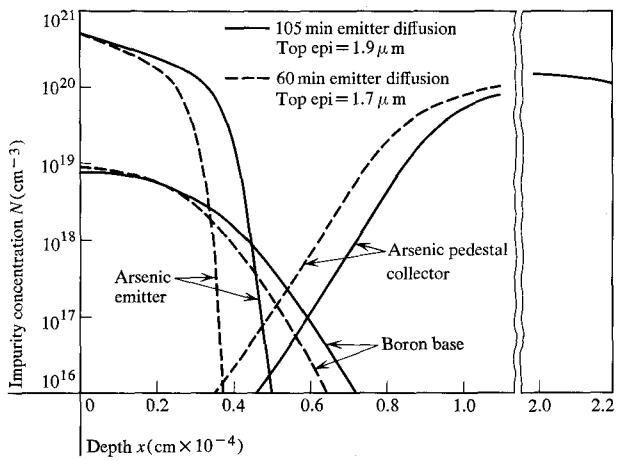



**Figure 4** Device horizontal geometry. Emitter, base stripes, and spacing between stripes are 75 $\mu$in. Pedestal is 25 $\mu$in. larger all around the emitter stripe. Emitter stripe length is 0.5 mil.

**Figure 5** Impurity profile simulated by process model.




$10^{18}$ cm$^{-3}$) is maintained in the intrinsic collector region only and thus such deterioration of high-frequency performance is prevented, even at current densities as high as 60,000 A/cm$^2$.

Hence, for operating current ranges of 3 to 10 mA, very small structures with an 0.1-mil (and smaller) wide and 0.3-mil long emitter could be fabricated to give good performance. Such small geometries (Fig. 4) in addition to providing increased component density, produce very low collector-to-base and collector-to-isolation capacitances. A high-resistivity epitaxial layer also allows the fabrication of Schottky-barrier diodes in the same chip

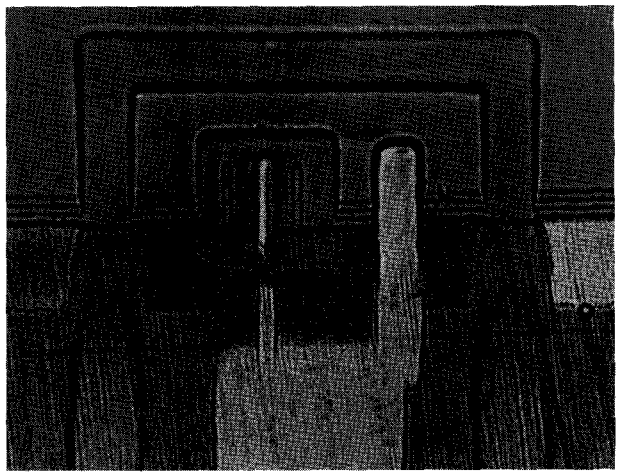


**Figure 6** Cross section of a pedestal transistor.

for use as clamps across the collector-base junction to provide high-performance operation of the switch in the saturated mode with lower power dissipation. Smaller collector capacitance and higher $f_T$ also produce smaller capacitive loading of the transmission line and allow a higher terminating resistance at the end of the line, reducing power dissipation.

The control of epitaxy is no greater than that required for a single-epitaxial-layer device with the base running into the buried layer, since the first epitaxial step is not critical. The impurity distribution of a pedestal transistor with a boron base, an arsenic emitter, and an arsenic collector is shown in Fig. 5. The profile was generated by computer simulation of the process using diffusion, oxidation, and epitaxial growth models. Note the penetration of the base region by the collector profile and the influence of emitter diffusion time on the total impurity distribution. The cross section of a fabricated pedestal transistor in Fig. 6 indicates the difference in the doping level between the $n^+$ pedestal collector and adjacent $n^-$ epitaxial layers.

It may be worthwhile to discuss the expected performance improvement in the pedestal transistor for typical impurity profiles as shown in Fig. 5. The predicted gain bandwidth and $C_{CB}$ for 0.1 × 0.5 mil emitter and 0.1 mil spacings are 6–9 GHz at $I_E = 7$ mA, $V_{CB} = 0$ V and $C_{CB} = 0.12$ pF at $V_{CB} = 0$ V. For a 0.1 × 0.3 mil emitter, $C_{CB}$ reduces further to 0.08 pF.

Tables 1 and 2 in the next section on experimental results show that the above assessment of the potential performance improvement in the pedestal transistor as compared with the nonpedestal structure is fairly accurate. Hence the complexity of the process can be justified where high performance, such as subnanosecond circuit performance, is desired.

**Table 1** Performance data for pedestal and conventional transistors with 0.1 × 0.5 mil arsenic emitters.

| *Parameters* | *Pedestal* | *Conventional* | *Bias* |
|---|---|---|---|
| $C_{CB}$ (with land capacitance ≈ 0.05) | 0.13 pF | 0.24 pF | $V_{CB} = 0$ |
| $C_{C\text{-}Iso}$ | 0.18 pF | 0.27 pF | $V_{C\text{-}Iso} = 0$ |
| Typical $f_T$ for $R_{DB} = 10\ k\Omega/\square$ | 5 GHz | 4.9 GHz | $V_{CB} = 0.5$ V; $I_E = 5$ mA |

**Table 2** Performance data for pedestal transistors having arsenic emitters of various geometries.

| *Device (Emitter size)* | *Parameter* | *Bias Conditions* $V_{CB}(V)$ | $I_E(mA)$ |
|---|---|---|---|
| | Peak $f_T$(GHz): | | |
| 1 (0.1 × 0.5 mil) | 6–8 | +0.5 | 7.0 |
| 2 (0.1 × 0.3 mil) | 5–7 | +0.5 | 4.0 |
| 3 (0.075 × 0.5 mil) | 10 | +0.5 | 3.0 |
| | Beta: | | |
| 1 | 100–240 | | 0.5 |
| | 70–120 | | 10.0 |
| 2 | 80–200 | +0.5 | 0.5 |
| | 45–90 | | 10.0 |
| 3 | 230 | | 0.5 |
| | 130 | | 10.0 |
| | $C_{CB}$: | | |
| 1 | 0.13 | | |
| 2 | 0.1 | 0 | |
| 3 | 0.08 | | |
| | $C_{C\text{-}Iso}$(pF): | | |
| 1 | 0.12 | | |
| 2 | 0.08 | $V_{C\text{-}Iso} = +3$ V | |
| 3 | 0.09 | | |

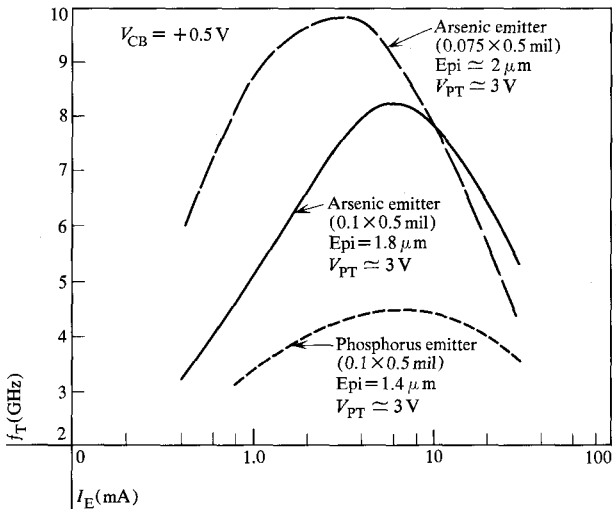
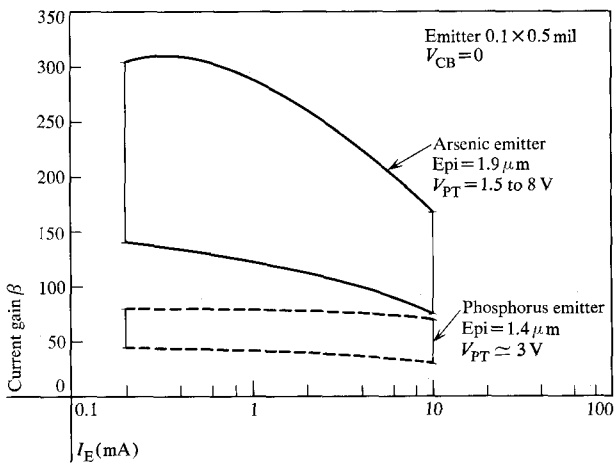



**Figure 7** Gain bandwidth $f_T$ for arsenic and phosphorus emitter pedestal transistors. (All devices have the pedestal structure.)

**Figure 8** Current gain for arsenic and phosphorus emitter pedestal transistors.




Extensive computer calculations with reduced stripe lengths (less than 0.5 mil) indicated no significant improvement of the average propagation delay in a fully loaded CSEF (current-switch emitter follower) circuit. Hence, from the consideration of lower contact resistance, a 0.5 mil emitter stripe length was used. Reduction of emitter stripe width, however, predicted a delay reduction to about 185 psec/circuit for spacing and stripe widths of 0.075 mil, which compares favorably with experimental results given in the next section.

## Experimental results

The results of testing a pedestal transistor processed with a 105-min. arsenic emitter diffusion and a 0.1 × 0.5 mil emitter geometry are shown in Fig. 7 for $f_T$ and Fig. 8 for current gain (beta). Note that further improvement in performance is achieved with an emitter mask of 0.075 × 0.5 mil as compared with the 0.1 × 0.5 mil device, even though both have comparable punch-through voltages. It has been shown in[4] that use of the arsenic emitter improved transistor performance by a factor of 1.6 to 2 over that with a phosphorus emitter. It is interesting to note from Fig. 7 that even for the pedestal structure the use of an arsenic emitter increased $f_T$ by a factor of 1.8 over that with a phosphorus emitter.

Performance data for pedestal and conventional transistors with arsenic emitters are compared in Table 1. Note that an over-all improvement of 50% has been

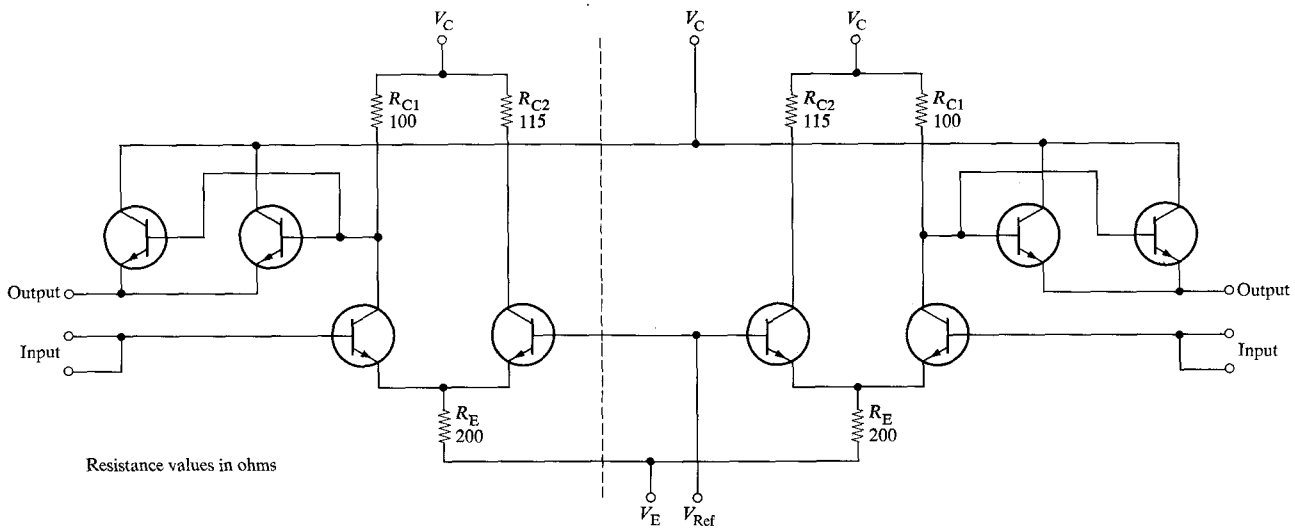
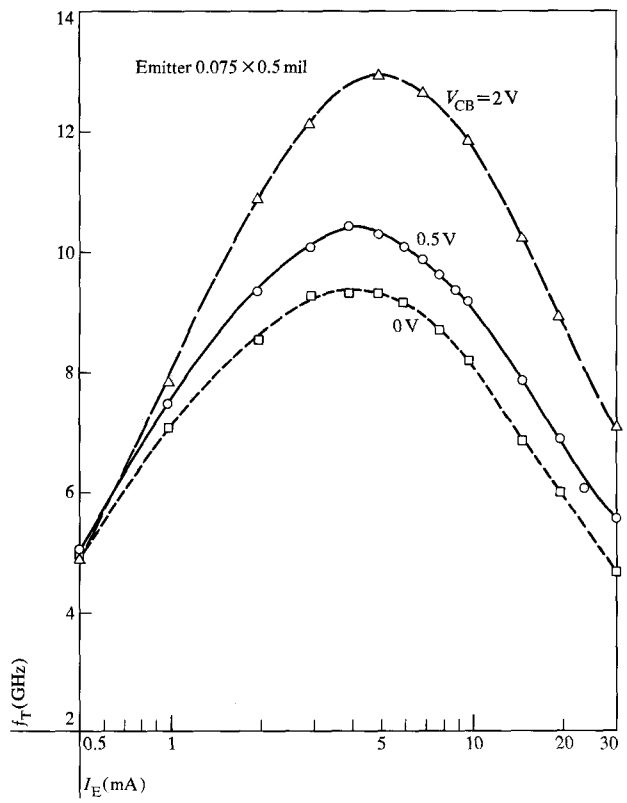



**Figure 9** Current switch emitter follower circuit.

**Figure 10** $f_T$ vs $I_E$ for 0.075 × 0.5 mil emitter measured at 400 MHz.




achieved in pedestal transistor capacitances in contrast with state-of-the-art nonpedestal transistors. At the circuit level, propagation delay for a current switch emitter follower circuit (Fig. 9) with a fan-in of three, a fan-out of one and an emitter mask of 0.1 × 0.5 mil has improved from 450 psec for nonpedestal transistors (conventional transistor structure) to 300 psec for pedestal devices, both types having arsenic emitters.

Performance data for various geometries are presented in Table 2. Also note from Fig. 10 that further improvement of gain bandwidth in operable devices up to 12.4 GHz is feasible in silicon technology from the combined results of small geometries, the arsenic emitter, and the pedestal collector. The emitter geometry of this device is 0.075 mil$^2$.

A hybrid emitter follower current switch with no fan-in and no fan-out and an emitter size of 0.1 × 0.5 mil has produced 190 psec by fabricating[2] a similar circuit with an emitter area of 0.075 × 0.5 mil. W. J. Kleinfelder and B. Malbec extended the development of the arsenic emitter pedestal transistor when they processed an 11-stage ring of machine worst-case paths. It consisted of six different chips of feedback CSEF circuits[7] in tandem, and it incorporated pedestal transistors of 0.1-mil emitter width and 0.2 mil spacings between stripes. Total delay observed (with an average fan-in of 3 and fan-out of 5) was 6.4 nsec, including 1.85 nsec cable delay and 0.55 nsec package delay. The net delay for the circuitry alone was 360 psec per stage (average) in the above system environment, which was designed to emulate practical application in large, fast machines. A similar model with nonpedestal transistors ran about 500 psec.

## Conclusions

A novel high-speed transistor structure has been described. Such structures have been shown to improve both circuit propagation delay and capacitive loading and to allow the use of extremely small geometries for increased component density.

## Acknowledgments

The authors thank Messrs. W. Rosenberg, A. Spiro, P. Melzer, R. Wilberg, T. Nagasaki, R. Joy and S. Magdo for their efforts during the various phases of this development effort. The assistance of L. Weiss and A. Pinck in device and circuit-speed measurements is greatly appreciated.

## References

1. K. G. Ashar, H. N. Ghosh, A. W. Aldridge and L. J. Patterson, *IBM J. Res. Develop.* **7,** 207 (1963).
2. A. S. Oberai and V. A. Dhaka, "Ultrahigh-Speed Current Switch Using a 12.6-GHz Silicon Transistor," presented at the IEEE Electron Devices meeting, Washington, D. C., October 1968.
3. H. N. Ghosh, *IEEE Trans. Electron Devices* **ED-12,** 513 (1965).
4. H. N. Ghosh, A. S. Oberai, J. J. Chang and M. B. Vora, *IBM J. Res. Develop.* **15,** 457 (1971, this issue).
5. S. L. Miller, U.S. Patent 3,220,896, November 30, 1965.
6. H. N. Yu, IBM Research Division, Yorktown Heights, N. Y., U.S. Patent 3,312,881, April 4, 1967; USP Re 27,045 February 2, 1971.
7. K. F. Matthews and L. Weiss, "Feedback Current Switching Circuits—General Concepts," *1970 IEEE International Convention Digest*, p. 254.

*Received April 16, 1971*

*The authors are located at the IBM Components Division Laboratory, E. Fishkill (Hopewell Junction), New York 12533.*