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A Self-Isolation Scheme for Integrated Circuits

Abstract: A self-isolation scheme is proposed for fabricating transistors in semiconductor integrated circuits. Such integrated circuits with double-diffused transistors require three diffusions and one epitaxial layer in the proposed process. Since no isolation or reach-through diffusions are involved, this technique could reduce the area of a memory or logic cell by 50% or more.

Introduction

Since the advent of planar silicon technology and its application in the fabrication of npn bipolar transistors, several integration schemes have been proposed. The most critical processing steps in planar technology are the diffusion of impurities into silicon at high temperature, the epitaxial vapor growth of a single-crystal silicon layer on a silicon substrate, and the selective etching of thermally grown oxide on silicon wafers with photoresists. The most commonly used structure, which utilizes epitaxy and diffusion to their fullest advantage, is shown in Fig. 1. Typical dimensions are as indicated. The complete fabrication process, in brief, is as follows: On a p^- substrate, an n^+ subcollector diffusion is made selectively, followed by an epitaxial growth of n^- type silicon. The next step is to make p^+ isolation diffusion to define n-type isolation pockets. Then, p^+ base and n^+ emitter diffusions are carried out. Finally, contact "windows" are opened through the insulation layer, and a metallic interconnection pattern is etched.

The reverse-biased pn junction surrounding each n pocket isolates each bipolar transistor within it from the ones in other pockets. The buried n^+ subcollector ensures low collector series resistance, and at the same time n epitaxy allows high collector-base breakdown voltage and low collector-base capacitance. The double-diffused p^+ base region and n^+ emitter region ensure high emitter efficiency and good basewidth control, which in turn yields superior common emitter current gain (h_{FE}) and cut-off frequency (f_T) characteristics.

When one considers modifying the structure described above, to obtain higher performance and density, it is important to examine the limitations of the epitaxy, diffusion, and photo-resist processes. The epitaxial silicon deposition process offers good control of doping in the low impurity concentration range ($10^{16} - 10^{18}$ cm^{-3}), but poor thickness control. Solid state diffusion of impurities (surface concentration $C_0 \geq 10^{19}$ cm^{-3}) into silicon allows formation of a pn junction at a dpeth that can be predicted fairly accurately. With low surface concentration ($\leq 10^{17}$ cm^{-3}), however, the formation of very deep junctions ($\geq 5\ \mu$m) is very difficult. Photo-resist limitations are well known. With present-day techniques, device geometries <0.10 mil wide are difficult to implement for LSI application. A number of structures have been proposed to improve performance[1] or density[2–4]. Each scheme, however, requires design "tradeoffs" in terms of performance, density and reproducibility. For example, one widely pursued effort is aimed at modifying the basic structure of Fig. 1, by making narrower bases and thinner epitaxial layers.

Thin epitaxy permits shallower isolation diffusions and hence reduced lateral diffusion, resulting in less spacing between devices. The limit of the epitaxial layer thickness is approached when base and subcollector outdiffusion meet, as shown by the dashed lines in Fig. 1. When this happens the current-carrying capability of the transistor increases significantly, but the basewidth becomes extremely sensitive to epitaxy variation.

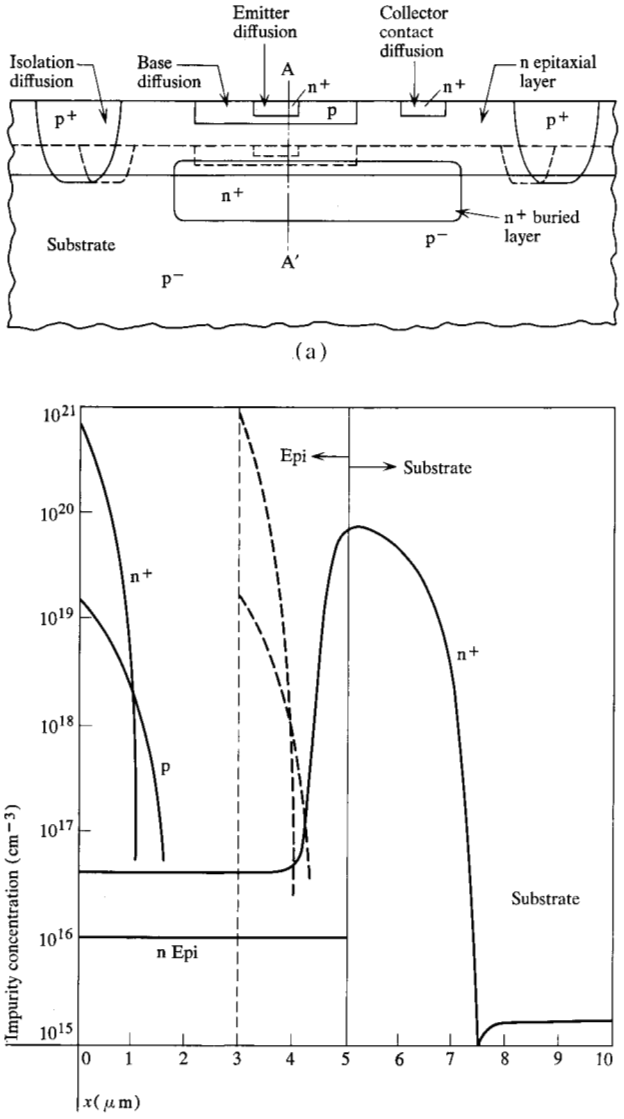


Figure 1 (a) Section of an integrated bipolar transistor made by conventional methods; (b) impurity profile along AA′.

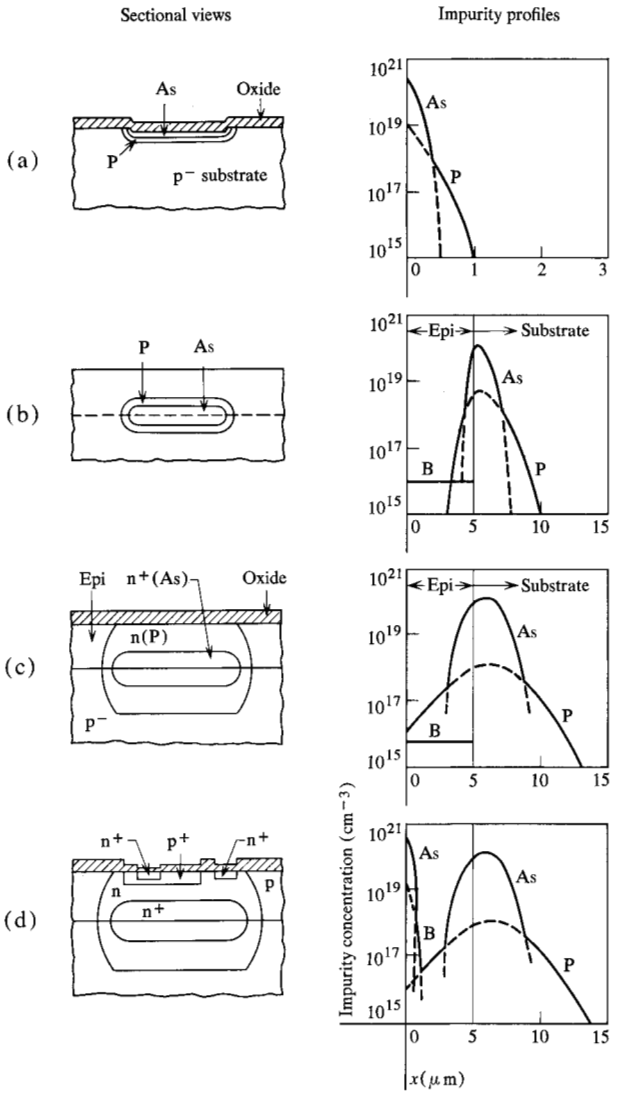
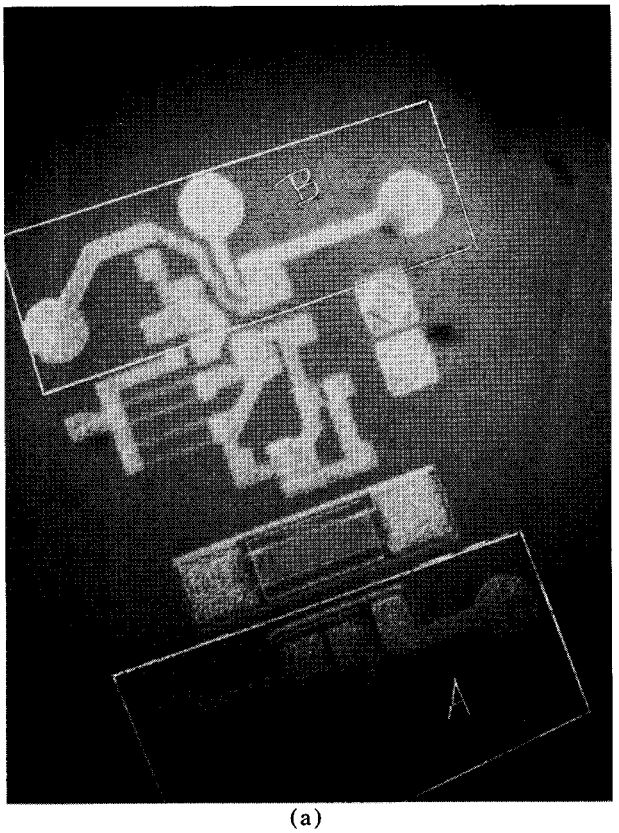


Figure 2 Sections and impurity profiles at various processing stages for transistor made by proposed self-isolation scheme. (a) Buried layer diffusion; (b) expitaxial deposition; (c) high-temperature oxidation; (d) base and emitter diffusion.

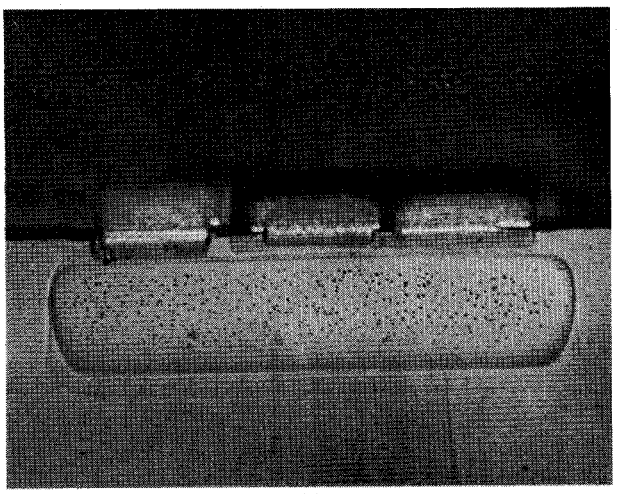
The approach described below permits higher density than the conventional structure of Fig. 1, while maintaining basewidth control that is comparable to that of the convential structure.

Description of concept

This paper describes an integration scheme that does not require an isolation diffusion step. Consequently, one oxidation and one masking step are also eliminated. As shown in Fig. 2(a), one starts with a p^- silicon wafer, oxidizes it, and then performs a photo-resist step to open a window for the subcollector diffusion. At this point, two types of impurities, high-concentration arsenic (2×10^{20} cm^{-3}) and low-concentration phosphorus (10^{19}), are diffused sequentially or simultaneously into the same window. The resulting impurity profile is also shown. The wafer is oxidized and stripped and made ready for epitaxial deposition. Now about 5 μm of p-type silicon is deposited by epitaxy. During the deposition step, arsenic and phosphorus outdiffuse into the epitaxial layer, as shown in Fig. 2(b). The impurity profile at this stage is also shown. Phosphorus outdiffuses much faster than arsenic. The next step is to oxidize the wafer at high temperature so that phosphorus comes up to the surface while the n^+ arsenic layer is still far below. Thus, an n phosphorus pocket with a buried n^+ arsenic layer and a



(a)



(b)

Figure 3 A finished chip fabricated by the self-isolation process, showing (a) two transistors and (b) a section view of device A.

surrounding p region is formed, as shown in Fig. 2(c). In the n pocket one can now make p^+ base and n^+ emitter diffusions, as shown in Fig. 2(d). The low concentration in the phosphorus-doped n region assures high collector-to-base breakdown voltage BV_{CBO}, while the n^+ buried layer permits low collector series resistance.

Experimental results

The proposed method has been used to make some bipolar transistors. On a p^- substrate, 5000 Å of SiO_2 are thermally grown at 970°C. Windows are opened for subcollector diffusion, which is made in two steps. First, phosphorus is diffused by the open-tube method at 900°C for 30 min. A sheet resistivity (ρ_s) of 45 Ω/□, a junction depth (x_j) of 0.02 mil, and a C_0 of 10^{20} cm^{-3} are obtained. A thin layer of P_2O_5 glass is also formed, which is immediately stripped after diffusion, still leaving the original thermal oxide intact. In the second step, arsenic is diffused through the same window by capsule diffusion at 1100°C for 5 hours. The source powder has a concentration of 5×10^{20} cm^{-3}. The resulting ρ_s is 2.3 Ω/□ and x_j is 0.12 mil.

The wafer is then reoxidized at 1200°C in dry oxygen for 60 min, followed by steam oxidation for 24 min. About 6000 Å of SiO_2 are formed. The high-temperature oxidation serves two purposes: to produce a visible step in the silicon at the subcollector-mask boundaries for further mask alignment after subsequent epitaxial deposition of silicon, and to lower the phosphorus concentration from 10^{20} to 10^{19} cm^{-3}. During this cycle, phosphorus forms a pn junction as deep as 0.18 mil. Then all the SiO_2 from the surface of the wafer is removed and a layer of p-type silicon is deposited epitaxially. Thickness of the silicon layer is 5 μm, and resistivity is 2 Ω-cm. At the end of the silicon deposition, phosphorus outdiffuses 2 μm from the subcollector. Outdiffusion of arsenic is less than 1 μm. The wafer is reoxidized again at 1200° C for 60 min in oxygen and 24 min in steam. This cycle is designed so that phosphorus outdiffuses up to the surface, and the slower arsenic impurities remain about 2 μm below the surface. Thus, one has an n-pocket surrounded by a p region, with a buried n^+ layer in the pocket. A window in the oxide over the n-pocket is opened, and boron base diffusion is made with a ρ_s of 70.4 Ω/□ and an x_j of 0.02 mil. Another reoxidation follows, resulting in a ρ_s of 170 Ω/□ and an x_j of 0.03 mil. After windows for emitter diffusion and contact diffusion are opened, arsenic is diffused to form an 0.030-mil emitter junction and a basewidth of 0.015 mil. Finally, base contact windows are opened, and Al is deposited and subetched.

Top and sectional views of the device are shown in Fig. 3.

Electrical characteristics

The common emitter current gain h_{FE} and cut-off frequency f_T of these transistors have been measured as a function of emitter current, and are plotted in Fig. 4. Cut-off frequency f_T is defined as the frequency at which small signal common-emitter current gain h_{FE} reaches unity. The collector-base capacitance was 0.18 pF/mil^2 and

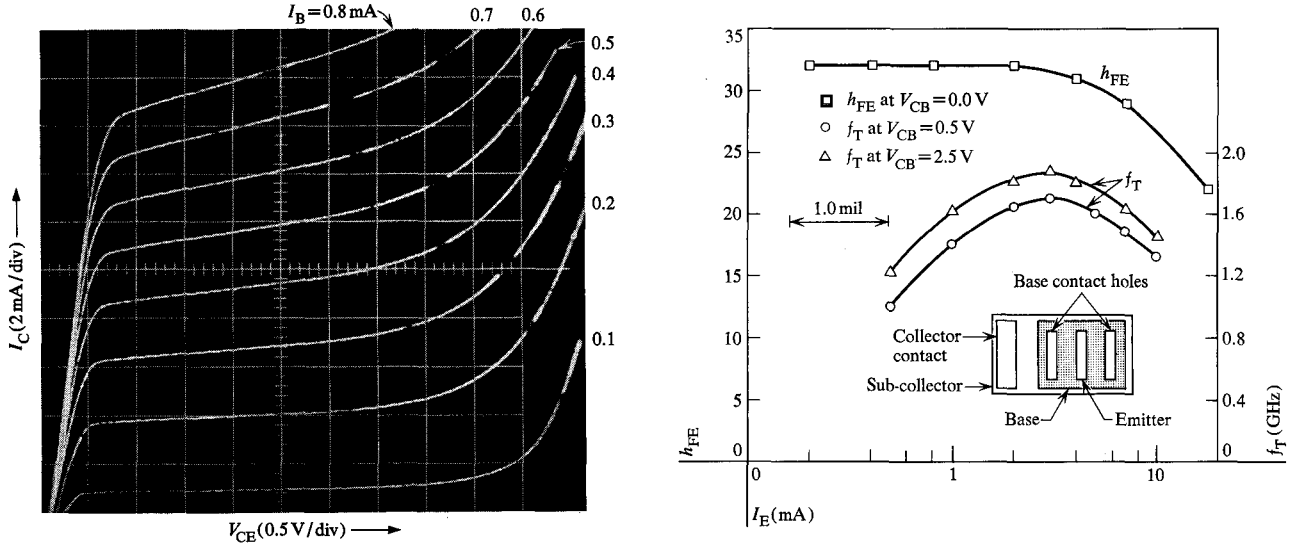
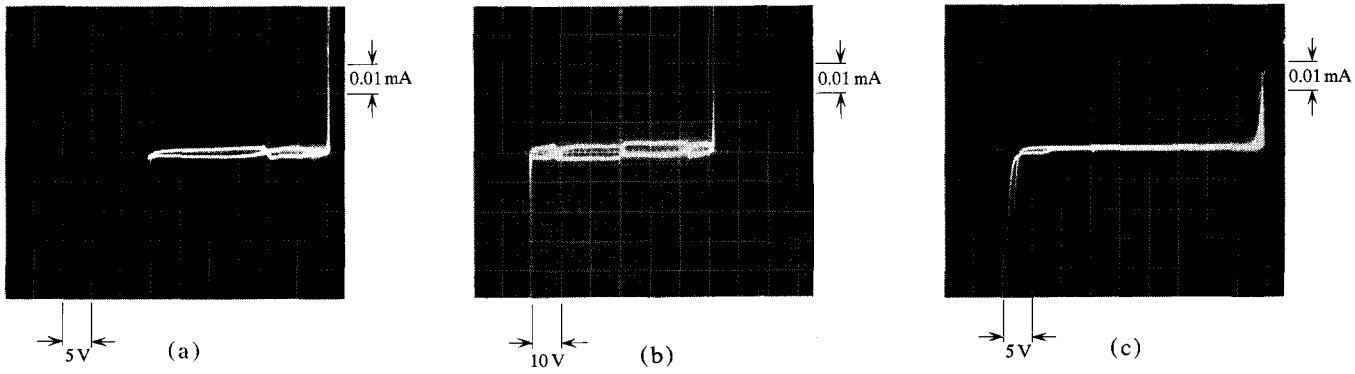


Figure 4 Common emitter current gain h_{FE} and cut-off frequency f_T as functions of emitter current. Horizontal geometry and I-V characteristic of device are also shown.

Figure 5 Various breakdown voltages for the experimental device. (a) Collector to substrate; (b) collector to collector; (c) base to substrate.



collector-substrate capacitance was 0.05 pF/mil^2. The f_T, h_{FE} and capacitance characteristics indicate that performance of these devices should be comparable to that of devices made by conventional techniques. The leakage currents of the emitter-base, collector-base, and collector-substrate junctions were all observed to be less than 1 μA before breakdown. The breakdown voltages were: emitter-base 5.0 V, collector-base 20 V, collector-emitter with base open 6.0 V, and collector-to-substrate 35 V. The breakdown characteristics of most interest for the proposed technique are those from collector to substrate, base to substrate, and collector to collector, as shown in Fig. 5. These characteristics show that isolation characteristics of the n pocket are acceptable for most of the bipolar applications.

Control of undesirable effects

During the processing of these devices, the two most critical problems that had to be overcome were 1) auto-doping of n^+ impurities and 2) the inversion of the p-surface.

Discussion[5–7] of auto-doping of n^+ impurities from the substrate into the n epitaxy during the epitaxial process began when epitaxial deposition was being done on an n^+ substrate and transistors were made one at a time. With the p epitaxy as in the proposed structure of Fig. 2, auto-doping creates a thin n^+ layer at the interface of the p^- substrate and the p epitaxial layer, as shown in Fig. 6. This n^+ layer between n^+ pockets results in electrical shorts between the collectors. It is possible to reduce the amount of auto-doping, however, by reducing the surface

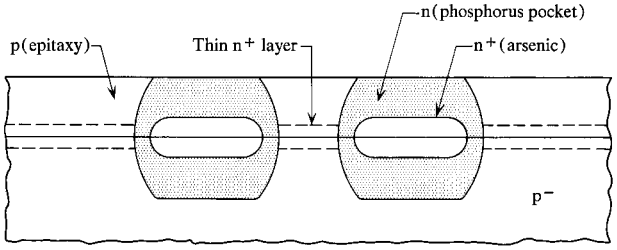


Figure 6 Auto-doping at interface of p^- substrate and p epitaxy, showing short between n-pockets due to auto-doped layer.

Figure 7 (a) Top and (b) sectional views of two integrated transistors, illustrating sub-collector spacing reduction.

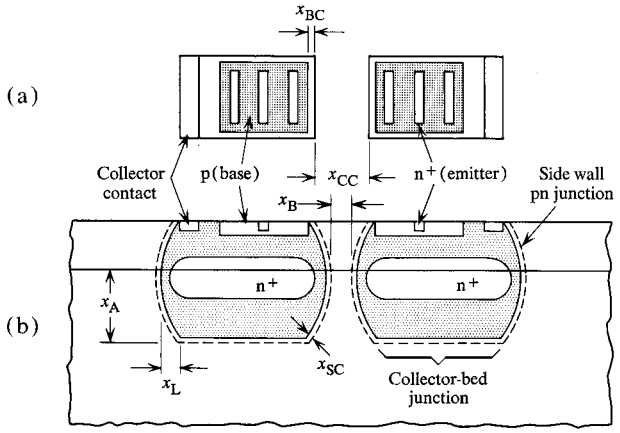
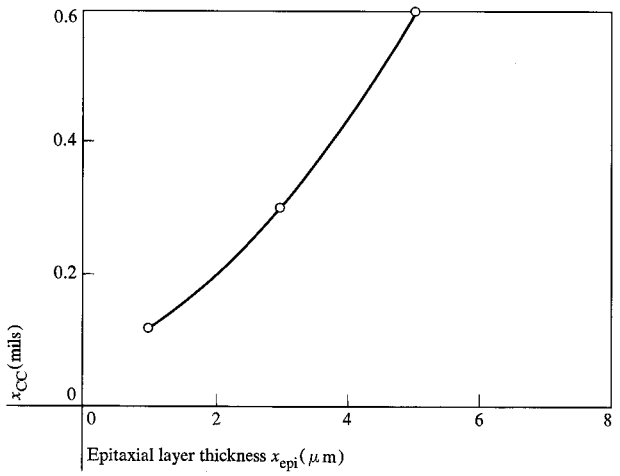


Figure 8 x_{CC} vs epitaxial layer thickness. ($x_L \approx$ epi thickness; $x_{SC} \ll x_L$; $x_B = x_L$ are assumed.)



concentration of the n^+ buried layer. Another possible method is to use SiH_4 instead of $SiCl_4$ for deposition of silicon epitaxially[8]; this permits a lower deposition temperature, with less auto-doping as a result.

The second major problem, inversion of the p-surface, also causes shorts between the n-pockets. By processing the wafers in a sodium-free environment, however, good isolation can be achieved. An alternative suggestion for eliminating this problem is to have a p^+ guard ring placed around the device during the base diffusion, thus avoiding an additional masking or diffusion step.

Discussion

In comparing one proposal for integrating bipolar transistors with another, the important properties to be examined are performance, density, and process simplicity.

Concerning performance, one parameter of interest is the cut-off frequency f_T. The most critical structural parameter that controls f_T is the basewidth W_B. Since the proposed scheme employs a double-diffused base and emitter, control of W_B is as good as in the conventional scheme. One favorable feature of the proposed scheme is the retrograde profile of impurities in the collector region near the collector-base junction. This type of profile tends to reduce base stretching at high current densities, thus maintaining high f_T at higher currents.

Other parameters that reflect the performance of an integration scheme are various capacitances: collector-base capacitance C_{BC}, base-emitter capacitance C_{BE}, and collector-substrate capacitance $C_{C\text{-sub}}$. The first two, C_{CB} and C_{BE}, are similar to the ones obtained by using the conventional structure of Fig. 1. The last one, $C_{C\text{-sub}}$, is improved with the proposed method. The two components of $C_{C\text{-sub}}$, side-wall junction capacitance and collector-bed junction capacitance (Fig. 7), are both made of graded junctions, as compared with the step junctions of the conventional process.

By eliminating the isolation diffusion, as in the proposal described here, one can bring two n pockets closer to each other. One of the measures of the compactability of an integration scheme is to minimize possible distance x_{CC} (Fig. 7) between two isolated collectors and the minimum clearance x_{BC} between subcollector and base on the mask level. In the process presented above, x_{CC} is comprised of the lateral diffusion distances x_L of the n pockets and x_{SS} of the space charge regions at the substrate-epitaxy interface. The x_{SC} depend upon the doping levels at the epitaxy-substrate interface. With the process described above, x_{CC} would be 0.6 mil for 5 μm of epitaxy. With conventional processes, this spacing would be about 1.4 mils for 5 μm of epitaxy. Figure 8 shows the possible improvement in x_{CC} with a reduction in epitaxy. The curve in Fig. 8 was derived from the following calculation:

$$x_{CC} = 2x_L + 2x_{SC} + x_B.$$

x_L, the lateral diffusion of the n pocket at the epitaxy-substrate interface is assumed to be approximately equal to the thickness of the epitaxy. x_{SC}, the space-charge region width, $\ll x_L$. This condition could be achieved by

controlling the doping in the p region. x_B is assumed to be equal to x_L to ensure safe isolation distance between the space charge regions. The x_{BC} are limited by photo-resist tolerance only. In the present case, x_{BC} is 0.05 mil.

As an example to demonstrate the suitability of the self-isolation scheme for large-scale integration, Fig. 9 shows a mask layout for a T^2L circuit. From this layout it can be seen that cell size can be reduced by a factor of 2 or more quite easily, as compared with the difficulty of the same reduction using conventional isolation.

Conclusions

A concept has been described for the integration of bipolar transistors that eliminates the isolation diffusion step and promises an increase in component density by a factor of two or more. Process details and results from an experimental device fabricated by using the self-isolation scheme have been presented. An example of mask layout for a given circuit demonstrates that the proposed scheme is suitable for large-scale integration.

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References

1. V. A. Dhaka, "Development of a High-Performance Silicon Monolithic Circuit," presented at the IEEE International Electron Devices Meeting, Washington, October 1970.
2. B. T. Murphy and V. J. Glinski, "Transistor–Transistor Logic with High Packaging Density and Optimum Performance at High Inverse Gain," presented at the International Solid State Circuits Conference, Philadelphia, February 1968.
3. V. J. Glinski, "A Three-Mask Integrated Circuit Structure," presented at the IEEE International Electron Devices Meeting, Washington, October 1969.

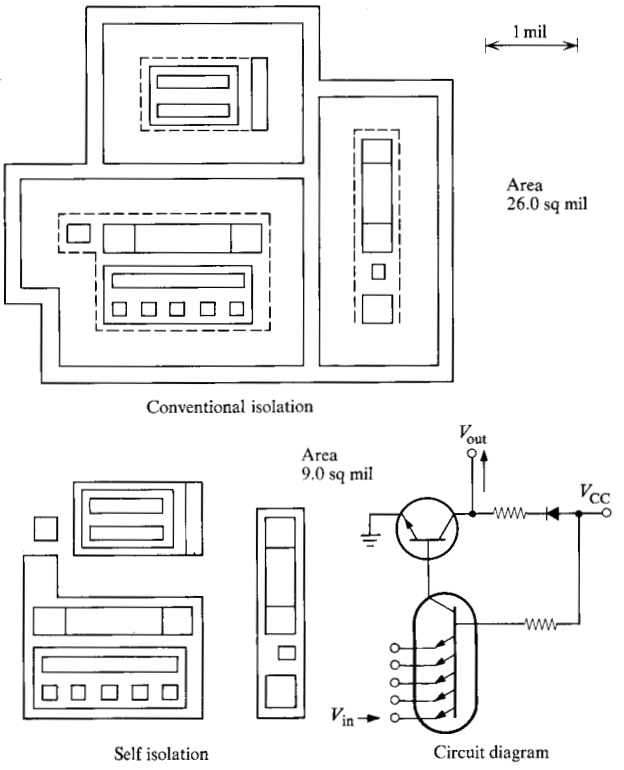

Figure 9 Reduced area for T^2L circuit when self-isolation is used, as compared with conventional means of isolation.

4. D. Peltzer and W. Herndon, *Electronics*, March 1, 1971, p. 52.
5. C. O. Thomas, D. Kahng and R. C. Manz, *J. Electrochem. Soc.* **109,** 1106 (1962).
6. D. Kahng, C. O. Thomas and R. C. Manz, *J. Electrochem. Soc.* **110,** 394 (1963).
7. T. Abe, K. Sato and N. Oi, *Japan. J. Appl. Phys.* **4,** 70 (1965).
8. C. D. Gupta and Roy Yee, *J. Electrochem. Soc.* **116,** 1561 (1969).

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