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Ultra-high-speed Operation of Josephson Tunneling Devices

Abstract: Switching times of large Josephson devices have been measured. We report gate switching times of 85 ps and array cycle times of an elementary memory cell of 550 ps. Although these times are expected to be smaller in more realistic miniaturized devices, they represent to our knowledge, the shortest times for such circuits ever reported in any technology.

Introduction

We report two new results that are of particular significance for the operation of logic circuits and memory cells using Josephson tunneling device technology. The first result is the direct measurement of a gate switching time of 85 ps; the second is the operation of an elementary memory cell with a cycle time of 550 ps. These results were achieved with large size devices that dissipate 10 μW of power in continuous operation.

In 1967 Matisoo [1] demonstrated the operation of a universal logic and memory element with a Josephson [2] tunnel junction as the active device. Because of high operating speed and low power dissipation, these devices have potential for use in high-performance central processing units and fast large-capacity memories [3]. In 1966 Matisoo [4] had directly measured an upper bound of 800 ps for the switching time of a current-driven Josephson junction. He later reported [5] current transfer times of about 2 ns in a flip-flop circuit. Since then, the only reported work in this field is that of Stewart [6], whose measurements in the 10^{-8} to 10^{-7} s time range were extrapolated to smaller transition times.

Device and experiment

To extend switching time measurements to values below 100 ps, a special sample configuration was necessary. The shape of the device, shown in Fig. 1, is that of a fork with four short leads on one side of the junction to permit four-point high-frequency contact. The handle of the fork is a 430-mil × 10-mil strip line with 2-μm spacing between lines. Eventually this strip line is mechanically shorted to form the memory loop.

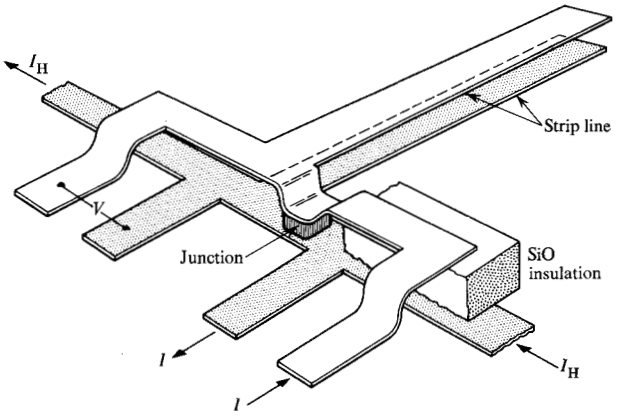


Figure 1 The device configuration used in these experiments. The forked structure has been specifically designed to permit resolution of millivolt signals having approximately 60-ps rise-times. Contact to the sample is made by two pairs of transmission lines pressed over the current (I) and voltage (V) leads. The open-ended strip line can be mechanically shorted to form an adjustable superconductive loop for the current transfer measurements in memory cell operation. A magnetic field can be applied to the junction by feeding a current I_H through the bottom line.

The device is made by evaporating a Pb alloy through a mask onto a glass substrate at 10^{-6} Torr. The insulation between top and bottom superconductors is a 2-μm layer of SiO. A window in the SiO defines the junction area, approximately 5 mils × 4 mils, which is subsequently cleaned and rf-oxidized [7]. The structure is completed by evaporating an upper Pb-alloy layer through a second mask.

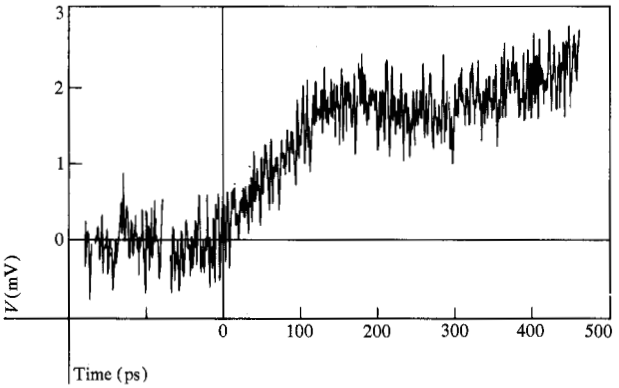
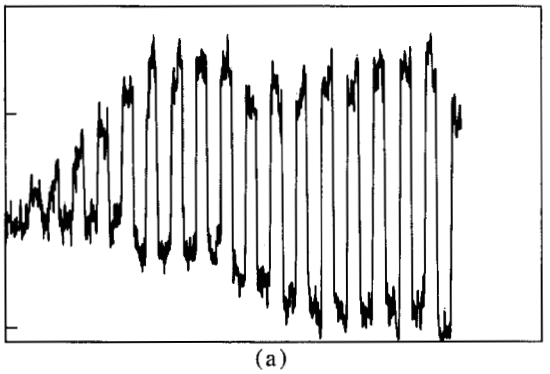
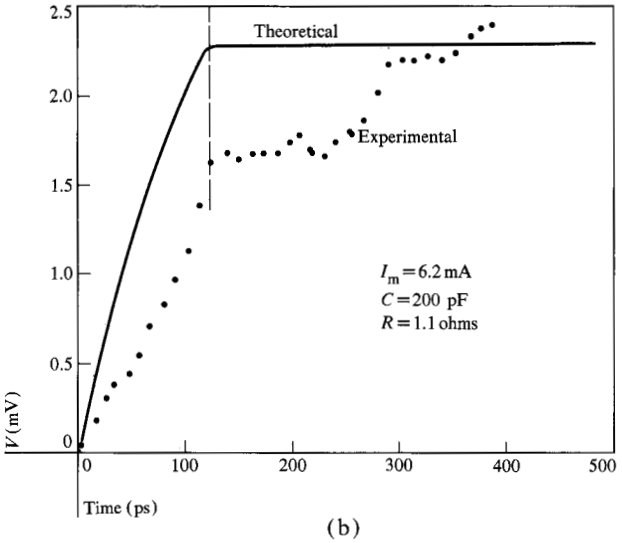


Figure 2 One of the recordings of the fastest junction transition times (85 ps; 10 to 90 percent) measured during these experiments. At the time of this measurement the switching times were "extracted" from a large number of similar noisy plots.

Figure 3 (a) A 105-ps (10 to 90 percent) transition of a large (4-mil × 5-mil) junction as recorded after the signal was filtered and multiplexed to the baseline. (b) The same signal, after being computer-processed, compared with the theoretical prediction obtained by solving the equations of motion for this configuration. The parameters were determined from the junction *I-V* curve. The signal attenuation and distortion apparent in the experimental curve are due to the cable and are not accounted for in the theoretical curve.



(a)



(b)

High-frequency contact is made by pressing onto the junction leads, only a few mils from the junction, two pairs of 25-ohm copper strip lines covered with an unconnected copper ground-plane. These lines are matched in pairs to two 50-ohm cables. The voltage cable is connected to a sampling oscilloscope (HP 141A) with a sampling time of 28 ps. The current cable is driven with slowly rising (60-ns) ramp pulses. To measure switching times, the junction voltage is observed at the time at which this current reaches the Josephson threshold current I_m, which has previously been measured. All measurements are made at 4 K.

Because of the large bandwidth (zero to 30 GHz) of the voltage measurement system, the signal ($\leq$ 2.5 mV) as recorded with the oscilloscope is distorted by about 1 mV of thermal noise, baseline drift (mainly in the oscilloscope), inductive signals from the current lines, and the attenuation and dispersion of the read cable itself. Initially, the junction transitions were determined by averaging over a large number of direct, and thus noisy, recordings. The more recent data, however, are subjected to extensive processing. Thermal noise is first reduced by integrating the signal using an RLC low-pass filter. Also, while the time axis of the sampling scope is slowly scanned, the device is alternately made to switch (signal) and to not switch (baseline), with both voltages being recorded. Baseline disturbances and drift are thus accounted for. These voltage-vs-time data are digitized and further processed by computer.

The theoretical calculations were made with the Josephson and circuit equations appropriate for our forked structure (see, for example, McCumber [8] and Stewart [9]). The nonlinear differential equations for both the open loop and the shorted loop, treated as strip lines, were solved numerically. All of the necessary parameters were measured on the junction. In particular, the junction capacitance was determined by measuring the time required to charge that capacitance. Precise measurements are obtainable because in each device the charging time is systematically variable by changing I_m (the charging current).

Results

Gate switching time is the time required for the junction voltage to increase from zero to the value of the gap voltage. For these measurements, the long strip line is open at the end. Figure 2 shows the gate switching signal of an early sample that had the highest value of I_m and thus the smallest transition time produced so far. In this sample, the switching time (measured between 10 and 90 percent of maximum signal voltage) obtained from averaging a large number of plots was found to be 85 ps. The multiplexed and filtered signal of a later, slightly slower junction is shown in Fig. 3(a), and the final computer-

processed data are compared with theory in Fig. 3(b).

Evident in the experimental signal, but not included in the theoretical curve, is the effect of cable distortion. It has been shown [10,11] that a short (and cooled) cable will attentuate a ramp current with negligible rise-time degradation up to the time at which the input signal reaches its flat top. At this point (with an expected 2.6-dB cable attenuation in our experiment), a break occurs, after which the output tends slowly toward the final input value. Experimental analysis of the sense system has confirmed this calculation. Therefore, the total (0 to 100 percent) transition time of the data shown in Fig. 3 has to be taken from zero to the break in the signal curve (dashed line). The agreement between theory and experiment is thus very good and is typical of all our recent measurements.

In the memory cell experiments we measured the transfer time of the current from the junction into the parallel loop. For these measurements the strip line (Fig. 1) was shorted at varying distances from the junction to form an adjustable superconductive inductance (L varies from 10^{-10} to 10^{-11} H). Data are shown in Fig. 4 for the case in which the loop has the maximum size (420 mils) and inductance (10^{-10} H). A memory cycle time of about 550 ps is indicated. The differences between theoretical and experimental values are again due to the distorting effect of the read cable, which is not included in the theory.

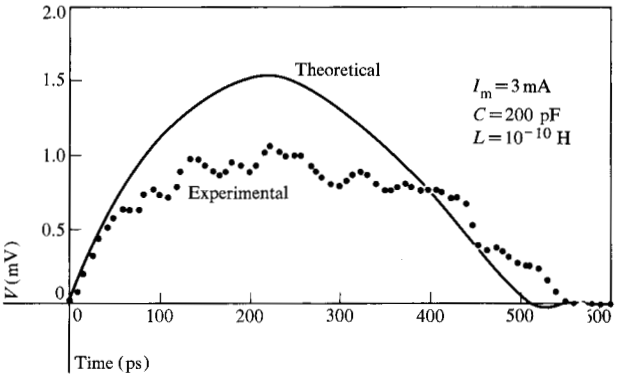


Figure 4 The signal observed during current transfer from the junction into a 420-mil-long superconductive loop. The memory cell cycle time is about 550 ps. Differences between the experimental and theoretical curves are due to cable distortion.

Conclusion

The gate switching time is directly related to the logic delay of Josephson junction logic circuits, and the current transfer time is related to the cycle time of a memory array. The measurements reported are, to our knowledge, the shortest times for such circuits ever reported in any technology: 85 ps switching time and 550 ps transfer time. These results have been achieved with relatively large devices. Because experiment and theory agree well and theory suggests that the switching time scales with device size, extrapolation of these results to shorter times with smaller devices can readily be done.

Acknowledgments

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