

Analysis of Defect Distribution in Transistor Structures with Reflection and Transmission X-Ray Topography

Abstract: Reflection and transmission x-ray topography can be combined to isolate and identify dislocations that penetrate the active junctions of transistor structures in integrated circuit wafers. This is accomplished by reconstructing the defect distribution normal to the surface as viewed in transmission (volume-sensitive) and reflection (surface-sensitive) x-ray topography. The combination of surface and bulk observations is exploited to demonstrate the effect of dislocation density on pipes (low-resistance paths from emitter to collector). A method is also described for estimating the depth of defect visibility in reflection x-ray topography.

Introduction

The application of x-ray topography to the problem of crystal defect studies is well known. This experimental method has proved invaluable in studies of dislocation generation during crystal growth [1], diffusion-induced defects in shallow junctions [2, 3], and thin-film adhesion studies [4]. Recently, Schwuttke [5, 6] has employed SOT (scanning oscillator technique) topography to relate crystal defects to device performance through yield map construction; i.e., he has correlated the electrical parameters for individual devices with the image of the defect distribution in the x-ray topographs. This approach has proved helpful in relating dislocations to increased reverse currents [6] and junction shorts [7, 8]. In these studies, the relationship between dislocation density and device characteristics was established by transmission x-ray topography only.

It is the purpose of this paper to demonstrate that reflection topography, used in addition to and conjunction with the transmission technique, can provide additional and complementary information in x-ray analysis. This has been found quite useful in the study of semiconductor junction defects. In particular, certain anomalies that appear in transmission topographs can be readily explained after inspection of the corresponding reflection topographs, and vice-versa.

To demonstrate the complementary nature of the reflection and transmission methods, the number density of dislocations penetrating a given transistor junction is related to the amount of emitter-collector leakage, the latter being a function of the number of low-resistance current paths (pipes) through the junction.

X-ray topography

• *Transmission x-ray topography*

Transmission x-ray topography reveals crystal defects throughout the *volume* of a silicon wafer. Images of these defects are superimposed in a two-dimensional photographic image. A defect is revealed because, when divergent-beam techniques are used with relatively thin specimens, primary extinction in the locally distorted lattice is less than in the perfect crystal matrix. Transmission methods are well developed, and topographs can be obtained even from highly stressed wafers with the scanning oscillator method [9]. The major drawback to the transmission method is that surface defects, in active junctions, are frequently obscured by dislocations in the lower regions of the crystal. An example of this problem is discussed in a later section.

• *Reflection topography*

The reflection method [10, 11] yields an image of the defects that outcrop at the wafer *surface* and thus the wafer can be inspected both before and after processing cycles. The image does not generally register volume defects because the penetration depth is of the order of only 7 μm (see Appendix). Thus the defects in the active regions of the device are dominant. The experimental method is simple, but problems such as fluorescence scattering and multiple images [12] have prevented the method from achieving the versatility of the transmission method. With proper procedures, however, the reflection method can yield a high resolution map of the crystal defects in the transistor

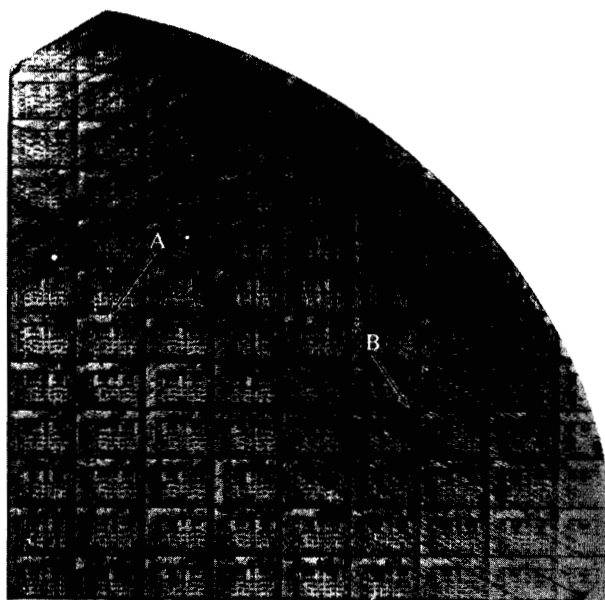


Figure 1 A transmission (SOT) x-ray topograph of a monolithic semiconductor wafer section. Chip A is located in the low-dislocation interior of the crystal, whereas B is near the heavily slipped wafer edge.

junction and thus facilitate the correlation of defects with device performance.

◆ Analysis of semiconductor junctions

A major portion of the yield loss in semiconductor components has been attributed to emitter-collector shorts (pipes). Goetzberger and Stephens [13] showed that phosphorus contamination in npn transistors resulted in a localized n-type region that penetrated the p-type base, thus producing a low resistance path (pipe) from emitter to collector. Barson et al. [14] demonstrated that structural defects such as stacking faults and dislocations can also provide sites for pipe activity. Recently, Plantinga [15] showed the effect of individual dislocations (grown-in) on transistor leakage, and Parekh et al. [16] identified emitter-edge dislocations [17] as the cause of excess leakage. In these investigations, pipes (dislocations) were identified by either sectioning and plating [14], etching under bias [15] (dislocations are difficult to delineate in highly doped emitter regions), or by means of Sirtl etchant [16]. The analysis of pipes (dislocations) by these methods is destructive and frequently time-consuming.

Experimental

The samples used in our experiments were sections from integrated circuit wafers; several sections were chemically stripped in HF acid to expose the silicon surface. The large test transistors (located between the integrated circuit chips and thus removed during dicing) were then

electrically probed for pipes. The pipe was identified from a linear resistance trace of BV_{CE0} through the origin and from the magnitude of the I_{CE} leakage at 1.0V bias. Typical leakage values of $\approx 250 \mu A$ at 1.0V were indicative of a pipe-free structure.

Reflection x-ray topographs were then obtained from the same sample to determine the relationship between leakage and crystal defects. The incident radiation was $CuK\alpha$ and the power was maintained at 40kV, 20mA. The resulting exposure time varied from 5 to 10 minutes when Ilford 25 μm G-5 plates* were used. The wafer was (111) oriented and the oblique {115} planes were used to obtain a topograph that displayed a shallow layer of defects (see Appendix).

Transmission x-ray topographs were recorded by the SOT method [9]; $MoK\alpha$ radiation was employed at a power level of 50kV, 20mA. The exposure time for a {220} reflection varied from 5 to 10 hours (depending on the amount of oscillation required) when Ilford G-5 50 μm plates were used.

Defect-device correlation

◆ Correlation of transmission and reflection x-ray topography

Transmission and reflection x-ray topography are compatible methods for crystal defect analysis and should be applied sequentially for the most descriptive view of the defect distribution in the crystal. Figure 1 shows an SOT transmission x-ray topograph of an integrated circuit wafer after electrical testing. The topograph reveals the defect extremes that can occur in most defect-device correlations. The dislocation density in the center of the crystal is low but increases dramatically toward the wafer periphery.

Figure 2 is an enlargement of a chip in the low-density region (A in Fig. 1). Because of a steep concentration gradient at the diffused-undiffused interface, several dislocation sources can be identified (Fig. 2, points 1, 2), but the inclination of the loops relative to the surface is difficult to determine in a single transmission topograph. The corresponding reflection topograph is displayed in Fig. 3, where the dark region delineates the isolation diffusion. Note that the observed dislocation density is reduced, since only the surface layer contributes to the image. The location of the loop images (relative to the chip edge) in the reflection topograph and the transmission topograph (Fig. 2) indicates that the loops are activated at the edge of the isolation diffusion. The loops are punched downward on {111} planes to relieve the stress buildup at the square edge of the isolation region (Fig. 2, point 1) or at the isolation diffusion boundary (Fig. 2, point 2). This is

* The plates were developed in Microdol X (trademark of Eastman Kodak Co.) for improved resolution.



Figure 2 An enlargement of A in Fig. 1. Note the dislocation loops (1) near the edge of the isolation region and (2) between adjacent chips. (Figures 2-7 are reproduced by permission from M. L. Joshi and J. K. Howard, "Defects Induced in Silicon Through Device Processing," *ASTM Symposium on Silicon Device Processing*, Gaithersburg, Md., June 2-3, 1970, to be published by the National Bureau of Standards.)

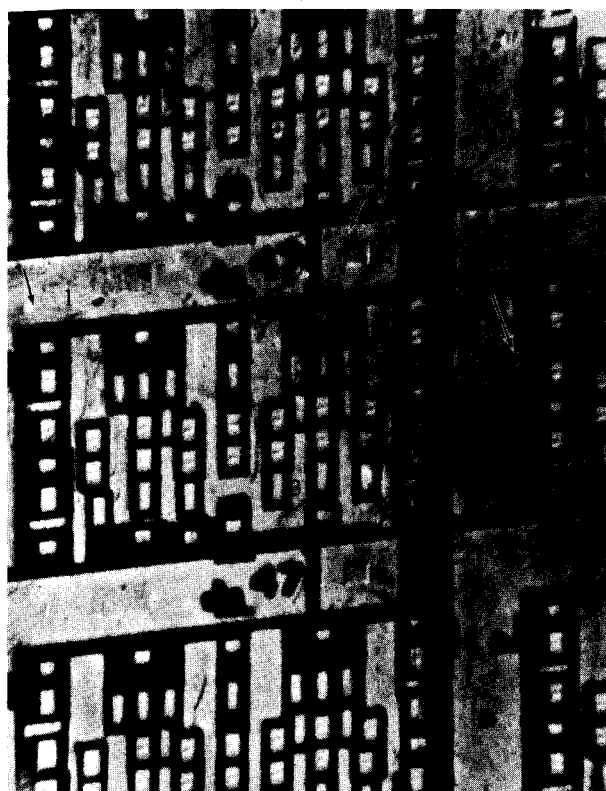


Figure 3 A reflection (surface) x-ray topograph of the chips in Fig. 2. The location of the dislocation outcrops (1) and (2) indicates that the loops are punched downward from the observed location in the surface topograph. The dislocation line (3) is identified from the transmission image in Fig. 2.

confirmed by the surface outcrop of the loops at the isolation boundary (Fig. 3, points 1 and 2). Accordingly, the loop contrast disappears as the loops penetrate the wafer. The complete loop structure is imaged in the transmission topograph (Fig. 2); this type of dislocation source is dominant for chips near the center of the wafer.

Individual dislocations can frequently be mapped from transmission topographs to surface topographs. The dislocation line (3) in Fig. 2 is seen to penetrate the surface layer in Fig. 3. The attitude of the defect can be inferred from the contrast broadening (diffuseness) with depth in the crystal. The image becomes sharply defined as the dislocation approaches the surface at a sharp angle. A one-to-one correspondence between defects in transmission and reflection topographs is complicated by the fact that the image contrast is very dependent on the specific set of reflecting planes used to obtain the topograph.

Figure 4 represents a transmission SOT topograph of several chips near the wafer periphery (Fig. 1, at B). The dark bands are dislocation bundles in $\langle 110 \rangle$ directions; the dislocations are generated during slip caused by

thermal stresses during heating and cooling. These dislocations were introduced during crystal growth or some oxidation cycle prior to epitaxial growth [19]. The spatial resolution is poor because of the superposition onto the photographic plate of defect images in the substrate and the epitaxial film. A reflection topograph (Fig. 5) from the same region, however, clearly shows individual dislocations in the slip array that penetrates the surface.

• Transistor leakage and dislocation density

A leakage current of $270 \mu\text{A}$ at 1.0V was measured in the large test transistors (Fig. 3, arrow 4), which contained relatively few defects in the reflection topograph. Note that the transmission topograph (Fig. 2) depicts numerous dislocation loops in the active junction. Recall that these loops had been punched *downward* on $\{111\}$ planes to relieve the stress at the interface of the isolation diffusion. The transmission topograph in Fig. 2 actually depicts overlapping sets of loops in the junction region. Since the $\{111\}$ planes make an angle of 70.5° with the wafer surface, the loops glide $\approx 75 \mu\text{m}$ into the crystal and their



Figure 4 An enlargement of chip B in Fig. 1. The heavy dislocation slip (superposition of substrate and epitaxial film defects) prevents any defect-device correlation.

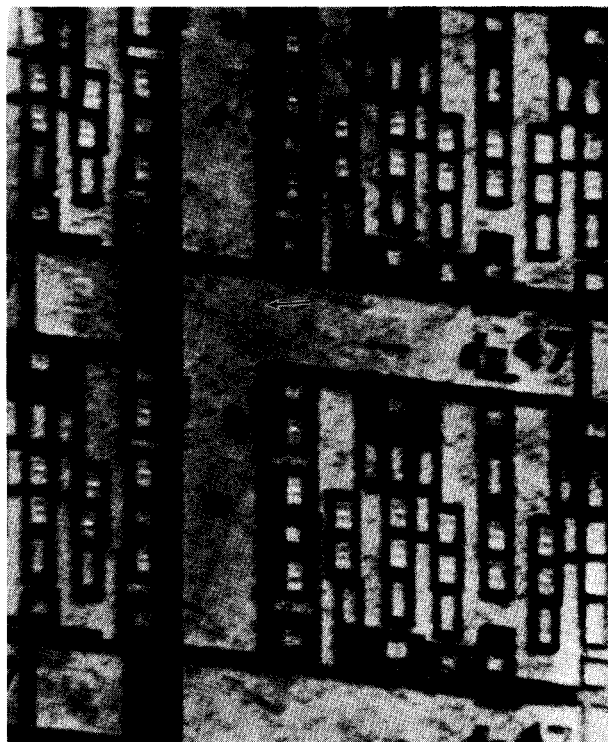
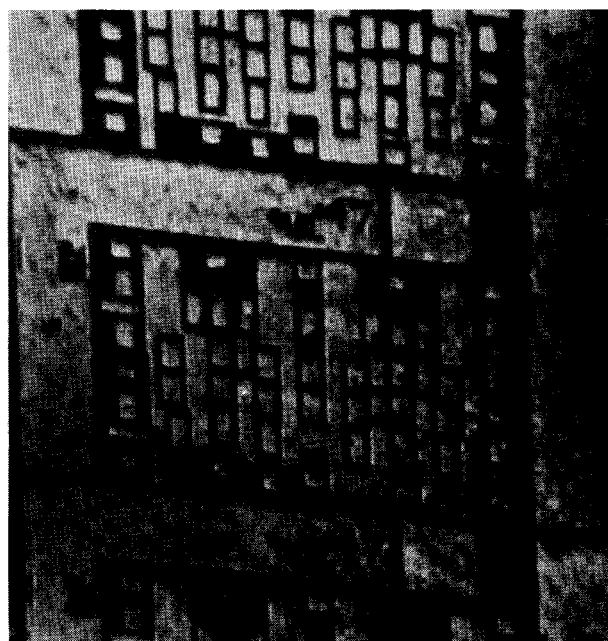


Figure 5 A surface x-ray topograph of the region in Fig. 4. The short line segments represent steeply inclined dislocation segments (slip array) that intercept the surface. Note the disparity in volume and surface defect density; the transmission (volume) topograph can obscure the surface defect density.

Figure 6 A surface topograph of another wafer section. The test transistor at the top of the figure yielded a leakage current of $240\mu\text{A}$ as compared with $1300\mu\text{A}$ for the lower chip. This is consistent with the observed dislocation density in each chip.



Figure 7 A surface x-ray topograph of other chips near the wafer edge. The top test transistor yielded a leakage current of $2000\mu\text{A}$, as compared with $4000\mu\text{A}$ for the lower test device.



projected image appears in the transistor region. However, the surface topographs (image depth $\approx 7 \mu\text{m}$) of this transistor are virtually defect-free, which is in agreement with the low leakage value of $270 \mu\text{A}$. It can be concluded that these loops do not link the emitter and collector junctions and thus are not active as pipes.

These results bring into focus the need for an analysis that combines reflection and transmission x-ray topographs. In this case the distribution of dislocations in depth is critical to the analysis of defect-induced junction leakage. If only the transmission x-ray topograph were recorded, it might be concluded that the low leakage current was obtained in a high-defect junction (Fig. 2). In the same manner, the presence of the dislocation loops at the isolation boundary might not have been noticed in a reflection x-ray topograph.

The effect of dislocation image superposition is apparent in Fig. 4. The dense slip image prevents any estimate of the number of dislocations that intercept the junction. The reflection topograph in Fig. 5 "strips" out the substrate effects and exposes individual dislocations in the junction (arrow). Leakage current measurements of transistors in the region of slip are in the range of 2000 to $3000 \mu\text{A}$. This measurement, coupled with the BV_{CE0} measurement, indicates that the dislocations in the slip array are sources for junction leakage.

An additional wafer was selected for device-defect study, but in this case the sample contained minimal slip, as verified by a transmission x-ray topograph. Figure 6 shows an enlarged area of a reflection topograph that depicts several integrated circuit chips and two test transistors. The leakage current of the upper test transistor was $240 \mu\text{A}$; the low leakage is in agreement with the low density of dislocations in the reflection topograph. Note that the lower chip, however, has considerably more dislocations (Fig. 6) than the upper junction. The leakage current was observed to increase to $1300 \mu\text{A}$, in correspondence to the increased defect density. Figure 7 is another reflection topograph from the same wafer, but closer to the edge. Note that the dislocation density is considerably higher than in Fig. 6. The increase in leakage current to $2000 \mu\text{A}$ is in agreement with the increased dislocation density. The lower chip in Fig. 7 is near the wafer edge; the leakage current of $4000 \mu\text{A}$ is consistent with the high defect density observed in the reflection topograph.

It should be recognized that the correlation between junction leakage and dislocations is statistical in nature; i.e., for a sufficiently large sample size, one determines how many piped junctions contain dislocations, how many piped junctions do not contain dislocations, and how many dislocated junctions are good. The results presented in this investigation appear to indicate a good correlation between junction leakage and the number of dislocations detected in the junction with reflection x-ray

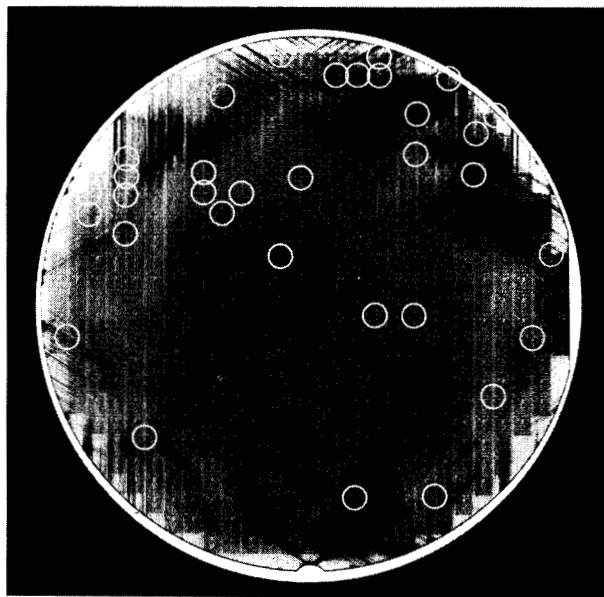
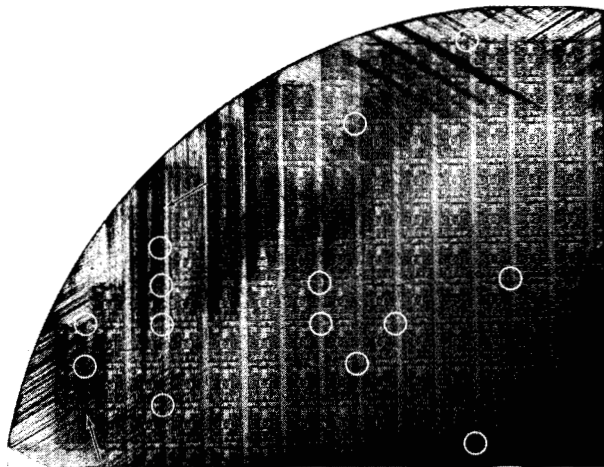


Figure 8 A SOT transmission x-ray topograph of an integrated circuit wafer after electrical testing. Approximately 5.5% of the test transistors contain pipes (circles). Note the apparent lack of correlation between the dislocation slip and the presence of pipes.

Figure 9 An enlargement of the upper left quadrant in Fig. 8. Note the occurrence of transistors with and without pipes (circles) along the same slip band (arrows).



topography. However, in another sample fabricated by a different process, the relationship between crystal defects and pipes is not as obvious. Figure 8 represents an SOT topograph of an integrated circuit wafer in which each test transistor was probed for pipes. The location of pipes (circles) does not track the dislocation slip pattern; good and bad devices are observed in similar areas of intense slip. It is also apparent that numerous pipes occur in the low-dislocation wafer interior. The dislocation structure

is depicted with greater clarity in Fig. 9, which is an SOT topograph of one quarter of the wafer in Fig. 8. Note the location of devices with and without pipes in the same slip band (arrow). The analysis of these exceptions is the subject of future investigations, but some possible explanations can be considered: Possibly the dislocations *do* penetrate the junction but are not activated by metallic impurities [14] or impurity clouds [15]; perhaps, however, the dislocations *do not* penetrate the junction [18], and the junction quality is masked by slip in the substrate. The first of these possibilities might be resolved by beam-induced current studies using the scanning electron microscope [20], and the second by reflection x-ray topography; i.e., if transmission and reflection topographs are compared, the surface defects can be separated in a manner similar to Figs. 2 and 3.

Summary

As an improved technique for evaluating semiconductor junctions, we have described an approach in which reflection topography and transmission x-ray topography are combined to separate the volume and surface defects in active junctions. Several examples have been presented to demonstrate the advantage of the combined reflection-transmission analysis over either method alone. It has also been shown that excess junction leakage could be related to the number of defects in the junction, as revealed by reflection x-ray topographs.

The observation through transmission topography of transistors with and without pipes in areas of heavy slip raises a question as to whether excess leakage is caused by all dislocations that penetrate a junction or only by those associated with a high density of impurities. However, the combined use of reflection and transmission topography should permit one to determine whether all dislocations that intersect a junction cause pipes. Experiments are in progress to evaluate a large number of electrically mapped transistors using the reflection-transmission method, and to study the effect of individual processes on the formation of pipes [14].

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Appendix: depth of defect visibility in reflection x-ray topographs

Experimental methods to determine the depth of x-ray penetration in single-crystal materials have been reported

in specialized cases. Some measurements have been described [21] for the depth of penetration in heteroepitaxial systems (GaP/GaAs), but this approach is not applicable to the silicon system. To that end, a preliminary analysis is presented to determine experimentally the depth of defect visibility in reflection topographs and the extent to which substrate flaws contribute to reflection topographs. A review of the theory is presented as a counterpart of the experimental approach, rather than as a basis for the measurements of defect visibility depth.

Theory

The crystals we are considering have, in general, relatively low dislocation densities. Hence, a complete description of the diffraction process requires the approach of the dynamical theory of x-ray diffraction [22]. Numerical calculation of the absorption depth and the extinction depth (both of which represent an estimation of the depth of penetration) were performed; the former is based on a kinematical approach and the latter on a dynamical approach.

The angular range of the *exit* beam diffracted from the crystal (the range of total reflection) is also calculated. This gives the major contribution to the integrated intensity and hence represents an estimation of the resolution. The depth of penetration can be described by the absorption length [22]

$$t_a = 1/\mu, \quad (1)$$

where μ is the linear absorption coefficient. This has been modified by Segmüller [23] to account for the glancing angle α in reflection topographs by

$$t_{a, \alpha} = t_a \sin \alpha. \quad (2)$$

Another measure of the penetration depth is the extinction length [22],

$$t_e = \frac{1}{\sigma_{e, \max}}, \quad (3)$$

where $\sigma_{e, \max}$ is the maximum extinction coefficient for the middle of the range of total reflection. By substituting the expression for $\sigma_{e, \max}$, the extinction length can be written [22]:

$$t_e = \frac{mc^2}{2\lambda e^2} \cdot V \cdot \frac{[|\gamma_h| \cdot \gamma_0]^{1/2}}{|F(h)| \cdot |C|}, \quad (4)$$

where

$F(h)$ = structure factor,

λ = wavelength,

V = volume of unit cell,

C = polarization factor (unity for σ and $\cos 2\theta$ for π polarization),

$$\gamma_0 = \cos \left[\frac{\pi}{2} - (\phi + \theta) \right],$$

$$\gamma_h = \cos \left[\frac{\pi}{2} - (\phi - \theta) \right],$$

θ = Bragg angle, and

ϕ = angle between surface and reflecting planes.

The angular range of the reflected beam is a measure of resolution in reflection topographs [23, 24]. (The resolution improves as the angular range decreases.) The angular range for the reflected beam, $\Delta\theta_h$, is related to the angular range of the incident beam, $\Delta\theta_0$, by the expression [22]

$$\Delta\theta_h = \Delta\theta_0 \cdot \frac{\gamma_0}{|\gamma_h|}, \quad (5)$$

where

$$\Delta\theta_0 = 2 |C| \frac{e^2}{mc^2} \frac{\lambda^2}{\pi V \sin 2\theta} \left(\frac{|F(h)|}{\gamma_0} \right)^{1/2}. \quad (6)$$

The equations were solved for reflection topographs from (111) silicon wafers in which $\text{CuK}\alpha$ radiation was used. The results are listed in Table 1 and are useful to compare with experimental observation. However, it should be realized that the relationship between the depth of penetration t_e and the depth of detectable defect contrast is not well understood.

• Line length method

Consider an x-ray beam (I_0) incident upon a crystal (C) at the proper Bragg angle θ for diffraction (Fig. A-1). The diffracting planes are assumed to make an angle ϕ with the slice surface. The incident beam impinges at an angle $\alpha = \theta - \phi$ to the wafer surface, whereas the diffracted beam is scattered at an angle $\beta = \theta + \phi$. Assume that a dislocation line D is contained in the plane of incidence (the plane containing the incident beam, the diffracted beam and the normal to the diffracting planes) and makes an angle γ with the surface. For the case of a (111) crystal, consider a straight dislocation line segment parallel to [110] where $\gamma = 54.7^\circ$ (angle between the [110] direction and the (111) crystal surface). The reflected beam is registered on a photographic plate placed parallel to the incident beam direction. Figure A-1 depicts a schematic of the diffraction geometry where b is the width of the beam diffracted from a line segment of length y and w is the measured length of the line segment on the photographic plate:

$$y = d/\sin \gamma; \quad (7)$$

$$b = y \sin (\theta + \phi - \gamma); \quad (8)$$

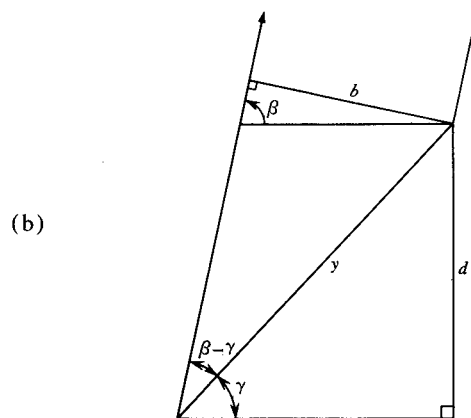
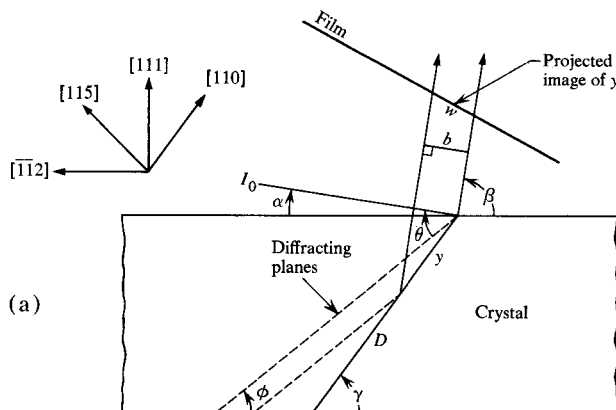
$$w = b/\sin 2\theta, \quad (9)$$

from which it follows that

Table 1 X-ray penetration depth calculation for (111) silicon using $\text{CuK}\alpha$ radiation.

(hkl)	ϕ	θ	α	$t_{a,\alpha}(\mu\text{m})$	$t_e(\mu\text{m})$	$\Delta\theta_h(\text{sec})$
115	38.94	47.53	8.59	10.5	8.0	0.18
440	35.26	53.42	18.16	22.1	9.1	0.53
422	19.47	44.08	24.61	29.6	7.9	1.07

Figure A-1 A schematic of the line length method to estimate the depth of defect visibility.



$$d = w \sin 2\theta \cdot \sin \gamma / \sin (\theta + \phi - \gamma). \quad (10)$$

Recall that the reason for the depth of defect visibility measurement is to insure that the defect density imaged in the reflection topographs is representative of the epitaxial film rather than the substrate. The line length method provides a geometrical approach to retrieve the depth of defect visibility from the projected image of linear dislocations in slip array. Figure A-1 illustrates the condition in which the dislocation is parallel to [110] and is contained

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