

Metal Edge Coverage and Control of Charge Accumulation in RF Sputtered Insulators

Abstract: The successful application of rf sputtered SiO_2 in the passivation of silicon semiconductor devices depends in part on the proper control of ionic charge migration in the insulator during sputtering, and on the adequate coverage of metal line edges by the insulator. It is shown that an appropriate combination of target purity, substrate temperature control and phosphosilicate blocking layer thickness can be used to achieve ionic charge densities at the silicon- SiO_2 interface of less than 1×10^{12} charges per square centimeter. The effects of argon ion bombardment are shown to be acceptably low for typical operating conditions. In a conventional system, the adequate coverage of metal line edges is shown to be influenced primarily by argon pressure and magnetic field. In a special system where the substrate potential can be varied, it has been shown that adequate edge coverage can be obtained at sufficiently negative potentials. These data are consistent with a mechanism requiring some resputtering to obtain the desired film coverage.

Introduction

RF sputtering for the deposition of insulator films has been shown¹ to yield films of high quality and excellent stability, and the potential usefulness of sputtered insulator films for the encapsulation of semiconductor devices has been demonstrated. However, for an insulator film to be satisfactory for semiconductor device use, two requirements have to be met in addition to the prerequisite of an intrinsic high quality of the film. These requirements are (1) that the deposition technique must have no adverse effect on the electrical device characteristics, and (2) that the thin film metal conductor land pattern of the device must be adequately covered by the insulator film. This paper discusses these two points for rf sputtered SiO_2 .

Under certain deposition conditions, devices passivated with rf sputtered SiO_2 show high leakage currents and generally degraded characteristics. In the literature, it has been shown that changes like these are primarily caused by a charge build-up at the SiO_2 -Si interface.^{2,3} A convenient device for use in studying semiconductor surface effects (e.g., charge build-up) is the MOS (metal-oxide-semiconductor) capacitor. The first part of this paper discusses the effect of several rf sputtering process parameters on charge build-up. The second part describes a method with which the coverage of metal land edges by insulator films can be conveniently studied and introduces the concept of the "edge protection factor," which defines the degree of metal edge coverage. In the latter section, the effect of key parameters on the edge protection factor is described.

Semiconductor surface effects

It is desirable to deposit sputtered films at slightly elevated temperatures to obtain the highest quality.¹ The temperature of silicon wafers can be controlled by placing them, through the use of a gallium layer, in intimate thermal contact with a temperature-controlled block.⁴ However, it is more convenient to simply place the wafer on a holder and let the temperature of the wafer reach a stationary value that is a function of the rf power density. For this purpose, the heat transfer between wafer and wafer holder has to be reproducible and low. This can be achieved readily by placing the wafer on a thin (1 to 2 mm) insulator spacer, such as a fused silica disk that rests on the wafer holder. In this fashion, the wafer "floats" both thermally and electrically with respect to the wafer holder. It has been observed, however, that semiconductor devices often exhibit the deleterious changes in characteristics mentioned earlier, when the SiO_2 films are deposited in this "floating mode."

Some of the conditions existing in the "floating mode" system during sputtering which might lead to charge migration in the insulator are

- 1) ionic contamination of the silica target;
- 2) high temperature (250–450°C), which will allow ionic migration in the insulator;
- 3) an electric field in the insulator;
- 4) electron bombardment; and
- 5) argon ion bombardment.

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To evaluate ionic contamination in the source, we have made electrical measurements of the total ionic content of films deposited from several different types of target material. Commercial grade natural fused quartz yields an ionic impurity density in the film of 10^{14} ions per cm^2 -micron or 10^{18} ions per cm^3 . High purity, synthetically formed silica targets yield lower (about an order of magnitude) total ionic content in the films. This is still, however, high enough to cause a problem if these ions are driven through the oxide layers of the device to the SiO_2 -Si interface.

Figure 1 shows some measurements that were made to determine the relative conductivity of bulk SiO_2 target materials to confirm the results obtained in regard to the relative ionic content of films deposited from these materials. The apparatus used for this has been described in the literature.⁵ All of the curves of current vs. temperature go through a maximum at the high temperature, presumably where the space charge build-up limits the field. At the low-temperature end, the conductivity of the natural silica is about an order of magnitude greater than the highest value exhibited by synthetic silica. These results do seem to confirm the measurements made on films but are strictly comparable only if the ionic mobility is identical in all materials. Nevertheless, one can decrease the possibility of charge migration by using target materials of higher purity.

The phosphosilicate glass layer, which is present on most integrated circuit devices, is known to be an effective block for positive ion migration at temperatures up to about 300°C .³ The temperature in a "floating" system results from a rather delicate balance between heat input through ion and electron bombardment and heat loss through conduction and radiation. Figure 2 shows the manner in which wafer temperature depends upon rf input power density for two different types of substrate. These temperatures were measured by using a thermocouple attached to the wafer. Argon pressure was 2.0 millitorr, magnetic field 60 gauss, and the system had a 30.5-cm diameter target soldered to a 29.0-cm diameter cathode. At least 20 minutes were allowed to elapse between each change of power and its temperature reading. Normally, the temperature rose to within 10% of its final value in a period of 2 minutes or less.

Since ion migration is temperature sensitive, increasing the power density should increase charge build-up in the insulator. Figure 3 shows this effect very well. Charge build-up is measured here using MOS capacitors with and without phosphosilicate glass (PSG). These curves were obtained by depositing, at different power levels, approximately 1.5 microns of silica over thermally oxidized silicon wafers with PSG. It can be seen from Fig. 3 that charge increases rapidly at power densities above 2.5 watts/ cm^2 . Without phosphosilicate glass, the charge

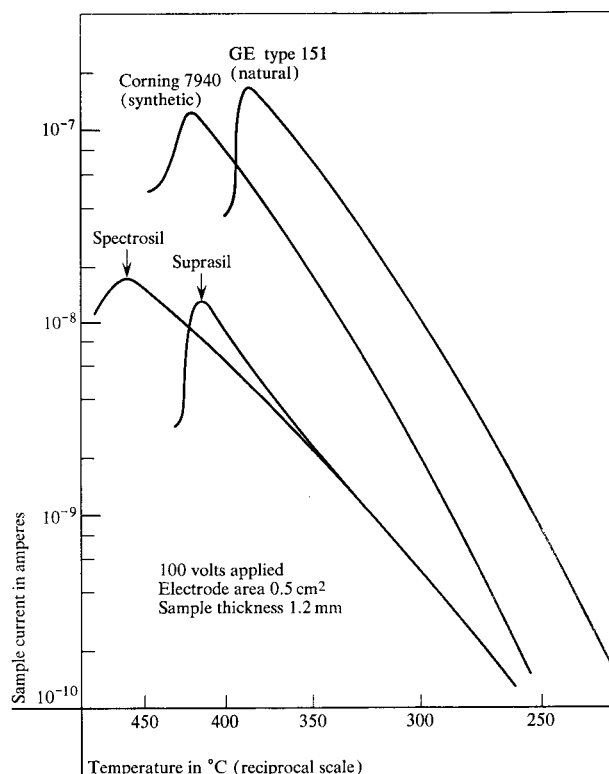
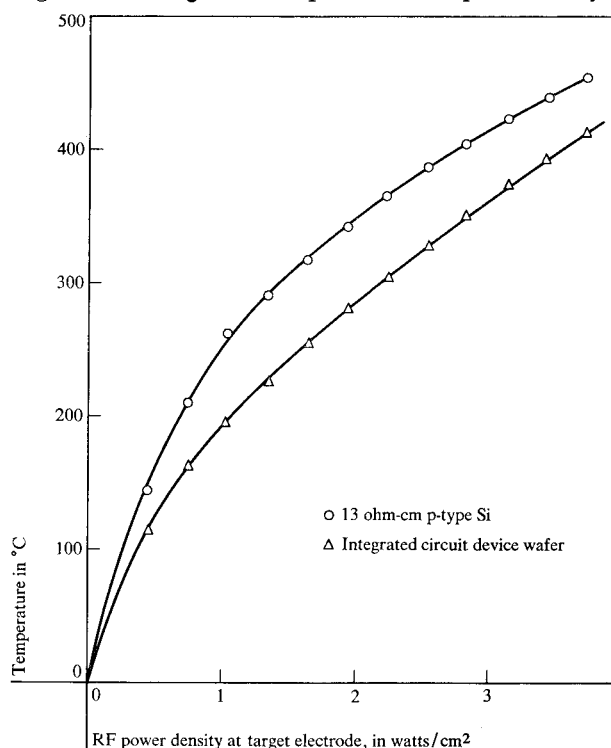


Figure 1 Leakage current vs. temperature for various types of silica.

Figure 2 Floating wafer temperature vs. rf power density.



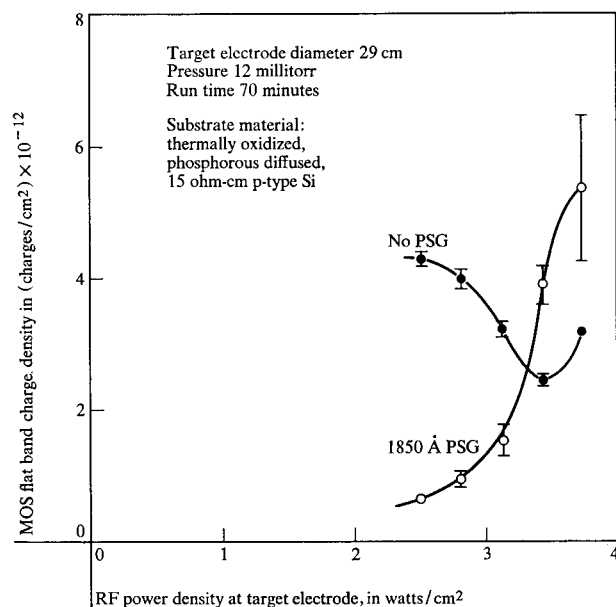
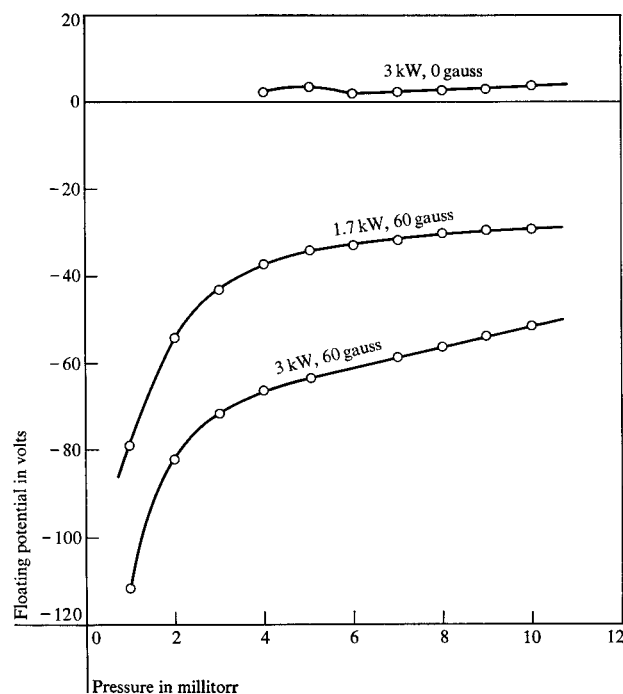


Figure 3 Flat band charge density vs. rf power density.

Figure 4 Wafer floating potential vs. pressure for different conditions of magnetic field and power. (Target electrode diameter, 29 cm.)



levels are consistently high through the range of investigation, dropping to a minimum probably because there is some charge relaxation occurring in the cool-down cycle after deposition. Obviously then, the conclusion from these experiments is that the power input should be

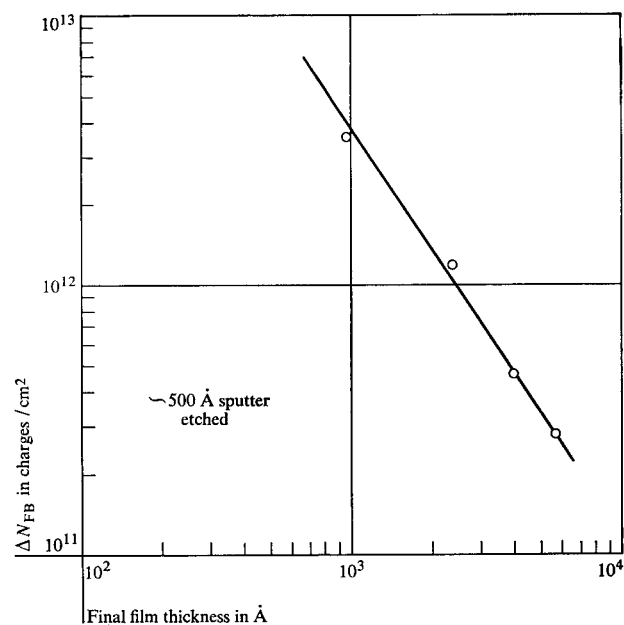


Figure 5 Charge build-up due to argon ion bombardment.

limited and that an adequate phosphosilicate glass layer thickness should be maintained to control charge build-up in films deposited in the "floating mode."

The motion of ionic charge in the insulator is known to be very much enhanced by an electric field, as can be readily shown by making a capacitor from a sputtered silica film and measuring the charge that flows at high temperature upon the application of positive or negative bias. Positive bias produces no charge flow, whereas negative bias (SiO_2 film surface negative with respect to substrate) produces a limited charge flow that is interpreted to be the movement of positive ions from the substrate interface to the glass surface. Further evidence of the accumulation of positive ions at the silicon-oxide interface is the fact that MOS capacitors recover from the inversion caused by the application of sputtered glass when a negative voltage is applied at high temperature.

The value of the electric field in the insulator during deposition is not known, but one would expect to be able to control charge buildup due to ionic migration by simply maintaining an electric field of the proper polarity in the insulator as it is deposited. However, in the "floating mode," no access is available to the silicon to control its potential. Furthermore, no information was available concerning the potential at the surface of the insulator. Because of this, we made some floating potential measurements on silicon wafers that were contacted by small wires. Even if the measured potential is not precisely that of the insulator surface, it should bear some close relationship to the surface potential if the dc resistance to ground is sufficiently high. Figure 4 shows the results

of such a measurement. With no magnetic field applied, a small positive potential is observed throughout the operating pressure range. With a magnetic field applied, the observed potentials become very much more negative and are also power level dependent. From this it appears that inversion could be controlled by connecting the silicon to ground and simultaneously using a magnetic field. This situation has been evaluated in a small system where the wafers were gallium-interfaced with a constant-temperature block. Under these circumstances, experiments showed that no charge build-up occurred up to deposition temperatures as high as 400°C, which was the highest temperature investigated.

It is known that high-energy electrons (up to 2 keV) are present due to the acceleration of secondaries from the target face toward the substrate.⁶ Other workers⁷ have shown that electron bombardment can cause positive space charge build-up in thermally grown SiO₂ films. However, this space charge has also been shown to be easily annealed. Another source of bombardment is from high-energy argon neutrals and from argon ions.⁶

To check the effects of argon ion bombardment, thermally oxidized silicon wafers were sputter-etched⁸ for 30 minutes at a power density of 0.36 watts/cm² (about 10% of the normal deposition level) and an argon pressure of 7.5 millitorr, to remove approximately 500 Å. The wafers were held at room temperature by a Dow-Corning high-vacuum silicone grease contact to the water-cooled electrode. Charge levels were measured by the MOS capacitor technique and are plotted in Fig. 5 as a function of the final oxide film thickness.

It appears that the ion bombardment produces a positive space charge that decreases as the film thickness is increased. For typical device applications, there is usually a layer (3000 Å or more) of thermally grown SiO₂ protecting the device. In addition, the argon ion bombardment in this experiment was greatly in excess of that which would be expected during a normal deposition. Therefore, we feel that argon ion bombardment damage is not a serious contributing factor to charge build-up in most applications for bipolar integrated circuits.

These findings have led us to the conclusion that charge build-up is caused primarily by the migration of positive impurities, i.e., sodium ions, to the silicon-oxide interface; this can be controlled by the following means:

- 1) reduction of the total number of impurity ions through the use of high-purity targets;
- 2) reduction of the mobility of the impurity ions through a lowering of the deposition temperature;
- 3) use of an adequate phosphosilicate glass layer to act as a barrier to migration of the impurity ions; and
- 4) control of the electric field in the insulator during sputtering.

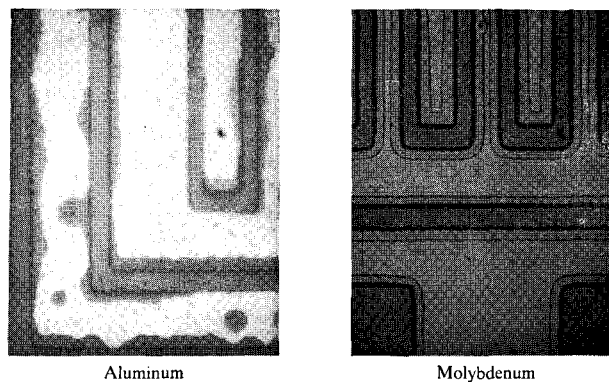


Figure 6 Attack of aluminum and molybdenum patterns due to inadequate sputtered SiO₂ edge protection.

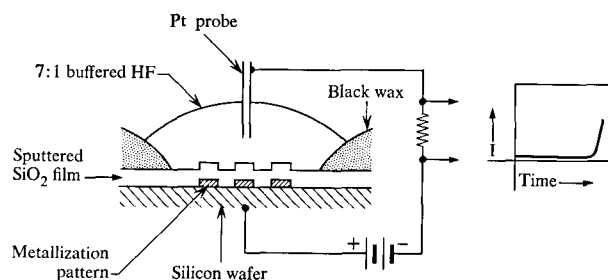
Obviously, the most satisfactory results can be expected by a combination of some or all of these factors.

Control of metal line edge protection

Although sputtered SiO₂ was found to be capable of adequately covering the edges of etched metal lines, it was also found that SiO₂ deposited under certain conditions would allow direct exposure of the metal line edges to a corrosive ambient, or would do so after only a very brief exposure to a dilute buffered HF etch. Examples of aluminum and molybdenum patterns attacked in this manner are shown in Fig. 6. The aluminum pattern also shows localized attack of the aluminum film, probably due to the failure of the SiO₂ film to protect the "hillocks" that are easily formed on that metal.

A simple test, illustrated in Fig. 7, has been used to study this problem. The metallization pattern used is not critical, but a long metal line periphery increases the sensitivity of the test. A unit cell of the metal pattern is masked off with Apiezon W wax, and a drop of buffered HF is applied to the cell. A voltage is applied between the metal pattern and a platinum probe, which is immersed in the buffered HF drop. Current is recorded as a function of time as shown. Under these conditions, the current through the cell will be practically zero until the etchant

Figure 7 Electrical edge attack test (7:1 buffered HF; room temperature).



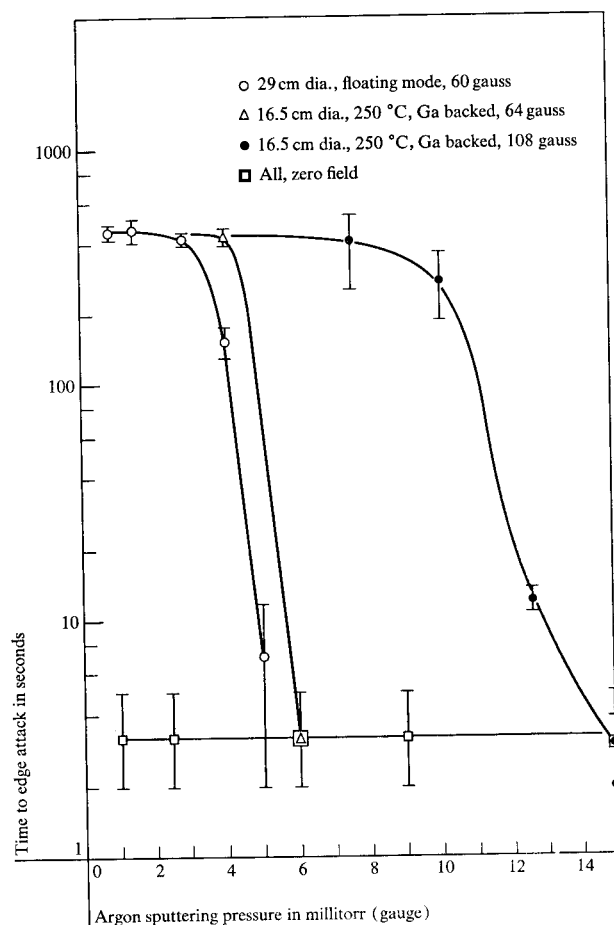


Figure 8 Time to edge attack for SiO_2 over molybdenum patterns vs. sputtering pressure at various magnetic field strengths.

Figure 9 Time to edge attack vs. SiO_2 thickness.

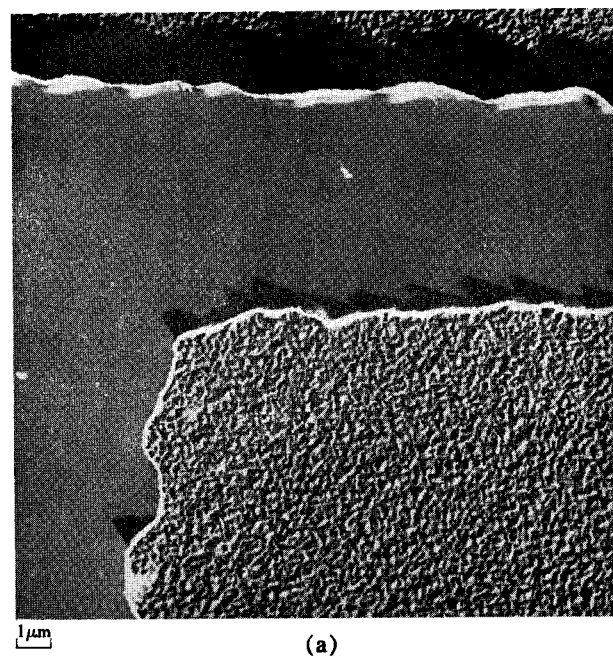
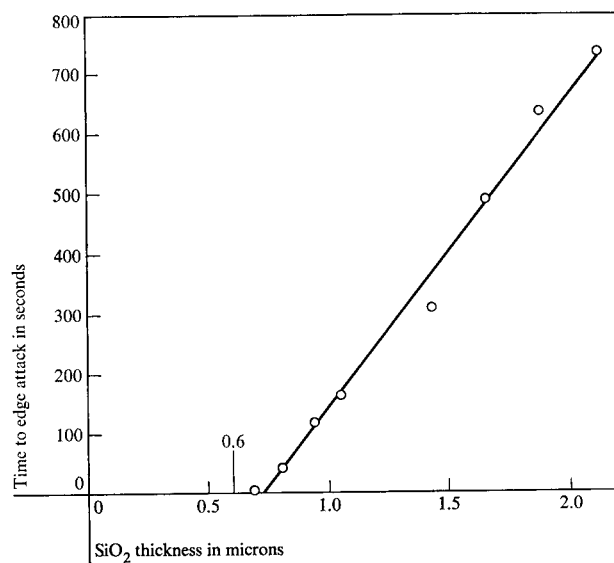


Figure 10 (a) Negative electron micrograph of molybdenum film pattern before SiO_2 deposition.

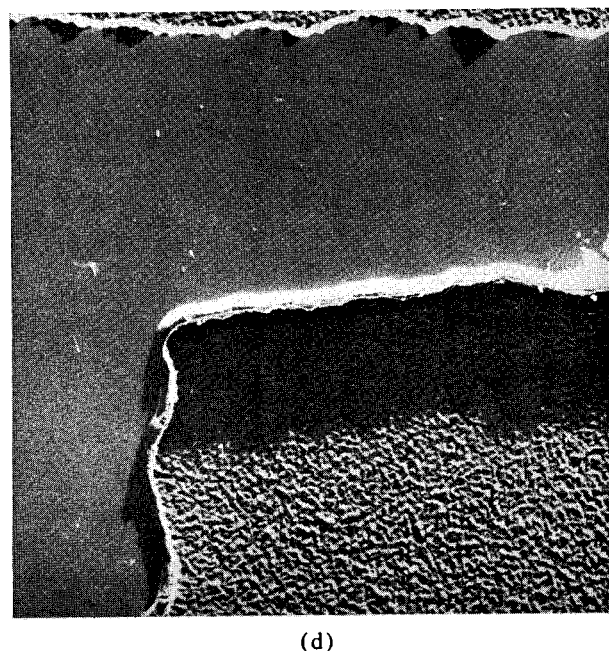
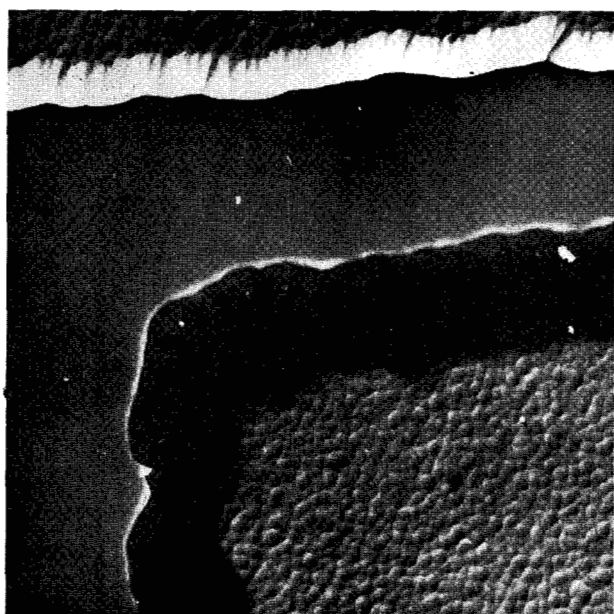


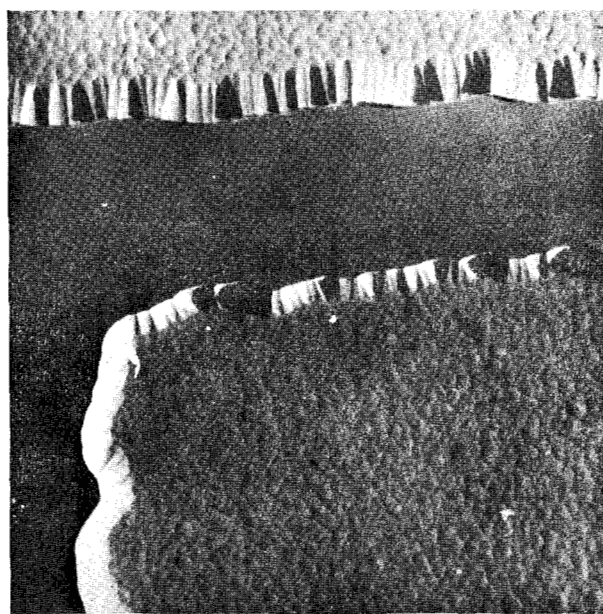
Figure 10 (d) Negative electron micrograph of molybdenum film pattern before SiO_2 deposition.

exposes the line edges; then a sudden large increase in current is observed. This "time to edge attack" can be used as a measurement of the edge protection of the film or, if greater precision is required, the thickness of glass removed at the moment of attack can be measured.



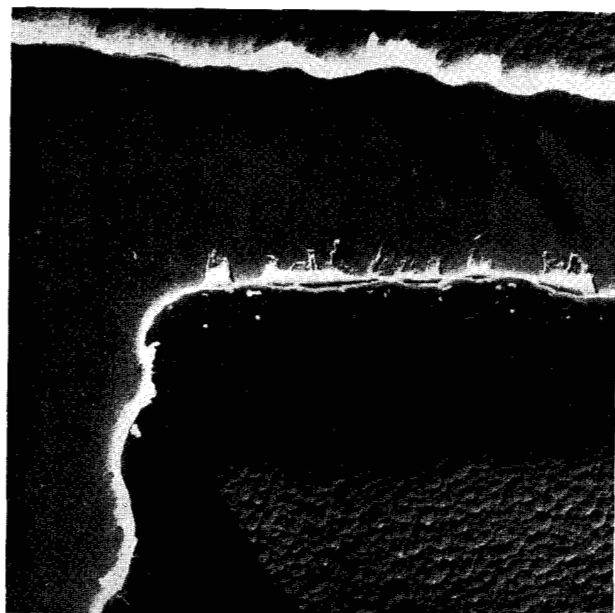
(b)

Figure 10 (b) Area of Fig. 10(a) after SiO_2 deposition at 108 gauss field strength and 2.5 millitorr (gauge) argon pressure.



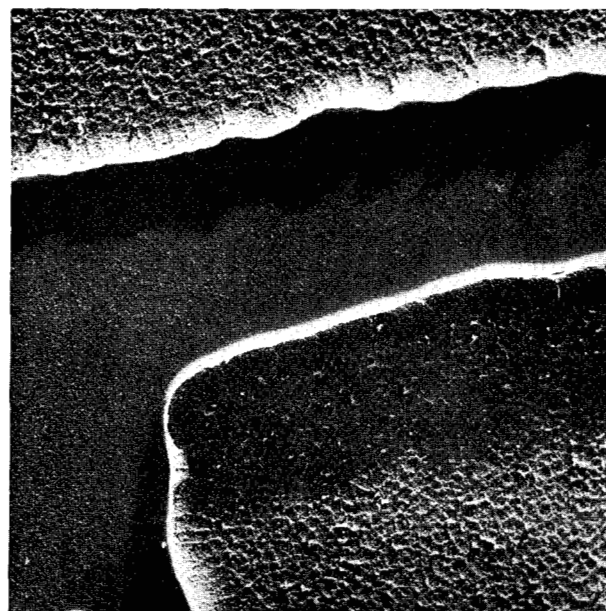
(c)

Figure 10 (c) Area of Fig. 10(b) after 15-second exposure to 7:1 buffered HF.



(e)

Figure 10 (e) Area of Fig. 10(d) after SiO_2 deposition at zero magnetic field strength and 2.5 millitorr (gauge) argon pressure.

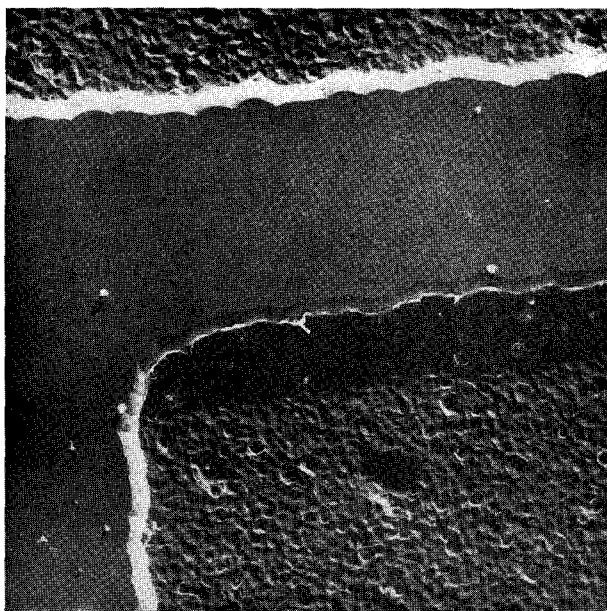


(f)

Figure 10 (f) Area of Fig. 10(e) after 15-second exposure to 7:1 buffered HF.

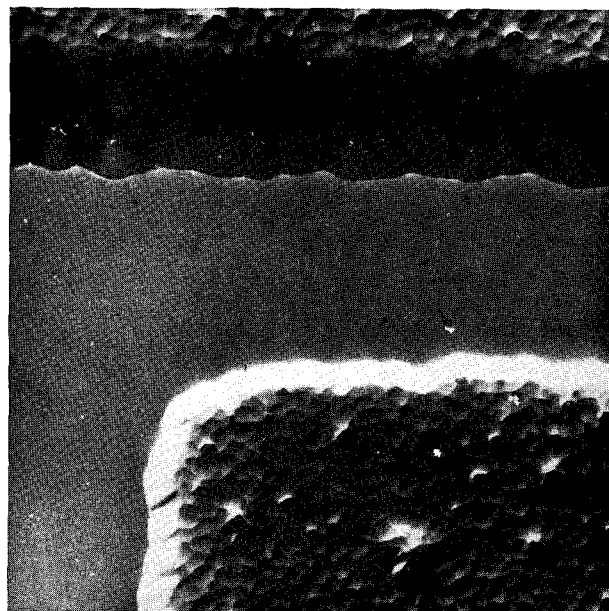
Using this test, edge protection as a function of a number of sputtering parameters has been studied in an experimental system similar to that described in the literature.⁴ The test vehicle was a pattern etched in a 6000-Å, pyrolytically grown molybdenum film on a silicon wafer,

and the sputtered SiO_2 films were 16,000 Å thick. Aluminum is commonly used in semiconductor devices. However, because of the presence of hillocks and because of the gradual and sometimes irregular taper of chemically etched aluminum lines, it is not a satisfactory metal for



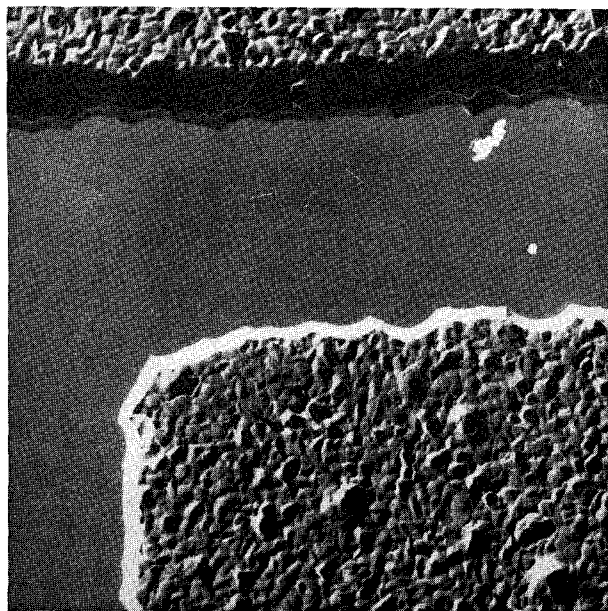
(a)

Figure 11 (a) Negative electron micrograph of aluminum film pattern before SiO_2 deposition.



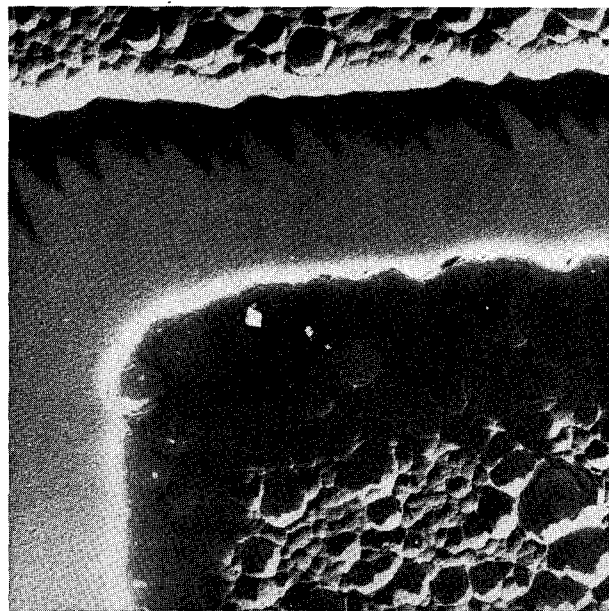
(b)

Figure 11 (b) Area of Fig. 11(a) after SiO_2 deposition at 108 gauss field strength and 2.5 millitorr (gauge) argon pressure.



(d)

Figure 11 (d) Negative electron micrograph of aluminum film pattern before SiO_2 deposition.

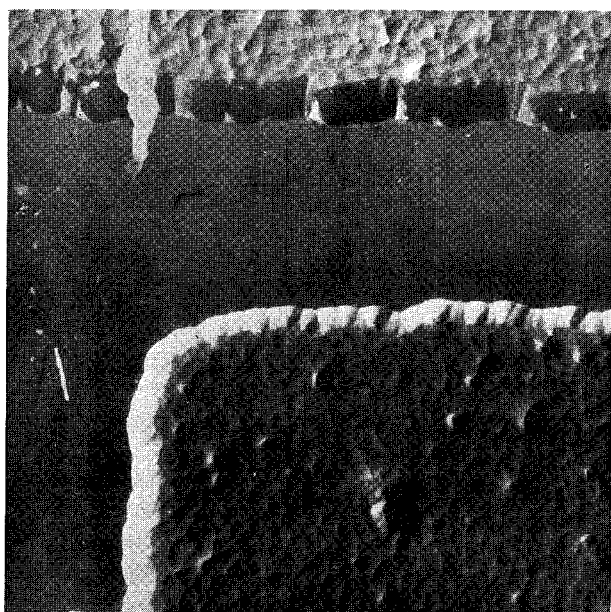


(e)

Figure 11 (e) Area of Fig. 11(d) after SiO_2 deposition at zero magnetic field strength and 15 millitorr (gauge) argon pressure.

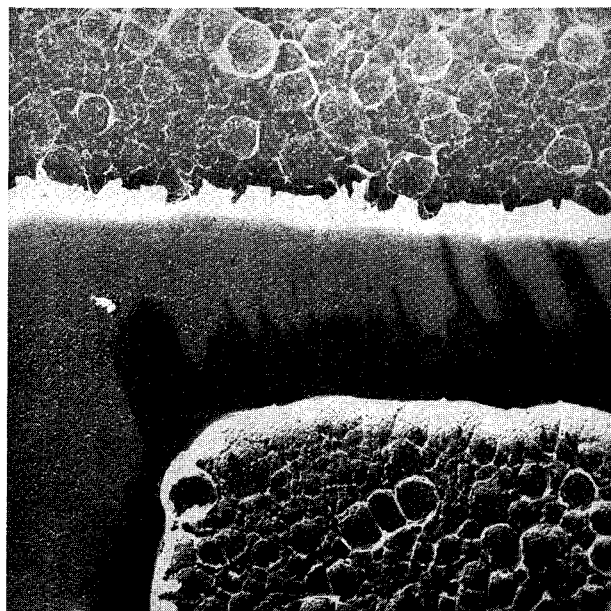
the study of edge protection. For this it is desirable to use a metal that is relatively smooth and can be etched to produce a rather sharp and abrupt step. We found that a metal like molybdenum is ideally suited (see Fig. 6). The results of some of this work are shown in Fig. 8,

where the time to edge attack as a function of argon sputtering pressure at several magnetic field strengths is shown. The curves show a strong relationship between argon pressure and edge protection. Also, as the various curves show, increasing the magnetic field strength widens the



(c)

Figure 11 (c) Area of Fig. 11(b) after 15-second exposure to 7:1 buffered HF.



(f)

Figure 11 (f) Area of Fig. 11(e) after 15-second exposure to 7:1 buffered HF.

pressure range over which good edge protection is achieved. It is interesting to note that for this metallization pattern, no edge coverage can be obtained without a magnetic field.

The edge protection test has also been useful in determining, for the conditions that give good edge coverage,

the sputtered SiO_2 film thickness required to protect metal lines of a given thickness. Figure 9 shows the "time to edge attack" for sputtered SiO_2 films of several thicknesses over a 6000-Å molybdenum metallization pattern. The SiO_2 films were deposited with a magnetic field under conditions of good edge protection, as shown to the left of the threshold in Fig. 8. In Fig. 9, it is seen that coverage is obtained when the SiO_2 film thickness is approximately equal to, or greater than, the metal thickness. These data also illustrate the fact that the "time to edge attack" can be used to compare the edge protection quality of sputtered films only when the metal and SiO_2 thicknesses are fixed. In practice, the metal thickness and, consequently, the SiO_2 film thickness are dependent on the required device characteristics. We have found it convenient to express edge protection quality in normalized terms, based on the observation in Fig. 9 that, for an etched molybdenum film of a certain thickness, a sputtered SiO_2 film of about equal thickness is required for minimum coverage. In practice, the test is performed in the same manner. When a current increase indicates edge attack, the cell is quenched with water. The initial glass thickness and the thickness removed before edge attack occurs are measured by fringe count or VAMFO techniques.⁹ From these thicknesses and from the metal film thickness, a normalized "degree of edge protection" can be calculated. For this we have introduced the concept of an "edge protection factor," which is defined as the ratio between the minimum glass thickness removed to expose the metal line edges and the difference between initial glass and metal thickness:

$$\text{Edge protection factor} = t_R / (t_G - t_M),$$

where t_R is the thickness of the glass removed, t_G is the initial glass thickness, and t_M is the metal thickness.

Typical values for the edge protection factor for etched molybdenum films and other patterns with a similarly abrupt line edge profile are from 0.8 to 1.0, irrespective of the molybdenum thickness. Values in excess of 1.0 are typical for aluminum films, because of the more gradual etched profile.

The detailed nature of edge protection has been studied by electron microscopy. Figures 10 and 11 show a series of negative replicas of the same molybdenum and aluminum patterns with sputtered SiO_2 films of high and low edge protection factors. The dark shadows at the edges of the bare molybdenum film indicate the very sharp, possibly undercut cross section which is typical of this metallurgy and which makes it particularly useful for the study of edge protection. Although the shadowing direction differs in the several pictures, one can see long shadows, indicating a deep crevice, at the line edges for the films deposited at zero magnetic field. This is schematically depicted in Fig. 12(a). It will be noted that these shadows

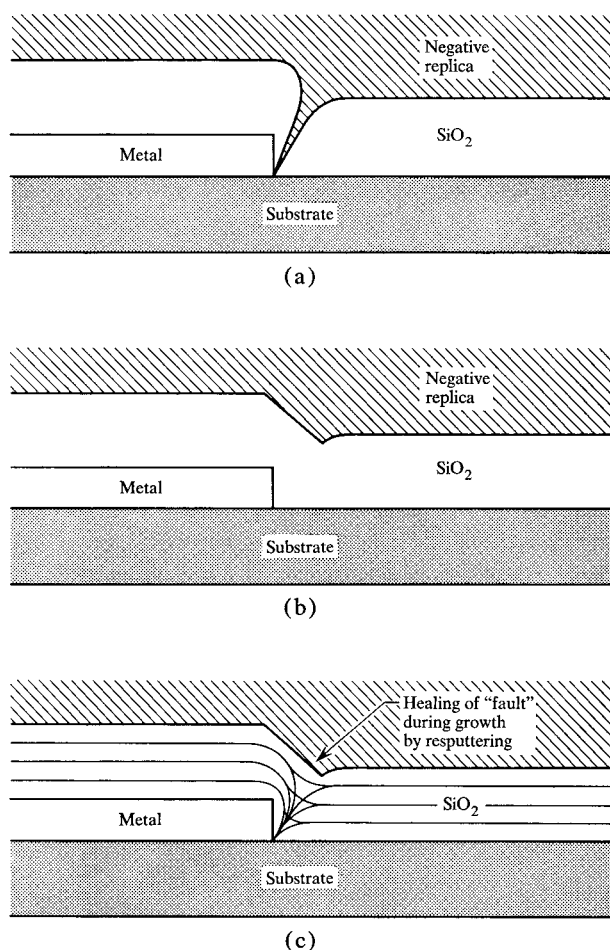


Figure 12 Schematic presentation of the edge protection mechanism: (a) poor edge coverage; (b) good edge protection; (c) "healing" mechanism.

Figure 13 Edge protection vs. substrate bias. (Target electrode diameter, 29 cm.)

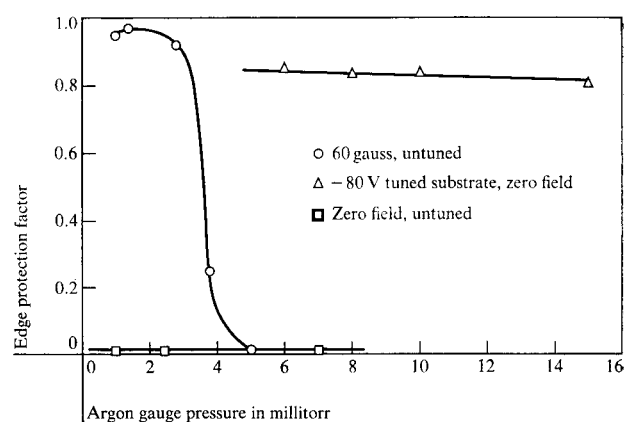
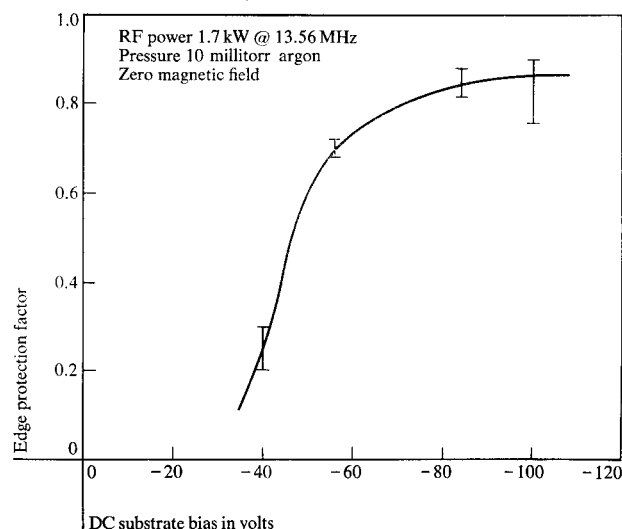


Figure 14 Edge protection vs. sputtering pressure for various conditions.

lengthen after brief exposure to buffered HF, showing the sensitivity of these areas to attack by glass etchants.

These results are interpreted to mean that on films that exhibit poor edge protection, there exists a crevice at the line edge in which the metal line edge is exposed or inadequately protected. In contrast, the films deposited with magnetic field show no long shadows, and practically no change upon exposure to buffered HF [see also Fig. 12(b)].

The explanation for the improved coverage that is obtained at a combination of low pressure and sufficient magnetic field strength can be found in Fig. 4. As can be seen from this figure, the dc potential of the substrate surface is negative in the presence of a magnetic field and becomes increasingly more negative at low pressures. This negative potential causes resputtering of the film while it is being deposited. For conditions with little resputtering or with a low re-emission coefficient,¹⁰ the sputtered SiO₂ thickness is considerably less at points near a step than at points away from it.¹¹ This condition, we feel, results in some sort of fault when an SiO₂ film is deposited over a metal film edge. This fault results in the crevice described earlier. When a considerable amount of resputtering takes place, i.e., under conditions which produce a high re-emission coefficient, one could say that a "healing" of the fault takes place during the growth of the film. This is caused by the redistribution of the sputtered material¹¹ and results in the absence of the crevice, i.e., in good edge coverage. A schematic illustration of this is given in Fig. 12(c). A comparable mechanism has been proposed by Seeman¹² for bias-sputtered metals.

Further evidence of this resputtering mechanism was obtained by measuring the edge protection factor for molybdenum patterns covered with sputtered SiO₂ films deposited in a substrate-tuned system.¹³ In this system,

the dc substrate and hence the resputtering potential are controlled by adjusting the rf impedance between substrate holder and ground.

The metal thickness in these experiments was 0.6 microns and the glass thickness was nominally 1.5 microns, although this varied slightly from run to run. The edge protection factor as defined above was measured and plotted against substrate potential in Fig. 13. It is clear that a threshold exists between -40 and -60 volts, with adequate coverage only at the more negative potentials. These runs were made at zero magnetic field, demonstrating that the film quality is really dependent on the potential, confirming that the improvement in edge coverage with magnetic field in untuned systems is due to the creation of the proper resputtering potential.

In Fig. 14 it is shown that, by substrate tuning, the pressure range for good edge coverage can be extended to higher pressures and that the presence of a magnetic field is no longer necessary. In the same figure are shown two of the curves from Fig. 8, with the dependent variable converted from time to edge attack to edge protection factor.

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