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Computer Aided Two-dimensional Analysis of the Junction Field-effect Transistor*

Abstract: A two-dimensional analysis is presented of the mechanisms of operation for a junction field-effect transistor. Particular emphasis is placed upon the process of electric current saturation in both wide gate and narrow gate structures. It is shown that velocity saturated carrier transport in a source-drain channel produces heretofore unreported mechanisms of device operation. Comparisons made between the conclusions derived from this two-dimensional analysis and the conventional one-dimensional theory of JFET operation are presented in graphic form.

Introduction

In his publication on the unipolar field-effect transistor,[1] Shockley presented a mathematical analysis of electrical conduction within a source-drain channel. Shockley's analysis was based upon two important simplifications: First, the gate junction space-charge layers were presumed to ideally satisfy all of the concepts used in his depletion layer theory[2] of abrupt p-n junctions and, second, the geometrical configuration of the structure was selected so the source-drain channel potential distribution could be approximated by one-dimensional mathematical models. Thereby, Schockley reduced a difficult two-dimensional boundary value problem into one that is separable into several mathematically tractable, one-dimensional problems. His simplifications were well justified, as shown by the many conclusions derived from his analysis that were subsequently verified by laboratory experiment. His analysis of the unipolar field-effect transistor provides fundamental insight into the mechanisms involved in junction field-effect transistor (JFET) operation.

The understanding derived from Shockley's analysis stimulated numerous subsequent investigations that further develop the theory of field-effect transistor operation. For example, Dacey and Ross[3] proposed a modification in which the carrier mobility is decreased throughout those regions of a source-drain channel containing a large electric field.[4] Later, Grosvalet et al.[5] suggested that the phenomenon of electric current saturation is directly attributable to the field-dependent mobility of carriers in the source-drain channel, although from theoretical considerations Kennedy and O'Brien[6] show that current saturation can exist in structures exhibiting a constant carrier mobility throughout the entire source-drain channel. Many unanswered questions remain concerning the mechanisms of operation within a JFET; such questions are answerable only by a rigorous mathematical analysis of this semiconductor problem.

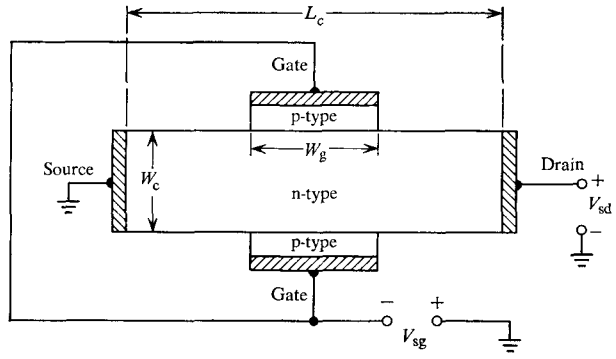

Figure 1 Illustration of JFET model.

The purpose of this paper is to present the results of a two-dimensional mathematical analysis of the structure shown in Fig. 1. The system of equations applied to this problem was previously outlined by Van Roosbroeck[7] in connection with his investigations of the flow of electrons and holes in a semiconductor. Finite difference methods are used, with the aid of an electronic computer; thereby, a rigorous evaluation is made of the mechanisms of operation that produce the electrical characteristics of junction field-effect transistors.

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* The analysis presented in this paper was supported in part by the Air Force Cambridge Research Laboratories, Office of Aerospace Research, under Contract F19(628)-C0116, Project 4608.

The mathematical model shown in Fig. 1 closely resembles the mathematical model used by Shockley and others in connection with their investigations of unipolar transistor operation. For this reason, the present analysis has provided an opportunity to study some aspects of the traditional theory of wide gate JFET's and, in particular, to establish the consequences of many approximations used in this theory. Furthermore, included here are some comparisons between the physical and electrical properties of narrow gate and wide gate structures; heretofore, narrow gate JFET'S have not been adequately considered in the technical literature.

Analysis

It has been shown[7] that the hole and electron distributions in semiconductor material are described by the equations

$$\text{(a)}\quad \text{div grad } \Psi = -\frac{q}{\kappa\epsilon_0}(N - n + p),$$

$$\text{(b)}\quad \mathbf{J}_p = -qD_p \text{ grad } p - q\mu_p p \text{ grad } \Psi,$$

$$\text{(c)}\quad \mathbf{J}_n = qD_n \text{ grad } n - q\mu_n n \text{ grad } \Psi,$$

$$\text{(d)}\quad \text{div } \mathbf{J}_p = qR_p,$$

$$\text{(e)}\quad \text{div } \mathbf{J}_n = qR_n, \quad \text{and}$$

$$\text{(f)}\quad \mathbf{J}_T = \mathbf{J}_p + \mathbf{J}_n, \qquad (1)$$

by assuming no trapping mechanisms within the structure under consideration.

Equation (1a) is Poisson's equation, and it relates the divergence of the electric field ($\mathbf{E} = -\text{grad } \Psi$) to the electrostatic charge distribution arising from both mobile charge carriers (holes p and electrons n) and immobile ionized impurity atoms N within the semiconductor lattice.

Equations (1b) and (1c) give the electric current distribution in a semiconductor arising from the transport of mobile holes and electrons. These equations express the dependency of each electric current component ($\mathbf{J}_p$ and $\mathbf{J}_n$) upon the concentration gradients of holes and electrons, the mobility of these charge carriers, and the electrostatic potential gradient (electric field) within the semiconductor material.

Throughout this analysis we have adopted the field-dependent mobility for electrons and holes as shown by Ryder,[4] from his investigations of this topic. In particular, there are two critical fields (E_{c1} and E_{c2}) in silicon at which the mobility relationship changes. The mobility is constant where the electric field is below E_{c1}. Throughout regions of this structure where the electric field is between E_{c1} and E_{c2}, the mobility depends upon the electric field as $\mu \propto E^{-\frac{1}{2}}$; for fields above E_{c2}, $\mu \propto E^{-1}$. Qualitative theoretical investigations of this subject[8] have led to a satisfactory phenomenological explanation for the large-field drift characteristics of electrons in silicon, although we are at present unable to quantitatively establish carrier velocities by other than experimental means.

Equations (1d) and (1e), the continuity equations for holes and electrons, assume an unspecified mechanism for carrier generation and carrier recombination. For simplicity, the present calculation is based upon the existence of a single recombination level located at mid-gap within the semiconductor material. Although recombination and generation of minority carriers are taken into account in this analysis, the magnitudes attributable to modern silicon devices are found to have little influence on the important mechanisms contributing to field-effect device operation. Therefore the manner in which field-effect device operation is influenced by minority carrier recombination/generation is not considered in the present analysis.

Equation (1f) states that the total electric current density ($\mathbf{J}_T$) is a vector sum of the electric current densities due to holes ($\mathbf{J}_p$) and electrons ($\mathbf{J}_n$).

The six equations (1) are combined into three simultaneous nonlinear differential equations in three variables: electrostatic potential, mobile hole density, and mobile electron density. The analysis presented here results from numerical solutions of these three equations. To accomplish this task, three two-dimensional nodal arrays are used to approximate the structure under investigation. Boundary conditions for each variable, in addition to the impurity atom distribution, are introduced as constraints upon the solution for each nodal array. Thereafter, using a finite-difference form for the associated differential equations, relaxation techniques[9-13] are applied sequentially to the three arrays; the simultaneity of the solution is assured by a Picard iteration[14] occurring among these arrays.

Throughout this mathematical investigation, particular emphasis is placed upon the selection of boundary conditions that do not introduce errors in the calculated results. In particular, the boundary conditions used in this analysis approximate the physical and electrical characteristics of the outer periphery of this semiconductor structure, rather than internal boundaries established by its physical or electrical properties. A homogeneous impurity atom distribution is assumed within both the n-type and p-type semiconductor material, and an abrupt impurity atom transition is used at the metallurgical boundaries of the gate junctions. The exposed semiconductor surface is assumed to be an ideal electrical insulator; i.e., no electric current is permitted normal to these bounding surfaces. The ohmic contacts are approximated by equipotential surfaces that are charge neutral; these ohmic contacts have been located sufficiently far from the active regions of this device to have no influence upon its calculated electrical properties.

In the calculations presented here, the physical and geometrical properties of the analytical model (Fig. 1) are consistent with a previously described high-frequency

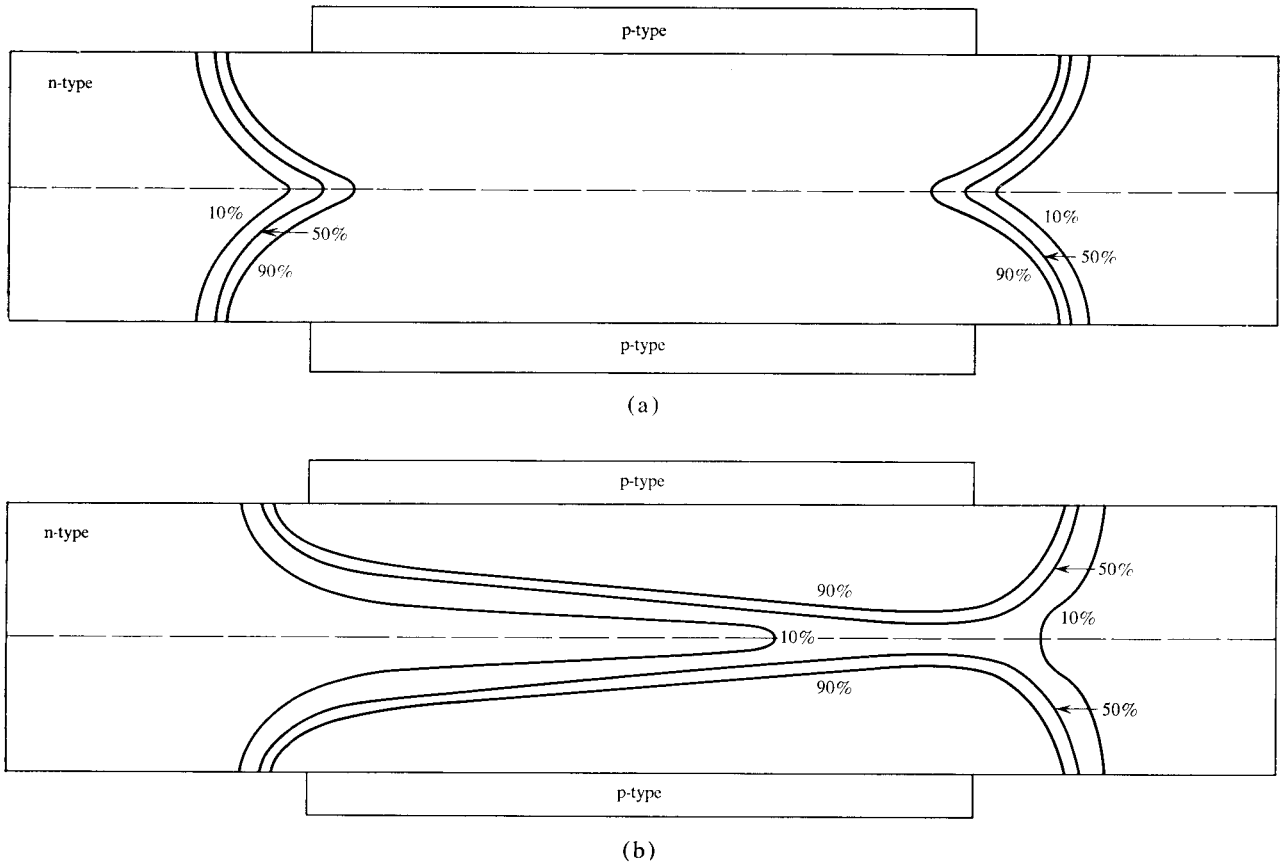


Figure 2 Calculated mobile electron distribution in a wide gate JFET (constant electron mobility). (a) $V_{sd} = 0$, $V_{sg} = 5.0$V; (b) V_{sd} as described in text, $V_{sg} = 0$.

JFET in silicon.[15] The dimensions of this structure are particularly small: The source-drain channel length L_c is 2 μm, and the channel width W_c is 0.4 μm. The source-drain channel is assumed to be doped n-type (1.5×10^{17} atoms/cm^3) and the gate junction region p-type (10^{19} atoms/cm^3).

Behavior of the JFET at pinch-off and beyond

In field-effect device operation, an important concept is source-drain channel pinch-off by the gate junction space-charge layers. From Shockley's analysis,[1] pinch-off is presumed to be the onset of electric current saturation. This concept is generally adopted in the theory of field-effect transistors, although it is conceded that the presence of a source-drain electric current eliminates the possibility of complete channel pinch-off. Complete pinch-off of the source-drain channel would produce an electrically insulating layer between the source and drain contacts, thereby eliminating all source-drain electric current.

Most physical models of JFET pinch-off have been taken from Shockley's theory of the unipolar transistor. The conducting channel between source and drain is divided into two regions:

Region I where the gate junction space-charge layer penetration is only partial, and Shockley's gradual approximation is applicable, and

Region II where the gate junction space-charge layer penetration is complete, and Shockley's gradual approximation is not applicable.

As noted by Shockley, this particular method of characterizing the regions of a source-drain channel is applicable only to JFET structures containing gate junctions that are wide (W_g in Fig. 1) when compared to the channel width (W_c in Fig. 1). For this reason, the present discussion is divided into two sections: first, the wide gate JFET and, second, the narrow gate JFET.

- *The wide gate JFET*

Figure 2 illustrates some fundamental properties of channel pinch-off with and without a source-drain electric

current. In Fig. 2(a), the source-drain biasing voltage V_{sd} is assumed to be zero and the source-gate voltage V_{sg} is sufficient to thoroughly deplete mobile carriers from the source-drain channel. Figure 2(b) shows the calculated mobile electron distribution when the source-gate voltage V_{sg} is zero and the source-drain voltage V_{sd} is selected so that the maximum gate junction biasing voltage equals the value assumed for V_{sg} in Fig. 2(a).

Unlike the depletion layer approximation for p-n junction operation, the present calculation does not produce a discrete boundary at the gate junction space-charge layer edge. For this reason, Fig. 2 shows three isoconcentration contours for mobile electrons bounding the gate junction space-charge layers: 90%, 50% and 10% of the electron density within the charge neutral semiconductor material.

In Fig. 2(a) the applied gate biasing voltage reduces the channel carrier density to about 10^{-6} of its magnitude in charge neutral material. Clearly, this source-gate voltage is far in excess of the value normally considered to be the pinch-off value for a JFET.

Although the maximum gate voltage in Fig. 2(b) is the same magnitude as in Fig. 2(a), many differences can be observed in the mechanisms of channel pinch-off. Along the longitudinal axis of symmetry in Fig. 2(b), the density of mobile electrons has been depleted to between 10% and 50% of the equilibrium value in charge neutral material. Therefore, a channel of mobile electrons resides between the gate junction space-charge layers; this channel maintains electrical conduction between the source and drain contacts. Figure 2(b) is typical of the electron distribution within a wide gate JFET when the source-drain biasing voltage is sufficient to produce electric current saturation. It should be noted that the calculations for Fig. 2(b) are based upon an assumption that the drift mobility for carriers is constant everywhere within the source-drain channel, although this assumption is recognized as an oversimplification.

Figure 2(b) illustrates a situation encountered throughout this investigation of JFET operation: In the presence of a source-drain electric current, complete pinch-off of the source-drain channel is never observed, regardless of the source-drain biasing voltage. At all values of applied voltage a channel of mobile carriers is found between the gate junction space-charge layers, and this channel maintains an electrical connection between the source and drain contacts. Furthermore, the dimensions of this channel (length, width, etc.) are modified by changes in the applied biasing voltages.

The calculations shown in Fig. 2(b) substantiate a proposal, first suggested by Grebene and Ghandhi,[16] that throughout the pinched-off region of this semiconductor device, any electric current between the source-drain contacts is confined to a very narrow conductive path near the center of the channel. The confinement of the electric current arises from a transverse electric field produced by electrostatic charges associated with the gate junction space-charge layers. This electric field opposes the transverse diffusion of majority carriers arising from a carrier density gradient appearing on each side of the channel; thereby, mobile charge carriers are confined to the longitudinal axis of symmetry between the two gate junctions.

An additional question concerns the departure of this narrow conducting path from charge neutrality. Jund and Grosvalet[17] have proposed that the free carrier concentration within this channel can become larger than its equilibrium value. In contrast, Wedlock[18] suggests that if the mobile carrier concentration exceeds its equilibrium value, the resulting electric field (due to the electrostatic charge) would tend to disperse the channel; this conclusion is contrary to the existence of a narrow conducting path between the source and drain contacts. From our calculations of wide gate JFET operation, the carrier density within this channel is always below its equilibrium value when a constant carrier mobility is assumed everywhere within the structure. A principal part of the resulting electrostatic charge is an integral part of the gate junction space-charge layers. Hence, the electrostatic charge within this channel produces an electric field component that is predominantly transverse to the direction of current flow between the source and drain contacts.

Numerous theoretical models have been proposed for JFET operation beyond pinch-off; some of these are shown in Fig. 3. Specifically, Shockley,[1] and Prim and Shockley[19] assumed that the boundary between regions I and II* moves toward the source contact with an increase in source-drain biasing voltage, Fig. 3(a). Little consideration was given to the details of carrier transport through this pinched-off region although Shockley recognized that a sufficient mobile carrier density must be present to support a source-drain electric current. Similarly, Grove,[20] Grebene and Ghandhi,[16] and others have adopted a modified form of the Shockley model; they assume that mobile carriers within the pinched-off region are confined to a narrow channel as in Fig. 3(b), and that the longitudinal electric field within this channel is sufficient to limit the average carrier velocity to its saturated value through lattice scattering. Wedlock[18] suggests that these models would predict a much softer current saturation than is experimentally observed because, in each model, the pinch-off point is assumed to change location with a change in applied voltage.

In contrast with the Shockley model, a frequently used model is one that was first suggested by Dacey and Ross[3]; they proposed that the pinch-off point of this channel appears immediately under the drain end of the gate

* Throughout this paper, the boundary between regions I and II will be called the pinch-off point within the source-drain channel.

junctions, and that this location is independent of the applied voltage. Both Sevin[21] and Wedlock[18] have adopted this proposal, with an addition that the gate junction space-charge layer extends toward the drain contact with an increase in applied voltage, Figs. 3(c) and 3(d). A fundamental difference between these two models is the manner of carrier transport through the pinched-off region. Sevin assumes a narrow conducting channel, Fig. 3(c), in which the longitudinal electric field is sufficient to attain the limiting carrier velocity. He gives no explanation concerning the mechanism by which this channel can be maintained for a reasonable distance beyond the gate junction edge.[18] Wedlock assumes that carrier transport through this pinched-off region arises from both drift and diffusion, Fig. 3(d), rejecting the possibility of a longitudinal electric field sufficient to introduce velocity saturation. It is emphasized that by maintaining the pinch-off point at a fixed location, both of these models predict a hard saturation of the source-drain electric current.

To answer some of these questions, a sequence of calculations has been performed throughout a range of source-drain biasing voltage upon the analytical model used in this investigation (Fig. 1). Figure 4 shows the calculated space-charge layer distribution at source-drain voltages of 4.0, 5.0 and 7.0 volts. It is emphasized that a sufficient electric field is present in the pinched-off region of Fig. 4 to produce velocity saturation of the mobile carriers, although this mechanism is not taken into account. For illustrative purposes, Fig. 4 shows the manner of channel pinch-off when a constant carrier mobility is assumed everywhere within this semiconductor structure.

In a fashion consistent with Shockley's theory, Fig. 4 shows that the pinch-off point within this structure moves toward the source contact with an increase in source-drain voltage. Pinch-off first occurs under the drain contact end of the gate junctions; in this particular model a gate voltage in excess of approximately 3.6 volts will produce channel pinch-off. Therefore, Fig. 4(a) shows the calculated carrier distribution at, or very near, initial pinch-off within this semiconductor device. It is emphasized that pinch-off represents only the onset of electric current saturation. For this reason, a further increase in the source-drain voltage will produce an increase in source-drain electric current. Associated with this increase in source-drain electric current is a movement of the pinch-off point toward the source contact.

As this structure is biased more deeply into current saturation, a change in source-drain voltage produces only a small relative change in the pinch-off point. For example, a comparison between Figs. 4(a) and 4(b) shows that a change in V_{sd} from 4.0 to 5.0 volts produces a relatively large motion of the pinch-off point toward the source contact. From Figs. 4(b) and 4(c), a relatively small change is observed in the location of this pinch-off point with a change in V_{sd} from 5.0 to 7.0 volts. It is implied by these calculations that in the absence of a field-dependent drift mobility, the pinch-off point moves toward the source contact with an increase in source-drain voltage, and that this motion is proportional to the change in source-drain electric current.

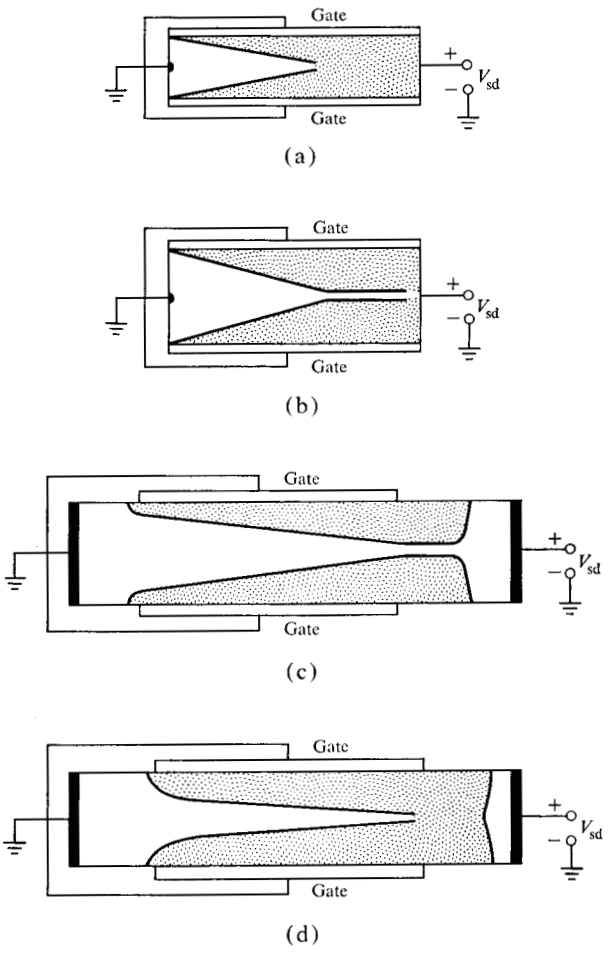


Figure 3 Proposed models for JFET operation beyond pinch-off (after Wedlock, Ref. 18).

In his discussion of this topic, Sevin[21] proposes that a narrow conductive channel starts at the drain end of the gate junction and extends toward the drain contact, Fig. 3(c). Furthermore, he proposes that the length of this channel increases with an increase of source-drain voltage. Wedlock[18] disagrees with this model because the electric field distribution beyond the end of the gate junctions could not produce a narrow conductive channel; he proposes that substantial flux spreading would exist throughout this part of the gate junction space-charge layer. Figure 5 illustrates the calculated electron flux distribution throughout the source-drain channel within this semiconductor device.

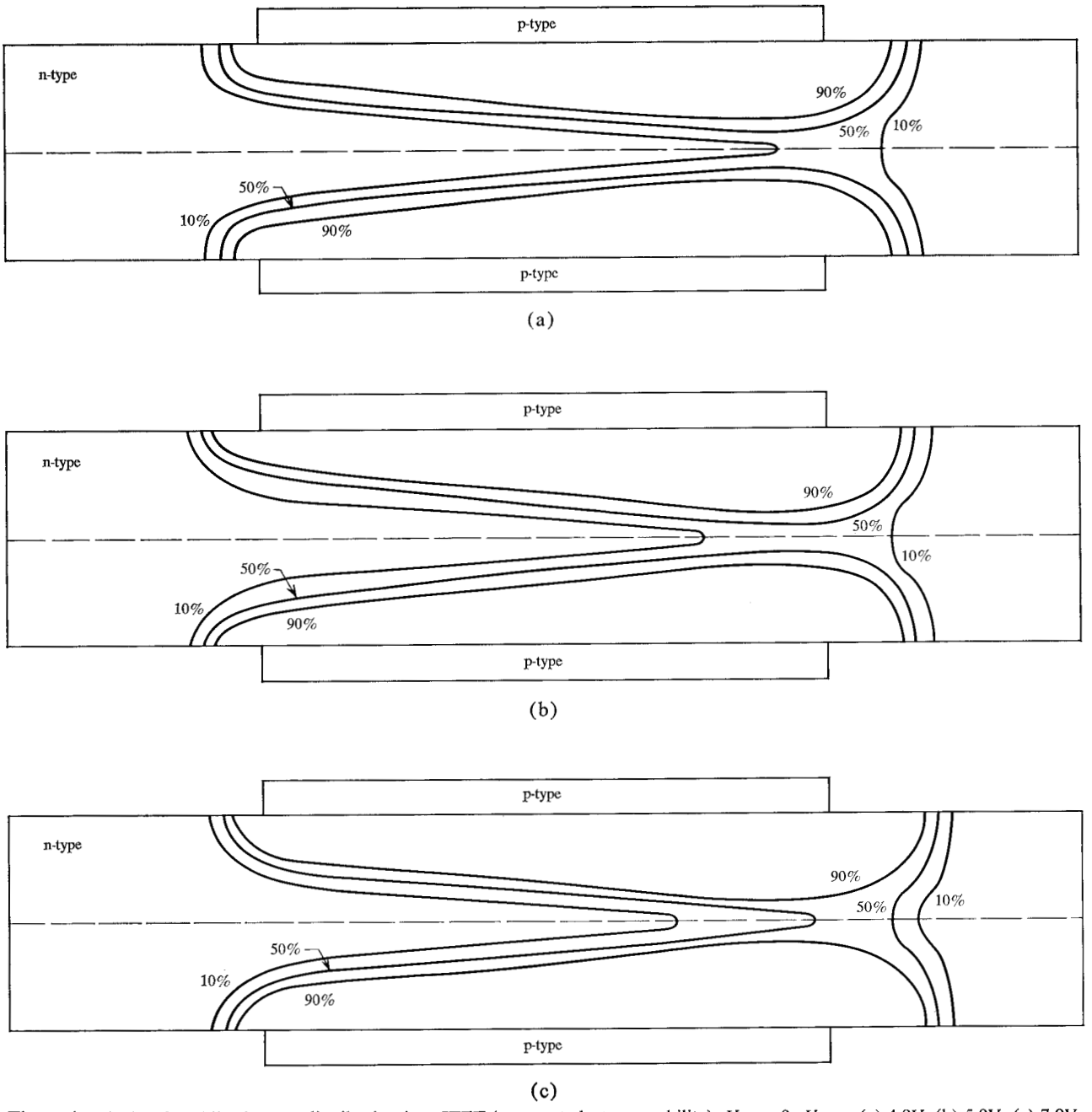


Figure 4 Calculated mobile electron distribution in a JFET (constant electron mobility). $V_{sg} = 0$; V_{sd} = (a) 4.0V, (b) 5.0V, (c) 7.0V.

Figure 5 shows that the electron flux is confined to a narrow channel throughout that portion of the pinched-off region lying between the gate junctions; this narrow channel terminates at the drain end of the gate junctions. Beyond this termination, the calculated flux distribution agrees with Wedlock's proposal; substantial flux spreading takes place and electron transport is a consequence of both drift and diffusion. Figure 5 also illustrates that the dimensions of this channel are modified by changes in the source-drain voltage. In particular, an increase in V_{sd} produces a channel of greater length and smaller cross-section.

Thus far we have considered only the mechanisms of JFET operation that result from assuming that no external biasing voltage is applied to the gate junctions ($V_{sg} = 0$). Figure 6 presents a sequence of electron distribution calculations for a constant source-drain voltage ($V_{sd} =$ 7.0 V) and three different values of source-gate voltage

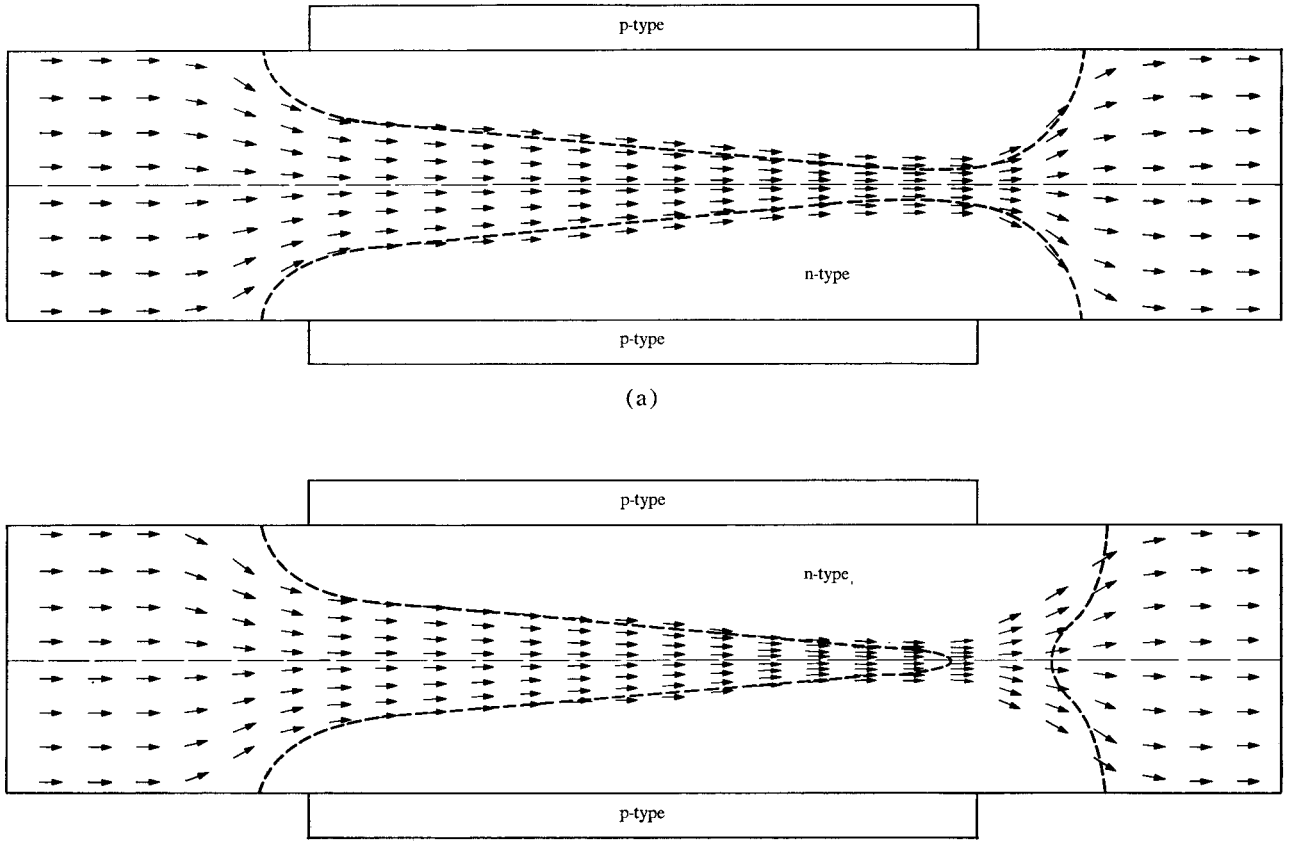


Figure 5 Calculated electron flux distribution in a wide gate JFET (constant electron mobility). $V_{sg} = 0$; V_{sd} = (a) 5.0V, (b) 7.0V.

(V_{sg} = 0, 1.21 and 2.42 V). From this illustration, an increase in source-gate voltage moves the channel pinch-off point toward the source end of this structure, and thereby the narrow conducting channel undergoes an increase in length. Furthermore, an increase in source-gate voltage produces a decrease in mobile carrier density within portions of this narrow channel. From these calculations, it is concluded that an increase in source-gate voltage increases the electrical resistance between the source and drain contacts, thereby decreasing the source-drain electric current. This increase in electrical resistance is attributable to an increase in length and a decrease in the mobile carrier density within this narrow conductive channel.

In field-effect device operation, channel pinch-off is presumed to be the onset of electric current saturation. This concept was adopted from a JFET theory in which carrier mobility is considered to be constant everywhere within the source-drain channel. If, instead, a field-dependent carrier mobility is assumed in the theory of JFET operation, electric current saturation can take place at a gate voltage below that required for channel pinch-off. Furthermore, a detailed analysis of this pinch-off process shows that mechanisms associated with the field-dependent mobility of carriers eliminate altogether any possibility of source-drain channel pinch-off within some JFET structures.

Figure 7 shows the calculated electron distribution within a source-drain channel at three different values of applied biasing voltage, V_{sd} = 3.0, 5.0 and 7.0 V ($V_{sg} = 0$). This calculation is based upon an assumed field-dependent electron mobility of the type described by Ryder[4] in his publications on this topic. In a later discussion, it will be shown that the mathematical model of Fig. 7 exhibits electric current saturation at a source-drain voltage in excess of approximately 2.5 to 3.0 volts, although the calculated pinch-off voltage for this structure is 3.6 volts. For this reason, Fig. 7(a) presents the calculated electron distribution for a structure biased almost to electric current saturation, but not to a value sufficient to attain channel pinch-off.

From Fig. 7, the channel pinch-off point remains at a nearly fixed location, regardless of the source-drain voltage; this location is close to the drain end of the gate junctions. Although these calculations appear to be in substantial

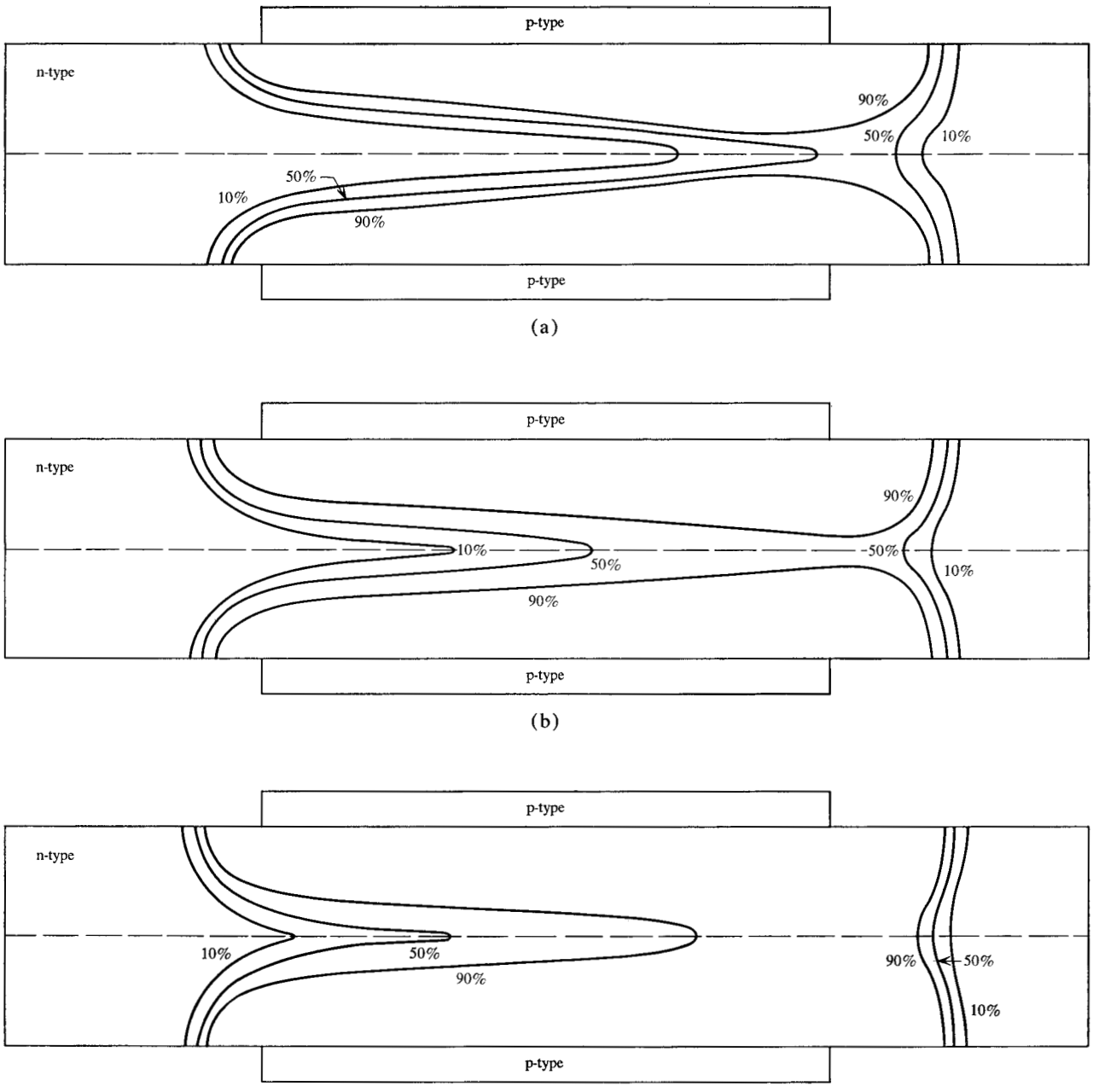


Figure 6 Calculated mobile electron distribution in the channel of a wide gate JFET (constant electron mobility). V_{sd} = 7.0V; V_{sg} = (a) 0V, (b) 1.21V, (c) 2.42V.

agreement with the model proposed by Dacey and Ross,[3] such is not the case. Figure 7(a) shows a region of carrier depletion extending across the entire source-drain channel, yet the applied voltage is less than the pinch-off voltage for this semiconductor device.

If a narrow gate JFET is biased into electric current saturation, it has been shown[22] that an electrostatic double-layer is induced into the source-drain channel. An important conclusion of the present investigation is that a similar double-layer is formed in any JFET when the longitudinal electric field is sufficient to produce a field-dependent carrier mobility. This mechanism has been encountered in all JFET calculations, although it is particularly evident in calculations pertaining to narrow gate structures. It is this double-layer formation that accounts for the characteristics illustrated in Fig. 7.

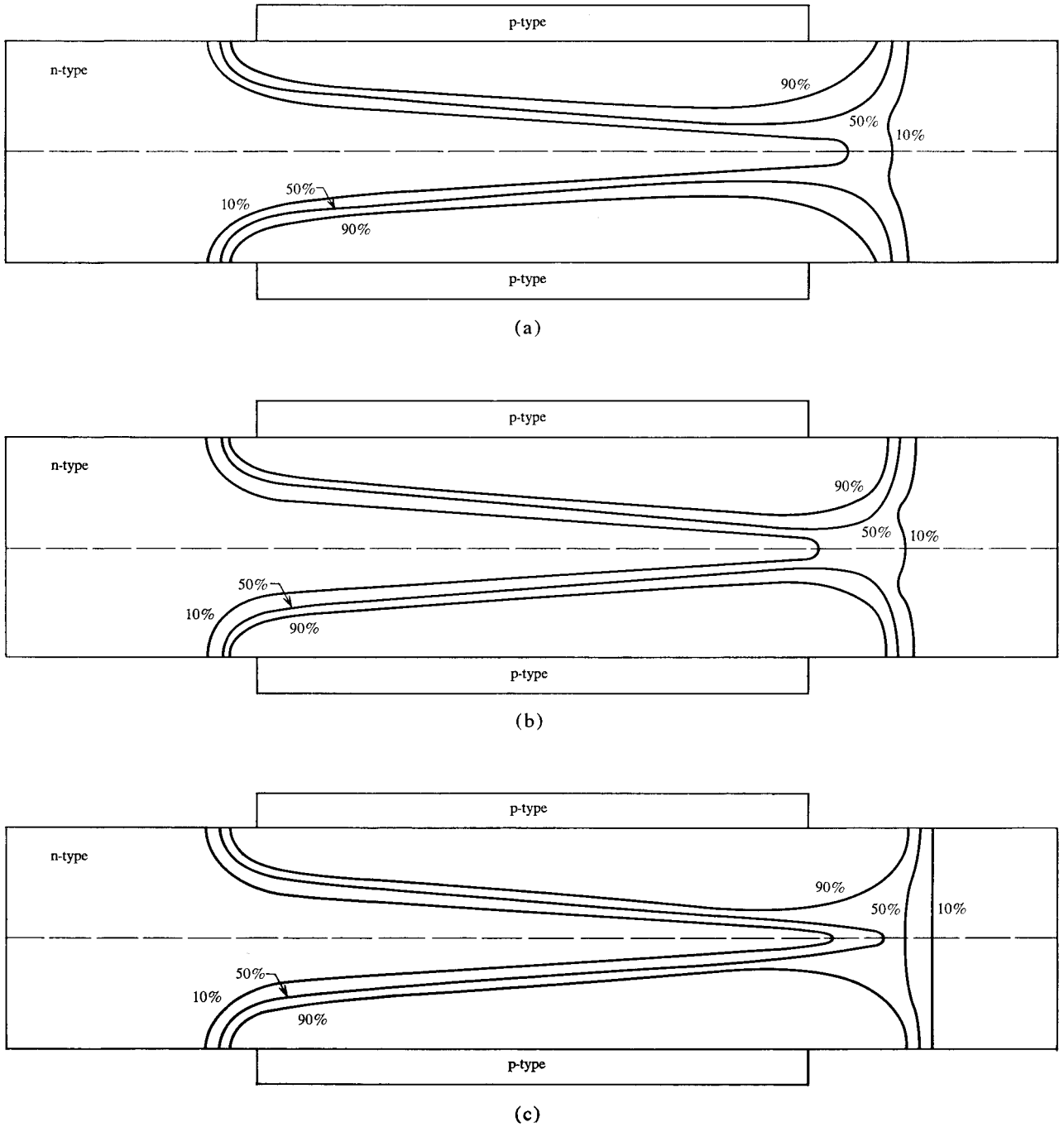


Figure 7 Calculated electrostatic charge distribution in a mechanical analog of a JFET (field-dependent electron mobility). V_{sg} = 0; V_{sd} = (a) 3.0V, (b) 5.0V, (c) 7.0V.

The fundamental nature of this double-layer-producing mechanism is illustrated by a mechanical analog of a JFET (Fig. 8). This analog is composed of silicon with the same physical dimensions (and electrical conductivity) as the structure shown in Fig. 1, except that the gate junction space-charge layers are represented by regions cut out of the semiconductor material. The geometrical configuration of this mechanical model produces a narrow conductive channel between the source and drain contacts; this channel is intended to approximate the conduction path in a pinched-off JFET. Figure 8 illustrates the electrostatic charge distribution within this mechanical analog, calculated after assuming an applied source-drain bias of 6.0 volts. It is emphasized that if a constant carrier mobility is assumed in this structure, charge neutrality is maintained throughout the source-drain channel.

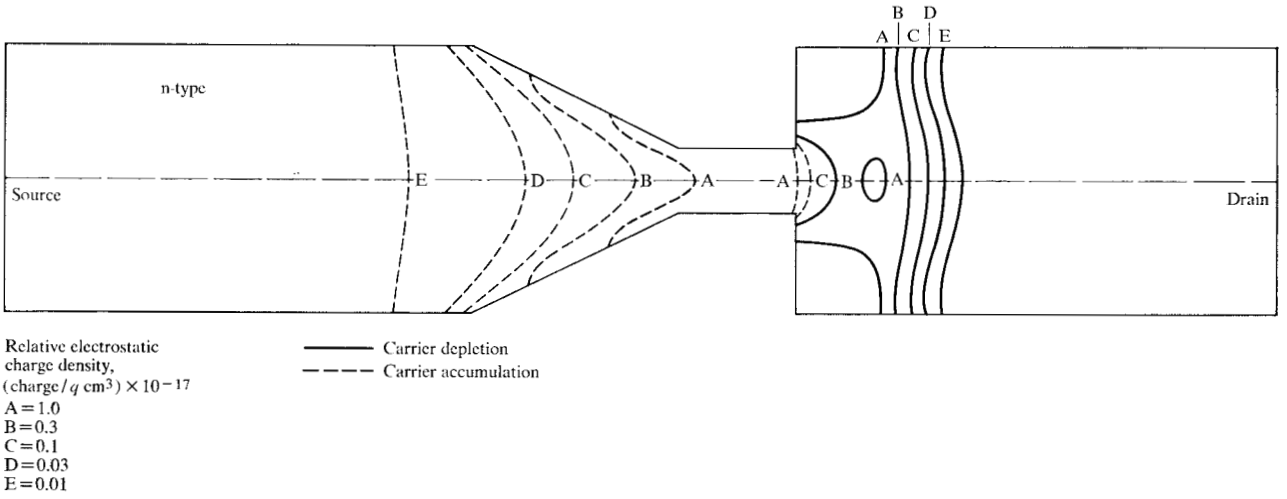


Figure 8 Calculated electrostatic charge distribution in a mechanical analog of a JFET (field-dependent electron mobility).

From Fig. 8, a region of mobile carrier accumulation exists on the source side of the narrow conductive channel. In a field-effect device, it is this process of carrier accumulation that renders immobile the pinch-off point, regardless of changes in source-drain voltage (Fig. 7). An increase in source-drain voltage increases the density of accumulated mobile carriers, and thus the region of carrier depletion cannot expand toward the source contact. Although only a limited amount of carrier accumulation is observed in a wide gate JFET, it nonetheless can be found in the computed characteristics of this semiconductor structure. A more detailed discussion of carrier accumulation in a source-drain channel is presented in the discussion of the narrow gate JFET semiconductor device. It should be noted that Hauser[23] suggested the possibility of carrier accumulation within a source-drain channel, although he did not recognize the consequences of this mechanism upon electric current continuity within the semiconductor structure.

Figure 8 also shows a region of carrier depletion on the drain side of this narrow conductive path. It is this region of carrier depletion that is observed in Fig. 7(a). The depleted part of the electrostatic double-layer extends between the gate junction space-charge layers, and thus it appears that channel pinch-off has taken place at a lower biasing voltage than theoretically predicted for this semiconductor device.

This redistribution of carriers (Fig. 8) arises from mechanisms that maintain electric current continuity despite the velocity saturation of mobile carriers in the narrow conductive channel. At small values of applied voltage the carrier velocity in this channel is directly proportional to the electric field; a decrease in channel cross-section produces an increase in electric field and, hence, an increase in electric current density. If, instead, the applied voltage is sufficient to attain velocity saturation within this narrow conductive channel, the increased electric field cannot produce a proportionate increase in electric current density. A consequence of this situation is mobile carrier accumulation until current continuity is established. In addition, a region of carrier depletion is formed to overcome the electrostatic charge attributable to the region of carrier accumulation; thereby longitudinal electric fields of equal magnitude exist at the source and drain contacts of this structure.

Figure 9 presents a sequence of electron distribution calculations assuming a constant source-drain biasing voltage (V_{sd} = 7.0 V) and three different values of source-gate voltage (V_{sg} = 0, 1.21 and 2.42 V). This illustration shows that field-dependent electron mobility and the associated electron accumulation produce channel pinch-off mechanisms differing from those encountered in structures containing a constant electron mobility (Fig. 8). In particular, little change is observed in the pinch-off point, up to a source-gate bias of 1.21 volts; a decrease in source-drain current (with an increase in source-gate voltage) arises from a decrease in channel width between the gate junction space-charge layers. Increasing the source-gate bias to 2.42 volts, Fig. 9(c), produces a relocation of the pinch-off point toward the source contact and substantial depletion of the narrow conductive channel. From Fig. 9(c) and the calculated electrical properties of this device, at large values of source-gate voltage the mechanisms of JFET operation approach those previously outlined for structures containing a constant channel mobility, Fig. 6(c).

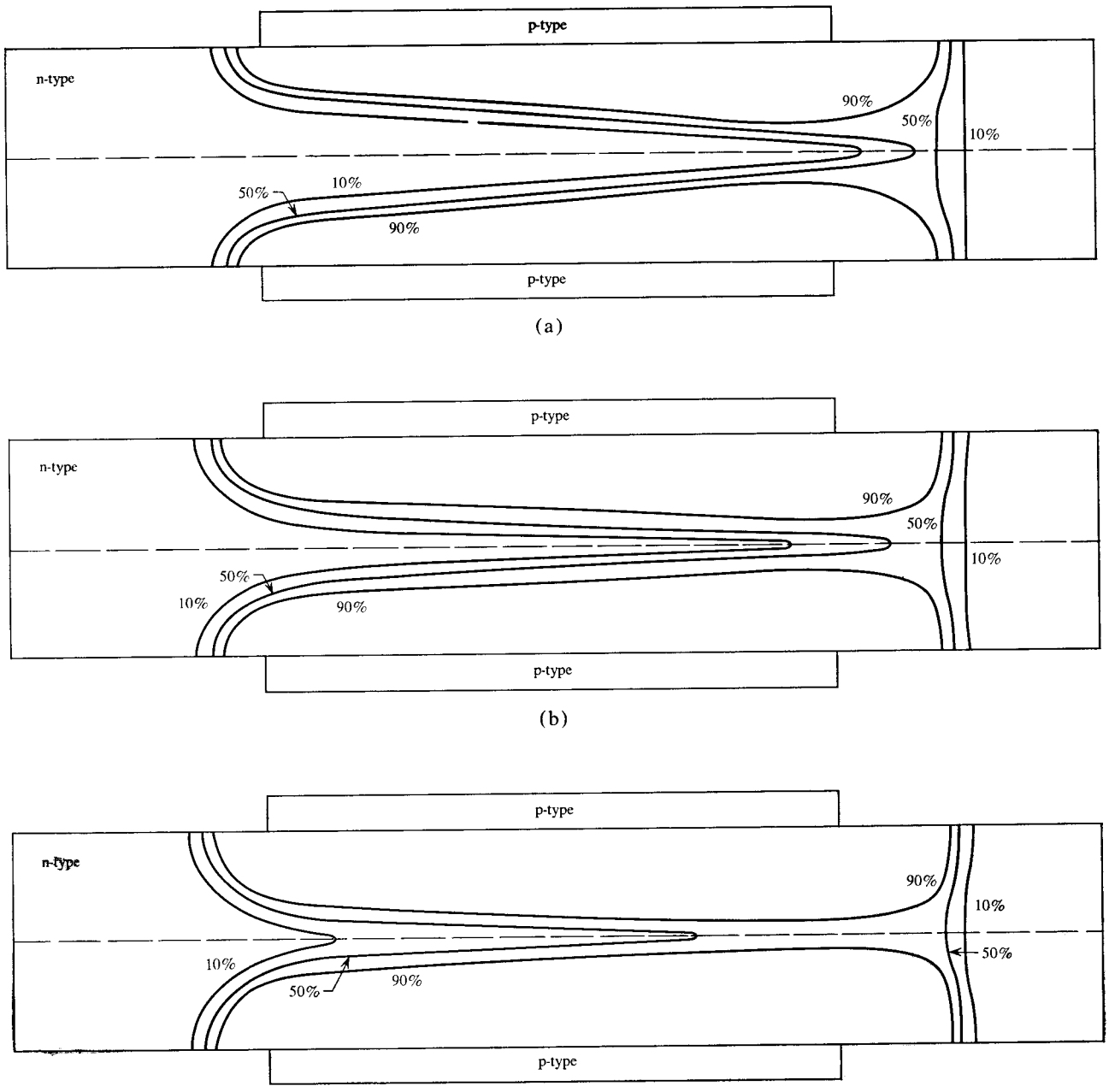


Figure 9 Calculated electron distribution in the channel of a wide gate JFET (field-dependent electron mobility). V_{sd} = 7.0V; V_{sg} = (a) 0, (b) 1.21V, (c) 2.42V.

• *The narrow gate JFET*

Induced carrier accumulation is most pronounced in the source-drain channel of a narrow gate JFET. It is proposed that this characteristic is qualitatively a consequence of two fundamental mechanisms within field-effect transistors: first, the non-ohmic properties of velocity-limited electrical conduction in semiconductor material and, second, the source-drain channel voltage distribution in a narrow gate device. It was previously shown that induced carrier accumulation is attributable to velocity-limited carrier transport, in association with a requirement of electric current continuity. From Poisson's equation, carrier accumulation produces an electric field that is proportional in magnitude to the integrated electrostatic charge arising from an excess of mobile carriers. In JFET operation this electric field, due to carrier accumulation,

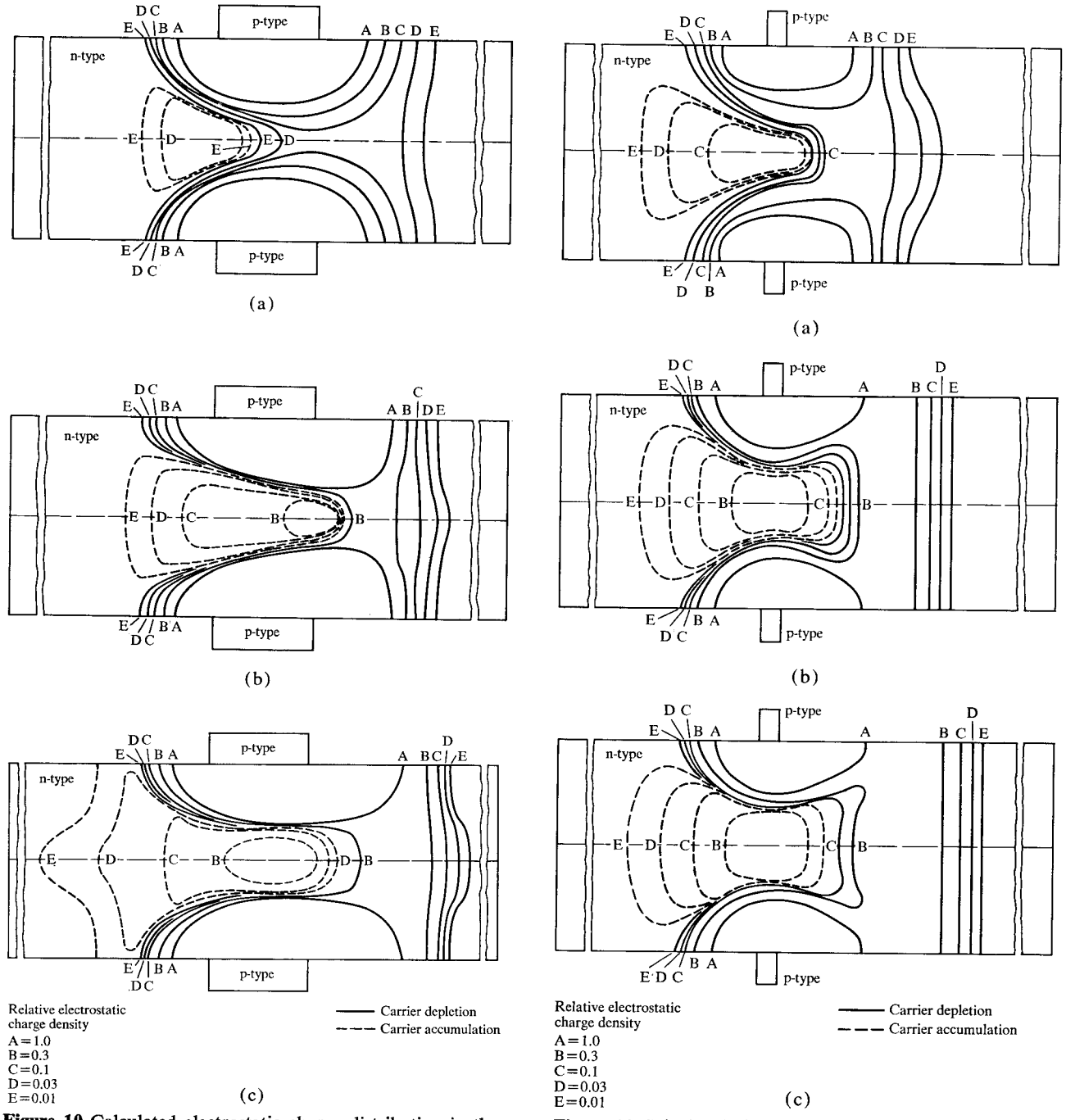


Figure 10 Calculated electrostatic charge distribution in the channel of a narrow gate JFET (field-dependent electron mobility; $2W_g/W_c = 1.0$). $V_{sg} = 0$; $V_{sd} =$ (a)3.0V, (b) 5.0V, (c)7.0V.

Figure 11 Calculated electrostatic charge distribution in the channel of a very narrow gate JFET (field-dependent mobility; $2W_g/W_c = 0.143$). $V_{sg} = 0$; $V_{sd} =$ (a)5.0V, (b) 7.0V, (c)9.0V.

must equal the electric field produced by the source-drain channel potential distribution; thus the gate junction width has a significant influence upon the density of accumulated carriers within a source-drain channel.

A substantial part of the applied source-drain voltage appears across the region of a source-drain channel that is restricted in cross section by the gate junction space-charge layers; the length of this region is commensurate with the gate junction width. Therefore, most narrow gate devices exhibit a maximum electric field of greater magnitude than wide gate devices for the same applied voltage. From Poisson's equation, this field is also proportional in

magnitude to the integrated excess carrier density along the longitudinal axis of symmetry for the structure. In a narrow gate device this integral is taken over a shorter distance, and it must have a greater magnitude, than in a wide gate device; Poisson's equation is therefore satisfied by an increase in the number of accumulated mobile carriers (and hence an increase in electrostatic charge) within the source-drain channel.

Throughout this discussion we shall consider the calculated characteristics for two different analytical models of a narrow gate JFET. The first model is assumed to characterize a narrow gate device ($2W_g/W_c = 1.0$) because it fails to satisfy Shockley's gradual approximation. The second analytical model is a very narrow gate device ($2W_g/W_c = 0.143$); the purpose of introducing this second model is to emphasize mechanisms of operation that are attributable to a narrow gate JFET.

Figure 10 shows the calculated electrostatic charge distribution within the channel of a narrow gate JFET for three different values of applied source-drain voltage (V_{sd} = 3.0, 5.0 and 7.0 V). As in a previous illustration (Fig. 7), a source-drain bias of 3.0 volts, Fig. 10(a), is not sufficient to produce channel pinch-off, yet this voltage is sufficient to produce current saturation. A sequence of similar calculations throughout the range 1.0 to 3.0 volts shows that the onset of induced carrier accumulation is coincident with the first indications of current saturation. Furthermore, the density of these accumulated carriers increases with an increase in source-drain biasing voltage; this introduces some basic differences in the mechanisms of operation between wide gate and narrow gate structures.

For example, the sequence of calculations illustrated in Fig. 10 indicates that the channel pinch-off point moves toward the drain contact with an increase in source-drain biasing voltage. This direction of motion differs from that suggested by conventional JFET theory, where an increase in biasing voltage either moves the pinch-off point toward the source contact (Shockley[1]) or the pinch-off point remains at a fixed location (Dacey and Ross[3]). In the present narrow gate model, induced carrier accumulation increases with an increase in voltage and the region of carrier accumulation expands along the longitudinal axis of symmetry; this expansion moves the boundary for carrier depletion toward the drain contact. At large values of applied voltage, Fig. 10(c), the pinch-off point of this narrow gate device is located well beyond the gate junction edge.

It is probably incorrect to identify a pinch-off point within a device exhibiting carrier accumulation. In Fig. 10(a), and also in Fig. 9(a), the maximum gate junction voltage is insufficient to produce channel pinch-off, yet the calculated electrostatic charge distribution shows a region of carrier depletion that extends across the source-drain channel. The boundary between carrier depletion and carrier accumulation (which we have been calling the pinch-off point) is more accurately defined as the electrostatic center of a double-layer induced into the source-drain channel by the gate junction space-charge layers.

Another consequence of induced carrier accumulation is the influence of this mechanism upon the gate junction space-charge layer width. In particular, accumulated mobile carriers in the source-drain channel appear as an electrostatic barrier that limits channel pinch-off by the gate junction space-charge layers, even when the structure is biased well into electric current saturation. Furthermore, from Fig. 10 an increase in source-drain voltage increases the channel width rather than decreasing it as would be consistent with conventional JFET theory. This increased channel width, due to induced carrier accumulation, results in an increase in source-drain electric current; further details of this topic are presented in the discussion of calculated volt-ampere characteristics for a JFET.

Induced carrier accumulation is even more pronounced in the source-drain channel of a very narrow gate JFET, Fig. 11. As in the narrow gate device, Fig. 10, carrier accumulation limits the amount of pinch-off obtained from the gate junction space-charge layers and thereby an increase is obtained in the width of this conducting channel between the source and drain contacts. Furthermore, a comparison between Figs. 10 and 11 shows that a decrease in the gate junction width produces an increase in the width of this conducting channel; thus when the device is biased into electric current saturation the source-drain electric current in a narrow gate JFET exceeds the current in a wide gate JFET. This conclusion has been derived from Figs. 10 and 11 and from a sequence of similar calculations for a number of other field-effect devices of various gate junction widths.

Further evidence of this increase in conducting channel width with a decrease in gate junction width is observed in a comparison of the calculated electron flux distribution among three models for a JFET: wide gate, narrow gate, and very narrow gate (Fig. 12). These calculated flux distributions are based upon an assumed source-drain bias of 7.0 volts and a source-gate voltage of zero. From Fig. 12, the wide gate device exhibits a relatively narrow conducting path between the two gate junctions and, in contrast, in the narrow gate structures the width of this conducting path is a substantial part of the total source-drain channel.

It is emphasized that not all of these differences in conduction path width (Fig. 12) can be attributed to the variation of gate junction width. The geometrical characteristics of these devices permit a greater maximum gate junction bias in the wide gate structure than in the narrow gate structures. Nonetheless these differences in gate junction biasing voltage are insufficient to account for the differences in conduction path width shown in Fig. 12; a

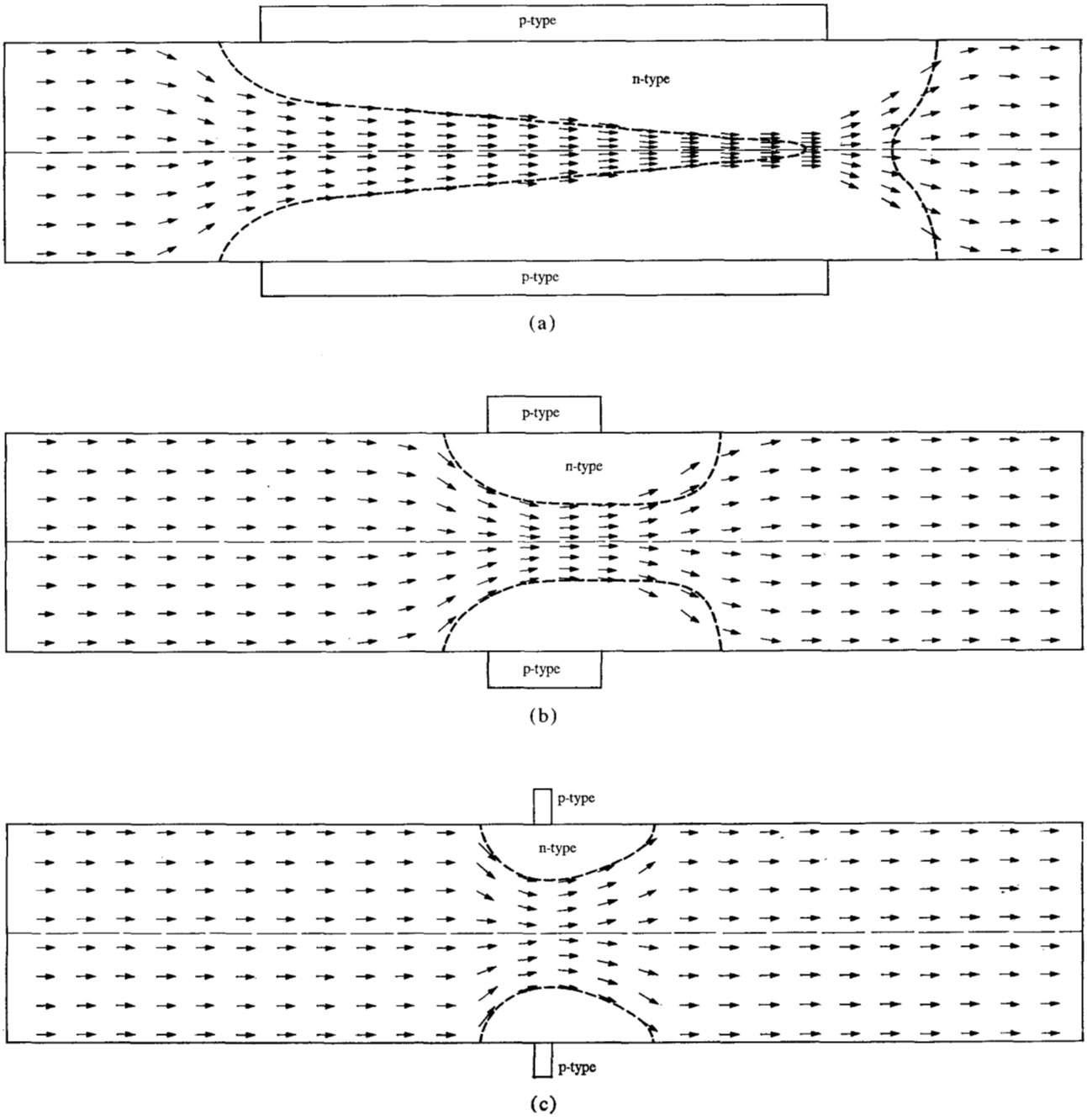


Figure 12 Calculated electron flux distribution in JFET structures biased into current saturation (V_{sd} = 7.0V; V_{sg} = 0). (a)Wide gate: $2W_g/W_c$ = 5.0; (b) narrow gate: $2W_g/W_c$ = 1.0; (c) very narrow gate: $2W_g/W_c$ = 0.143.

large part of this difference in conduction path width is attributable to carrier accumulation within the source-drain channel.

The foregoing calculations imply a need to restate the basic mechanisms of JFET operation, as applied to structures exhibiting a field-dependent carrier mobility. From Shockley's analysis of the unipolar transistor,[1] it is tacitly assumed that the gate junction space-charge layers pinch off the source-drain channel and thereby produce a narrow path, of large electrical resistance, between the source and drain contacts. This concept of JFET operation appears most applicable when a constant carrier mobility exists everywhere within the structure. If, instead, the longitudinal electric field is sufficient to produce velocity-limited transport of mobile carriers within a source-drain channel, Ohm's law cannot be used to describe the resulting poten-

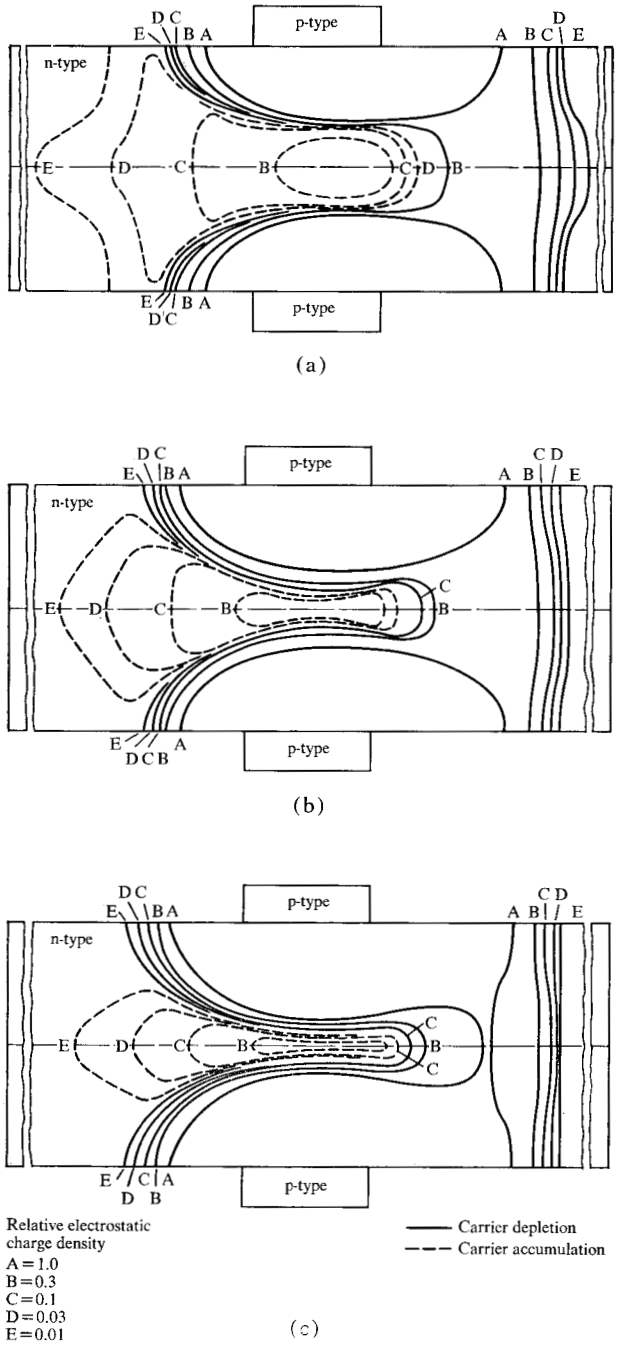


Figure 13 Calculated electrostatic charge distribution in the channel of a narrow gate JFET (field-dependent electron mobility; $2W_g/W_c = 1.0$). $V_{sg} = 7.0$V; $V_{sd} = $ (a)0, (b) 1.21V, (c)2.42V.

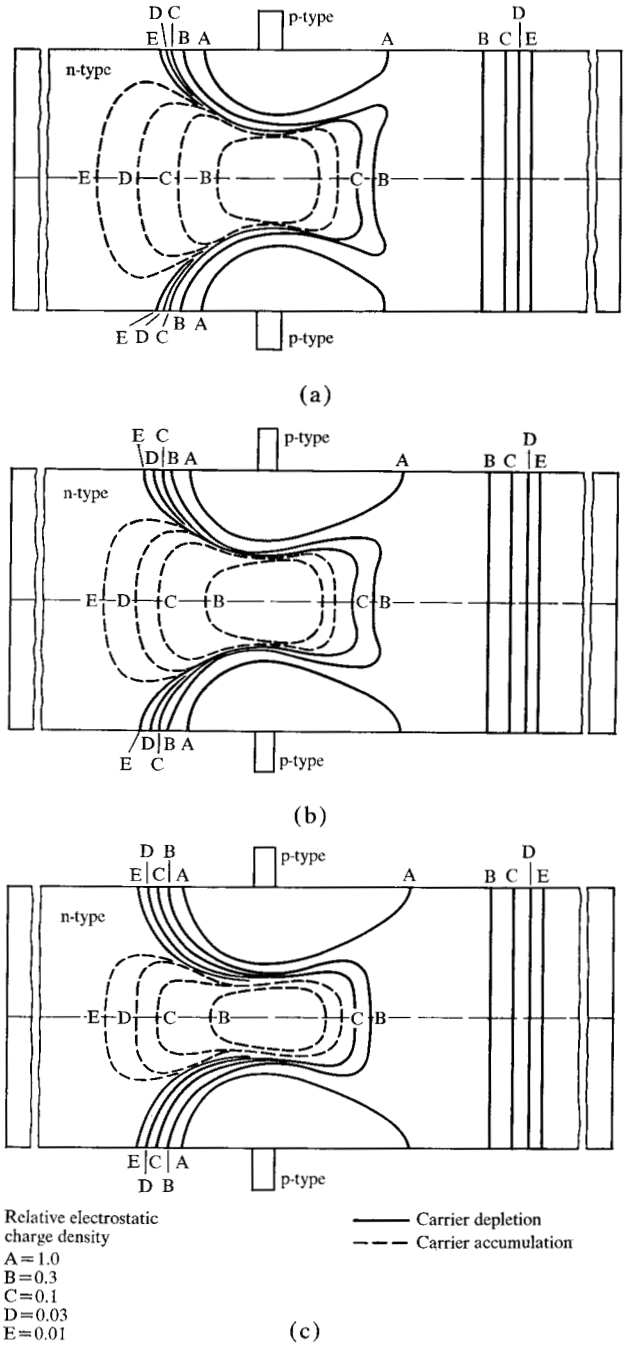


Figure 14 Calculated electrostatic charge distribution in the channel of a very narrow gate JFET (field-dependent mobility; $2W_g/W_c = 0.143$). $V_{sd} = 9.0$V; $V_{sg} = $ (a)0, (b) 1.21V, (c) 2.42V.

tial distribution. In this situation the gate junctions constrict (but do not pinch off) the source-drain conduction path, and this constriction induces a region of carrier accumulation. A large part of the potential distribution in a source-drain channel is thus attributable to an electrostatic double-layer that is located throughout a region previously assumed to be pinched off by the gate junction space-charge layers.

This process of channel constriction is observed in electrostatic charge calculations when a source-gate voltage is applied to the semiconductor structure, Figs. 13 and 14. Because a large part of the applied source-drain voltage

is supported by the induced electrostatic double-layer, the double-layer cannot be eliminated in narrow gate devices by the application of a source-gate voltage. Instead, the gate junctions constrict the channel of conduction between the source-drain contacts and thereby reduce the source-drain electric current. This process of channel constriction is accomplished without a substantial reduction in the electrostatic charge distribution along the longitudinal axis of symmetry.

This reduction of the source-drain electric current produces a redistribution of (and an increase in) the induced electrostatic charge within the channel. This situation arises from a decrease in the voltage drop in the material adjacent to the gate junction region; hence an increase is obtained in the voltage that must be supported by the induced double-layer. It is proposed that a consequence of this redistribution (and increase) of accumulated carriers is a reduction of g_m for the semiconductor device.

Potential distribution in a JFET

Shockley defined two different regions within the source-drain channel of a unipolar transistor.[1] The first region is essentially charge neutral and bounded on both sides by the gate junction space-charge layers. The second region is depleted of mobile carriers by the gate junction space-charge layers (this is traditionally called the pinched-off region), although this second region contains sufficient mobile charge carriers to maintain the source-drain electric current. An important part of Shockley's analysis is a mathematical determination of the voltage distribution along the axis of symmetry of this channel, due to an applied source-drain biasing voltage.

From a mathematical point of view this potential distribution calculation involves the solution of a very difficult boundary value problem. In this problem, the physical dimensions of the source-drain channel are dependent upon the voltage distribution within this region of the structure, yet this voltage distribution is precisely the unknown parameter to be established by such an analysis. To overcome this difficulty Shockley solved the problem on a piecewise basis and thereby obtained an approximate solution.

In Shockley's analysis, the potential distribution within the charge neutral region of a source-drain channel was determined from solutions for an approximating differential equation. It was assumed that the unipolar transistor could be segmented into narrow slices (of width dx) between the source contact and the extrapolated pinch-off point; these slices were taken in a direction perpendicular to the longitudinal axis of symmetry. The center of each slice contained a section of the charge neutral region, and each slice was bounded on each end by the gate junction space-charge layers and the gate junction regions. Thereby, he subdivided this part of the unipolar transistor into individual sections that could be mathematically analyzed on a one-dimensional basis. After calculating the electrical resistance of each individual slice, the potential distribution within the charge neutral region of this source-drain channel could be readily determined from the solution of an elementary differential equation.

The applicability of this approximation method is dependent upon the potential distribution both in the charge neutral region and in the gate junction space-charge layers. Ideally, throughout the charge neutral region the contours of constant potential should lie perpendicular to the longitudinal axis of symmetry. In addition, throughout the space-charge region these contours of constant potential should lie parallel to this longitudinal axis of symmetry. The first requirement (throughout the charge neutral region) is easily satisfied and therefore produces little difficulty. In contrast, the constant potential contours within the space-charge layers cannot lie parallel to the axis of symmetry; this situation represents an inherent approximation associated with Shockley's analysis. Recognizing this difficulty, Shockley restricted his analysis to structures in which the space-charge layer width changes gradually with distance (his gradual approximation) and thereby limited the error introduced by his method.

The purpose of this discussion is to emphasize a situation encountered throughout this mathematical investigation and, in particular, in the analysis of narrow gate JFET's. Specifically, if the constant potential contours in the gate junction space-charge layers are not parallel to the longitudinal axis of symmetry, the width of these space-charge layers cannot be established on a one-dimensional basis. At a given gate junction biasing voltage, structures not satisfying Shockley's gradual approximation contain a gate junction space-charge layer width that can be substantially less than the width given by elementary one-dimensional p-n junction theory.

The calculations plotted in Fig. 15 show that the wide gate device considered in this investigation ($2W_g/W_c = 5.0$) is not particularly wide gate, when viewed in terms of Shockley's gradual approximation. In a truly wide gate device, the electric field within the gate junction space-charge layers would be nearly perpendicular to the metallurgical p-n junctions; in Fig. 15, this electric field contains a significant component that is parallel to the metallurgical junctions. A consequence of this situation is a small reduction in the space-charge layer width as compared with the space-charge layer width of a one-dimensional abrupt p-n junction. It is estimated that the structure shown in Fig. 15 ($2W_g/W_c = 5.0$) represents a limit to the applicability of Shockley's gradual approximation; a further reduction in gate junction width would probably produce a situation in which the source-drain channel potential distribution could not be calculated on a one-dimensional basis.

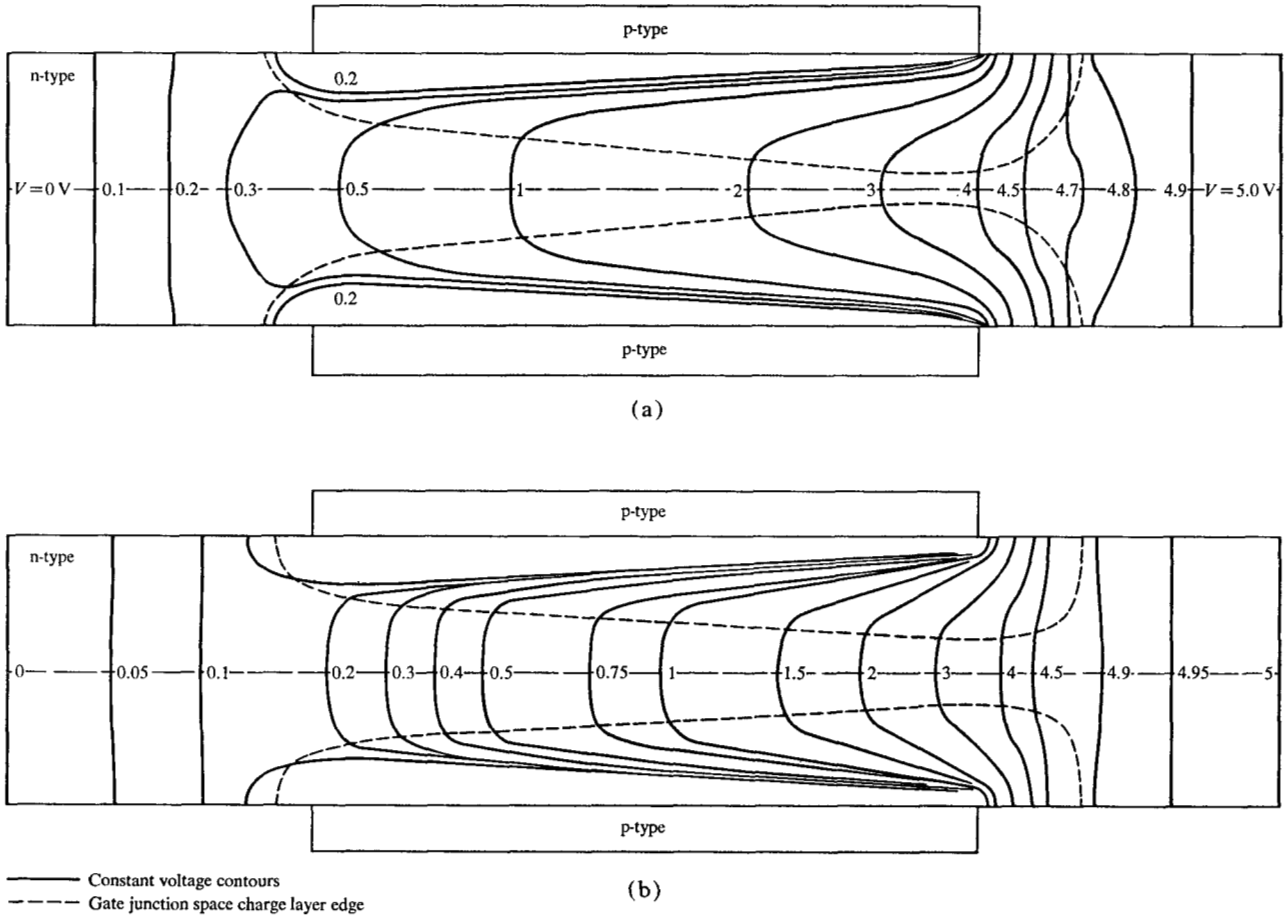


Figure 15 Calculated voltage distribution in a JFET ($2W_g/W_c = 5.0$; $V_{sg} = 0$V; $V_{sd} = 5.0$V), for (a) constant and (b) field-dependent mobility in the source-drain channel.

For illustrative purposes, Fig. 15 shows constant potential contours within a wide gate device calculated after assuming a constant carrier mobility, Fig. 15(a), and a field-dependent carrier mobility, Fig. 15(b), within the source-drain channel. These calculations are based upon an assumed source-gate voltage of zero and a source-drain bias of 5.0 volts. In this illustration the space-charge layer edge is designated by a contour along which the mobile carriers are depleted to 50% of their equilibrium density. Calculations similar to those shown in Fig. 15(a) were performed by Jund and Grosvalet,[17] using approximation methods; the results of their calculations are in substantial agreement with the calculations shown here.

Some important differences exist between the two potential distributions illustrated in Fig. 15. For example, the relative location of the constant potential contours in this illustration shows that a field-dependent drift mobility, Fig. 15(b), produces a reduction of source-drain electric current. In addition, it should be noted that this reduction of source-drain electric current is observed in Fig. 15(b) despite an increase of width in the conducting channel between the two gate junction space-charge layers. By direct comparison between Figs. 15(a) and 15(b), a field-dependent drift mobility is observed to produce an increase in voltage drop throughout the narrow part of this channel; this increased voltage drop is attributable to the electrostatic double-layer that is induced into the source-drain channel by the gate junctions.

From Fig. 15(a) (constant drift mobility), a comparison has been made between the source-drain channel potential distribution calculated using Shockley's approximation methods and a two-dimensional analysis of the problem. This comparison is presented for an assumed source-drain bias of 7.0 volts, and for four different values of source-gate voltage: 0, 1.21, 2.42 and 3.63 V. Figure 16 shows the distribution of voltage along the longitudinal axis of symmetry, as calculated with respect to the potential upon the gate junction region of this structure. The abscissa in

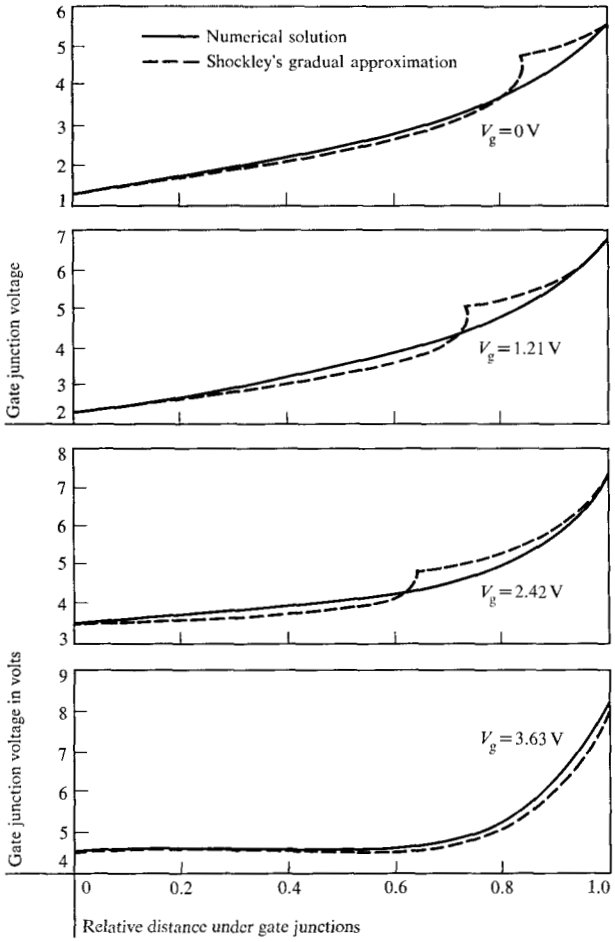


Figure 16 Calculated gate junction voltage distribution in the wide gate JFET. $V_{sd} = 7.0$V.

Fig. 16 is a normalized distance under the gate junctions; the origin of this normalized spatial coordinate is the source-contact end of the gate junctions.

Shockley's analytical methods produce a discontinuity in the calculated voltage distributions within a source-drain channel. This discontinuity appears at the boundary between the charge neutral region and the pinched-off region; it is approximately this location that Shockley called the extrapolated pinch-off point (or EXPOP). Recognizing the existence of this discontinuity, he proposed that the correct voltage distribution would be adequately approximated by introducing a smooth graphical transition between the voltage distributions associated with these two regions of the structure. From Fig. 16, this type of approximation method would indeed produce a theoretical voltage distribution that is in essential agreement with the voltage distribution obtained from a rigorous two-dimensional solution of the problem.

Figure 17 illustrates the calculated voltage distribution within each structure considered in this mathematical investigation ($2W_g/W_o = 5.0$, 1.0 and 0.143), for $V_{sg} = 0$ and $V_{sd} = 5.0$ volts. As in previous illustrations, the solid lines represent contours of constant potential within this semiconductor device and the dashed lines represent the contour of 50% mobile carrier depletion that is due to the gate junction space-charge layer. From these calculated results, the constant potential contours in Fig. 17 are located in such a fashion as to clearly show that an increase in source-drain electric current, and an increase in source-drain channel width, are coincident with a decrease in gate junction width.

All the calculations shown in Fig. 17 are based upon a field-dependent carrier mobility within the source-drain channel. As a consequence, substantial carrier accumulation and depletion are present within this semiconductor structure. The potential distributions shown in Fig. 17 therefore result both from an ohmic type of voltage drop within charge neutral regions of this structure and from an electrostatic charge that is attributable to the regions of mobile carrier accumulation and depletion.

In a manner similar to Fig. 16, a comparison has been made between the calculated voltage distributions shown in Fig. 17 and the voltage distributions derived from Shockley's one-dimensional (gradual) approximation. The detailed results of this comparison are not presented here, although conclusions drawn from this comparison can be quickly summarized. In general, poor agreement is obtained between the rigorously calculated voltage distribution within these three devices and the voltage distribution calculated from these same devices but using Shockley's gradual approximation. This situation is attributable to two different mechanisms within the JFET: first, mobile carrier accumulation and depletion within the source-drain channel and, second, the narrow gate width relative to the source-drain channel width. In these narrow gate devices the rate of change of the gate junction space-charge layer width cannot be assumed to be gradual. It therefore appears unwise to apply the one-dimensional technique to such structures, since Shockley's approximation specifically excludes them by definition.

In Fig. 17 the same source-drain biasing voltage has been assumed for each field-effect transistor, yet substantial difference is observed in their relative gate junction space-charge layer widths. A small amount of this difference is attributable to the relative voltage distribution within each structure; from elementary considerations a wide gate device should contain a larger maximum source-gate voltage than a narrow gate device. However, this difference between the voltage distributions within the two devices is insufficient to explain the differences shown between their gate junction space-charge layer widths. If, instead, we consider the electric field distribution within the space-charge layer of the narrow gate device, the mechanism producing this difference of space-charge layer width

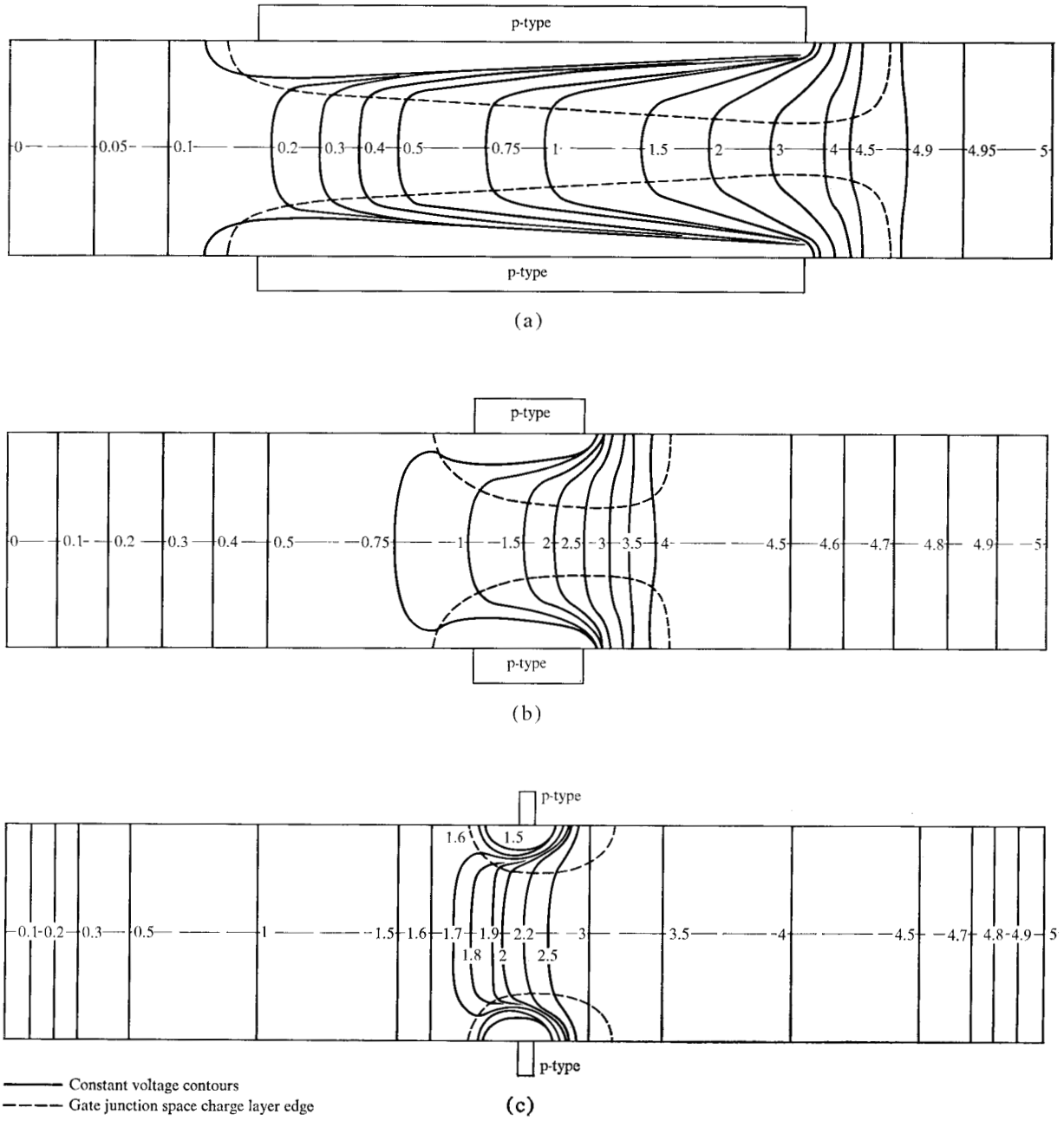


Figure 17 Calculated voltage distribution (field-dependent electron mobility; $V_{sg} = 0$; $V_{sd} = 5.0$V). (a) Wide gate: $2W_g/W_c = 5.0$; (b) narrow gate: $2W_g/W_c = 1.0$; (c) very narrow gate: $2W_g/W_c = 0.143$.

becomes evident. The contours of constant electric field exhibit substantial curvature within the space-charge layer of a narrow gate structure, and this curvature produces a decrease in space-charge layer width at a given source-gate voltage.

Electrical properties of a JFET

In his publication on the unipolar transistor, Shockley proposed that electric current saturation in a JFET is attributable to a pinch-off of the source-drain channel by the gate junction space-charge layers.[1] Shockley's analysis of this problem was subdivided into two parts: first, the source-drain electric current just prior to channel pinch-off and, second, after complete pinch-off by the gate junction space-charge layers. A consequence of this analytical technique is an uncertainty about the magnitude of source-drain electric current when the applied voltage is at (or near) pinch-off for the particular semiconductor structure

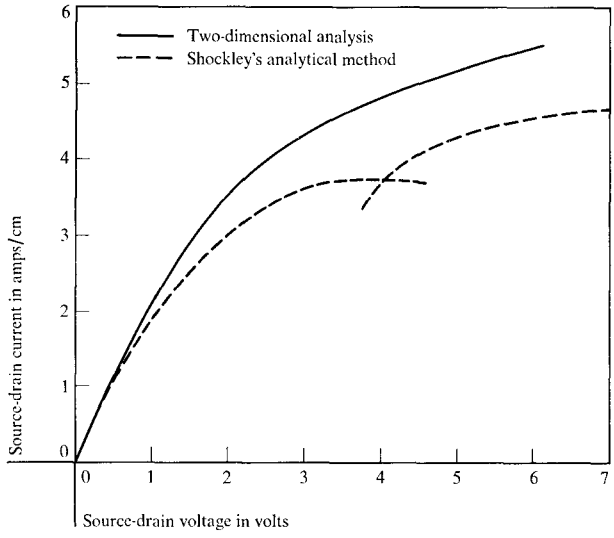


Figure 18 Calculated volt-ampere characteristics for the model illustrated in Fig. 1, for $2W_g/W_c = 5.0$ and $V_{sg} = 0$.

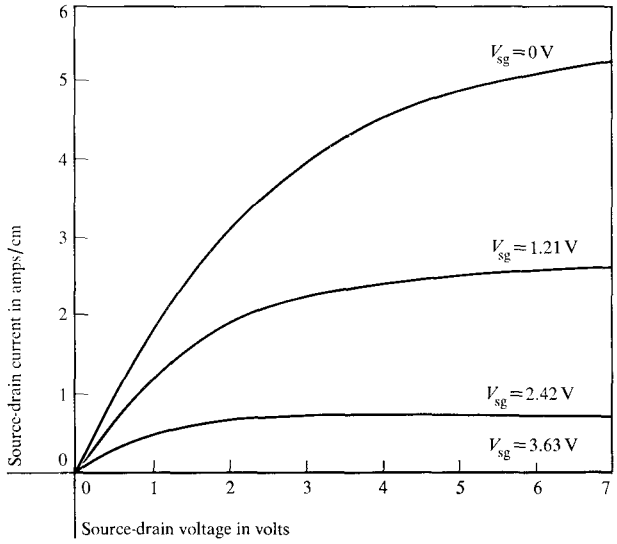


Figure 19 Electrical characteristics for the model of Fig. 1, calculated for constant drift mobility in the source-drain channel and $2W_g/W_c = 5.0$.

under consideration. In addition, Shockley limited his analysis to structures in which the longitudinal electric field is insufficient to produce velocity saturation of mobile charge carriers.

Figure 18 presents a comparison between the numerically calculated (two-dimensional) volt-ampere characteristics for this semiconductor device, and the volt-ampere characteristics calculated from Shockley's gradual approximation. Throughout both of these calculations the mobile carrier (electron) mobility is assumed to be constant (and thus independent of the electric field). It is again emphasized that the model used for this comparison contains a gate junction width ($2W_g/W_c = 5.0$) that may represent a limit for the applicability of Shockley's gradual approximation. Although very good agreement is obtained between these two analytical techniques, a substantially better agreement might be obtained for a JFET containing a wider gate junction, relative to its channel width.

From Fig. 18, Shockley's analytical method produces a discontinuous transition between the electric current just before pinch-off and the electric current just after pinch-off. To eliminate this difficulty one could introduce a smooth graphical transition between these two regions, and thereby obtain a volt-ampere characteristic that is in satisfactory agreement with the numerically calculated (two-dimensional) properties of this semiconductor device.

The electrical characteristics calculated by Shockley's approximation method exhibit a slightly harder current saturation than the electrical characteristics derived from a two-dimensional solution of this problem. Clearly, both of these mathematical methods yield a relatively soft current saturation, and this characteristic represents a principal source of disagreement between theory and experiment. To further emphasize this situation, Fig. 19 shows the calculated volt-ampere properties of this wide gate JFET,[6] retaining the assumption of a constant drift mobility for electrons within the source-drain channel.

As previously stated, Dacey and Ross[3] first proposed that a hard saturation of the source-drain electric current was attributable to velocity saturation of mobile carriers within the source-drain channel. Later, Grosvalet et al. provided further information[5] on this topic. They suggested that electric current saturation is not obtained when the two gate junction space-charge layers pinch off the source-drain channel but, instead, when carriers within the channel reach their limiting velocity. An experimental test of this hypothesis consisted of measuring the variation of source-drain electric current with temperature in a germanium field-effect device; below saturation this current varied as $T^{-\frac{3}{2}}$ while above saturation it varied as $T^{-\frac{1}{2}}$. The $T^{-\frac{1}{2}}$ type of dependence was considered consistent with previously published estimates for the electron mobility in n-type germanium.

A comparison between Figs. 19 and 20 shows the consequence of a field-dependent drift mobility on a given JFET. From Fig. 19, if the field-dependent drift mobility is neglected the calculated volt-ampere characteristics are in substantial agreement with Shockley's theory, although our calculations do indicate a smaller saturation resistance than Shockley's theory will predict. In contrast, Fig. 20 shows the presence of a hard saturation, which is entirely attributable to the field-dependent carrier mobility. From these calculations it is concluded that the field-dependent carrier mobility may or may not be an important mech-

anism in the operation of a JFET, depending upon the initial design of the structure. Furthermore, structures in which the mobile charge carriers attain their terminal velocity do indeed exhibit a much harder current saturation than structures in which the carrier mobility is constant. It has been suggested[24] that a detailed analysis of the source-drain conductance would provide substantial further insight into the theory of JFET operation; this investigation is now planned for the near future.

To conclude this analysis Fig. 21 shows a comparison among the volt-ampere characteristics of the three JFET structures considered here ($2W_g/W_c$ = 5.0, 1.0 and 0.143). For this comparison a field-dependent carrier mobility has been assumed within the source-drain channel of each model used in these calculations; it is presumed that the longitudinal electric field in such devices would be sufficient to produce the implied saturation of electron velocity.

Consistent with our previous discussions of current saturation in a narrow gate device, Fig. 21 demonstrates the presence of an increased electric current with a decrease in gate junction width. This situation is attributed to the substantial amount of carrier accumulation encountered within these narrow gate devices. As illustrated in Figs. 10 and 11, carrier accumulation produces an increase in width of the source-drain conduction channel. Thereby we obtain an increase in electric current, which is observed despite the presence of a well-defined saturation of the source-drain volt-ampere characteristics.

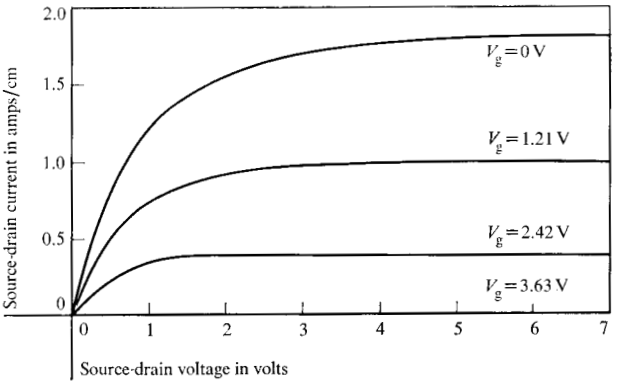
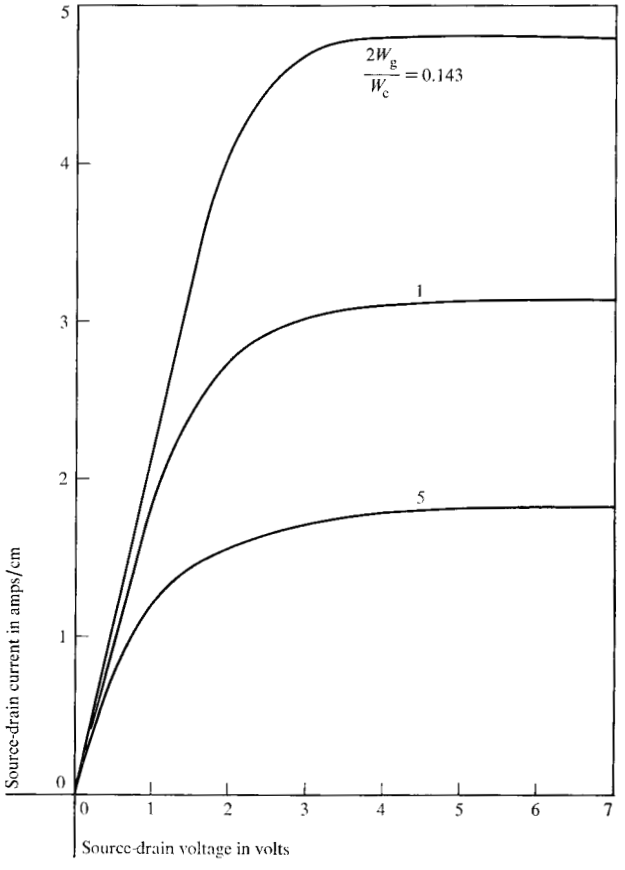


Figure 20 Electrical characteristics for the model of Fig. 1, calculated for field-dependent drift mobility in the source-drain channel and $2W_g/W_c$ = 5.0 (from Ref. 6).

Figure 21 Volt-ampere characteristics for the three mathematical models (wide, narrow and very narrow gate), calculated for field-dependent electron mobility and V_{sg} = 0.



Conclusions

In the absence of a limiting carrier velocity within the channel of a wide gate JFET, the mechanisms of device operation are found to be in substantial agreement with Shockley's theory for unipolar field-effect transistors.[1] For example, the pinch-off point does indeed move toward the source contact with an increase in source-drain voltage. Thereby a narrow channel of high resistance semiconductor material is formed between the two gate junctions; this channel supports that portion of the applied voltage that is in excess of the pinch-off voltage. Although Shockley gave little consideration to the process of carrier transport through this pinched-off region, our calculations substantiate the proposal of Grebene and Ghandhi[16] that throughout the pinched-off region any electric current is confined to a narrow conductive path near the center of the channel.

Wedlock[18] suggested that the Shockley theory would predict a much softer current saturation than is experimentally observed, because the pinch-off point is permitted to change location with a change of applied source-drain voltage. Our analysis indicates that the Shockley theory does indeed predict a soft current saturation. In fact, the models used in this investigation exhibit a softer theoretical current saturation than one would calculate from Shockley's theory. We conclude that the Shockley model for unipolar field-effect transistor operation should not be applied to devices for which it was not originally intended. In particular, it should not be applied to devices in which

the gate junction width is small (relative to the channel width) nor to devices in which the longitudinal electric field is sufficient to produce velocity-limited carrier transport within the source-drain channel.

Dacey and Ross[3] first proposed the consequences of a field-dependent carrier mobility within the channel of a JFET. Furthermore, they recognized that the hard saturation associated with velocity-limited carrier transport implies an immobile pinch-off point within this semiconductor structure, although no mechanism was suggested whereby this situation could be attained. A conclusion of our investigation is that a field-dependent carrier mobility, in conjunction with the requirement of electric current continuity, produces regions of carrier accumulation and depletion within the source-drain channel. These regions of accumulation and depletion form an electrostatic double-layer residing parallel to the longitudinal axis of symmetry, and located throughout that portion of the source-drain channel normally assumed to be pinched off by the gate junction space-charge layers. The electrostatic charge associated with this double-layer redistributes the source-drain channel potential and hence changes the gate junction space-charge layer width. It is concluded that this redistribution of source-drain channel voltage produces mechanisms of operation similar to those proposed by Dacey and Ross.

It is shown here that the double-layer induced into a source-drain channel is most pronounced in narrow gate structures. Our calculations imply a potential distribution, from this double-layer, that produces substantial contraction of the gate junction space-charge layers and therefore an increase in width of the conducting source-drain channel. As a consequence the gate junctions in a narrow gate device do not pinch off the source-drain channel; instead they constrict the cross section of a highly conductive path between the source and drain contacts. In this type of structure, current saturation is obtained at applied biasing voltages substantially below the pinch-off requirement imposed by Shockley's theory.

References

1. W. Shockley, "A Unipolar Field-Effect Transistor," *Proc. IRE* **40,** 1365 (1952).
2. W. Shockley, "Theory of p-n Junctions in Semiconductors and p-n Junction Transistors," *Bell System Tech. J.* **28,** 435 (1949).
3. G. C. Dacey and I. M. Ross, "The Field-Effect Transistor," *Bell System Tech. J.* **34,** 1149 (1955).
4. E. J. Ryder, "Mobility of Holes and Electrons in High Electric Fields," *Phys. Rev.* **90,** 766 (1953).
5. J. Grosvalet, C. Motsch and R. Tribes, "Physical Phenomenon Responsible for Saturation Current in Field Effect Devices," *Solid-State Electronics* **6,** 65 (1963).
6. D. P. Kennedy and R. R. O'Brien, "Electric Current Saturation in a Junction Field-Effect Transistor," *Solid-State Electronics* **12,** 829 (1969).
7. W. Van Roosbroeck, "Theory of the Flow of Electrons and Holes in Germanium and Other Semiconductors," *Bell System Tech. J.* **29,** 560 (1950).
8. W. Shockley, *Bell System Tech. J.* **30,** 990 (1951).
9. R. V. Southwell, *Relaxation Methods in Engineering Science,* Oxford University Press, London 1940.
10. R. V. Southwell, *Introduction to the Theory of Elasticity,* Oxford University Press, London 1941.
11. R. V. Southwell, *Relaxation Methods in Theoretical Physics,* Vol. I, Oxford University Press, London 1946.
12. R. V. Southwell, *Relaxation Methods in Theoretical Physics,* Vol. II, Oxford University Press, London 1956.
13. G. E. Forsythe and W. R. Wasow, *Finite Difference Methods for Partial Differential Equations,* John Wiley & Sons, Inc., New York 1960.
14. R. E. Bellman and R. E. Kalaba, *Quasilinearization and Nonlinear Boundary Value Problems,* American Elsevier Publishing Co., New York 1965.
15. K. E. Drangeid et al., "A Microwave Schottky-Barrier Field-Effect Transistor," *Int. Conf. on Electron Devices,* Washington, D. C., Oct. 23–25, 1968.
16. A. B. Grebene and S. K. Ghandhi, "The Behavior of Junction-Gate Field-Effect Transistors Beyond Pinch-Off," *1968 Int. Solid-State Circuit Conf. Digest, IEEE,* Philadelphia 1968.
17. C. Jund and J. Grosvalet, "Two-Dimensional Distribution of Carriers in a Semiconductor Space Charge Region with Current Flow," *Solid State Electronics* **9,** 13 (1966).
18. B. D. Wedlock, "Improved Theory for the Junction Field-Effect Transistor Volt-Ampere Characteristics Beyond Pinch-Off," M.I.T. Department of Electrical Engineering, *Industrial Liaison Program Reprint No. 961,* Nov. 5, 1968.
19. R. C. Prim and W. Shockley, "Joining Solutions at the Pinch-Off Point in Field-Effect Transistor," *IRE Trans. Electron Devices* **ED-4,** 1 (1953).
20. A. S. Grove, *Physics and Technology of Semiconductor Devices,* John Wiley & Sons, Inc., New York 1967.
21. L. S. Sevin, Jr., *Field-Effect Transistors,* McGraw-Hill Publishing Co. Inc., New York 1965.
22. D. P. Kennedy, "Mathematical Investigations of Semiconductor Devices, Final Report II," *AFCRL-66-358* (II), April 1, 1966–April 1, 1967, Air Force Cambridge Research Labs., Bedford, Mass.
23. J. R. Hauser, "Characteristics of Junction Field Effect Devices with Small Channel Length-to-width Ratios," *Solid State Electronics* **10,** 577 (1967).
24. C. T. Sah, private communication.

Received October 29, 1969