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Design and Fabrication of Subnanosecond Current Switch and Transistors*

Abstract: A junction-isolated integrated circuit in silicon is described, having a switching speed of 320 picoseconds in a package which by itself causes a 120 ps delay. The design of the transistor used in this circuit was obtained by simulating the transistor as a computerized, two-dimensional distributed model. The improvements required in the transistor technology were thus predetermined and the design was realized without a large number of iterations. It is shown that the primary parameters affecting the performance of the transistor are (a) mobile carrier storage in the emitter-base junction; (b) emitter crowding; (c) stretching of the base into the collector at high forward-current densities and (d) conductivity modulations in the active base region. The resulting transistors have a cut-off frequency of 7.15 GHz at $V_{CB} = 2$ V and $I_C = 20$ mA. The total number of impurity atoms forming the emitter and the base region are 5.57×10^9 and 5.7×10^5, respectively.

Introduction

Development of a 7.15-GHz transistor and fabrication of a 320-ps logic current switch in a package which by itself causes a 120-ps delay is part of a program for designing high-performance switching devices. An earlier paper by Langdon et al[1] describes the development of ASLT (Advanced Solid Logic Technology) transistor with 950-MHz cutoff frequency. The inadequacy of lumped-transistor models to design and predict the performance of high-frequency transistors was spotlighted by DeWitt[2] when he proposed a two-dimensional model. Subsequently Ghosh[3] advanced this concept significantly when, with an input of low-level measured parameters, horizontal geometry and other device characteristics, he accurately predicted the circuit performance. Ghosh[4] has further extended this computer model to predict transistor performance from its fabrication parameters. This model was variously tested and improved against the performance of the ASLT transistor.

This paper describes the application of transistor modelling to develop new high-speed transistors. Specifically, the design for two types of transistor, one with 0.1-mil wide and the other with 0.075-mil wide emitter, was modelled and studied. Subsequently these transistors were fabricated and their performances compared to predicted values. The final result of this effort was the development of a three-input current switch with 320 ps delay.

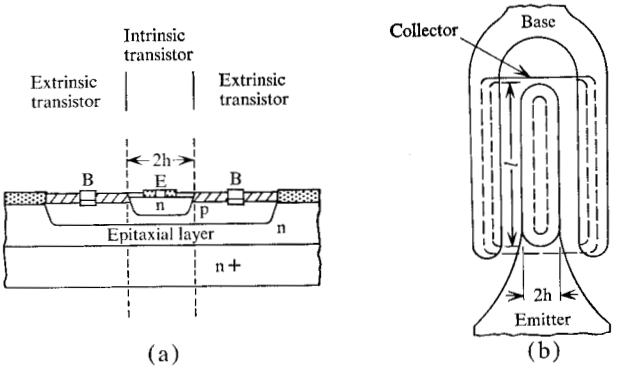

Figure 1 Schematic diagram of the three-strip transistor.

Theoretical development of the model, its comparison with ASLT transistor, 0.1-mil emitter transistor[5] and 0.075-mil transistor are described. The 0.075-mil transistor was then used to fabricate a 3-input logic current switch described in this paper.

Transistor model

Figure 1 shows the schematic of a 3-strip npn double-diffused epitaxial transistor. A two-dimensional distributed model for such a transistor in a common emitter configuration is shown in Fig. 2. The active transistor region is represented as a series of elementary transistor sections having no base resistance but interconnected by resistors which simulate the distributed base resistance. Starting with the

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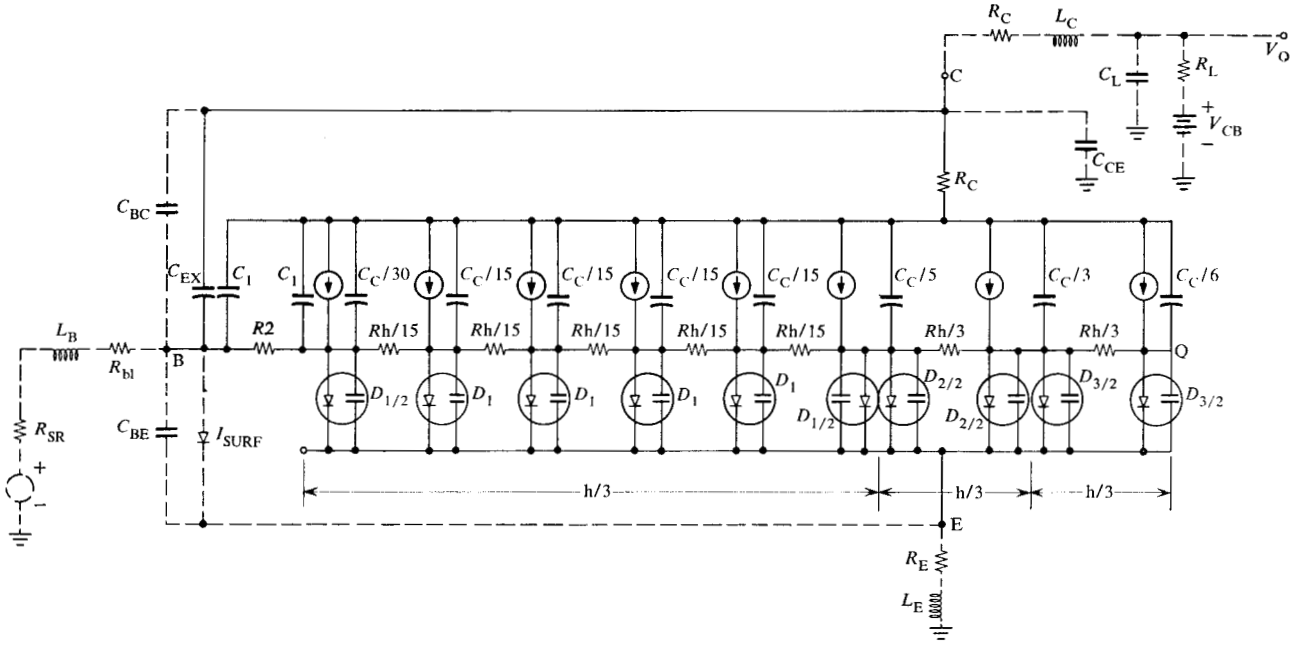


Figure 2 Distributed equivalent circuit model of a transistor in common emitter configuration.

input of the program, which consists of transistor geometry, semiconductor properties, and impurity profiles,[6] one calculates the small-signal equivalent circuit of each transistor section appropriate to the current and voltage levels in that section. Then a small interval of desired switching operation is assumed with this equivalent circuit. At the end of this time interval, new currents and voltages are computed and from these, in turn, new equivalent circuit parameters are calculated and used for the next time interval. The nonlinear features of the model are included in the calculation of the elements of the equivalent circuit.

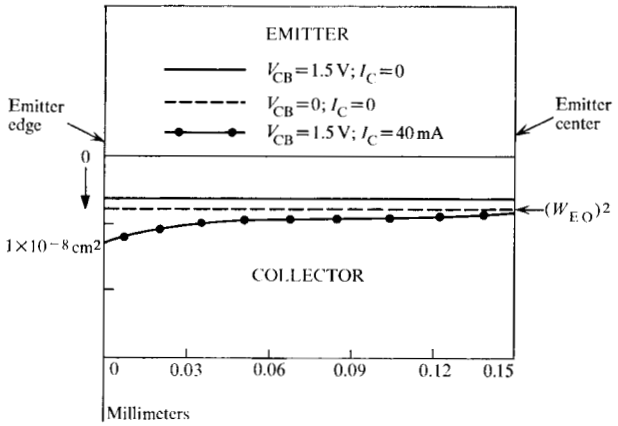
The phenomena included in the model are (1) nonuniform injection under the emitter; (2) Early[7] and Kirk[8] effects; (3) injection dependence of transistor parameters; (4) surface effects; (5) conductivity modulation in the base region; and (6) storage of mobile carriers in the emitter-base junction.

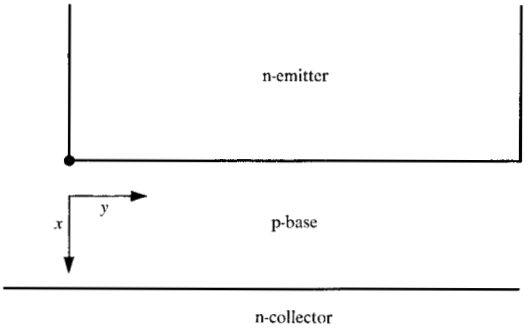
Nonuniform injection under the emitter is taken into account as a direct consequence of the two-dimensional distributed model. The Early effect and Kirk effect are well-known phenomena and their effect on ASLT transistor operation is shown in Fig. 3. Surface effects are simulated by $I_S = P_E S_E e^{(qV_{BE})/(nkt)}$, where S_E and n depend mainly on the characteristics of the Si-SiO_2 surface which were determined experimentally.

The formulation for conductivity modulation in the base region in the diagram below is obtained by assuming that there is no hole current flow from emitter to collector.

This gives $J_{p_x} = q\mu_p pE_x - qD_p(\partial p/\partial x) = 0$

Figure 3 Variation of the electrical base width for 0.3 mil-wide transistor with current flow.





or,

$$E_x = \frac{kT}{q}\,\frac{1}{p}\,\frac{\partial p}{\partial x}$$

One can now obtain the electric field in the y direction in the base region by using

$\nabla \times E = 0$ (Ref. 9)

For a two-dimensional analysis, in the base region this gives

$$\frac{\partial E_x}{\partial y} = \frac{\partial E_y}{\partial x},$$

giving

$$\frac{\partial E_y}{\partial x} = \frac{kT}{q}\,\frac{\partial}{\partial x}\left(\frac{1}{p}\,\frac{\partial p}{\partial x}\right)$$

which, on solving, gives

$$E_y = \frac{kT}{q}\,\frac{1}{p}\,\frac{\partial p}{\partial y} + f(y),$$

where $f(y)$ is a function of y alone.

Making use of the diode injection law,

$$n = \frac{n_i^2}{\bar{N}_A}\, e^{qV(y)/kT}$$

and the charge neutrality condition (in the base region) $p = n + \bar{N}_A$; one can then solve for $f(y)$ and obtain expression for I_{py} and I_{ny}:

$$i_{py} = 2l_E w_b q \mu_p \bar{N}_A \frac{(2m+1)(m+2)}{2(m+1)} E_{(0,y)}$$

and

$$i_{ny} = 2l_E w_b q \mu_n \bar{N}_A \left\{ \frac{1}{m} \ln (1+m) - \frac{m+2}{2(m+1)} \right\} E_{(0,y)}.$$

In the above expressions,

n_i = the intrinsic carrier concentration

$V(y)$ = the applied voltage across the junction depletion layer

$\bar{N}_A$ = the average acceptor concentration in the base region

n and p = the electron and hole concentrations, respectively

l_E = the emitter length

w_b = electrical base width

q = electronic charge

μ_p = hole mobility; μ_n electron mobility and

$m = \frac{n_{(0,y)}}{\bar{N}_A}$

($n_{(0,y)}$ is the injected carrier density at the emitter base junction.)

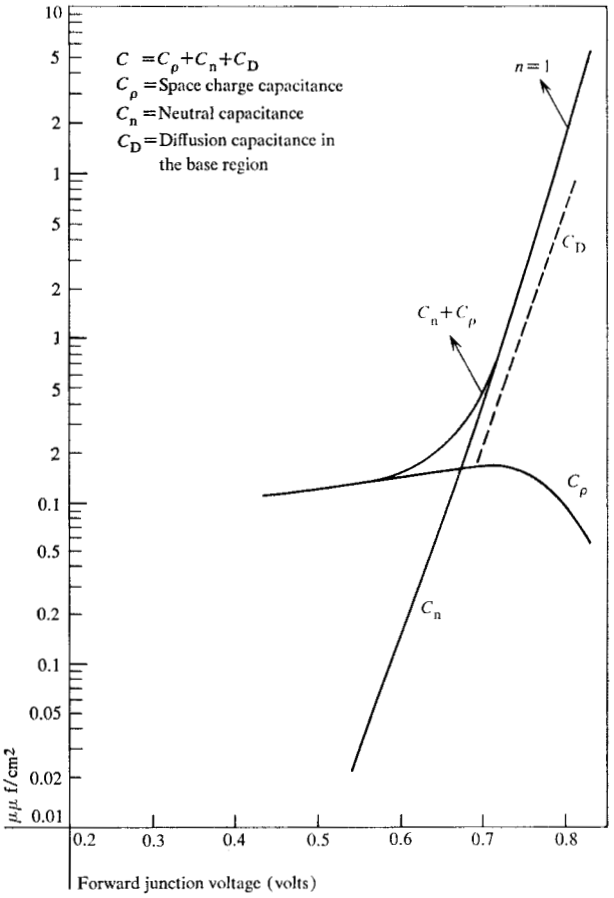


Figure 4 Forward-biased emitter junction capacitance.

The emitter crowding obtained from the above equations is significantly smaller than that calculated by Hauser[10] for a nonconductivity modulated case. Table 1 shows the comparison of current crowding for the two cases when the emitter-base junction is biased deep in the forward direction, and this indeed is the case for high-frequency transistors; a large number of mobile carriers, holes and electrons are present in the junction. The storage associated with these carriers was called "neutral capacitance" by Shockley.[11] This capacitance begins to play a significant role in the high-frequency transistors. Morgan and Smits[12] have solved this junction characteristic numerically for a linearly graded junction. For the purposes of this analysis the *E-B* junction has been approximated to a linearly graded junction. The components of the capacitance associated with an *E-B* junction of a transistor are (1) the space-charge capacitance C_P (2) neutral capacitance C_n and (3) diffusion capacitance C_d of the injected carriers in the base region. The behavior of these capacitances with applied forward bias is shown in Fig. 4 for the ASLT transistor with an impurity gradient of $3.24 \times 10^{22}/\text{cm}^4$.

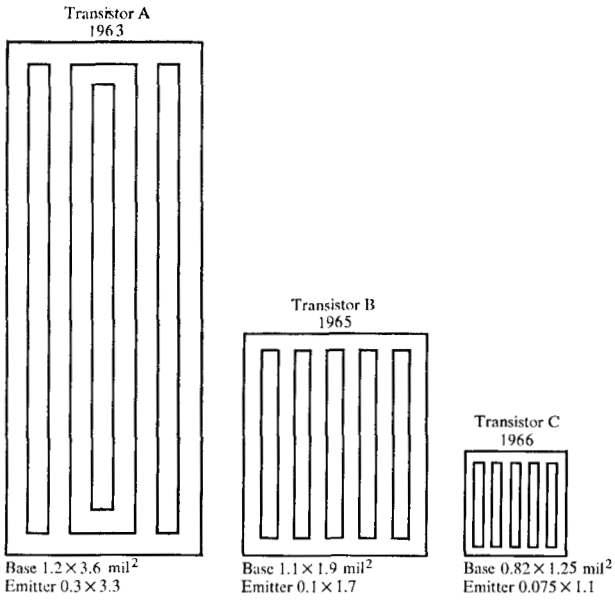


Figure 5 Horizontal geometry of the transistors A, B and C (A is an ASLT transistor).

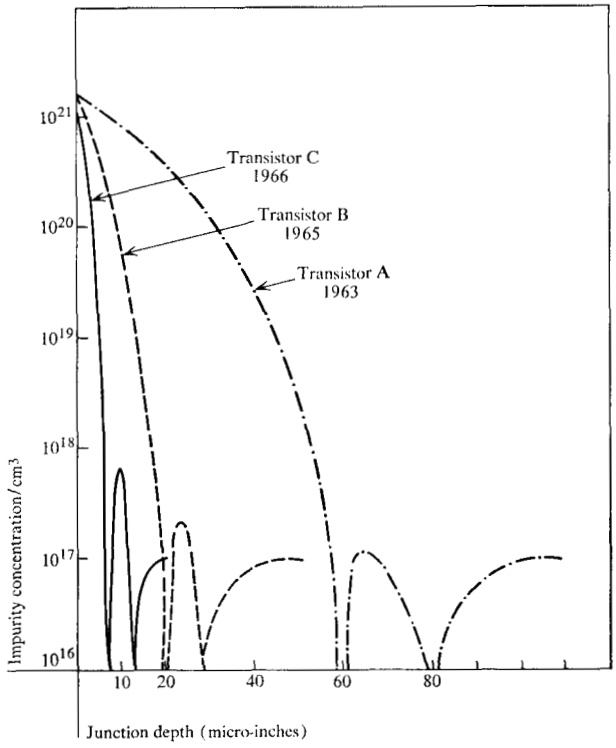


Figure 6 Impurity profiles for the transistors A, B, and C.

Table 1 Comparison of calculated emitter crowding with and without conductivity modulation for 0.3-mil wide emitter transistor.

I_E (*ma*)	$J_{(C)}$ *Current density at the emitter center* / $J_{(E)}$ *Current density at the emitter edge*	
	Nonconductivity modulation	*Present computations*
11.2	0.3	0.375
19.1	0.2	0.300
29.6	0.07	0.250
42.2	0.04	0.220
56.0	0.01	0.216

Table 2 Comparison of the design parameters of three transistors.

	Transistor A 1963	*Transistor B 1965*	*Transistor C 1966*
Emitter width, mils	0.3	0.1	0.075
Emitter area, mil²	0.99	0.34	0.157
Collector area, mil²	4.32	2.1	0.96
Collector junction depth, Å	20,000	7000	3200 Å
Emitter junction depth, Å	15,000	5000	2000 Å
Emitter-base cap, pF	1.16	0.73	0.29
Collector-base cap, pF	1.4	0.8	0.58
Cutoff frequency at V_{CB} = 2 volts, GHz	0.95	2.4	7.15

• *Results of the design study*

By varying the fabrication parameters, the performance of several transistor structures was studied. This type of analysis significantly reduced the actual fabrication iterations and spotlighted the areas of technology where the effort must be concentrated to improve the performance of the transistors. Salient features that resulted from this study were: (1) The gradient of impurity at the emitter-base junction should be increased to reduce neutral capacitance (2) The collector-base gradient should also be increased to reduce stretching of the base into the collector even at high current densities. (3) Both (1) and (2), by allowing larger current densities to be handled, permit a significant reduction in the junction area. (4) Emitter should be made narrower. Application of these conclusions meant developing shallow, high-surface-concentration emitter and base diffusions and improving photolithographic technique to realize 0.1 -mil and 0.075-mil-wide emitters.

Description of the high-frequency transistors

Figures 5 and 6 show three transistor geometries discussed in this paper and their impurity profiles.

Table 2 compares the design parameters of these three transistors. The horizontal geometrics have progressively become smaller and diffusion depths shallower. Thus in

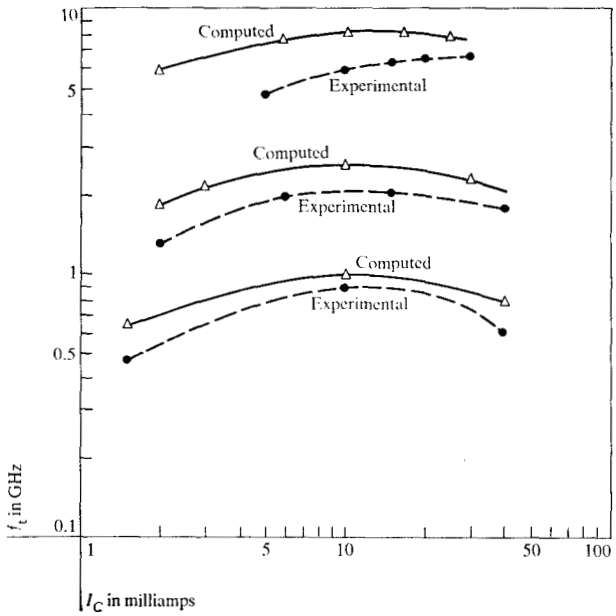
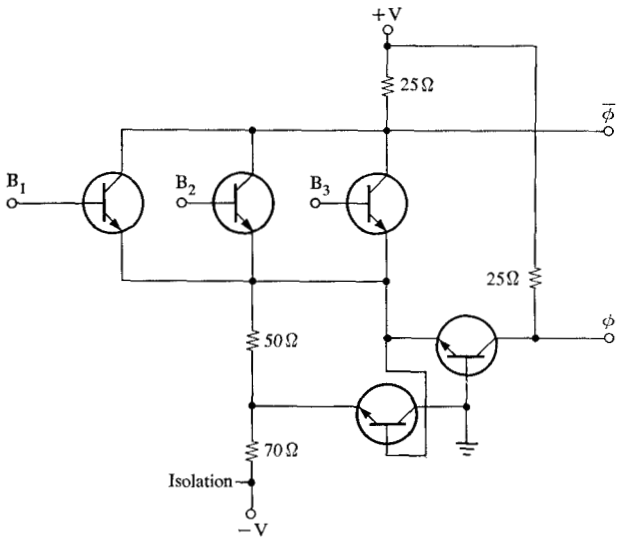


Figure 7 Comparison of computed and measured cut-off frequencies for transistors A, B and C.

	A lower curve	B central curve	C upper curve
emitter width, mils	0.3	0.1	0.075
x_{je}, Å	20,000	7,000	3,200

Figure 8 Schematic of the three-input current switch circuit.



spite of the reduction in emitter areas from 0.99 mil² for transistor A to 0.157 mil² for transistor C, both transistors can handle the same amount of current because the shallower diffusions in transistor C have increased the current-handling capacity of this transistor.

In all three transistors the impurity doping per unit area in the base region has been kept constant. Nevertheless, the progressive decrease in the transistor areas has resulted in a rather small number of impurity atoms in the base and emitter regions of the transistor C. The collector and emitter junctions of this transistor are 3200 Å and 2000 Å deep. The number of impurity atoms forming the electrical base region is 5.7×10^5. The electrical base width contains 220 atomic layers of silicon.

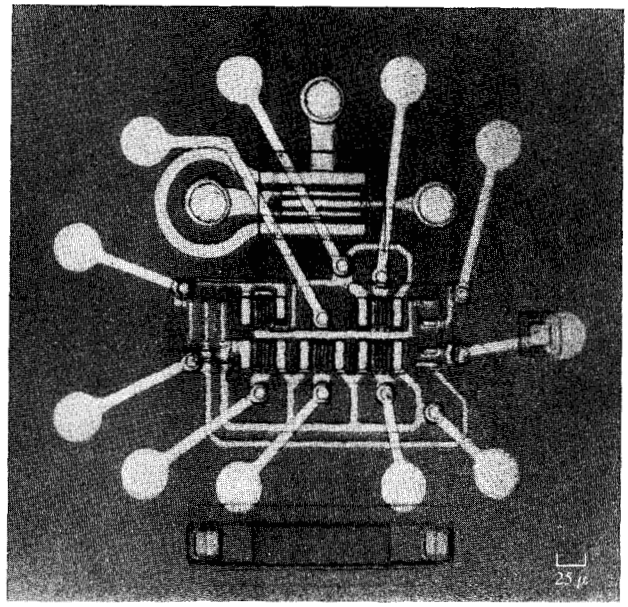


Figure 9 Photomicrograph of the double-level monolithic three-input current switch.

Figure 7 compares the computed and measured cutoff frequencies of these transistors. Further computation shows that with an emitter width of 0.04 mils and a collector junction depth of 1600 Å, it would be possible to obtain a transistor structure in silicon with a cutoff frequency about of 13 GHz. Figure 7 indicates increasing divergence in the measured and computed performance as the transistor performance improves. This is attributed to the approximations used in the model described as well as difficulties encountered in the measurement of the cutoff frequency.

Fabrication of 320-ps logic current switch

The transistor C with f_t of 7.15 GHz was used in the fabrication of a 3-input monolithic current switch. The circuit had junction isolation and diffused resistors were used. The schematic of the circuit is shown in Fig. 8. The fabrication of this circuit required two levels of metallization to interconnect the transistors and resistors to form a 3-input current switch. A photomicrograph of the completed circuit is shown in Fig. 9.

The circuit was then thermocompression-bonded onto a TO-5 header. The switching performance of this circuit was determined using a Tektronix sampling oscilloscope. The

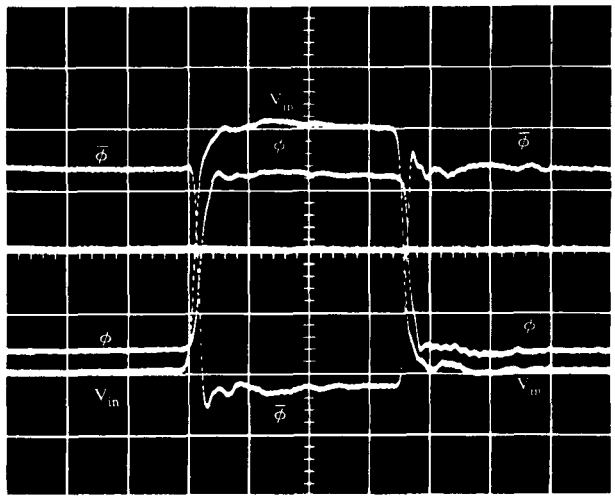


Figure 10 Oscillogram of input and output waveforms.

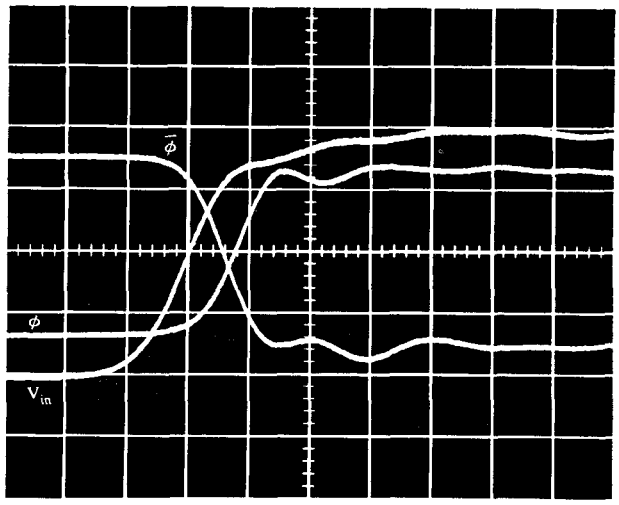


Figure 11 Oscillogram of turn-on delay.

switching waveforms thus obtained are shown in Fig. 10. Expanded views of in-phase and out-of-phase switching wave forms for turn-on and turn-off are shown in Figs. 11 and 12.

The switching delays thus obtained are listed below:

	In-phase switching	*Out-of-phase switching*
Turn-on (ps)	275	380
Turn-off (ps)	285	340

The average of these delays is 320 picoseconds. This number includes the delays contributed by the package. The delay in the package itself between the two nearest and two farthest pins is shown in Fig. 13. The average of these two delays is 120 ps.

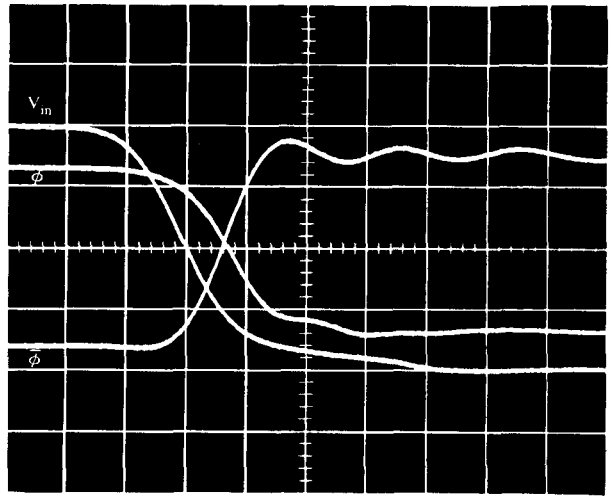


Figure 12 Oscillogram of turn-off delay.

Conclusions

A two-dimensional distributed model of a transistor which has been simulated on a computer has been verified by fabrication. These computations have been used as guidelines in the design of a 7.15-GHz cutoff transistor. It is also shown that, for still higher performance transistors, improvements in the model will be needed.

Additionally a 3-input monolithic current switch with 7.15-GHz transistors and diffused resistors was fabricated using junction isolation. The average switching delay in this circuit is 320 ps including the delay in the package.

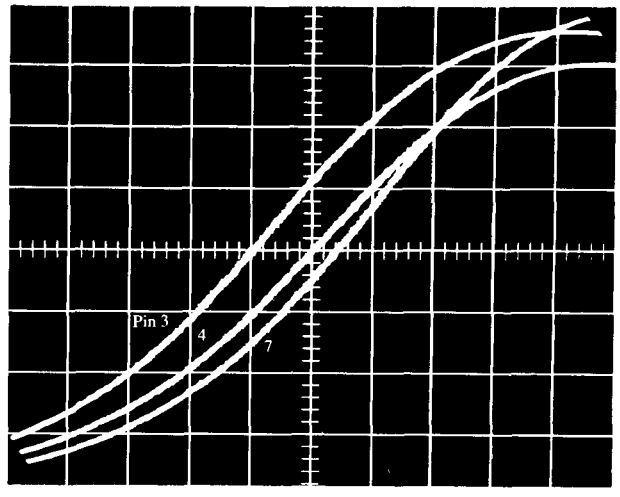


Figure 13 Oscillogram of 12-pin TO-5 package delay.

Acknowledgments

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