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A Balanced Capacitor Read-Only Storage

Abstract: The design of a control storage system of 90 nsec access time and 200 nsec cycle time with permanently stored microinstructions is described. The storage medium used is the capacitive coupling between two groups of orthogonal conductors forming an information plane and a sense plane. There are 2816 words of 100 bits each, divided over two gates. The selection of an address line in the information plane is achieved through a transistor selection matrix. The output signal is sensed differentially at the mid-point of the sense line, which is matched at both ends. The sense amplifier output plus a "strobe" pulse set a latch for a portion of the cycle time and this provides the necessary inputs to the central processing unit. The major contributions to noise, such as sneak-path noise and select noise, are discussed and evaluated. The timing of the different pulses necessary to drive the array and the resulting outputs are explained and the marginal effects of time and amplitude variations are considered. Information can be changed off-line by replacing bit planes. Transcription of information in the bit planes is fully automated and can be speedily accomplished.

Introduction

The balanced capacitor read-only storage (BCROS), embodying one of three ROS technologies[1,2] currently employed in IBM System/360, is a basic element[3] in the operation of System/360 Models 50, 65, and 67. It controls the central processing unit through the use of permanently stored microprogram instructions. It is also utilized to provide emulation features enabling the use of customer programs from other systems, and may be used to provide storage for table look-up data such as character generation for graphic and display units. In addition, the BCROS contains small diagnostic, self-checking programs permitting faster "debug" of the processor and ROS. Importantly, the logic design and implementation of System/360 models incorporating read-only storage units have been greatly simplified through the control automation system, which is capable of functionally debugging a system on an IBM 7090 computer whose input consists only of a general machine description and the available control microprograms. Such simulation of proposed system operation greatly reduces engineering design and debugging time on all these models. Although the stored information pattern remains unchanged during any number of machine cycles, it can be replaced off-line when necessary. As the name implies, this type of read-only storage utilizes as a unit cell the capacitances formed at the intersections of two groups of suitably shaped orthogonal conductors,[4] one in an information plane (bit plane) and the other in a sense plane.

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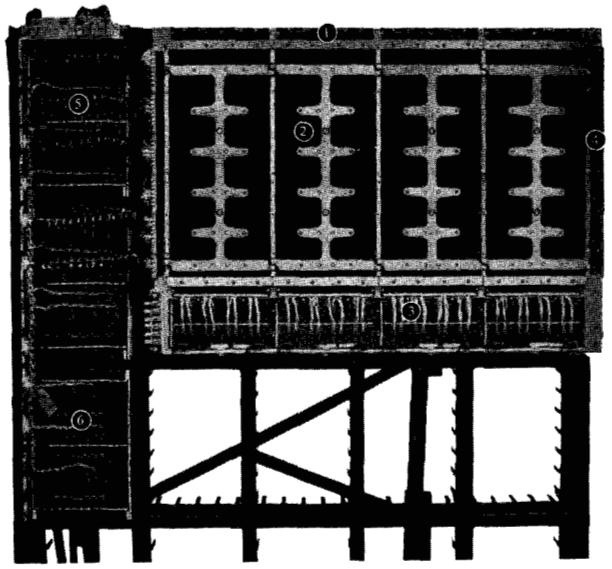
Array structure

The balanced capacitor read-only storage is a word-organized storage system with a 200-nsec cycle time and a 90-nsec access time. Its total capacity is 281,600 bits, made up of 2816 words of 100-bit length. Each address line contains 200 bits, which are alternately parts of two 100-bit words designated upper and lower. The number of address lines is therefore 1408, and these are divided over two gates, a fixed gate and a "swinging" gate. Each gate has 704 address lines whose individual selection is achieved by a 22 $\times$ 32 transistor matrix. Below each array gate are four laminated printed circuit boards which contain the selection matrix, and word drive circuits for driving the 704 address lines (Fig. 1.) To the left of the array are three boards mounted vertically. These contain the sense amplifiers, latches, timing circuits, and power distribution circuits.



1. Address lines and terminating resistances
2. Bit planes
3. Drive circuits
4. Sense lines and terminating resistances
5. Sense amplifiers
6. Latches

Figure 1 General view of BCROS.

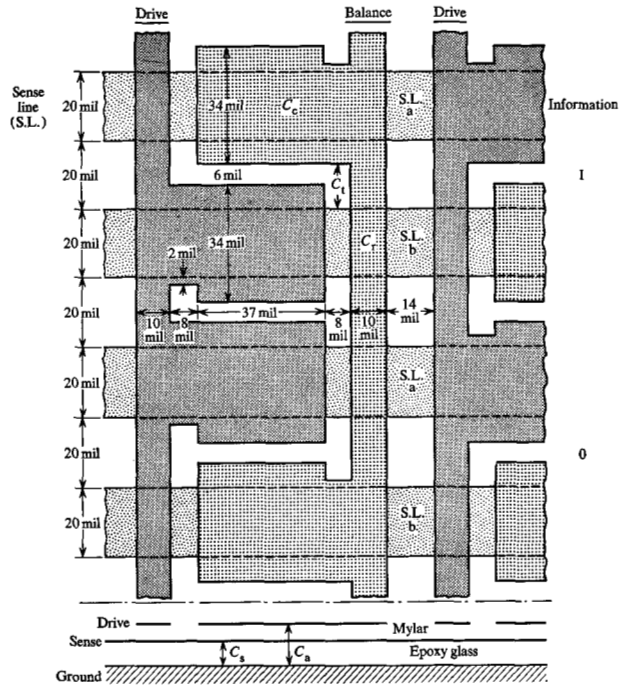


Figure 2 "Flag" configuration showing two bits.

The selection of one particular address line causes a voltage swing along that line, which is capacitively coupled to the sense lines. To ensure that the characteristic impedances and delays along the address and sense lines are independent of the information patterns used, a balanced scheme is introduced. The address line has associated with it a balance line,[5] which contains a complementary pattern that couples it capacitively to the sense lines. In other words, each bit is made up of the capacitive intersection of an address line and a balance line with a pair of sense lines (Fig. 2). Detection of stored data is accomplished by sensing differentially at the midpoint of the terminated sense lines. The differential sense amplifier between the pair of sense lines will give a positive output for one polarity of bit stored and a negative output for the opposite bit stored. The differential signal is amplified, "strobed," and stored in a latch. By appropriate logical gating only one word, either upper or lower, is stored in the latches during one cycle. Since the sense lines are in pairs, extraneous noise will be common mode at the amplifier input.

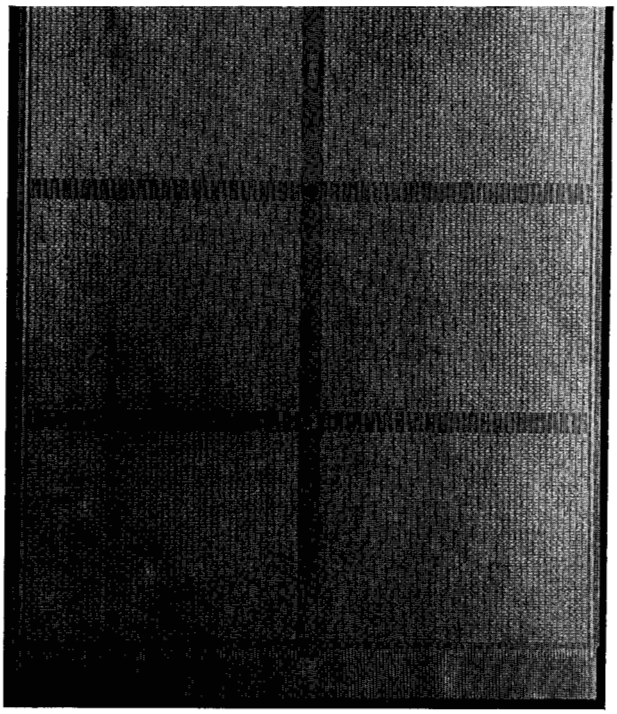
In each gate the information plane is subdivided into eight bit planes—four on each side. Part of a bit plane is shown in Fig. 3a. Figure 3b shows the two gates containing 16 bit planes. Each gate has four planes on each face. Each bit plane is copper-clad epoxy glass laminate, approximately 8 in. × 18 in., with the bit pattern etched in accordance with a given configuration. The capacitive storage is achieved by means of a 1-mil Mylar dielectric, which is "sandwiched" between the bit plane and the sense plane and maintained in that position by means of a pressure plate system. The address lines are terminated in 100-ohm resistances through "flat on flat" pressure connectors at one end of the bit plane and are connected to the array drivers by a similar arrangement at the other end. To obtain optimum differential capacitance, alignment between the bit planes and the sense plane must be accurate to within ±4 mils. The alignment mechanism must also permit easy replacement of the bit planes when the need arises to alter the microinstructions. The planes are positioned by two guide pins mounted on the sense plane and two corresponding precision-cut holes in the epoxy-copper bit plane.

Information storage

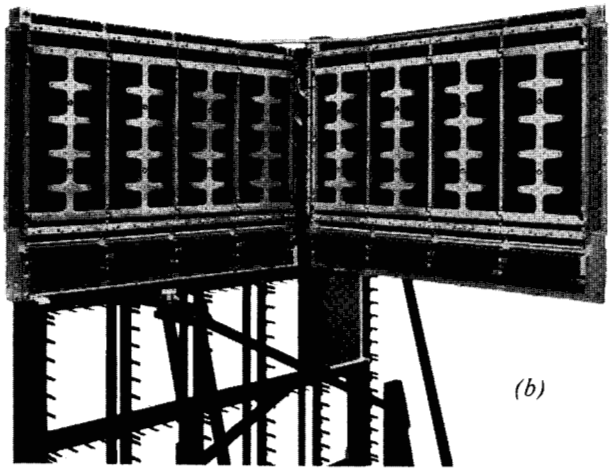
- *Bit configuration*

Information is stored by capacitive coupling between orthogonal sets of address and sense lines. The configuration for a two-bit position is shown in Fig. 2. Each pair of lines is connected to a sense amplifier that amplifies the difference mode current and rejects the common mode current.

At each bit position, the address line is connected to a "flag," so called because of its shape. This flag may be positioned over either sense line of the pair. The position of the flag is dependent upon the desired stored information. If the flag is positioned above sense line *a* and the



(a)



(b)

Figure 3 (a) Bit plane; (b) fixed and swinging gates.

address line is pulsed with a voltage ramp, then the voltage on sense line *a* will swing negative with respect to the voltage on sense line *b*. If the flag is reversed, so will be the polarity of the signal.

• *Capacitance calculations*

The pertinent capacitances are those between the address and the sense lines, between the address line and ground, and between the sense lines and ground. They are shown in Fig. 2 and defined below.

C_c Capacitance between the drive flag and the sense line underneath.

C_r Capacitance between the address line and the sense line underneath.

C_t Cross-capacitance between the drive flag and the adjacent sense line.

C_d Net differential capacitance $= C_c - C_r - C_t$.

C_s Sense line capacitance to ground (per bit).

C_a Address or balance line capacitance to ground (per bit).

C_S Total sense line capacitance to ground per bit $= C_c + C_r + C_t + C_s$.

C_A Total address line capacitance to ground per bit $= C_c + C_r + C_t + C_a$.

For the dimensions shown in Fig. 2 and dielectric constants $\epsilon_r = 3$ for Mylar and 4.2 for epoxy glass, both at 1 MHz, the calculated parameters are

$C_c = 0.79$ pF (0.64 pF parallel-plate, 0.15 pF fringing);
$C_r = 0.18$ pF (0.12 pF parallel-plate, 0.06 pF fringing);
$C_t = 0.06$ pF (mostly fringing);
$C_d = C_c - C_r - C_t = 0.55$ pF;
$C_s = 0.29$ pF/bit;
$C_a = 0.17$ pF/bit;
$C_S = 1.33$ pF/bit; and
$C_A = 1.21$ pF/bit.

The values calculated above represent the design objectives. In practice, the tolerances in the array system would alter these values appreciably. The tolerances are especially critical when they influence those capacitances that directly affect the sense signal, namely those contributing to C_d.

• *Tolerance considerations*

Several factors can alter the capacitance values in the array. These will be discussed briefly below.

Etching

The etching tolerance affects the address and sense line widths. The limits are $+0$ to -3 mils for sense lines of 20-mil nominal width and $+1$ to -2 for the drive lines of 10-mil nominal width on one-ounce copper.

Separation

The thickness of the Mylar dielectric between the address line and sense lines directly affects the parallel-plate capacitance. The limits on height are ± 0.1 mil for a nominal 1-mil thickness. The tolerance on the dielectric constant is $3 \pm 10\%$ at 1 MHz.

Registration

The mechanical alignment between the bit plane and the sense plane is not perfect. The component of malregistration along the address line also affects the array capacitance; the limit is 4 mils.

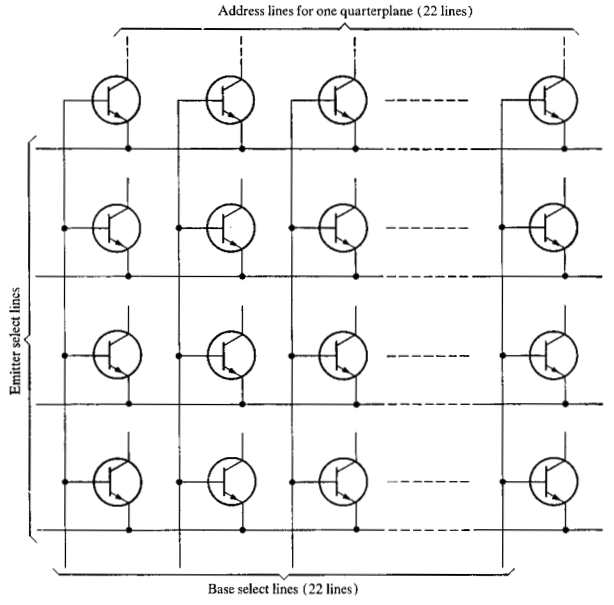


Figure 4 A portion of the selection matrix. The four rows shown select the address lines for one bit plane. Sixty additional rows are required for the 16-plane array.

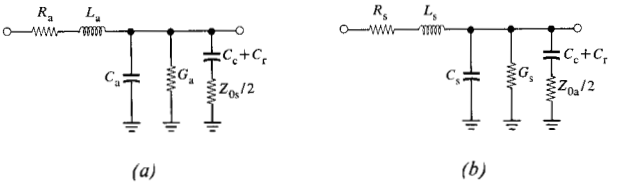


Figure 5 Differential elements of (a) address line and (b) sense line.

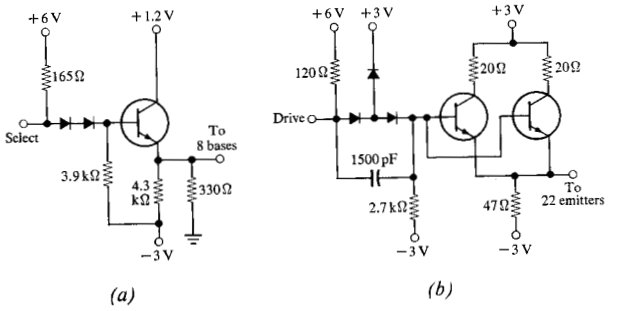


Figure 6 (a) Base driver; (b) emitter driver.

The influence of the above factors on the nominal C_d capacitance value is summarized below:

- Percentage change in C_d due to etching, $\pm 27\%$;
- percentage change in C_d due to variation in the thickness of Mylar, Δh_1, $\pm 6.6\%$;
- percentage change in C_d due to variation in the dielectric constant of Mylar, $\Delta \epsilon_r$, $\pm 6.7\%$;
- percentage change in C_d due to malregistration, 1.6%.

If all these factors add up adversely to reduce the capacitance, the worst case C_d is $58\% \times 54$ pF, or 0.31 pF. The average measured C_d was found to be 0.35 pF.

- *Fabrication of bit planes*

An automatic process for the scribing of the desired information patterns on the bit planes has been developed through the use of the control automation system (CAS). Starting with data flow charts, a microprogrammer prepares the logical organization, which is stored on tape. Using the stored information and three glass artwork masters (for the ladder patterns, all zeros and all ones), a computer program determines the required information pattern and final merged master glass artwork is prepared. After etching the bit plane using one-ounce copper laminate with epoxy glass,[6] the one-mil Mylar is permanently bonded along the edges in a special "clean" room. Each bit plane is electrically tested under simulated operating conditions and its information contents are checked with the desired patterns.

The bit planes must be held in intimate contact with the sense plane to ensure that the separation is about one mil. A pressure system has been devised that can be mechanically set to provide almost uniform pressure on the back of the bit plane.

Drive system

The drive system is oriented about two 22×32 transistor selection matrices, each of which drives one gate. The bit plane is divided into four quarter planes of 22 lines each. Each of the address lines goes to the collector of one of the selection matrix (array driver) transistors. The emitters of the 22 array drivers associated with a particular quarter plane are connected to a common-emitter select line. These emitters are selected simultaneously but only one of the bases in the group will be conditioned at a time. This uniquely selects one address line. There are 16 such planes, or 64 quarter planes, in the total array (see Fig. 4).

An address line consists of a string of 200 bits connected serially; it is terminated at one end with 100 ohms to +6 volts. The address line is essentially capacitive. A differential element is shown in Fig. 5a. Average practical values for this element are

$R_a = 0.0039\Omega$,
$L_a = 1.2$ nH,
$G_a = 0.0236 \times 10^{-4}$ mhos,
$C_a = 0.17$ pF,
$C_r = 0.15$ pF,

C_c = 0.50 pF,
Z_{0a} = 37Ω, and
t_a = 0.0320 nsec.

There are 200 such sections per address line, which has a one-way delay of 6.0 nsec.

Two sets of drives are used to drive the selection matrix, as shown in Fig. 6. The select bus base drive (SBBD) is an emitter follower driving a positive 1.5-volt pulse to the bases of 8 matrix transistors (array drivers). Eight of the SBBD circuits are driven in parallel. (The number of array drivers driven by the SBBD is limited by the circuit loading.) The positive level of the selected bases serves as a clamp for the select bus emitter driver (SBED). The SBED is an emitter follower driving a 1.5-volt negative pulse to the emitters of 22 drivers. Since the emitter driver depends on the selected base to provide its down level, timing restriction was adopted and the base drive must be fully selected for 5 nsec before the emitter drive is turned on. Unless the timing is set this way, there exists the possibility of partially turning on as many as 22 array drivers.

The requirements on the drive system were to provide a dV/dt of 6 volts in 25 nsec since the maximum value of dV/dt determines the signal peak. This was accomplished by using the SBED as a current switch in conjunction with the selected array driver. When the array driver is turned off, the recovery is determined by an RC time constant, where R is the terminating resistance and C is the capacitance of the address line.

Sense system

To determine the physical length of the sense lines and the location of the sense amplifier with respect to the sense line, it was necessary to consider a number of approaches. A paramount consideration was meeting the design objective for the 90-nsec access time as given earlier.

The first approach was to terminate the lines at one end and sense at the other. The sense planes on either side of a gate were connected by feedthrough pins. This approach was unacceptable because it introduced increased sense line skew and increased access time.

The second approach was to treat each pair of lines on either side of the sense plane independently. Although this gave much better control of delay and skew, the number of sense amplifiers was doubled and packaging within the allotted space became impossible.

The third approach was to use a folded array with midline sensing. This method was adopted since it met prescribed criteria for access time and packaging, namely, the 90-nsec access time and the allowable space equivalent to the size of 11 SLT[7] boards per gate. The lines are physically 36 inches long and 20 mils wide. The fold is accomplished by using 2 inches of twisted-pair cable. The node at this point also feeds the sense amplifiers, as shown in Fig. 7.

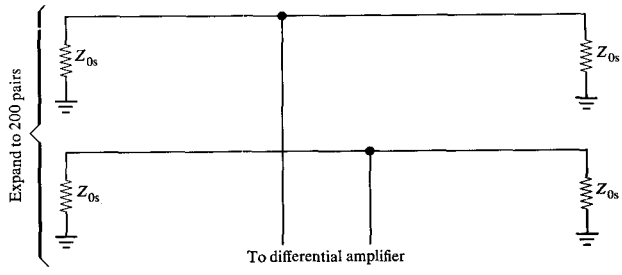


Figure 7 A pair of sense lines with their terminating resistances.

Since the output signal from the array contains both common mode and difference mode signals the sense lines will be treated in pairs. Both ends of the sense lines are terminated in the characteristic impedance to ensure that there are no reflections of pulses. The signal energy reflected by an open circuit termination would be of no value as the access time requirements would not allow the reflections to be used at the amplifier. Although this reduces the amount of energy transferred to the sense amplifier, it has the desirable effect of reducing the noise level on the sense line by initially damping out the common mode noise.

The line has been characterized on a per-bit basis, and a typical differential element is shown in Fig. 5b. There are 704 such elements per line and the average per-element values are

R_s = 0.0021Ω,
L_s = 0.94 nH,
G_s = 0.0236 × 10^{-4} mhos,
C_s = 0.29 pF,
C_r = 0.15 pF,
C_c = 0.50 pF,
t_s = 0.031 nsec, and
Z_{0s} = 33 ohms.

The one-way delay is 22.0 nsec. However, since the line is center-tapped, energy is transferred to the sense amplifier after a worst-case delay of 11.0 nsec.

Differential stage of sense amplifier

Since the signal from the array can be interpreted in terms of a common mode and a difference mode, the technique of differential sensing was employed. As a first approach, a two-transistor differential amplifier was considered. This was rejected mainly because of the limitations of the physical package. (The requirements were to package 10 preamplifiers and 5 main amplifiers on a standard 24-pack SLT card.)

The second approach, which was a single-transistor differential amplifier,[8] was adopted. The circuit is shown in Fig. 8. Differential action is accomplished by applying

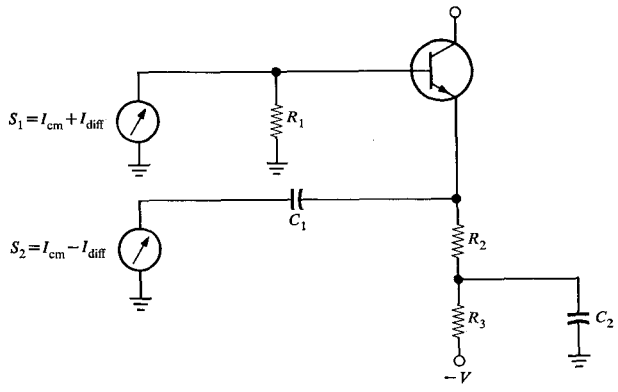


Figure 8 Differential stage of sense amplifier.

signals S_1 and S_2 simultaneously. C_2 is a bypass capacitor to reference R_2 to ground; R_3 is a small resistor used as a noise suppression filter. The common mode impedance is essentially $R_1/2$.

For a calculation of the differential input impedance, the following assumptions will be made:

Each signal (S_1 or S_2) may be broken into two components: a common mode current I_{cm} applied to both terminals simultaneously and a difference mode current I_{diff} as shown in Fig. 9.

Since the common mode impedance has already been stated as $R_1/2$, only the difference mode current will be used. By the use of superposition, loop equations may be written and solved for Z_{in}, which equals V_{eb}/I_{diff}. This yields the following solution.

$$Z_{in} = \frac{2(r_e + rB/h_{fe})}{1 + 1/h_{fe}} = 2\alpha(r_e + rB/h_{fe}) .$$

Since $\alpha \approx 1$, we may say that $Z_{in} \approx 2(r_e + r_B/h_{fe})$, which happens to be twice the grounded-base input impedance.

In the memory it was desired to make the input impedance equal to the characteristic impedance of the sense line for maximum power transfer. The predominant term of Z_{in} is $2r_e$. By proper adjustment of the emitter current the desired impedance was obtained.

The single-transistor differential amplifier has excellent common mode rejection, provided each of the lines has identical impedance with respect to ground. Capacitors C_1 and C_2 were chosen such that their impedances throughout the dynamic range of the signal content were small compared to the resistor R_1.

The major factor that has an adverse effect on the common mode rejection is the collector-base capacitance, C_{OB}, of the transistor. (For the particular device used, C_{OB} is about 5 pF.) This does have the effect of converting common mode signals at high frequency to difference mode. However, a compensation capacitance, which is K times the value of C_{OB}, may be added if better rejection is desired. By applying a common mode voltage source and solving a set of equations for the collector current, a value of K may be found. This has been calculated to be about 3.

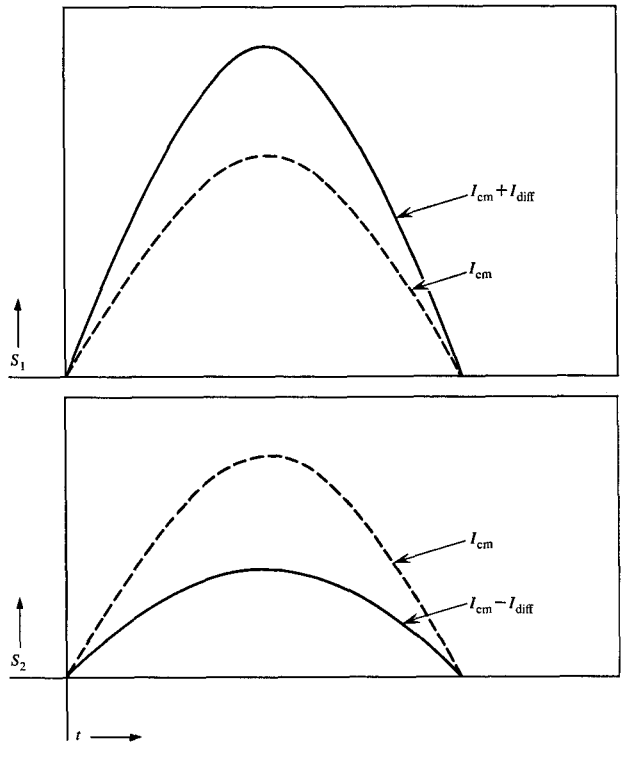
The main amplifier

Following the differential amplifier is a multistage single-ended amplifier, whose output is coupled into a circuit that discriminates positive signals (ones) from negative signals (zeros) during the period of the "strobe" gate, and latches the output for use until reset just prior to the time the next word address is selected.

The differential amplifier output presents a signal source which can be closely represented by a current source shunted by a transistor output capacitance of approximately 4 pF. Due to the very short time constants involved in the generation on the input signal, its time-integral returns to zero at the end of each cycle. The amplifier is therefore ac-coupled as required and, provided the nonlinearity is minimized, no significant shift in the output signal's base reference level will occur as a function of information sequence, such as is found in ac-coupled ferrite-core memory sense amplifiers.

However, there is inherent nonlinearity in the input impedance of the discriminator stage, and the need to

Figure 9 Common mode and difference mode of S_1 and S_2.



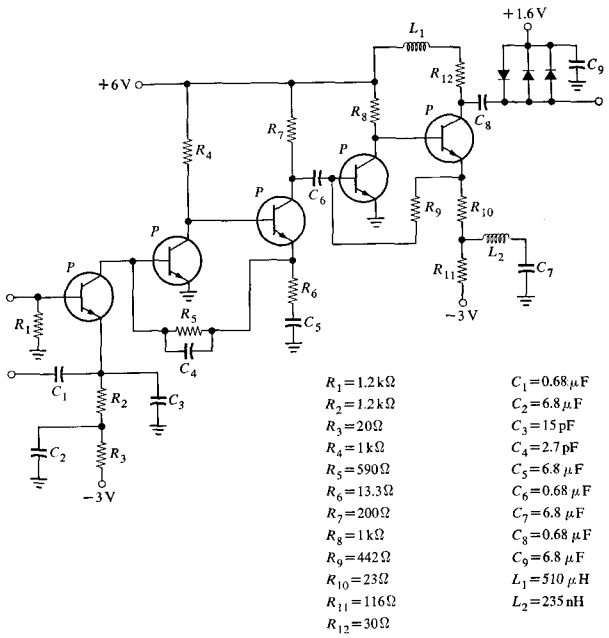


Figure 10 Sense amplifier circuit.

minimize the range of voltage swing at the amplifier's output to avoid special high-voltage power supplies and high power dissipation implies the need for a high degree of nonlinearity at the output node; specifically, positive and negative diode signal limiters are used. This non-linearity would present a serious problem of signal reference level shift with conventional *RC*-coupling due to the multicycle build up of charge on the coupling capacitance.

Three possible solutions were considered. The first was to make the coupling time constant short compared with the cycle time to effect complete recovery each cycle. This was rejected because the resultant high-pass frequency characteristic favored amplification of the high frequency noise signals relative to the desired information content.

The second possible solution was to couple the amplifier output directly into the discriminator. However, variations of the amplifier output stage's quiescent operating point due to component and voltage supply tolerances and the effect of temperature changes exceeded acceptable bounds. Therefore this solution was also rejected.

The third possible solution, which was adopted, was to provide a high-impedance current source output from the amplifier and to ac-couple this output to the discriminator using the network of Fig. 10. The high reactance of the inductor over the passband of the amplifier forces practically all of the output signal current through the coupling capacitor and into the reference level-setting resistor network and its signal limiting diodes at the discriminator input. Because the ac component of the current source is a linear function of the input signal, it also has a current-time integral of zero at the end of each cycle. Therefore, it will leave no difference in charge on the coupling capacitor between the beginning and the end of each cycle.

The Thevenin equivalent impedance of the reference voltage level-setting resistor network at the discriminator input was chosen to correctly terminate the characteristic impedance (150 Ω) of up to three feet of twisted-pair cable connecting the amplifier output to the discriminator input. The coupling capacitor and the signal-limiting diodes were retained on the amplifier to minimize the amplitude of unwanted coupled signals between adjacent twisted pairs.

To provide adequate discrimination between signal and noise, a minimum of 15 mA peak at signal time must be provided by the amplifier output. The input differential amplifier delivers 15 μA in response to a minimum signal from the array. Thus an intervening amplifier having low input impedance, high output impedance, and a current gain of 1000 is implied. Two similar feedback pairs, in each of which a small portion of the current in the output transistor is shunt-fed back to the input, are cascaded through an *RC*-coupling network.

The dominant pole determining the bandwidth of the overall amplifier is controlled by the small capacitor shunting the feedback resistor in the first feedback loop. This deliberate limitation of bandwidth provides consistent semi-integration of the signal, substantially minimizing the effects of variations in device frequency response characteristics and of array drive circuit rise time variations.

The discriminator and latch circuits are conventional DTL circuits such as those used throughout the computer products using this control store.

Noise

• *Sneak-path noise*

A major source of noise in a balanced capacitor read-only storage is the sneak-path noise.[9] This is the result of undesirable capacitive coupling between the sense lines via the address and balance lines. The desired sense output is obtained through one capacitive coupling between the driven address line and the sense lines, while the sneak-path noise has to go through two more capacitive couplings from one sense line to another. Although the noise is highly attenuated in comparison with the signal, the existence of many possible paths, depending on the size of the array and the information pattern used, will lead to a substantial strengthening of the noise which places a certain limitation on the size of the array.

In Fig. 11 a few of the sense lines and address lines are shown. Let the total number of words be m and the number of bits be n. Driving address line 1 (AL1), one can calculate the sneak-path noise injected into other sense lines by address line 2 (AL2). Apart from the driven address line, address and balance lines play similar roles as far as noise coupling is concerned.

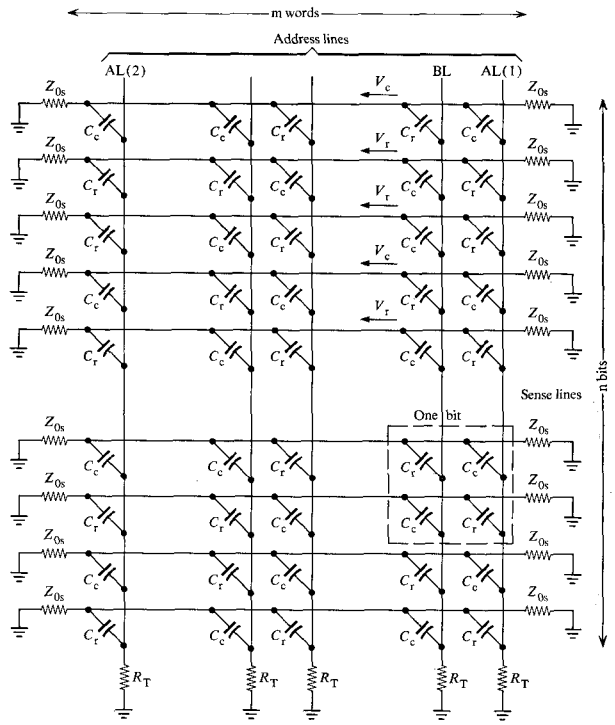


Figure 11 Representation of partial array.

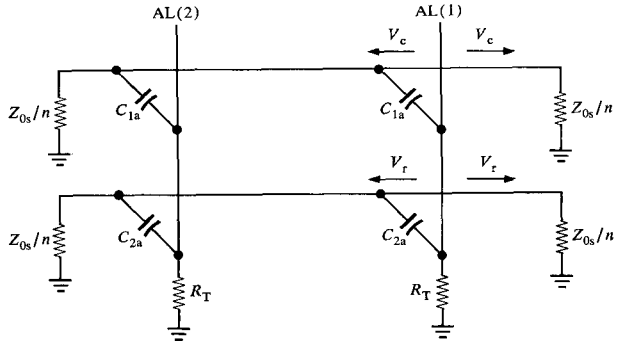


Figure 12 Representation of sense lines by two equivalent transmission lines.

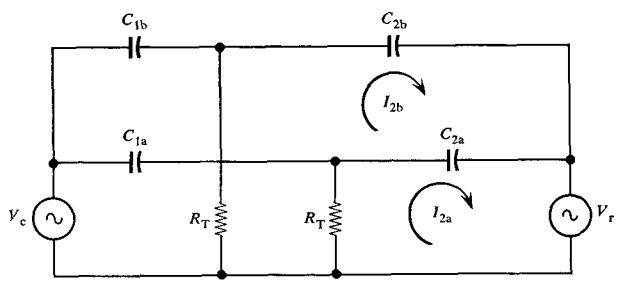


Figure 13 Simplified equivalent circuit at the junction of sense line with a pair of address and balance lines.

Since there are $2n$ sense lines, on driving AL1 there will be n sense lines propagating a voltage V_c and n sense lines propagating a voltage wave V_r from right to left. Similar voltage waves propagate from left to right on the other side of AL1.

For purposes of simplification, the following assumptions are made:

1) All V_c and V_r reach address line 2 at the same time. This is, in fact, not quite true because of the delay along the driven address line.
2) All V_c and V_r are equal and identical and any changes induced in their magnitude as they propagate along the sense lines are of second-order effect.
3) Direct capacitive and inductive coupling between adjacent sense lines is neglected.

On the basis of these assumptions one can lump all the sense lines into two groups. Each group can be represented by an equivalent transmission line—one propagating a voltage V_c and the other a voltage V_r. Each transmission line has a characteristic impedance Z_{0s}/n and is matched at both ends. The situation can therefore be reduced to that shown in Fig. 12.

Although discrete, the coupling regions via the address and balance lines between these two groups of transmission lines can be considered continuously distributed, giving rise to directional properties. If the two ends of the sense lines that are terminated by their characteristic impedances are designated left and right, then as far as the termination of the lower transmission lines on the left is concerned there will be two types of voltages due to sneak paths. First, there will be a forward voltage induced by the voltage wave propagating to the left on the upper transmission line; second, there will be the backward voltage caused by the voltage wave propagating to the right. The two types are fundamentally different, and for extreme positions of AL1 either one or the other will be observed. If AL1 is situated at the extreme right, the only voltage is the forward voltage; if it is situated at the extreme left, only the backward voltage is observed. For AL1 somewhere between, the sneak-path voltage is a combination of both.

The capacitive coupling between address line 2 and the transmission lines carrying V_c and V_r are, respectively, C_{1a} and C_{2a}. The magnitude of C_1 and C_2 depends on the information pattern along address line 2. Now, V_c can couple to AL2 through C_c or C_r, and V_r can couple through C_c or C_r. The sum of $C_1 + C_2$ is constant and given by $n(C_c + C_r)$. Due to the complementary nature of the information along the balance line associated with the address line, C_{1b} is equal to C_{2a}, and C_{2b} is equal to C_{1a}. A simplified equivalent circuit for an address line and its balance line is shown in Fig. 13.

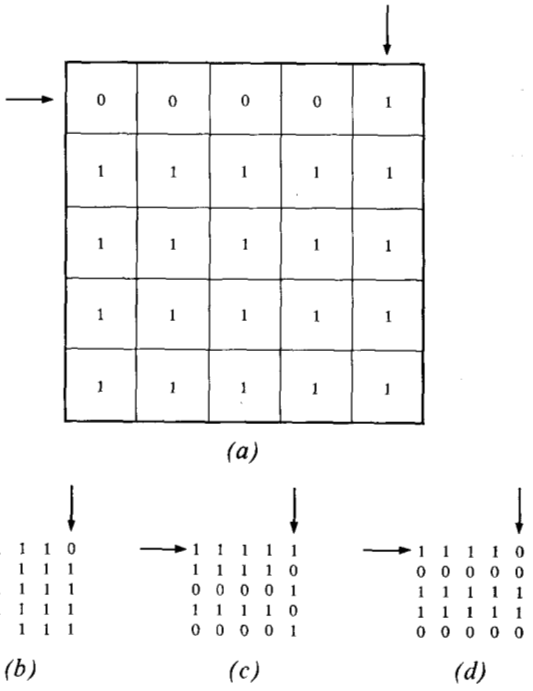


Figure 14 A number of worst-case sneak-path noise information patterns.

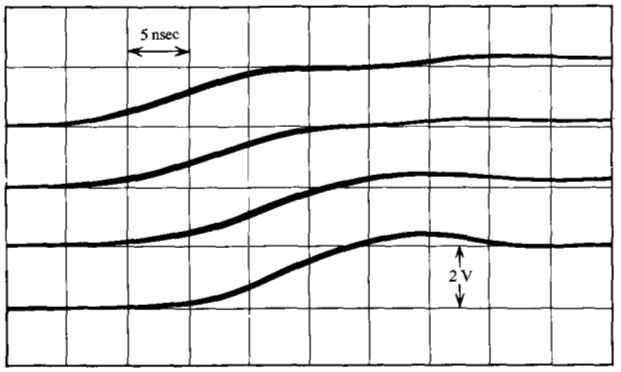


Figure 15. Time skew of the select voltage from the non-hinged side.

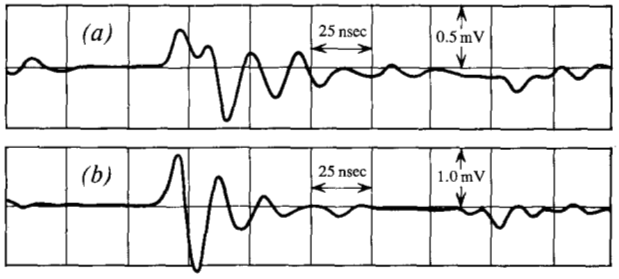


Figure 16 Select noise as observed from (a) hinged side and (b) nonhinged side.

In solving for the sneak-path current, it is possible to define the worst-case information pattern by maximizing this current. It has been found that many worst-case patterns can be constructed. Some of these patterns are shown in Fig. 14. As a rule of thumb, a worst-case information pattern can be found by assuring an odd parity in the four corners of all squares having sides that are coincident with the driven address line and the monitored sense lines.

A typical value for the forward sneak-path noise voltage per gate using average values for the array parameters is about 0.8 mV, compared with a signal of about 2.1 mV.

• *Select noise*

In the selection of a particular address line, one gate is selected; hence, a voltage is applied to 31 other address lines—one in each group of 22 across the base-collector capacitance (C_{OB}) of their respective array drivers. The current into each of the unselected address lines is given by

$$i_{\perp} = C_{OB}(dV_s/dt)\,,$$

where V_s is the select voltage. This can be justified by the fact that the time constant $Z_{0a}C_{OB}$ is small. The voltage of the unselected address line can be written

$$V_a = C_{OB}Z_{0a}(dV_s/dt)\,,$$

where Z_{0a} is the characteristic impedance of the address line.

The voltage of the unselected address line couples through C_c and C_r into the sense lines, giving rise to an undesirable signal called select noise. Clearly, depending on the information pattern of the array, the select noise can accumulate so that the effects of the 32 select voltages can add up together either to oppose or to aid the signal. This is the worst-case select noise and is characterized as

$$V_{sn} = kN(Z_{0s}/2)Z_{0a}C_dC_{OB}(d^2V_s/dt^2)\,,$$

where N is the number of array drivers half-selected (one gate is normally selected, making $N = 32$), and k is a factor introduced to take into account the two possibilities of selecting either from the hinged side or the nonhinged side of the gate.

Selecting from the nonhinged side means that the select voltage propagates in the same forward direction as the noise, and this causes progressive strengthening of the select noise. In this case, k is unity. On the other hand, selecting from the hinged side causes the various contributions to the select noise to be staggered in time, and now k is less than unity. In Fig. 15 the time skew of the select voltage from one end of the gate to the other is shown. In Figs. 16a and 16b, the select noise signals for the hinged and nonhinged cases are shown. In the hinged case, k is about 0.5. The calculated value of the select voltage from the previous equation, using $k = 1$, has a peak value of 0.85 mV.

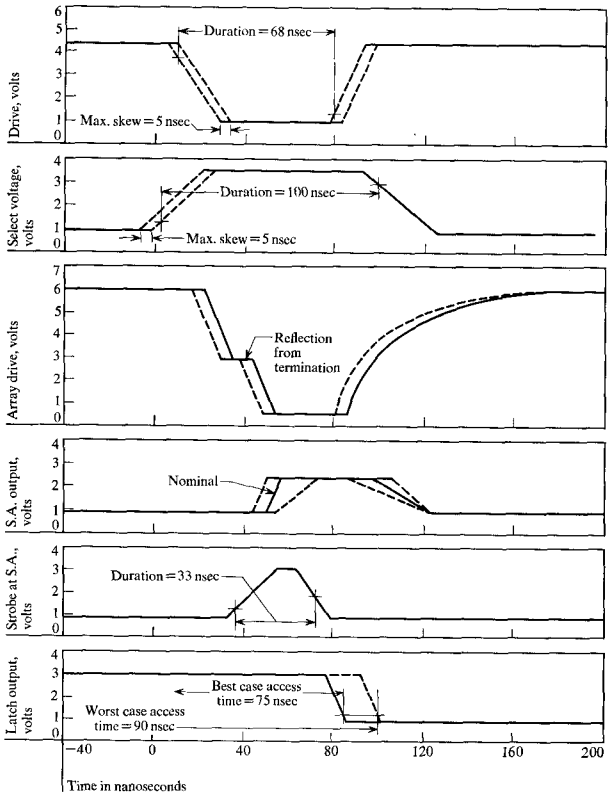


Figure 17 Pulse timing.

Timing

Proper timing of the various pulses ensures not only that the access and cycle time requirements of the machine are satisfied, but also that the margin of operation is maximized. The timing of different pulses is shown in Fig. 17. The access time is defined as the difference in time between the leading edge (+1.9 volt level) of the latest "+select" time and the leading edge (+1.2 volt level) of the latest "CROS bit" one output. The cycle time is defined as the repetition rate of the clock or the time between the leading edges of succeeding reset pulses. The access time is specified as less than 90 nsec and the cycle time as 200 nsec. The margin of operation is measured by the range over which the supply voltages and the strobe pulse timing can be varied without any machine error.

The access time is essentially determined by the delays in the system. Figure 18 shows this in block diagram form. The values included are worst-case delays, of which the circuit delays total 55 nsec, array and cabling delays total 20 nsec and timing delays total 12 nsec. In practice, all the worst-case delays do not add up in series. At present, the system operates with a nominal access time of 80 nsec.

The cycle time is essentially determined by the time constants in the system. The longest time constant is the address line when the address drive is turned off. The time constant, which is 24 nsec, is the product of the terminating resistor, 100 ohms, and the address line capacitance, 240 pF. In 100 nsec, or about 4 time constants, the address line has recovered. The drive pulse (flat top plus leading edge) time of 68 nsec adds directly to the address line recovery time, resulting in an address line voltage pulse width of about 170 nsec. Other cycle time considerations are in the power dissipation of circuit components and power supply ratings. However, none of these are limitations in the present system. The specified 200 nsec is a conservative limit and is easily met.

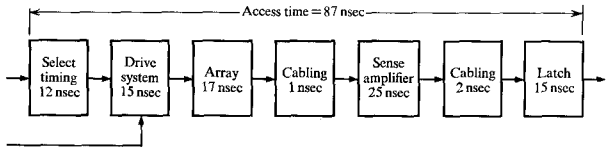


Figure 18 System delays.

The skew of the system accumulates at the input of the latch, where the margin of operation is determined. Several factors that influence this margin are shown in Fig. 19. These include:

Sense amplifier output skew. This is the combined effect of tolerance accumulation from the drive system, array cabling, and sense amplifier. It is affected, and can be somewhat controlled, by the timing. The different delays, for a sense signal generated along any one sense line, to the sense amplifier are minimized by staggering the timing of the emitter drive pulses. Figure 20 shows how this is accomplished. The drive cables are divided into four groups, each delayed with respect to another by a fixed interval. This delay, ΔT, can be designed so that the drives in group D are delayed behind those of group A by the full propagation time of the sense line. When this is so, the sense signal will arrive at the sense amplifier at the same time regardless of where it has been generated along the sense line. The sense signal skew contributed by the array is only that of the address line, which is about 6 nsec.

Latch gray area. This is the range of voltages within which the operation of the latch is unreliable. Below the lower boundary the latch would never operate. Above the upper boundary, the latch would always operate provided that the input stays on long enough. The gray area defines the gain of the amplifier for a given signal and the signal-to-noise ratio. The smaller the gray area, the more reliable the latching operation.

Latching time. This is the minimum time available for the latch to operate. It should always exceed the maximum latch-around time and is a function of the width of the drive pulse. Thus the drive pulse width is made as great as can be permitted without causing the recovery of the address line to interfere with the cycle time objective.

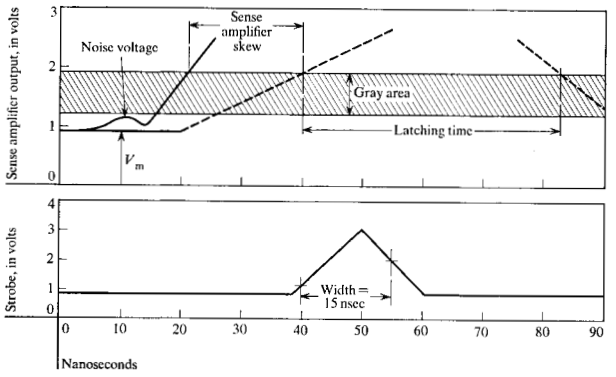
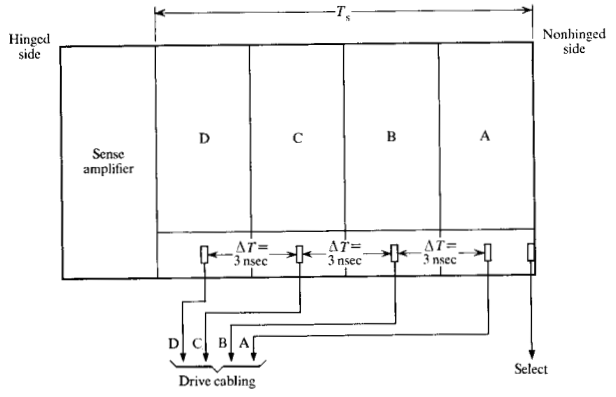


Figure 19 Sense amplifier output and strobe.

Figure 20 Drive and select cabling.



Noise voltage. It is obvious that the noise voltage should be minimized for reliable machine operation. Some of the high-frequency noise components are integrated out in the sense amplifier. The most prominent noise is that caused by the select circuits turning on. This, however, occurs sufficiently ahead of the signal that it does not seriously interfere with the signal during the strobing time.

Strobe timing. The width of the strobe pulse is determined by the maximum latch-around time of the latch circuit. This is about 15 nsec at the latch. The pulse width should not be any longer than necessary; otherwise it would provide time for possible noise to set the latch. The timing of the strobe determines the access time. The possible variation in the strobe timing without machine error (or latching error) indicates the operational margin of the machine. This time is about 30 nsec, with supply voltages set 4% off their nominal values for lowest system gain.

Conclusions

In a storage system of this type, a limitation on the access time and consequently the cycle time is imposed by the delays through the drive and sense circuits. Improvement in the delays of the circuits will be reflected directly in better access and cycle times.

One limitation of this system is the relatively large size of the array and the ground plane. Besides the undesirable aspect of bulkiness, ground noises of intractable behavior can be generated. In addition, the general trend in system architecture requires the progressive reduction of access time, cycle time, and array size. These factors interact favorably with each other as the intersection capacitance is decreased. The lowering of capacitance means an improved cycle time, since the major portion of the latter is taken up by the recovery of the address line. The reduction in the size of the array will shorten the access time, since delays through the array are also reduced. Furthermore, diminution of signal is accompanied by a corresponding decrease in sneak-path and select noise. The impact on the sensing circuitry would be to require a wider bandwidth response and, therefore, less delay.

The original requirements, however—90 nsec access time, 200 nsec cycle time, 281,600 bits in a read-only configuration—have been met in the present design. Array size, as related to performance and storage capacity, is consistent with System/360 architecture. The design margins for worst-case signal delays and for noise control with worst-case information patterns, as described above, have been validated in extended service tests and the BCROS is now in use in several models of System/360.

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