

# Automatic Dynamic Response Analyzer

**Abstract:** The Automatic Dynamic Response Analyzer (ADRA) is a laboratory tool for developing improved methods of characterizing and measuring the dynamic performance of integrated circuit logic packages. ADRA consists of ensembles of computer controlled electronic equipment which provide a suitable electrical environment for the logic unit under examination, subject the unit to appropriate patterns of shaped pulses, measure and digitize the input/output waveforms, and process the resulting data. This paper describes the ADRA system, its organization and hardware characteristics, and an example of its use.

## I. Introduction

The trend to integrated circuit technology in digital computer systems has affected many aspects of circuit development, notably, testing. Typical integrated circuit packages may contain 20 to 40 logic decision elements which are interconnected to perform prescribed logical functions, e.g., decoders, switches, registers, adders, etc. The limitations on the number of input/output pins and the inaccessibility of internal circuit points, will, in general, preclude direct testing of the time dependent performance of individual active circuits within the package, a practice which is currently followed in testing discrete and hybrid circuits. Since dynamic testing at some level of packaging is considered mandatory for high quality assurance, improved methods of characterizing and measuring the time dependent behavior of functional logic units must be developed in order to predict and verify their performance. The Automatic Dynamic Response Analyzer (ADRA) system is a laboratory tool to aid in this development.

This paper describes the ADRA system, its organization, the characteristics and operation of its hardware, and an introductory example of its use. An Appendix describes the ADRA pulse shape control hardware and a companion paper<sup>1</sup> describes the use of ADRA in the analysis of unit logic behavior.

The ADRA system consists of ensembles of laboratory equipment associated with and controlled by a large digital computer. The laboratory equipment, for the most part, consists of commercially available instruments, modified

and augmented to render the various units operable with each other and with a digital interface. Though not described in this paper, the system also includes extensive control and sequencing software to set up tests, acquire and analyze data, and present test results. Together, the ADRA system hardware and software provide a simulated computer environment for the functional logic unit under examination, subject the unit to patterns of shaped pulses, measure input/output waveforms, and process the resulting data. Throughout, operation is controlled by stored programs, the ADRA system being an extension and expansion of computer based techniques used in other systems.<sup>2,3</sup>

## II. System organization

### • Computer facilities

The complex control requirements of the typical ADRA experiment and its extensive data collection and processing needs can only be met by a large scale computer facility. The ADRA laboratory facilities are coupled to the central processor of a time-shared system, an approach which provides large processor capability at lower cost than is possible with a dedicated computer of comparable performance. Figure 1 is a block diagram of the ADRA system. The time-shared system is an experimental one which is in operation at the IBM Research Center.<sup>4</sup> The system is based on a modified IBM 7044 (M44) equipped with extensive peripheral equipment and an IBM 7750 transmission control unit for communication with user terminals.

The time-shared system is available to 16 users who communicate with the system through IBM 1050 keyboard-

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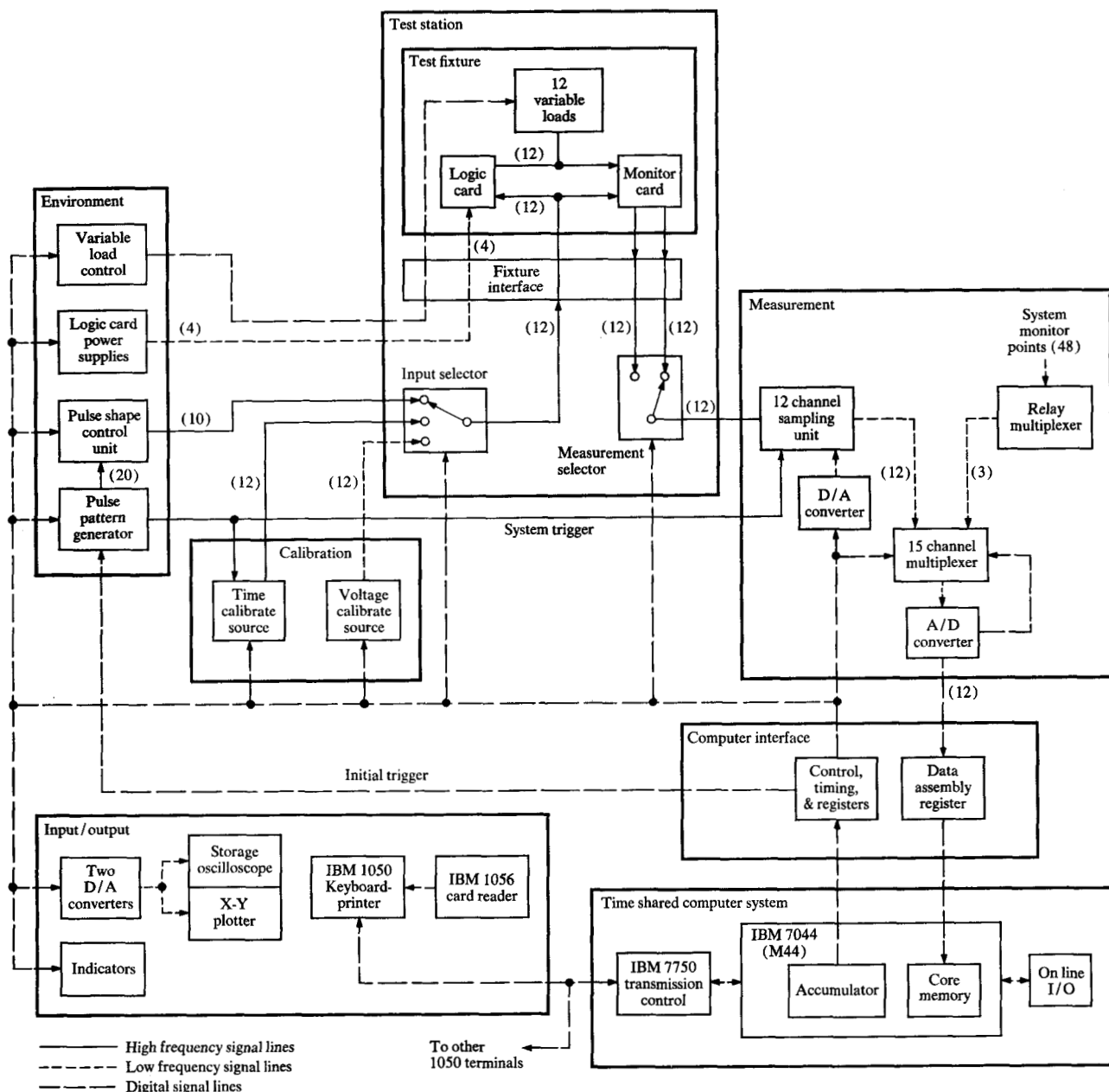


Figure 1 Block diagram of the ADRA system.

printers. The operating system program provides each user with a virtual computer which he can operate in a conversational mode. Each virtual computer has the equivalent of two million words of random access storage, permanent files for storing programs and data, and access to the M44 input/output equipment. The system programming facilities include a Command Language, an Assembly Program Language, and a Load and Go FORTRAN IV compiler, all supported by extensive debugging and library routines. One of the IBM 1050 terminals is the control console for the

ADRA experimenter and is located adjacent to the ADRA laboratory facilities. These facilities are coupled to the M44 and are treated as an on-line input/output device assigned to the experimenter's virtual machine.

The M44 is, of course, remote from the ADRA laboratory facilities. Communication is via high speed data channels between the M44 and the computer interface unit, as indicated in Fig. 1. The interface unit contains registers for receiving control words and for temporarily storing measurement data and logic for sequencing measurement

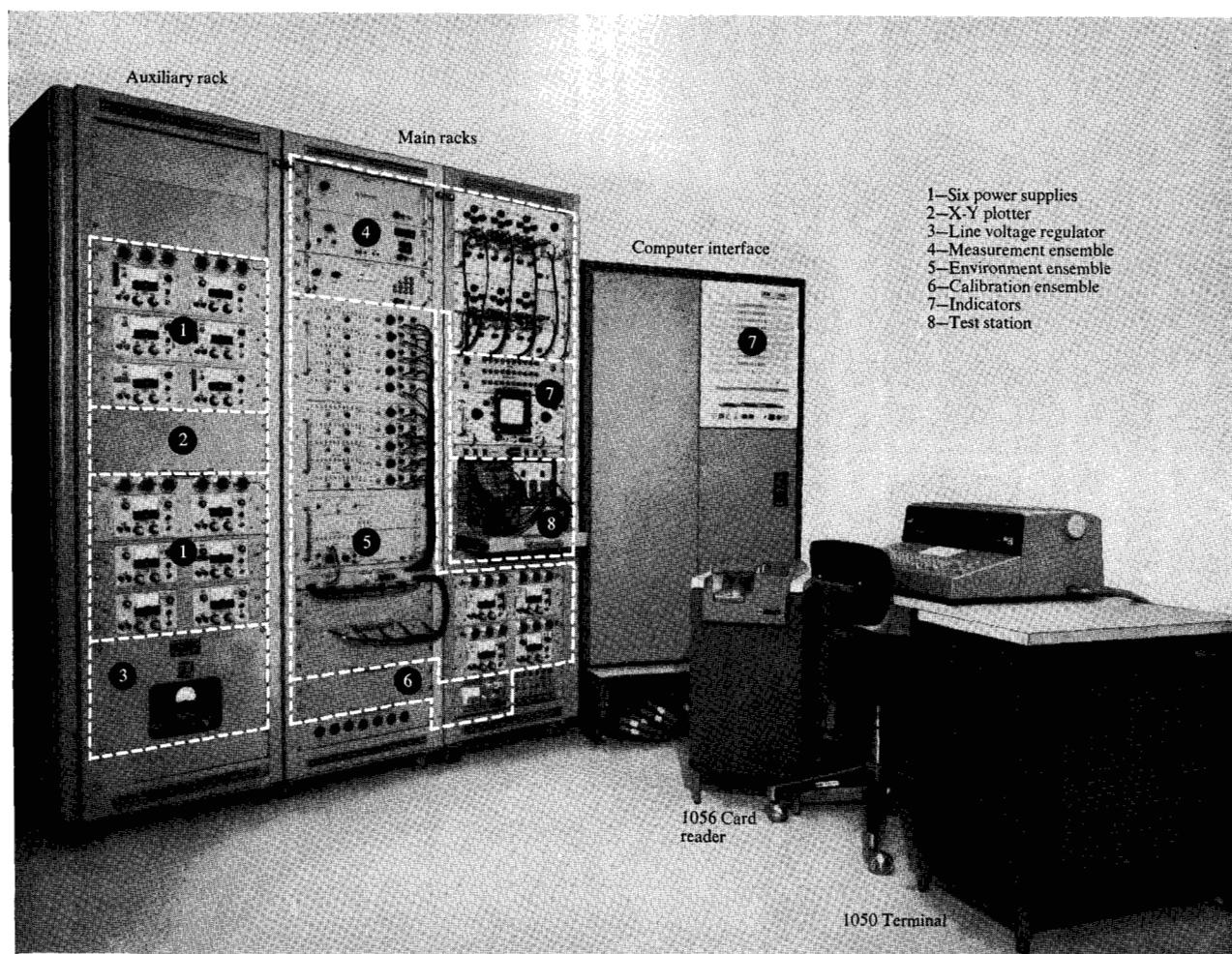


Figure 2 ADRA laboratory installation.

operations. The ADRA laboratory facilities are controlled by the sequential transfer of words from the M44 accumulator to registers in the interface.

Measurement data are assembled in a 36-bit register in the interface unit before transfer to the M44 core memory. Data words are stored in sequential memory addresses where they are available for immediate processing or analysis.

#### • Laboratory facilities

The blocks in Fig. 1 not referred to above comprise the unique hardware elements of the ADRA system. As previously stated, the system performs experiments on functional logic units, the results being used to develop techniques for analyzing their time dependent behavior. In an experiment of this type, the logic unit under examination must be provided with a suitable electrical environment and means for measuring its performance. Of equal practi-

cal importance is a generalized means for connecting the system to a variety of logic families. A method of calibrating the measuring equipment is also essential.

The ADRA system will accept logic circuits that have up to 10 input connections and 12 output connections and which require up to 4 power supply voltages. These quantities were determined by compromises between flexibility, capability, and cost. The interface between the test fixture and the ADRA facilities is located in the test station and has all the means necessary to connect the system, via a fixture, to a variety of logic circuits. The fixture itself is not an integral part of ADRA; it must be specifically designed to handle the particular circuit package one wishes to test.

The input selector is a 12-pole, 3-position, coaxial relay which, under program control, connects either the pulse sources, a time calibrate source, or a voltage calibrate source to the fixture interface. The pulse source contains the pulse pattern generator and the pulse shape control

unit. The 10-channel pulse pattern generator, when triggered, produces a burst of 10 sequential pulses simultaneously on all channels. The presence or absence of a pulse in each sequential time position of each pulse channel is determined by the contents of ten 10-bit registers in the computer interface. The pulse pattern generator outputs connect to the pulse shape control unit which, in turn, connects to inputs of the input selector. The shape and polarity of the pulses in each channel are independently determined by the pulse shape control unit which, depending on the contents of another register array, selects predetermined values of polarity, rise time, offset, amplitude, and delay relative to other channels.

The measurement selector is a 12-pole, 2-position, coaxial relay which, under program control, delivers signals on 12 of the 24 monitor lines from the logic unit under examination to the 12-channel sampling unit. The sampling unit is an assembly of 6 modified dual-channel sampling units and a single timing unit triggered from the output of an eleventh channel in the pulse pattern generator. Within a selected measurement interval the sampling time is determined by the output of a digital-to-analog converter whose input is a register in the computer interface. The 12 sampling-unit outputs connect with an equal number of inputs to the 15-channel multiplexer. The remaining 3 multiplexer inputs connect to the 3 outputs of a relay multiplexer which, under program control, scans 48 dc voltage monitor points throughout the system. Upon completion of a sampling cycle, the 15 input voltages to the multiplexer are sequentially scanned, digitized by the analog-to-digital converter, assembled into five 36-bit data words, and transferred to the M44 core memory.

The calibration ensemble is used to calibrate the measurement ensemble. Two different sources are used: the voltage source is a well regulated programmable power supply which is controlled by a register in the computer interface; the time source is a tunnel diode step generator triggered by the sampling unit trigger. The absolute time delay between the sampling unit trigger and the output of the time source is programmable and precise.

In addition to the IBM 1050 keyboard-printer, the input/output facilities include an IBM 1056 card reader, a storage oscilloscope, and an X-Y plotter. The oscilloscope and the plotter are driven by 2 program controlled digital-to-analog converters, permitting the graphic display of processed information in a variety of formats. Arrays of indicator lights allow the operator to monitor system and control register status.

### III. Hardware description

Figure 2 shows the ADRA laboratory facilities and indicates the locations of the major equipment ensembles. The units located in the main racks are further identified in Fig. 3.

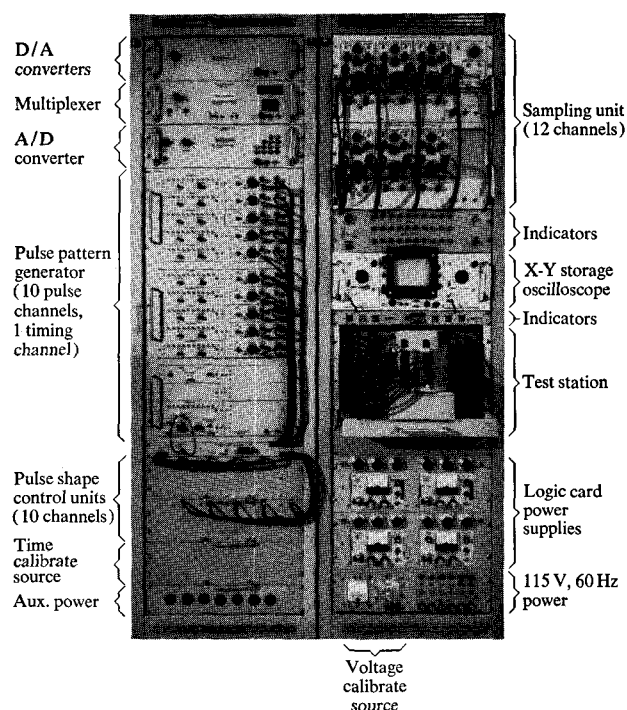


Figure 3 ADRA main racks.

The following paragraphs expand on the equipment summary of the previous section. Of particular interest are the test station, the environment ensemble, the measurement ensemble, and the calibration ensemble.

#### • Test station

The heart of the test station (Fig. 4) is the fixture interface (Fig. 5) where all ADRA input and output facilities (summarized in Table 1) are brought together. Coaxial relays which comprise the input and measurement selectors are housed behind the fixture interface panel.

Although test fixtures must be designed specifically for the circuit family to be tested and, hence, are not part of ADRA, it is appropriate to mention as an example the fixture constructed to hold the circuits tested during ADRA development. These were simulated integrated circuit packages made with Motorola current-switch emitter-follower circuits mounted on IBM SLT cards. The edge of one of these cards can be seen in the lower central region of the fixture in Fig. 4. On either side of the card are pluggable assemblies which connect and adapt signals from the interface to the fixture. On the back side of the fixture, opposite the test card, is the monitor card, an assembly of 24 passive probes, which connects to 24 signal pins on the test card and delivers, via coaxial cables, 24 signals to the fixture interface. Additional circuitry within the fixture provides dc distribution and grounding.

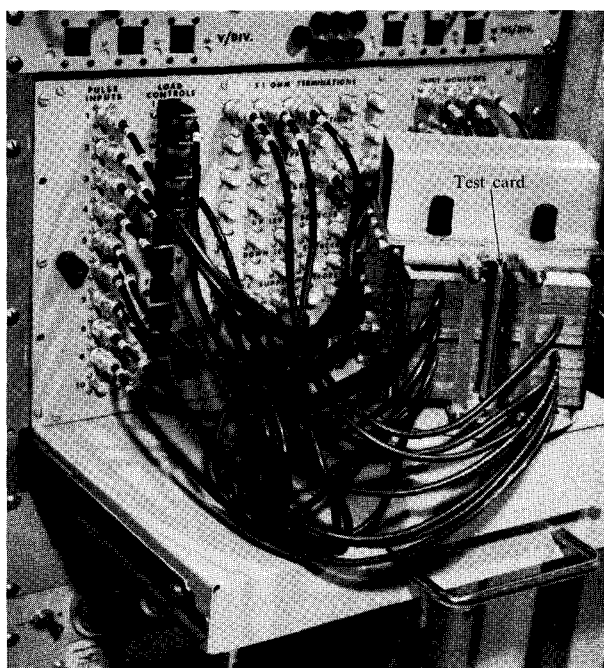


Figure 4 Test station.

Table 1 Fixture interface facilities.

| Facility                                                  | Number          | Type of signal line | Description                                                                                                                                             |
|-----------------------------------------------------------|-----------------|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| Pulse Inputs<br>(Also, voltage and time calibrate inputs) | 10<br>(12)      | coaxial             | Inputs to the fixture via the input selector from the environment ensemble or from the calibration ensemble. Inputs 11 and 12 do not have pulse inputs. |
| Load Controls                                             | 12              | digital             | Each control can actuate two load changing relays in the test fixture.                                                                                  |
| 51-ohm Terminations                                       | 12              | —                   | Terminations for fixture output lines which need not be monitored.                                                                                      |
| Up Level Sources                                          | 6               | low freq.           | Alternate inputs to the fixture for logic card inputs which are invariant in a test.                                                                    |
| Down Level Sources                                        | 6               | low freq.           |                                                                                                                                                         |
| Dc Supply Monitors                                        | 6               | low freq.           | Means for monitoring fixture dc voltages or up and down level voltages.                                                                                 |
| Dc Supplies                                               | 4               | low freq.           | Inputs to the fixture from the programmable dc supplies in the environment ensemble.                                                                    |
| Input Monitors                                            | 12 <sup>a</sup> | coaxial             | Connections for outputs from the fixture to the measurement ensemble via the measurement selector.                                                      |
| Output Monitors                                           | 12 <sup>a</sup> | coaxial             |                                                                                                                                                         |

<sup>a</sup> The division into 12 input and 12 output monitors is arbitrary. Since all monitor lines are electrically identical, any combination of inputs and outputs (up to a total of 24), with proper control programming, is possible.

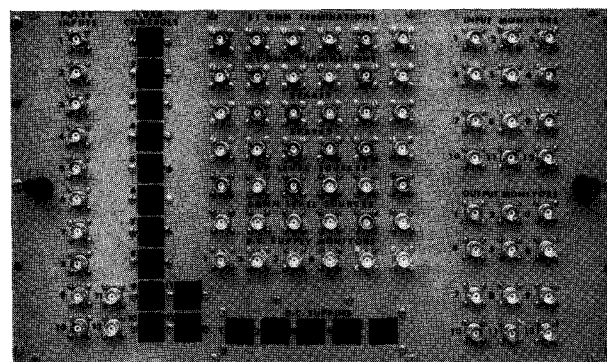


Figure 5 Fixture interface.

#### • Environment ensemble

Under program control the environment ensemble establishes all input and output conditions for the logic package under test. A variable load control provides binary control line connections on the fixture interface for actuating load changing relays in the fixture. In contrast to all other environment facilities, load control is effected in the fixture because the loads must be located as close as possible to the logic package outputs.

Four logic circuit power supplies are mounted directly below the test station. The output voltage of each supply is determined by its three associated 10-turn potentiometers which, in conjunction with control relays, cause one of four voltages (zero, low, nominal, or high) to be delivered to the fixture interface. These power supplies operate with remote sensing at the fixture to minimize the effect of ohmic drops. Power supply output polarity is not programmable; manual polarity control is retained as a precaution against damage to a logic card due to programming error. A 10-channel pulse pattern generator,\* under program control, develops the required output pulse patterns. Figure 6 illustrates the operation of the generator. In the Figure, the contents of 11 control registers in the computer interface are indicated, a block diagram of the generator is shown, and the output pulse patterns corresponding to the register contents are identified. Operation is as follows: The contents of each control register determine the occurrence of enabling pulses at the output of its associated pattern generator; clock pulses, in conjunction with these enabling pulses, trigger the delay circuit which, in turn, triggers the pulse width control circuit. Each channel has positive and negative output amplifiers with individual manual control of output pulse amplitude. The delay, width, amplitude, and pulse repetition frequency controls are set manually for each test. Control registers 1 through 10 may contain any

\* A Texas Instruments, Inc. Model 6325X1 Pulse Generator, built specifically for ADRA.

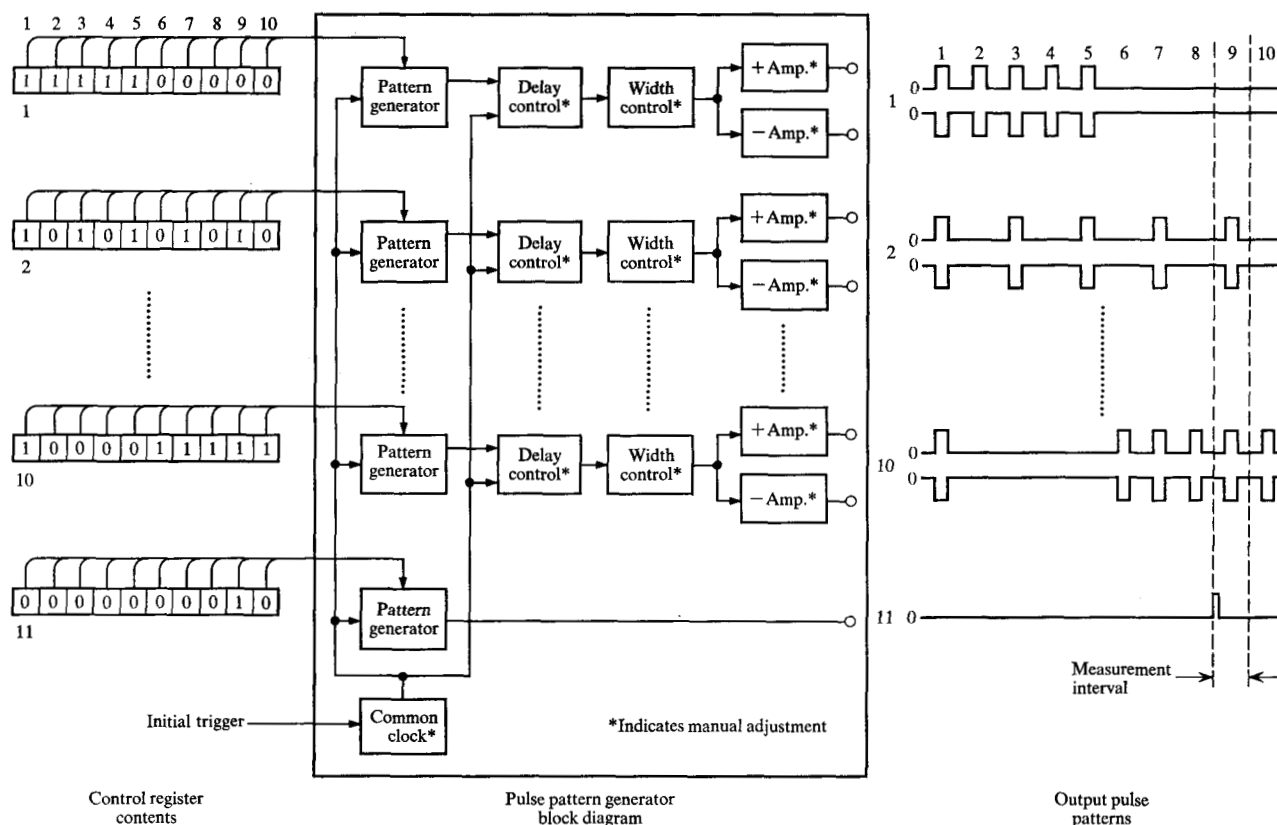


Figure 6 Pulse pattern generator operation.

binary pattern; the eleventh register, which determines the measurement interval in a test, may have only a single 1 in any position.

After the 10-pulse pattern and the measurement interval registers are set, each trigger from the computer interface initiates one occurrence of the programmed pulse patterns. As indicated in Fig. 1, the 20 output pulse patterns connect to the pulse shape control unit before being delivered to the fixture interface; the trigger pulse from the eleventh channel is the trigger input to the 12-channel sampling unit.

The pulse shape control unit is described in detail in the Appendix. Briefly, under program control it modifies the pulses from the pattern generator to produce pulses which have the polarity, up and down levels, rise times, and relative delays required for a test.

#### • Measurement ensemble

The measurement ensemble includes a 12-channel sampling unit, a multiplexer, an analog-to-digital converter, and one digital-to-analog converter. The last three instruments are commercially available\* and operate in a conventional

manner in response to control signals from the computer interface. The 12-channel sampling unit was built specifically for ADRA† and operates in the same manner as the sampling oscilloscope in the Strobed Analog Data Digitizer.<sup>2</sup> Suitable programming sequentially:

- (a) sets an input to the D/A converter,
- (b) issues a trigger which, via the pulse pattern generator, causes signal pulses to appear at the sampling unit inputs and causes a trigger to be delivered to the sampling unit,
- (c) initiates multiplexer and A/D operation and simultaneously,
- (d) initiates the assembly of 12-bit A/D converter output words into 5 successive 36-bit words in the assembly register in the computer interface,
- (e) transfers the contents of the assembly register to the computer core memory,
- (f) augments the D/A converter input and returns to step (a) to repeat the sequence.

This sequence causes digitized waveform images to be stored in core memory. Images can be visualized as twelve

\* Texas Instruments, Inc. Model 845A01 Multiplexer, Model 846E1A A/D Converter, and 854B1B D/A Converter.

† Tektronix, Inc. 6 Type 3S76 Dual-Trace Sampling Units and a Type 3T77 Sampling Sweep Unit mounted in 2 Type S-390 Power Supplies (all modified).

2-column tables consisting of paired D/A converter inputs (proportional to time) and A/D converter outputs (proportional to waveform amplitude).

ADRA has no provision for waveform display during the collection of waveform images; in fact, waveform display is specifically avoided because: (a) a simultaneous display of 12 waveforms is frequently not comprehensible, (b) sequential display of waveforms, either individually or in groups, slows down the data collection process, and (c) the data delivered to the computer core memory is raw data which, for high accuracy, must be corrected for sampling unit drift.

There are times, however, when the display of waveforms is necessary; for example, during system checkout and program debugging or when difficulty is encountered in the course of a test. In such instances, waveforms may be displayed on the storage oscilloscope at the option of the operator.

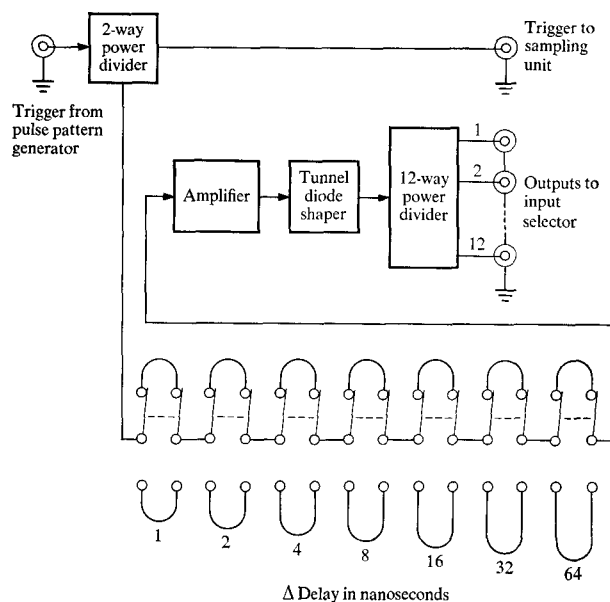
Twelve of the 15 multiplexer inputs service the sampling unit; the remaining 3 multiplexer inputs come from a relay multiplexer that functions as a system monitor. Under program control, the relay multiplexer sequentially scans, in groups of 3, dc voltages at 48 critical points throughout ADRA. Voltage dividers, where necessary, reduce the monitored voltages to values within the range of the A/D converter, and the comparison of measured voltages with permanently stored upper and lower limits provides for the detection of excessive equipment drift or failure.

#### • Calibration ensemble

The voltage calibrate source and the time calibrate source, under program control, deliver known calibration signals to the fixture interface. With the measurement selector properly set, these calibration signals are impressed on the inputs of the 12-channel sampling system for individual channel calibration.

The voltage calibrate source is a well regulated dc power supply which is programmable from  $-9.95$  V to  $+9.95$  V in  $0.05$ -V steps. When the system is in the voltage calibrate mode: (a) a sequence of known voltages is impressed on the sampling unit inputs, (b) for each voltage in the sequence, data from the sampling unit outputs are collected, via the multiplexer and the A/D converter, in the manner described previously, and (c) the data stored in a special location in the core memory. The data thus stored and the known inputs comprise 12 voltage input/output transfer characteristics, one for each sampling channel. Subsequently, when the system accumulates test data, these transfer characteristics are used to correct "raw" waveform amplitude data to "true" data.

The time calibration process is similar, but before presenting an operational description, further description of ADRA triggering is necessary. The initial trigger originates, as shown in Fig. 1, at the computer interface and triggers



All lines and relays are coaxial  
Relay controls not shown

Figure 7 Block diagram of the time calibrate source.

the pulse pattern generator. This generator, in turn, emits a secondary, or system, trigger at the beginning of the measurement interval determined by the contents of the eleventh control register in the pulse generator. This system trigger is the input to the 2-way power divider in Fig. 7 where, as indicated, one output triggers the time calibrate circuit and the other triggers the sampling unit. In all ADRA operating modes, this triggering system is invariant.

Figure 7 is a block diagram of the time calibrate source wherein the system trigger first passes through the coaxial delay selection relays. These relays insert precise lengths of coaxial cable so that, under program control, delays from 0 to 127 nsec in 1 nsec steps may be inserted in a trigger path. The trigger path terminates in an amplifier/tunnel diode monostable circuit which generates a pulse of approximately 250 nsec duration. The 12-way power divider converts the monostable output into 12 identical outputs.

When ADRA is in the time calibrate mode, coincident positive voltage steps with rise times of approximately 200 psec are impressed on the 12 sampling unit inputs. By suitable programming of the delay control relays these steps can be positioned in the measurement interval relative to the sampling unit trigger. For each value of delay a program determines the D/A converter input values corresponding to the relative time positions of the steps. A sequence of such determinations permits the calculation of correction tables (one for each sampling channel) which relate D/A converter input values and time. Subsequently,

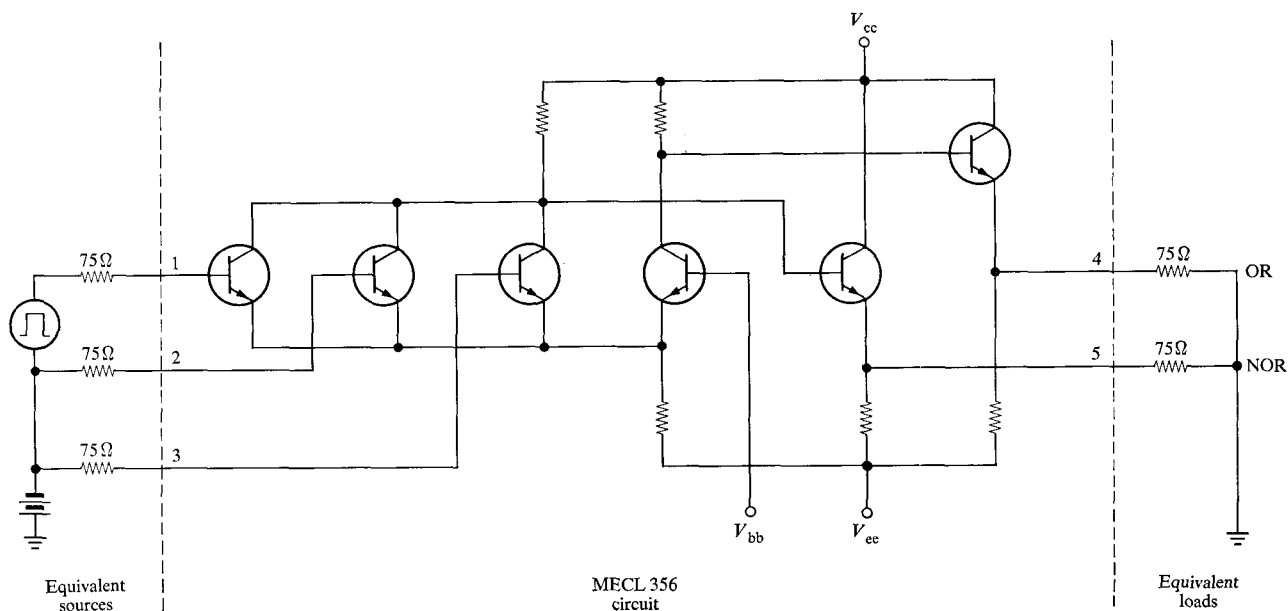


Figure 8 Circuit tested in example of ADRA operation.

when the system accumulates test data, these tables are used to correct raw waveform time data to true data.

#### • Input/output facilities

ADRA has several Input/Output (I/O) facilities, some of which are always present and others which may be employed at the option of the operator. The 1050 terminal, as described previously, is always used in any computer operation of ADRA. The optional I/O facilities peculiar to ADRA include indicator panels, an X-Y storage oscilloscope, and an X-Y plotter.

The computer interface indicator panel (see Fig. 2) has approximately 350 lights which indicate the status of the control registers, the input register from the M44 accumulator, and the output data assembly register. These register indicators are used mainly for manual operation or single-step computer operation in hardware or software testing and debugging.

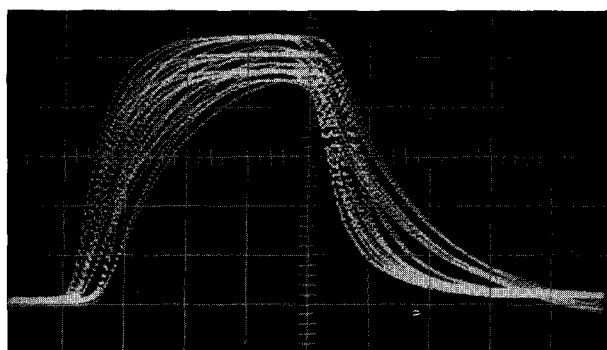
The storage oscilloscope operates in the X-Y mode from two D/A converters in the measurement ensemble. The operator, by calling an appropriate program, may display on the oscilloscope any waveform image in the computer core memory. During waveform display the oscilloscope operates in the storage mode to eliminate the need for continuous regeneration. An operator may either photograph the oscilloscope presentation or call a program which, via the same D/A converters, traces the waveform on the X-Y plotter.

Numeric indicators in the panel between the storage oscilloscope and the test station are programmed to indicate the horizontal and vertical sensitivities pertinent to a waveform display. The lights in the center of the panel indicate the status (i.e., normal, store, erase) of the upper and lower storage oscilloscope screens.

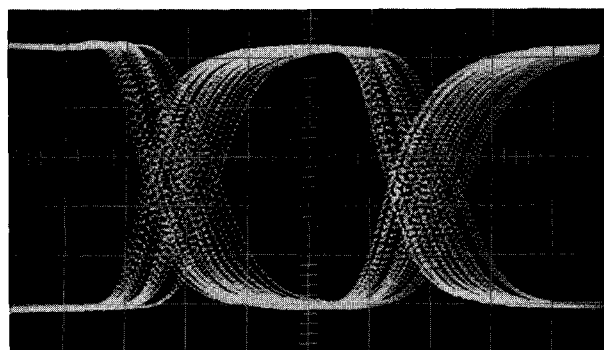
The panel between the sampling units and the storage oscilloscope contains three special 10-bit indicators, a sonic alarm, and line power control. The uppermost indicator, MODE, shows the ADRA mode, e.g., test, time calibrate, voltage calibrate, etc.; the lower ones, INDICATORS 1 and 2, are register controlled lights to which the test programmer may assign any meaning, e.g., program status, failure type, failure count, etc. The sonic alarm may be programmed to sound when any event, normal or abnormal, occurs in the course of a test.

#### IV. Experimental results

The flexible and extensive experiment control, data acquisition, and data analysis capabilities of ADRA prohibit a full presentation of experimental results in this paper. A typical test may entail the collection of hundreds of waveform images which must be analyzed by statistical methods before trends can be distinguished. The companion paper<sup>1</sup> by Maling and Schnurmann describes one such test. Here, the authors have chosen to present experimental results in terms of the input and output waveforms from a partial test of a single circuit on a single logic card. Figure 8 shows



(a)



(b)

**Figure 9** Waveforms obtained from test: (a) 27 input waveforms superimposed, (b) 27 OR output and 27 NOR output waveforms superimposed.

**Table 2** Test conditions

| Parameter                                       | Number of Values | Parameter Values <sup>a</sup>                 |
|-------------------------------------------------|------------------|-----------------------------------------------|
| Collector supply voltage                        | 1                | Nominal value = +1.29V                        |
| Base Supply voltage                             | 1                | Nominal value = -3.50V                        |
| OR output load                                  | 1                | Nominal value = 75 ohms                       |
| NOR output load                                 | 1                | Nominal value = 75 ohms                       |
| Input pulse shape—all possible combinations of: |                  |                                               |
| Rise time                                       | 3                | 8, 12, and 30 nsec.                           |
| Transition <sup>b</sup>                         | 3                | -90 to +390, -95 to +425, and -95 to +465 mv. |
| Relative delay                                  | 3                | 0.0, 1.5, and 6.0 nsec.                       |

<sup>a</sup> The parameter values below are the same as those used in the tests described in the paper<sup>1</sup> by Maling and Schnurmann.

<sup>b</sup> The term "transition" includes both the up and down levels of a pulse. See the text of the companion paper<sup>1</sup> for the definition of transition.

the circuit and the equivalent sources and loads provided by the test fixture. The test was performed with the test conditions listed in Table 2 and yielded the 27 input waveforms shown in Fig. 9a and the 27 OR and 27 NOR output waveforms shown in Fig. 9b.

The rudimentary experiment described above was performed—except for operator intervention to take photographs—by calling the FORTRAN IV subroutine shown and described in Fig. 10. This subroutine, for the most part, calls subroutines in the FORTRAN-based problem program package which was written for ADRA.

## V. Conclusions

The ADRA system has been operational since June, 1967. Since then, a continuing series of logic unit experiments and system tests have been conducted. The experience gained has convinced the authors that ADRA is a versatile and powerful laboratory instrument. It is equally apparent that much remains to be learned in the methodology of performing computer controlled experiments.

**Figure 10** Program written for example of ADRA operation.

| Fortran code                                       | Remarks                                                                   |
|----------------------------------------------------|---------------------------------------------------------------------------|
| SUBROUTINE TEST14                                  |                                                                           |
| CALL VCAL                                          | (Invokes routine to calibrate sampling channels.)                         |
| CALL RSET                                          | (Resets all ADRA control registers.)                                      |
| 100 CALL ERAS(2)                                   | (Erases X-Y storage oscilloscope.)                                        |
| CALL STOR(2)                                       | (Sets X-Y oscilloscope in storage mode.)                                  |
| CALL NCSA(1,1)                                     | (Sets number of samples per dot equal to 1.)                              |
| CALL NPT(256,1)                                    | (Sets number of points per waveform equal to 256.)                        |
| CALL TMSL(10,1)                                    | (Specifies measurement interval number 10.)                               |
| CALL PC(1,00000,00001)                             | (Sets up pulse pattern on pulse input 1.)                                 |
| CALL DC(1,2)                                       | (Sets DC power supply 1 to nominal value.)                                |
| CALL DC(2,2)                                       | (Sets DC power supply 2 to nominal value.)                                |
| CALL LD(1,0)                                       | (Sets load 1 to 75 ohms.)                                                 |
| CALL LD(2,0)                                       | (Sets load 2 to 75 ohms.)                                                 |
| PAUSE                                              | (Pause to allow operator to ready camera.)                                |
| DO 10 M=1,2                                        | (DO to provide for two pictures.)                                         |
| DO 10 J=1,3                                        | (DO 10 J=1,3).....(DOs to provide indices for 27 pulse shapes.)           |
| DO 10 K=1,3                                        | (DO 10 K=1,3).....(DOs to provide indices for 27 pulse shapes.)           |
| IF (M.EQ.2.AND.1.EQ.1.AND.J.EQ.1.AND.K.EQ.1) PAUSE | (Pause between pictures.)                                                 |
| CALL SM(1,100+J*10+K)                              | (Sets up 27 input pulse shapes from indices.)                             |
| IF (M.EQ.2) GO TO 101                              | (Skip for second picture.)                                                |
| CALL MODE(12)                                      | (Sets measurement selector to monitor inputs.)                            |
| CALL GTDATA                                        | (Invokes routine to collect digitalized input.)                           |
| CALL DSPL(1)                                       | (Invokes routine to display digitalized input.)                           |
| IF (M.EQ.1) GO TO 10                               | (Skip for first picture.)                                                 |
| 101 CALL MODE(10)                                  | (Sets measurement selector to monitor outputs.)                           |
| CALL GTDATA                                        | (Invokes routine to collect digitalized outputs.)                         |
| CALL DSPL(1)                                       | (Invokes routine to display digitalized OR output.)                       |
| CALL DSPL(2)                                       | (Invokes routine to display digitalized NOR output.)                      |
| 10 CONTINUE                                        | (For all DOs.)                                                            |
| CALL MSG(1)                                        | (Invokes routine which allows operator to either repeat test or to exit.) |
| GO TO (100,99),N                                   |                                                                           |
| 99 RETURN                                          |                                                                           |
| END                                                |                                                                           |

The following specific conclusions and comments can be made at this time. The ADRA hardware design and program control are balanced; that is, no control sequence required in testing requires a disproportionate share of test time, despite the extensive use of relay switching. The pulse shaping, distribution, and monitoring used are internally consistent and can be extended to the subnanosecond region when faster sampling systems and programmable pulse generators become available.

The limits of system accuracy have not been established; however, sufficient data is available to state that a  $\pm 1\%$  measurement repeatability is routinely achieved.

The desirability of operating a data acquisition and control system directly from a general purpose time-shared system is confirmed. System features such as extensive programming libraries, large random access storage and files, and high performance processing capabilities are distinct advantages. In addition, the conversational mode of operation has high value for setting up and debugging new programs. To some extent these advantages are offset by a re-

duction in system response time due to the time share mode of operation.

Finally, the control and data acquisition capabilities of systems such as ADRA can be effectively used only when the experiments, or tests, are carefully designed.

## Appendix - Pulse shape control circuit (PSC)

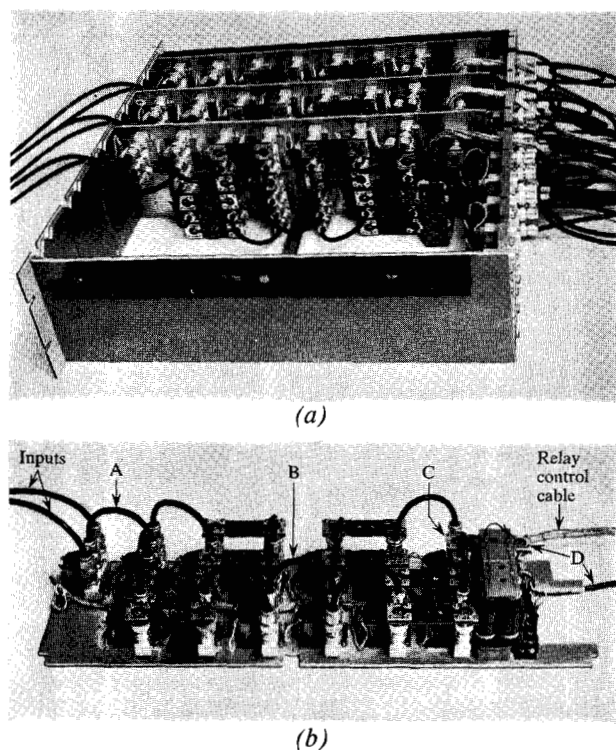
by P. E. Stuckert

### • Design

Figure A1a is a photograph of one of the two PSC chassis in ADRA. Each PSC channel (Fig. A1b) in the chassis provides the coaxial relay switching for the selection of circuits which determine input pulse polarity, rise time, and pulse up and down levels. The delay control relays for each channel are mounted on the back panel of the chassis, permitting installation of the delay cables outside the chassis.

Nine plug-in subassemblies of the types shown in Fig. A2 are included in each channel assembly. Four of these plug-ins (between points A and B in Fig. A1b) are rise time control circuits, four (between points B and C) are attenuator circuits, and the last (between points C and D) is the circuit which, when energized via relay switching of external power supplies, provides dc offset.

Figure A1 (a) PSC chassis for five channels (two channels removed.); (b) PSC channel.



Referring to the channel schematic (Fig. A3), one sees that operation is straightforward with propagation from left to right, the pulses being successively modified by the circuits which are inserted in the signal path by the coaxial relays as follows:

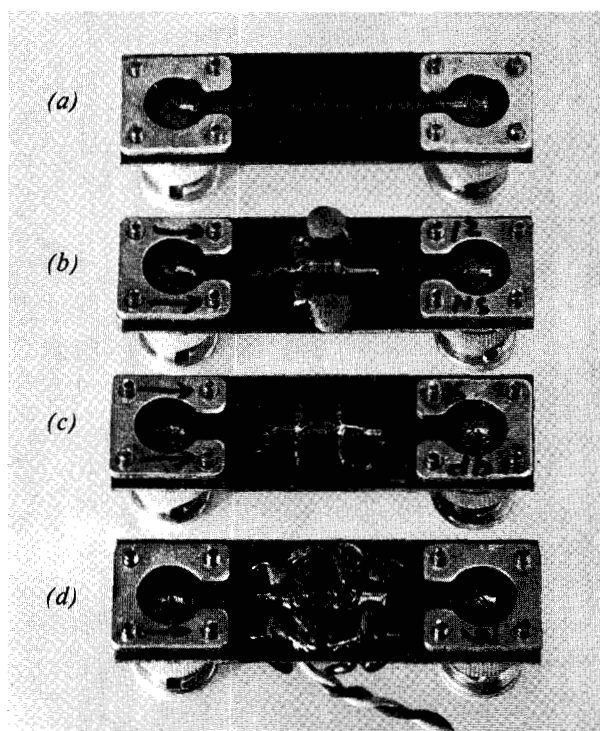
(1) Bursts of programmed pulse patterns from the pulse generator appear continuously at the two inputs. The position of the polarity relay delivers either positive or negative pulses to point A.

(2) The rise time relay trees insert one of the four predetermined rise time circuits in the signal path and deliver the pulses to point B. The rise-time circuit configuration used in ADRA is the same as that described by Franks.<sup>5</sup> Other types of passive rise-time circuits could, of course, be used.<sup>6,7</sup>

(3) The attenuation and dc offset sections, in combination, alter the pulses to the programmed up and down levels. Figure A4 shows the input reference pulse levels and the output pulses derived from each. This figure also shows that the four possible output amplitudes (calibrate, low, nominal, and high) require the same attenuations regardless of the input pulse polarity. The relay trees insert one of the four predetermined attenuations into the signal path and deliver the pulses to point C.

The design and operation of the dc offset circuit between points C and D in Fig. A3 is described elsewhere.<sup>8</sup> In the

Figure A2 Typical PSC plug-in subassemblies; (a) 50 ohm micro-strip line, (b) rise time circuit, (c) pi attenuator circuit, (d) dc offset circuit.



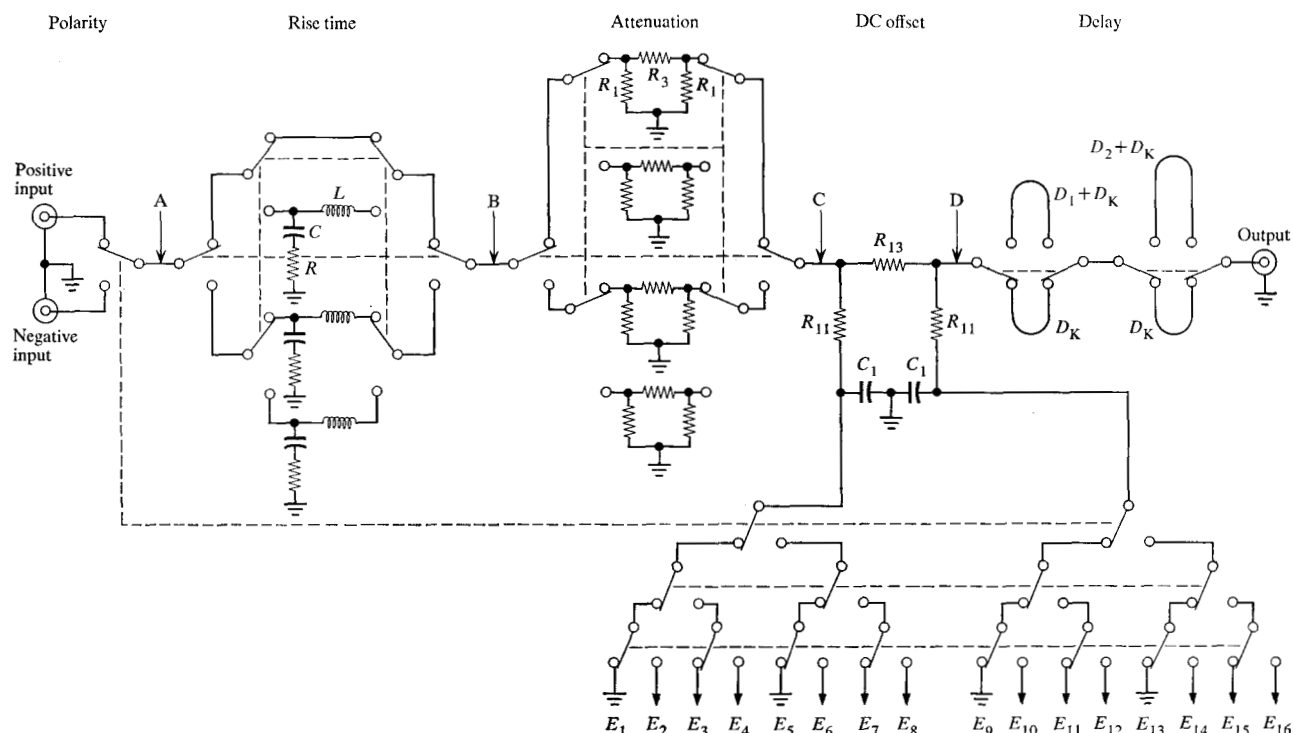


Figure A3 PSC channel circuit diagram.

Figure A4 PSC pulse levels; (a) input, (b) output.

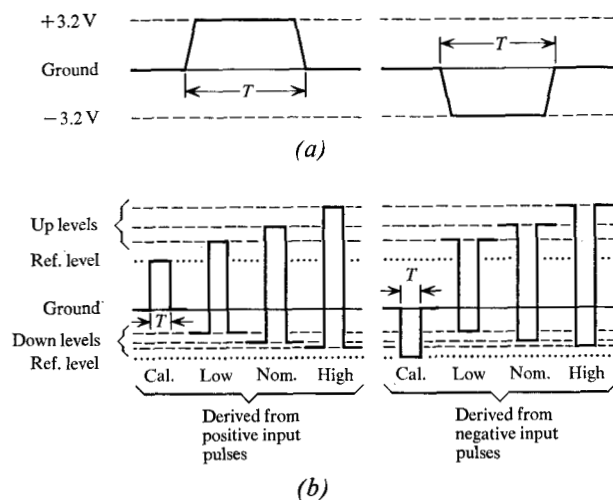


Table A1 Pulse parameter and control register summary.

| Pulse parameter          | Number of values allowed | Value designations    | Bits per PSC channel | 10 bit reg. req'd. for PSC |
|--------------------------|--------------------------|-----------------------|----------------------|----------------------------|
| Polarity <sup>a</sup>    | 2                        | pos., neg.            | 1                    | 1                          |
| Rise Time                | 4                        | cal., low, nom., high | 2                    | 2                          |
| Attenuation <sup>b</sup> | 4                        | cal., low, nom., high | 2                    | 2                          |
| Dc Offset <sup>a,b</sup> | 4                        | gnd., low, nom., high | 2                    | 2                          |
| Delay                    | 3                        | low, nom., high       | 2                    | 2                          |
| Total <sup>c</sup>       | 96                       |                       | 9                    | 9                          |

<sup>a</sup> Interlocked by hardware to permit 4 values of dc offset for each polarity and to prevent programming of prohibited polarity-offset combinations.

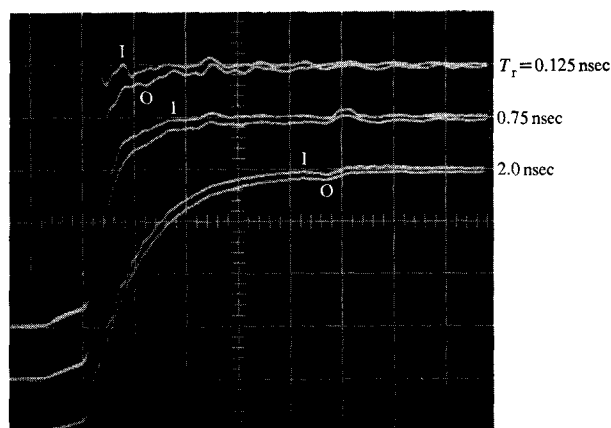
<sup>b</sup> Interlocked by software to permit 4 predetermined dc offset-attenuation pairs.

<sup>c</sup> Total = 4 (Rise Time) × 3 (Delay) × 2 (Polarity) × 4 (Attenuation and dc offset combined) = 96.

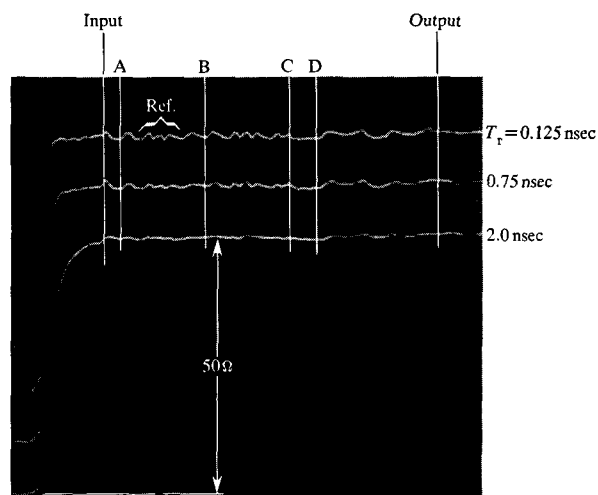
PSC the offset circuit is a modified 2:1 pi attenuator which offsets the baseline of the input pulses to predetermined levels as a function of the voltage pair ( $E_1$ - $E_9$ ,  $E_2$ - $E_{10}$  . . .  $E_8$ - $E_{16}$ ) selected by the external relay trees shown in Fig. A3. Parenthetically, it is not necessary that, as indicated in Fig. A4, ground be located between the up and down levels, since the magnitude and polarity of the dc offset is deter-

mined solely by the voltages applied to the offset circuit. (4) From point D the pulses proceed to the delay circuit where, as a function of programmed relay positions, one of three relative delays is inserted in the signal path.

Table A1 summarizes the allowed pulse parameter values and the number of control registers needed for actuating the relays in the PSC.



(a)



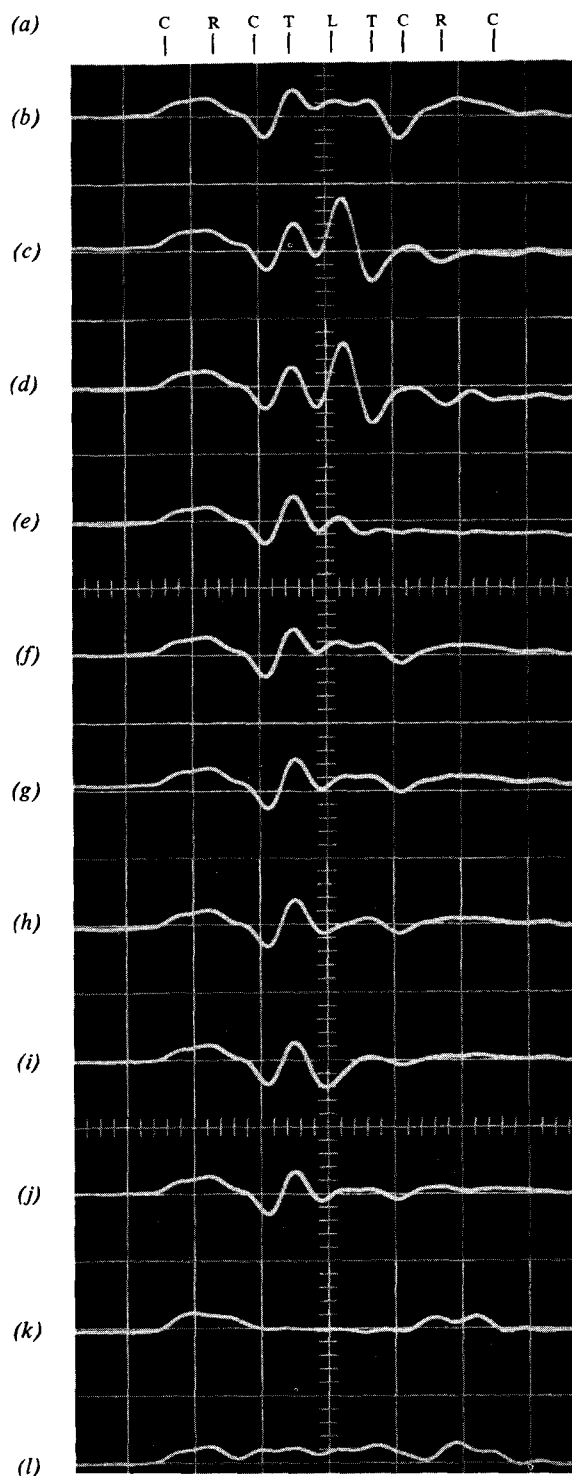
(b)

**Figure A5** (a) Superimposed PSC input and output waveforms at three values of rise time; horizontal sensitivity: 1 nsec/cm, vertical sensitivity: arbitrary; (b) PSC time domain reflectometer waveforms at three values of rise time; reflection coefficient: 0.2. Points A through D correspond to the same points identified in Figs. A1b and A3.

#### • Channel transmission characteristics

The transmission characteristics of the PSC channels were measured with all of the passive circuits in a signal path replaced by 50-ohm microstrip plug-ins of the type shown in Fig. A2a. With these plug-ins installed, a channel is a continuous 50-ohm system consisting of coaxial relays, connectors, coaxial transmission line, microstrip transmission line, and compensated coaxial to microstrip transitions. Two types of measurements were made: (a) comparison of input and output waveforms and, (b) observation of reflections with a time domain reflectometer.

Figure A5a shows superimposed input and output waveforms for a PSC channel at three values of rise time. The differences between the input and output waveforms are due to three effects: (a) the dc resistance of the channel,



**Figure A6** Time domain reflectometer waveforms for PSC plug-in units and reference circuits; (a) location of various parts of circuits: C = BNC connector pair, R = relay, T = coax to stripline transition, and L = stripline and passive circuit; (b) stripline (compare with Figure A5b); (c), (d), and (e), 8.5, 12.0, and 30.0 nsec rise time circuits; (f), (g), (h), and (i) 1.43:1, 1.54:1, 1.67:1, and 2.00:1 attenuators; (j) offset circuit; (k) and (l) for comparison only: plug-in circuit replaced by length of RG58A/U, and by BNC right angles and union, respectively. Horiz. sens.: 2 nsec/cm; refl. coeff.: 0.05;  $T_r$ : 0.125 nsec.

(b) series eddy current losses, and (c) attenuation of high frequency components.

The channel dc resistance of approximately 0.4 ohms produces the reduction in output amplitude which is present in all waveform pairs at the extreme right of Fig. A5a. This reduction is constant throughout the pulse duration and is compensated by a corresponding increase in the magnitudes of the input pulses.

Series eddy current losses produce the "dribble up" effect that is most noticeable in the upper waveform pair of Fig. A5a. This effect is present in all three output waveforms during the 2 to 3 nsec following the initial transition, distortion being significant at 0.125 nsec, moderate at 0.75, and almost negligible at 2.0 nsec rise time.

The loss of high frequency content parallels eddy current loss in its relative severity, but is almost negligible at 0.75 and 2.0 nsec rise times.

Figure A5b shows time domain reflectometer waveforms observed for the same three rise times used in Figure A5a. Reflections, of course, increase with a decrease in rise time, being small at 0.75 nsec and almost negligible at 2.0 nsec rise time.

#### • Plug-in unit characteristics

The quality of the passive plug-in units in the PSC was also evaluated by the observation of waveforms and by time domain reflectometry. Figure A6 shows reflectometer waveforms for a typical plug-in of each type installed in the PSC. In this figure the discontinuities are accentuated by the choice of reflectometer sensitivities and by the use of an incident step of 0.125 nsec rise time. For purposes of comparison it should be noted that the region indicated by "ref." in Fig. A5b, and Fig. A6b show the discontinuity due to the same plug-in. Figures A6b, k, and l, together, provide comparative references for Figs. A6c-j.

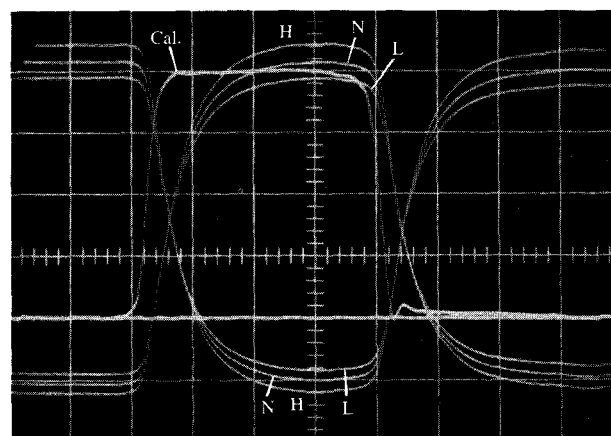
**Table A2** Pulse parameter set used in this paper. This set, except for levels, is identical to the set used in the logic circuit tests described in the companion paper by Maling and Schnurmann.<sup>1</sup> Here the up and down levels are altered to permit separation of all levels in an oscilloscope display.

| Pulse parameter | Programmable values    |          |           |                        |
|-----------------|------------------------|----------|-----------|------------------------|
|                 | Calibrate <sup>a</sup> | Low      | Nominal   | High                   |
| Rise time       | 2.0 nsec               | 8.5 nsec | 12.0 nsec | 30.0 nsec <sup>c</sup> |
| Up level        | +0.8V <sup>b</sup>     | +0.78V   | +0.83V    | +0.88V                 |
| Down level      | 0.0V <sup>b</sup>      | -0.24V   | -0.21V    | -0.18V                 |
| Delay           | 0.0 nsec               | 0.0 nsec | 1.5 ns    | 4.5 nsec               |
| Pulse width     | —                      | —        | 40 ns     | —                      |
| Pulse period    | —                      | —        | 100 ns    | —                      |

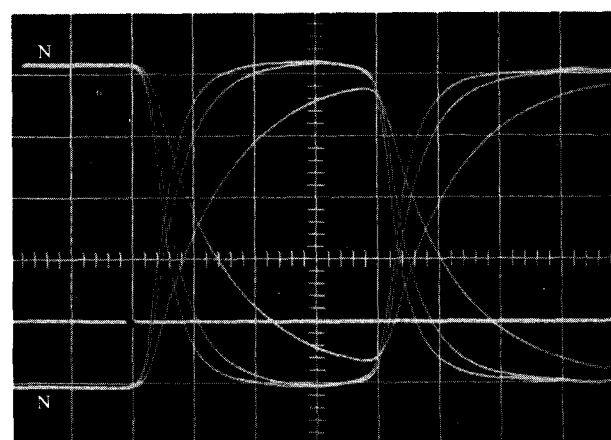
<sup>a</sup> For system calibration only; not used in logic tests.

<sup>b</sup> For positive calibration pulses.

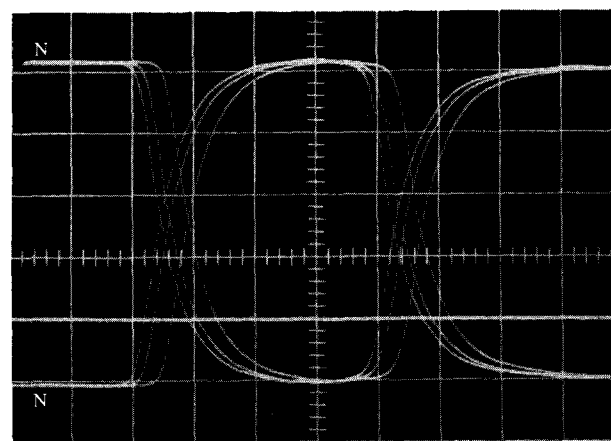
<sup>c</sup> With this rise time the pulse does not reach its quiescent level in 40 nsec. This was deemed desirable by the designers of the test.



(a)



(b)



(c)

**Figure A7** PSC output waveforms. Horizontal sensitivity: 10 nsec/cm; vertical sensitivity: 0.2 V/cm. (a) Nominal delay and rise time and low, nominal, and high amplitudes for both polarities; also a positive calibration pulse with zero offset, unmodified rise time, and low delay; (b) nominal delay and amplitude and low, nominal, and high rise time for both polarities; (c) nominal rise time and amplitude and low, nominal, and high delay for both polarities.

### • Conclusions

A total of 96 different waveforms, 48 each for positive and negative pulses, can be produced by a PSC channel. Of these a subset of 54 waveforms, 27 for each polarity, combining 3 values of rise time, 3 values of amplitude and offset combined, and 3 values of delay are useful in the evaluation of logic circuits. A smaller subset comprising one polarity, one (the unmodified) rise time, and 3 delays is used for system test and calibration. Figure A7 shows waveforms produced by a typical channel with the pulse parameter set given in Table A2.

### Acknowledgements

Adequate acknowledgement for a project such as ADRA is very difficult. We make a sincere attempt below.

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J. Cocke gave the ADRA project its original impetus and, together with R. E. Meagher, provided early technical counsel and established some of the basic principles on which the ADRA system design was based.

The data presented in the preceding sections demonstrate that the PSC is capable of shaping pulses from a source with 2 nsec rise time. Extension of the technique to the shaping of pulses from a 0.75 nsec rise time source would require only modest improvements in the circuitry and in the components used. A further extension to the shaping of pulses with even faster rise times would require significant improvements, with particular emphasis on the reduction of series eddy current losses and the reduction of discontinuities throughout the circuit.

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