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Design Considerations for the Chain Magnetic Storage Array

Abstract: A computer storage design using the chain store device as both a DRO and an NDRO storage element is discussed for an array organization of one megabit capacity and 500-nsec cycle time. The bit/sense system and schemes for minimizing the longitudinal fields inside the array during the "write" portion of the cycle are presented.

Noise due to difference in the information states of the device is studied experimentally and through evaluations of computer solutions of simulated bit/sense lines. The word-line characteristic impedance and its dependence on the magnetic behavior of the device during the "read" portion of the cycle and on the sending and receiving end terminations are examined with consideration given to long word lines. Sources of noise and bit-to-bit interaction are discussed and comparisons between calculated and experimental results obtained from a small model of the array are given.

Introduction

The chain store magnetic film element,[1] which was developed from the chain magnetic memory element,[2] is evaluated here on the basis of its actual collective performance in a typical DRO and NDRO storage system. The objective of this study was a large (10^6-bit) and fast (500-nsec) word-organized memory with diode selection, using the relatively large signal output and the high packaging density which are possible with this device.

This paper considers a possible packaging arrangement, the characteristics and problems of the bit/sense wiring scheme, and the transmission properties of the chain as a word line. Interaction and noise problems, as well as noise rejection means, are also discussed.

Memory package

Because copper chains are exposed to a plating bath on all surfaces, they must be self-supporting structures. To facilitate handling during etching and plating, 32 chains of 72 bits each are tied together with small tie-bars and treated as a batch (Ref. 1, Fig. 10a). In the designed memory package, these chains are inserted into a "nest" (Ref. 1, Fig. 10b), etched from 10-mil-thick copper-Mylar-copper laminate, which acts as support, protection, and word current return for the chain, and as a container for the selection diodes in strip form. The ends of the chains are welded to provided tabs in the nest and the tie-bars are then removed.

Sixty-four of these nests are stacked to form a module (Fig. 1), containing 2048 words of 72 bits each. Eight of these modules would be connected by a double bit/sense segment of 8192 bits each to form a 1.2×10^6-bit memory array. Chains on each plane are connected in pairs at one end with a common "return" which is vertically connected to the returns of adjacent planes to form a "gate slice" (Fig. 1). This gate slice has a minimum capacitance with respect to other memory parts since only its sides face other gate slices. The capacitance to all bit-sense wires in this segment is the largest portion of the gate capacitance.

The chains are word lines, and may be shorted to the returns since the delay time (2 nsec) is small compared to the designed word current rise time (20 nsec), resulting in a minimum need for selection circuitry, 1 diode per word. The selection matrix is square, 128 drivers $\times$ 128 gates. The 128 drivers supply two 16-diode strips in each of the 64 planes. The total of 16 gate slices per module multiplied by 8 modules yields 128 "gate drivers."

To simulate the array just described, a cross-section model was designed, built and tested. It consisted of two hand-wired modules, one of which contained chains with

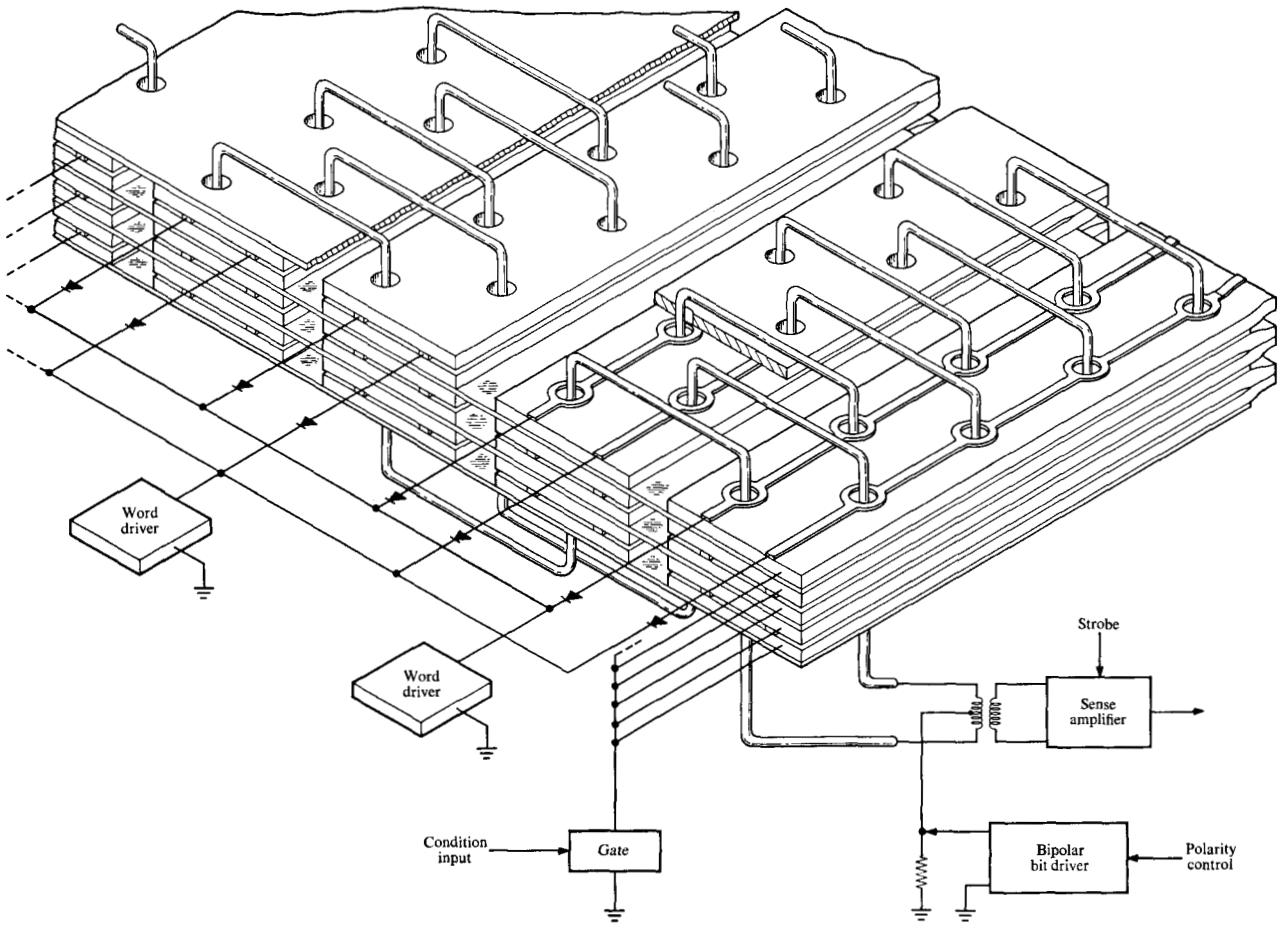


Figure 1 Array configuration.

36 bits per word (Fig. 2). Although few planes in the working module were operational, they were all populated with tested devices. All the bits were wired, including the dummy module, with connections brought out to allow several bit/sense winding schemes to be examined for intramodule and intermodule interactions.

Bit/sense system

The design objectives of the bit/sense system were to minimize interaction between the lines and to satisfy transmission requirements in terms of impedance, attenuation, delay, and bit noise. It was also necessary to minimize fields generated by the bit/sense wires along the chain (the longitudinal direction). A schematic of the system, shown in Fig. 3, consists of two common bit/sense lines, each linking n bits with a bipolar current driver at one end and a differential sense amplifier at the other end. A cross-section of the wiring pattern is shown in Fig. 4. The dimensions indicated in Fig. 4 were those used in the experimental model.

In the pattern shown in Fig. 4, called the alternating pattern, two features are to be noticed. First, along the bit line the current direction across the array stack alternates from chain to chain. This has the effect of reducing the longitudinal field generated by the total bit/sense system. It also reduces the self-inductance of the bit/sense lines. Second, the wiring pattern involves cross-over, so that two chains on a gate slice would consist of one chain linking line A and the other chain linking line B. The purpose is to cancel the gate noise components by making them of the common-mode type.

- *Bit/sense transmission*

A computer program was used to calculate the transmission line properties. The parameters were defined in terms of an equivalent circuit per unit bit section (the length of line between two adjacent planes) as shown in Fig. 5. The parallel network R_1L_1 was the linear model for chain loading. A spacing (Δx) of 10 mils between planes was used in the calculation. Other parameters were defined as:

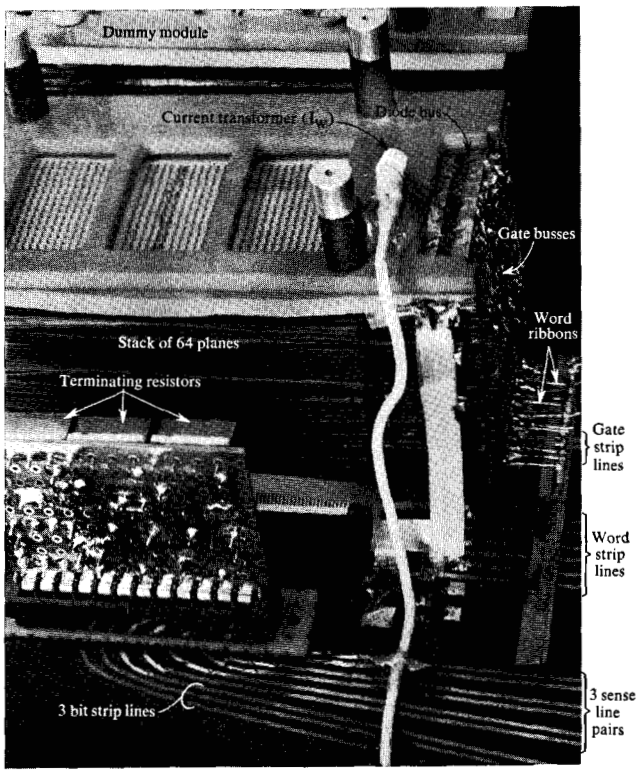


Figure 2 Test model.

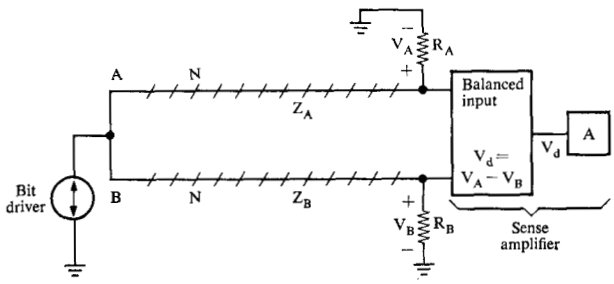


Figure 3 Bit/sense system schematic.

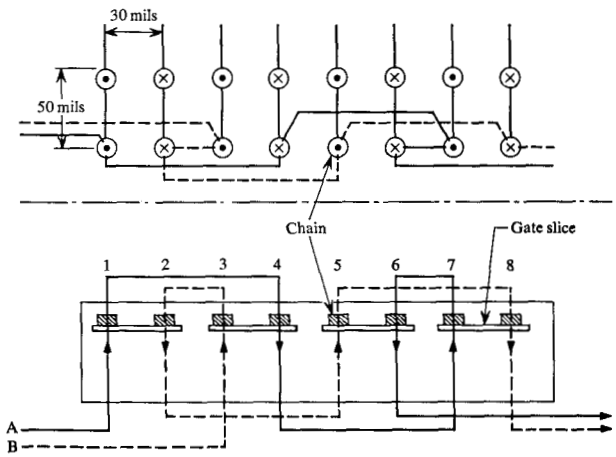


Figure 4 Alternate bit-wire pattern.

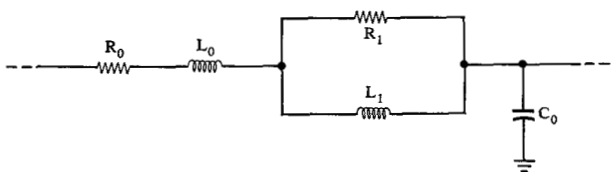


Figure 5 Bit/sense line equivalent circuit per bit.

1) R_0 – resistance of either line A or B (for #36 wire, $R_0 = 0.346 \times 10^{-3}$ Ω).

2) C_0 – capacitance between adjacent bit/sense lines as shown in Fig. 6. This capacitance is found by two intersection capacitances C_B in series. The value is 0.01 pF per plane.

3) L_0 – line inductance of line A or B. This is composed of three inductances:

(a) L_D – inductance of line A or B (the self-inductance of the line plus the mutual inductance resulting from the alternate wiring pattern with crossovers).
$L_D = 0.107$ nH/bit

(b) m – mutual inductance between lines A and B.
$m = 0.0122$ nH/bit.

(c) M – mutual inductance between line A or B and the rest of the bit lines in the array.

$M = \pm .0285$ nH/bit (36th bit of a 72-bit chain plane). The polarity of M is dependent upon the polarity of the bit current, and is also a function of the position in the array. The worst-case value is quoted here.

4) R_1, L_1 – the equivalent circuit values for the chains. They are obtained from a computer curve-fitting program, using as input the back voltages of chains disturbed by a bit current in the same (favorable disturbs) and opposite direction (unfavorable disturbs) as the bit current used in the previous write cycle. The data are:

Unfavorable disturb	*Favorable disturb*
$R_1 = 0.00845$ Ω	$R_1 = 0.0085$ Ω
$L_1 = 0.0435$ nH	$L_1 = 0.0311$ nH

Various transmission properties have been calculated. The results are:

1) $Z_0 = 110$ Ω ± 12%. The variation in Z_0 is due to coupling from the neighboring bits and the worst-case bit loading effect.
2) Delay, β, is 1.6 psec per bit.

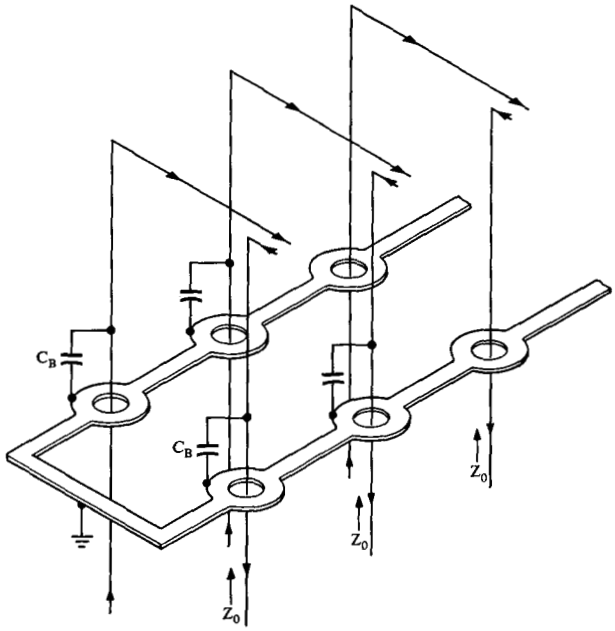


Figure 6 Bit/sense wiring details.

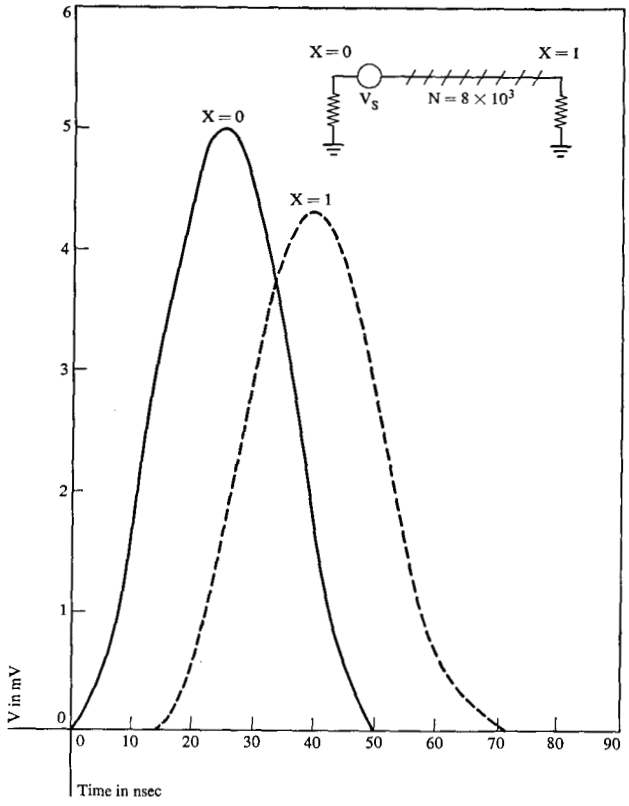


Figure 7 Sense signal transmission.

3) Fig. 7 shows the sense signal distortion for a bit segment of n = 8k bits, using #36 wire. The attenuation is about 13%.
4) Fig. 8 shows the noise recovery due to the bit current.

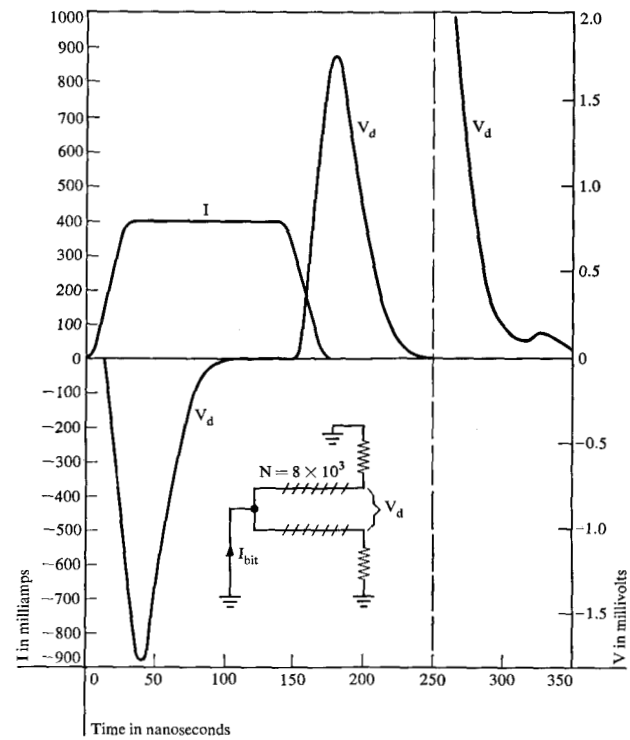
The experimental model was used to verify some of the calculated values. Because of the small size of the model, four parameters were investigated, M_{12} (mutual inductance between adjacent bit lines), C_B, Z_O, and β. All checked well with the calculated values.

• *Information noise*

In general, the impedances of line A and line B are not equal. One of the causes for their difference is that the bits linking them have unequal loading because of their differently magnetized states or because of the information stored. The resultant voltage is called information noise.

A special test jig was built to study this noise contribution. It was found that the worst-case pattern is one in which the two lines are uniformly stored but with oppositely magnetized information states. The peak difference voltage per bit was observed to be between 0.05 and 0.2 mV for I_B = 200 mA (20 nsec risetime). Tests also showed no clear correlation between the information noise voltage and the shape of the S-curves.[1] Thus, one might think of S-curve values as those reflecting the total or integrated effect of the different disturb pulses, since the values are taken after the disturb pulses are completed. On the other hand, the information noise is measured during the disturb and

Figure 8 Bit-voltage recovery.



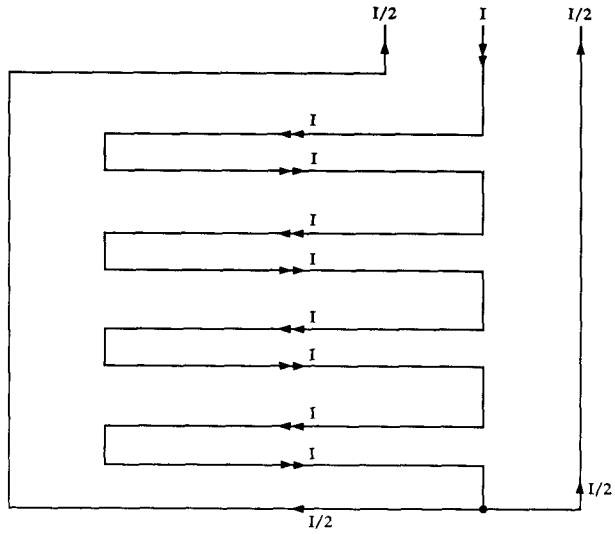


Figure 9 Split-return winding (cross section).

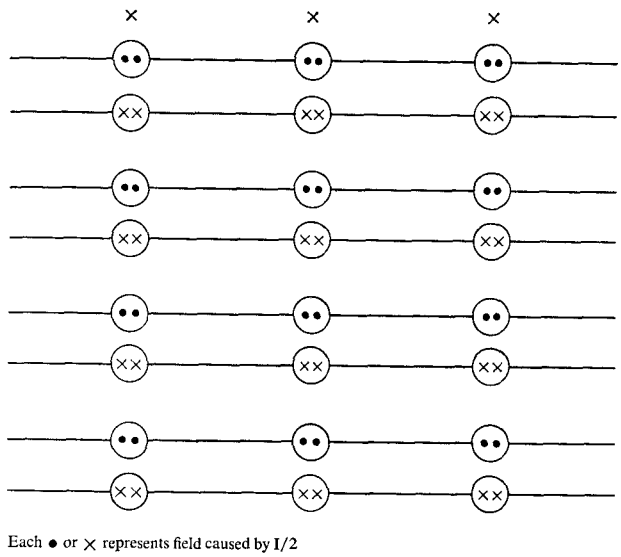


Figure 10 Split-return winding (planar view).

therefore is dependent on the dynamic behavior of the disturb process.

• *Longitudinal field (H_L)*

It was mentioned earlier with reference to Fig. 4 that the alternate wiring pattern reduces the field generated by the bit wire along the longitudinal direction. Detailed analysis shows that with a single return, in the array dimensions being considered, a longitudinal field of 2 Oe can be accumulated with a worst-case pattern in bit current polarities. In order to minimize this longitudinal field, a wiring scheme called split-return wiring was developed. Fig. 9 shows a cross-sectional view of the wires running through the array stack. Fig. 10 shows a planar view of all the currents in the bit wires having the same direction so that the resulting fields will be additive in the worst case. By assuming that the rows of currents form infinite current sheets, it is possible to show that the split-return winding establishes a boundary condition within which the longitudinal field is zero. For the practical dimensions involved, experimental results from the model show that a factor-of-5 reduction in H_L is achieved by this winding scheme as compared to one with only a single return wire.

• *Crossover scheme*

In the design of a large memory, the coupling between bit/sense lines must be minimized. Capacitive coupling is small in the chain array. To minimize net inductive coupling between bit/sense lines, a crossover scheme can be used; however, the use of an alternating winding pattern to reduce the longitudinal field precludes crossover within an array stack or module. Nevertheless, if a number of array blocks is used to constitute a large memory, crossovers can be introduced in the wiring between blocks. Fig. 11 shows an example using eight blocks. Each block is shown with four chain positions for simplicity. The crossover scheme minimizes coupling between any bit line and seven neighboring bits. For example, consider the current directions shown in segments of line 1 in Fig. 11. The polarity of the resultant voltages coupled in the neighboring bit-line segments are shown as positive (+) or negative (−). It can be seen that the sum of the coupled voltages over eight blocks is zero.

Word line

The word line can best be examined by considering it as a distributed-parameter transmission line. Each differential element of this transmission line consists of the inductance, capacitance, resistance, and leakage of the copper strip with respect to the gate return. In addition, the contribution of the deposited magnetic film manifests itself as a certain inductance and eddy-current resistance per bit as shown in Fig. 5.

The inductance of the magnetic film is caused by the change in flux from the easy direction of magnetization towards the hard direction as a result of word current flow along the chain. The inductance contribution of the magnetic material depends to a large extent on the magnitude of the word current. It is, furthermore, a function of time and hence exhibits significant nonlinear behavior. Under ideal conditions, the magnetic film should exhibit a constant inductance in the rotational mode of switching, which reduces to zero when the film is totally magnetized in the hard direction. However, due to eddy-current

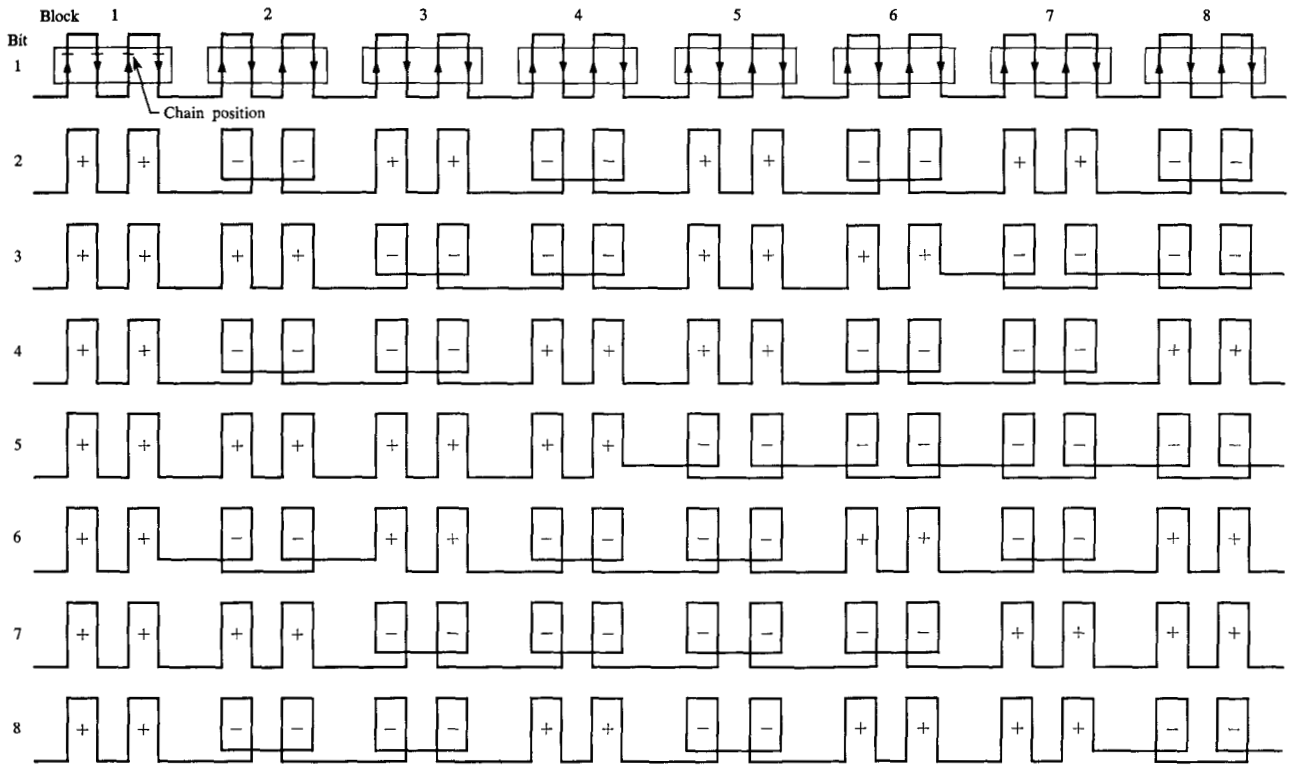


Figure 11 Crossover scheme for eight blocks.

losses, hysteresis losses, dispersion, and nonrotational modes of switching, especially in the branching areas, the inductance of the magnetic film will vary considerably during the switching interval. For this reason it is not possible to assign one value for the inductance, and one must resort to piece-wise linearization. To retain such useful parameters as the characteristic impedance and delay, one must employ some average inductance over the switching interval, which amounts to about 4 nH/bit.

For NDRO operation, the amplitude of the word current is small and the inductance of the chain device can be considered as constant and equal to about 6 nH. For DRO operation, the amplitude of the word current is high (in comparison) and the device is switched into the hard direction. After the switching interval is over, the inductive contribution of the device is considerably reduced. The other distributed parameters of the word line (as shown in Fig. 5), and especially the capacitance and inductance per bit, depend on the packaging scheme employed and on the proximity of the chain to the gate return. Calculations show the capacitance per bit, C_0, to be about 0.5 pF (including fringing effects) for a height of 2 mils above the ground return with Mylar as a dielectric. The air inductance per bit, L_0, is about 1 nH, which is smaller than the inductance of the film during switching, The resistance per bit, R_0, for the BeCu conductor is about 0.5×10^{-3} Ω. The attenuation due to the rise time loss is very small. These values are typical for Type E chains.[1]

For experimental verification of the word line characterization, a 288-bit chain of the E configuration was used. Difficulty was encountered when attempts were made to position the chain flatly and evenly along the gate return without straining the chain, so as to obtain the best value of capacitance that was theoretically possible. Typical values measured were lower than calculated (in the range of 90 to 100 pF) because the plane spacing was higher than nominal. The input impedance of the word line as a function of time for different terminating resistances is shown in Fig. 12. From this figure it can be seen that the input impedance is relatively independent of the termination for the first 15 nsec. This is to be expected since the input impedance will be equal to the characteristic impedance of the word line during that interval. The characteristic impedance ranges between 40 and 90 Ω.

One method of increasing the capacitance of the word line was to load it with discrete capacitors as shown in Fig. 13. The input impedance is shown in Fig. 14, and it can be seen that the range of variation has decreased considerably from that in Fig. 12.

In propagating the current pulse along the word line, the degradation of the rise time due to the different losses is of major interest, since the output signal at each bit

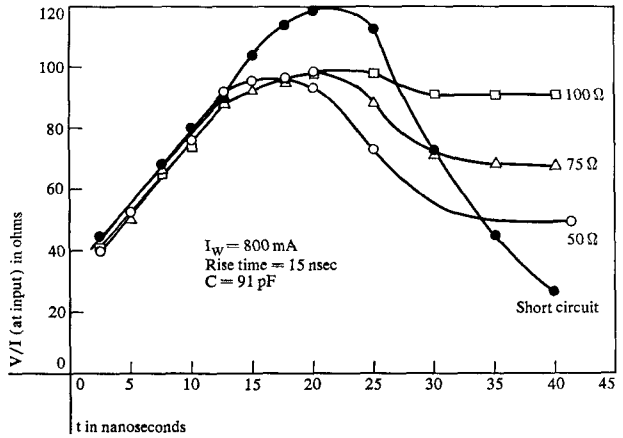
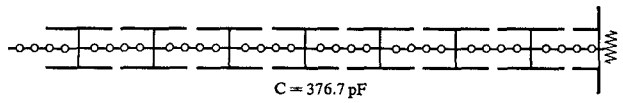


Figure 12 Input impedance of 288-bit word line.

Figure 13 Discrete capacitive loading along word line.



depends strongly upon the rate of change of current at that bit. The natural process is to degrade the rise time of the current pulse due to conductor, dielectric, and hysteresis losses. It has been observed, however, that because of the nonlinearity of the magnetic material, the degradation is counteracted, and a slight improvement in the rise time can be discerned in the 288-bit line. This phenomenon has been studied elsewhere.[3] This particular aspect of the word line behavior was confirmed by experimenting with a much longer word line (1380 bits, Type E configuration). In Fig. 15, the currents at both the sending and receiving ends are shown.

The explanation for this can be found in the difference in the propagation velocity of the front of the current wave as compared with the later portions where the film has already switched. The portion with faster propagation tends to compress the slower front portion and thus counteract rise-time degradation.

The termination of the word line is essentially determined by the delay along the line and the rise time of the word current pulse. For a long word line whose delay is twice the current rise time, it is preferable that the terminating resistance be equal to the average characteristic impedance. For shorter lines in which twice the delay is less than the rise time, it is better to short circuit the word line to the gate return. This is an advantageous arrangement when one considers the ease of packaging, the reduction of capacitive coupling, and the decrease in power dissipation and back voltage. In Fig. 16, the output voltage for 10 bits at the input of the word line with the word line short-circuited is compared with the voltage for the same 10 bits with the word line terminated by 50 Ω. The signal output is greater with the short-circuit termination because of the reflected current wave.

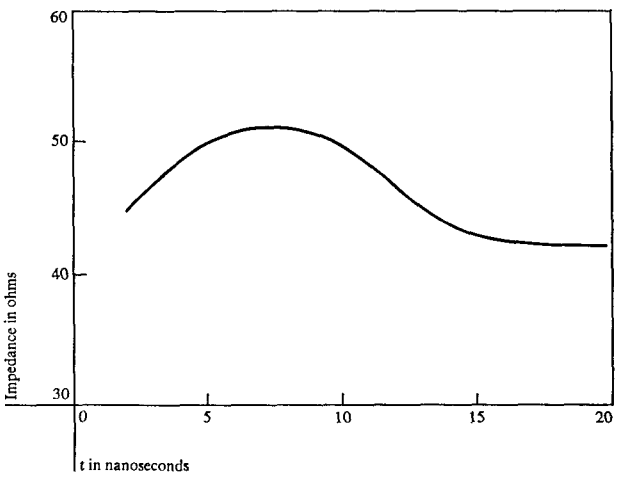
The choice of the diode selection scheme means that the selected word line will be capacitively loaded by the half-selected diodes along the driver. This can be considered as a lumped capacitance at the input of the word line and will somewhat degrade the rise time of the word current, reducing the signal output. This is a limiting factor in memory size, since this capacitance is directly related to the number of chains on a word line.

Chain array interactions

Bit-to-bit interaction on the same word line was investigated for all combinations of stored information in a "test" bit and on both sides of the "test" bit. Direct magnetic interaction between bits is not expected since there is no magnetic material between bits. Nevertheless, the effect of adjacent bit current fields and the possibility of magnetostatic coupling across the unplated area between adjacent bits were investigated. Interactions during precycling, writing, and disturbing were also investigated, but virtually none were observed.

Word-to-word interaction between adjacent words on 25-mil centers on the same gate, adjacent words on different gates, and adjacent words separated by a gate return were also investigated. Interactions were found to be negligible in every case. Field plots and relative magnitudes of the magnetic fields around a word line were determined using a resistive-paper analog mapping technique. Moreover, it was found that the closed flux and thick-film properties of chains tend to shield themselves from external stray fields.

Figure 14 Z at input as a function of time for a 10-nsec rise-time current pulse.



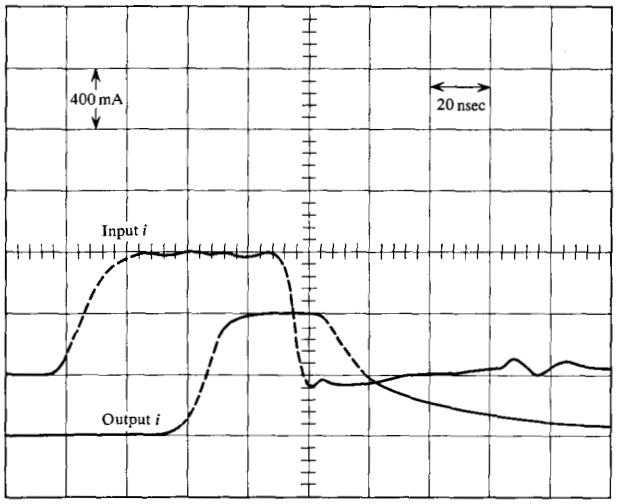


Figure 15 Input and output currents of 1380-bit transmission line.

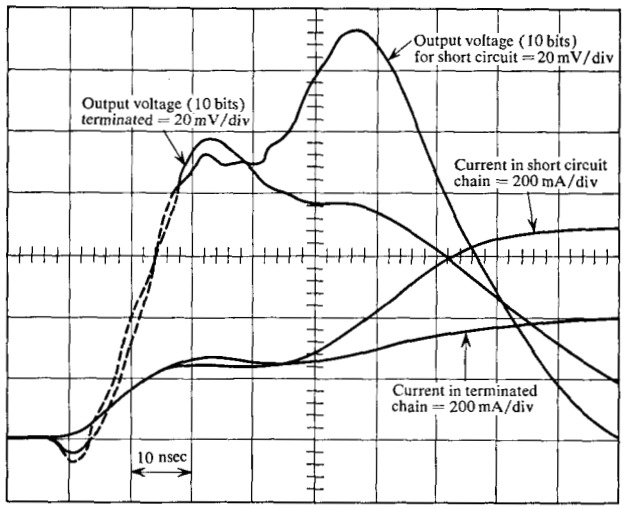


Figure 16 Output voltage for 50Ω termination and for short circuit.

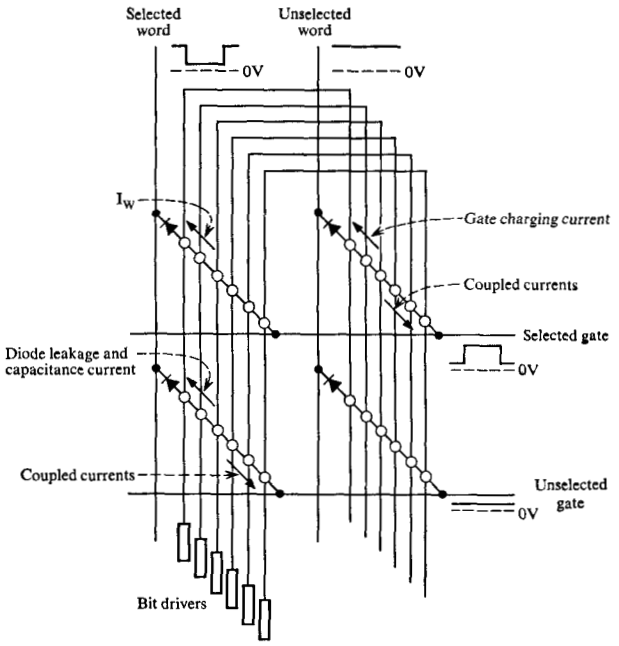
Noise analysis

Any charging current which passes through a chain will induce a voltage on the bit/sense line. Word disturb current components include the gate-charging current, current capacitively coupled from bit lines, and diode leakage currents (see Fig. 17). Word-to-word coupling is negligible.

In addition, noise can be capacitively coupled to the bit/sense line at the points where it intersects the chain and its return. This is because of the back voltage developed across the selected chain, voltage changes caused by word and word-disturb currents, and the finite impedance of the gate with respect to ground. Noise on the bit/sense line at read time may be itemized as follows:

a) capacitive (selected chain) noise
b) reflected gate noise
c) disturb current noise
d) inductive (stray field) noise
e) gate and write noise

Figure 17 Disturb currents.



• *Capacitive (selected chain) noise*

Selected chain noise is difference-mode noise, capacitively coupled to the sense line, and is caused by the back voltage across the chain,

$$V_n = \tfrac{1}{2}(C'_B/2)Z_{BS}L_c(d^2I_w/dt^2) \approx 1 \text{ mV},$$

where C'_B is the capacitance from bit-wire to chain, Z_{BS} is the characteristic impedance of the bit/sense line, L_c is the chain inductance and I_w is the word current.

Since C'_B is merely the inside-edge capacitance from one element to the wire, it is very small (typically 0.01pF). Therefore, the noise is very small compared with a sense signal of 10 mV. Higher-order capacitive noise due to indirect coupling, sneak paths, and disturb currents is also low.

• *Reflected gate noise*

In diode selection systems, the gated chains and their returns have a finite impedance with respect to ground. Thus, the word current causes a voltage change, which in turn creates a capacitive noise in all bit/sense lines. This noise appears in the array arrangement as common-mode noise on both segments of the bit/sense line and is rejected by the sense amplifier.

Table 1 Summary of array parameters and noise voltages

Parameter	*Calculated value*	*Experimental value*
C_D (nominal capacitance of reverse biased diode)	2 pF	2 pF
C_G (gate line capacitance)	17.2 pF/plane	22 pF/plane
C_B (capacitance between bit/sense line and chain plus return)	0.034 pF	0.4 pF
C_c (capacitance between bit/sense line and return line)	0.017 pF	0.02 pF
C_{cc} (capacitance between 2 chains on same return)	7 pF	Not measured
L_c (equivalent chain inductance 36 bits)	150 nH	150 nH measured on previous models
Z_{BS} (characteristic impedance of bit/sense line)	110 Ω	100 ohms

Noise parameter	*Mode*	*Calculated values*, mV	*Experimental value*, mV
Gate turn-on	Common	690.0	440
Gate turn-on	Difference	2.1	2.0
Selected chain	Difference	0.99	Not measured
Reflected gate	Common	67.0	200
Unselected (adjacent chain)	Difference	0.03	Not measured (using experimental parameters, recalculated value = 0.023 mV)
Unselected (adjacent chain) (NDRO)	Difference	0.1	Not measured
Word line (information) noise	Common	1.54	Not measured
Word line (information) noise	Difference	0.78	Not measured

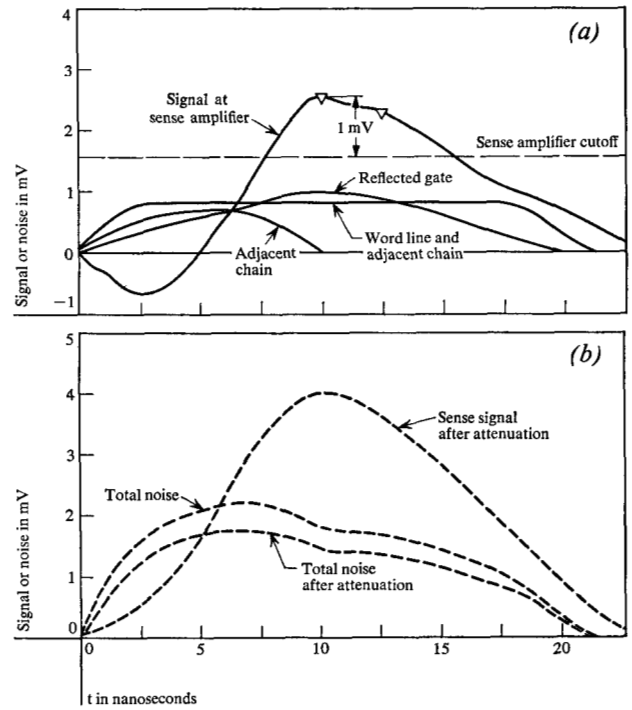


Figure 18 Noise waveforms assuming 800-bit-per-line (#36 wire) and device specification of 10 mV with $I_w = 700$ mA.

• *Disturb-current noise*

Disturb currents generate both inductive and capacitive noise at read time on each of the unselected lines on which they occur. Inductive noise is actually a nondestructive read-out of the information stored in each bit location. For a word disturb current of 2.5 mA with a rise time of 5 nsec, the inductive noise signal was found to be 0.03 mV per bit for the worst case. In general, this noise signal will assume a fairly complex wave shape. If propagation delay is neglected (i.e., if the bit line is short), the noise signal would be multiplied in the worst case by the number of back-biased diodes per selected word driver. Fortunately, when the bit line is long, only portions of the NDRO noise are additive.

• *Inductive (stray field) noise*

Minor deviations from orthogonality between the bit wires and the word lines do not result in a detectable noise.

• *Gate and write noise*

The most significant noise is read noise, since it is concurrent with the signal. In addition, gate and write noise caused by the turn-on of the gate and the bit drivers must be considered in the design of a sense system. This noise is common-mode and is adequately handled by the common-mode rejection of the sense amplifier. The information dependency of the differential write noise has been discussed in an earlier section.

The values of array parameters and noise sources derived in this section are summarized in Table 1 and have been added graphically to the sense signal in Fig. 18.

Conclusions

It has been shown that high-speed chain memories can be built in very high-density arrays with minimum electromagnetic interactions. The bit/sense wires can be treated as homogeneous transmission lines with relatively high characteristic impedance (100 Ω) and good signal-to-noise ratios. The word lines are high-impedance strip lines whose inductance is mainly determined by the nonlinear magnetic film. This makes evaluation more difficult, but implies favorable properties for the design of very long lines.

Based on the analysis of recently plated chains with smaller dimensions and better films,[1] the characteristics of various possible chain memories have been extrapolated. Straightforward design philosophy, using transistor selection can be applied for a 0.3×10^6-bit NDRO memory, a 10^6-bit, 100-nsec DRO memory, and a 38×10^6-bit, 500-nsec DRO memory.

These performance predictions reflect the merits of a film device with complete flux closure and high-quality oriented films as exhibited in the chain device; they appear quite attractive for their size, speed, and circuitry requirements. Chains imply a simple semi-batch process and combine fast rotational switching properties of oriented films with the larger signal capability of cores.

In contrast to the optimistic evaluation and projection concerning the device and array properties, a considerable amount of development work is still required to establish the handling, assembly, and packaging techniques. Further development in this area would provide a more complete assessment of this technology as compared with fully batch-fabricated film memories and the well-established ferrite core storage.

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