

G. Kohn
W. Jutzi
Th. Mohr
D. Seitzer

A Very-High-Speed, Nondestructive-Read Magnetic Film Memory

Abstract: A very-high-speed thin magnetic film memory has been designed and built as a cross sectional test model for 140 000 bits. It can be operated in the NDRO mode with a 20-nsec read cycle time and a 30-nsec access time, and it can be read 65 nsec after the beginning of a write operation.

Introduction

It is well known that thin magnetic films can be used as storage elements with a switching time down to 1 nsec,¹ and a number of proposals for film memories have been made in the past.²⁻⁴ The results reported, however, show that there is a big gap between the element switching time and the memory speed, which is in the 100-nsec region (as fast as 60 nsec for small memories⁵).

This large gap is only partly due to the spatial extension of a memory array with its unavoidable delays. It is mainly due to the big drive currents and the weak signals which require several orders of magnitude in gain. The delays in the circuits and their recovery time, therefore, determine the speed to a great extent.

With nondestructive-read memory elements, the rewrite loop can be omitted and the speed can be much increased, at least for the most frequently occurring read operation.⁶ In the following, the design of a thin magnetic film memory will be described. It employs eddy-current braked, NDRO memory elements,^{7,8} an array consisting of laminated and evaporated striplines, and very high-speed circuits. The experimental results reported demonstrate that a 140,000-bit NDRO memory with a 20-nsec read cycle time and 65-nsec writing time can be built.

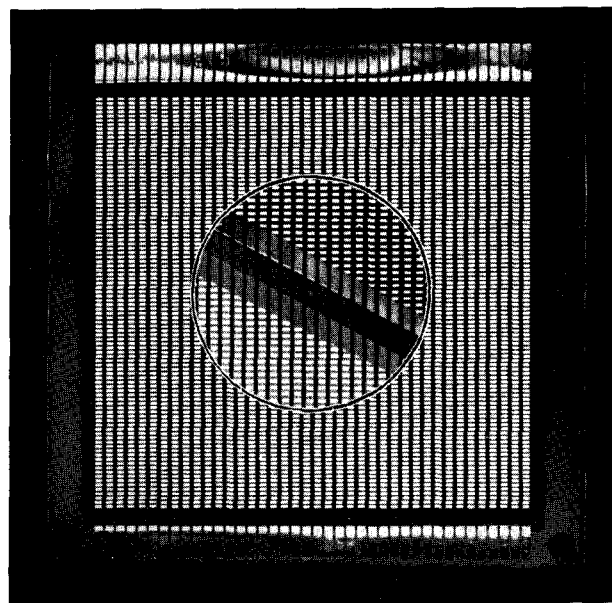
NDRO memory element

The memory element, Figs. 1 and 2, consists essentially of two NiFe films, which are antiparallel-coupled in the easy axis direction.⁹ Eddy currents in the nearby conductors are employed for nondestructive read operation.^{7,10}

The memory plane, Figs. 1 and 2, is built up on a silver-copper alloy substrate, 5 cm $\times$ 5 cm in size, by vacuum

deposition (10^{-5} mm Hg). Three successive pumpdowns are used to etch the first NiFe film into a pattern of rectangular spots (0.3 mm $\times$ 0.65 mm), the copper film into a digit line pattern, and the second NiFe film into a second pattern of congruent rectangular spots. All layers must be in good registration. SiO films are deposited as insulating

Figure 1 Memory plate with two congruent patterns of $96 \times 40 = 3840$ rectangular magnetic films $300\mu \times 650\mu$ and evaporated copper striplines between the film layers. Center-to-center spacings are 400μ and 1000μ , respectively. The plate size is 5 cm $\times$ 5 cm.



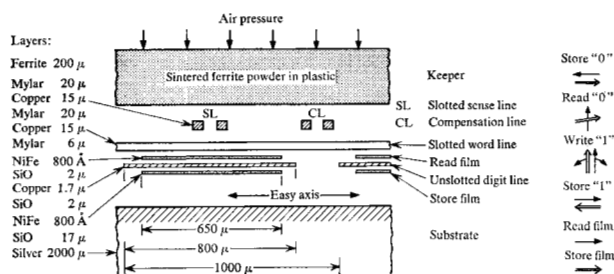


Figure 2 Cross section through the memory element with typical geometrical dimensions. The mode of operation is indicated schematically.

layers and for smoothing, to confirm reproducible preparation of the magnetic films. Very thin ($<100 \text{ \AA}$) chromium films between metal and oxide layers improve adhesion.

The magnetostatic parameters of both NiFe films are identical: $H_c = 2.6 \text{ Oe}$, $H_k = 6 \text{ Oe}$, and skew and dispersion are $\pm 1.5^\circ$. These average values have been measured with a magneto-optical Kerr apparatus. The memory plates can be prepared within $\pm 10\%$ for H_c and H_k , and the maximum values for skew plus dispersion do not exceed 2.5° . The word, sense and compensation lines are laminated on Mylar foils in a conventional manner.

The mode of operation will now be described. To store digital information, the two films are in one or the other of the two possible equilibrium states where the magnetizations are antiparallel in the easy direction. The magnetic flux is closed within the films, which leads to excellent stability against demagnetization. The closing flux penetrates the unslotted digit line.

To read the stored information, a word field perpendicular to the easy axis must be applied. The magnetization of both films tends to align with it. The magnetization rotation of the lower film, which is imbedded between the metallic substrate and the unslotted digit line, is retarded by eddy currents in these conductors. The thickness and separation of the digit lines determines the duration of this eddy-current "braking," which is chosen to be longer than the reading word pulse. This means that at the end of a sufficiently short word pulse, the lower film magnetization has been rotated out of its original position by only a small angle. This lower film is called the store film. The magnetization of the upper film rotates quickly, i.e. within the risetime of the word pulse, into the hard direction, thereby inducing a voltage in the sense line. This film is called the read film. Fast rotation is possible because the word and sense lines are slotted and the read film is therefore prevented from being eddy-current braked. After the word pulse, the magnetic stray field of the store film forces the read film back into its original position; the read operation is therefore nondestructive.

The word pulse for write is so large and so long that eddy-current braking of the store film is surmounted and its

magnetization can be rotated nearly to the hard direction. The digit field coincident with the trailing edge of the word pulse forces the store film into the desired position. The read film enters the antiparallel position.

Every digit pulse is preceded by a pulse having the same shape but opposite polarity. These bipolar digit pulses, Fig. 9, tend to reduce creeping because domain wall motion initiated by the first part of the pulse is essentially cancelled by the second part of the pulse. A further advantage of bipolar digit pulses is the avoidance of pumped-up currents in the metallic ground-plate, especially for high-speed memory operation.

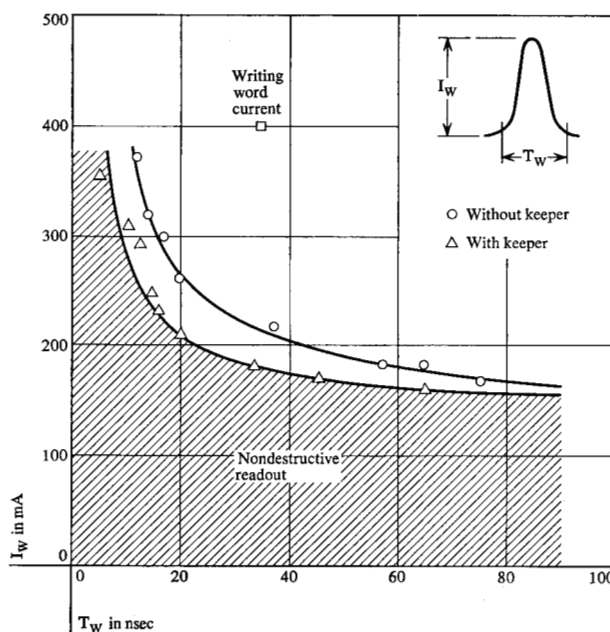
The keeper, Fig. 2, is a soft magnetic material with a permeability of about 10. It reduces the word currents required for achieving the necessary fields and therefore improves the sense-signal/drive-current ratio.

Some experimental results demonstrate the properties of this memory element. Figure 3 shows the critical word pulse width T_w and amplitude I_w up to which the memory element can be read out nondestructively. More than 10^9 read operations have been found to have negligible influence on the stored information.

The memory element has been subjected to a disturb program which simulates actual memory conditions with three adjacent word and digit lines.

For example, the memory element under test is magnetized in the "0" direction by 10^3 prewrite operations. After these, a "1" is written in. This 1 is then disturbed $10^4 \dots 10^8$ times by writing a 0 into the adjacent cells with digit

Figure 3 Measured critical NDRO curve, Word pulses with amplitude I_w and width T_w in the shaded area do not destroy the stored information. The writing word current is also indicated.



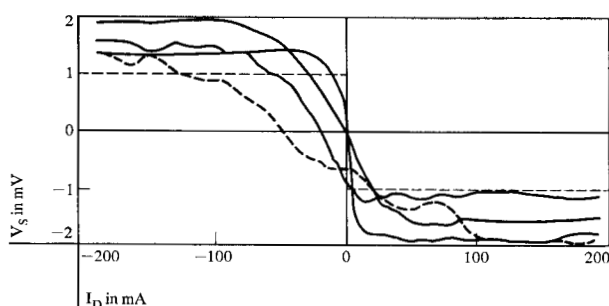


Figure 4 Sense signal after a disturb program, vs. the used digit current. Voltage measured at the output of terminated sense lines.

currents having 1.4 times the nominal amplitude. The bipolar digit current consists of two adjacent pulses of equal amplitudes and opposite polarity as shown in Fig. 9.

After this, the stored 1 is read out. The signal amplitude is recorded as a function of the writing digit current. Figure 4 shows the result for various memory elements, one near the edge, another near the center, and a third between them. The coupled-film NDRO element operated with bipolar digit pulses shows excellent stability.

If the influence of preceding write operations is taken into account by an even more sophisticated disturb program,¹¹ the dashed curve results, representing the worst case. It follows that the memory element can be operated in all these cases with 150 mA of digit current and a 1 mV signal.

Normally, large unipolar digit pulses disturb the stored information and even cause reverse signal polarity. This is not the case with bipolar digit pulses within the measured range of Fig. 4.

Stripline array

For close film coupling, the memory element requires an evaporated digit line insulated by thin evaporated SiO layers. Therefore, the digit line has a small characteristic impedance of about 5Ω , and a series resistance of $0.12\Omega/\text{cm}$. This results in a relatively large attenuation. It demands that no more than three memory plates be connected in series in the digit direction if the maximum tolerable digit current attenuation is to be 3 db. Such a 15 cm-long digit line covers more than 256 word lines.

The word line has a characteristic impedance of 35Ω and a total series resistance at low frequencies of 7Ω . The resulting attenuation of 1–2 db does not determine the maximum length of the wordline. This is done instead by the word pulse rise time deterioration. If a sense signal of $1\text{ mV} \pm 10\%$ is required, and if half of its margin is allowed for the word pulse rise time, this rise time should be within 2.3–2.5 nsec. The maximum word line length can

then be 40 cm. This word line covers 8 memory plates, and this means, with the packing density indicated by Fig. 1, that a word length of 288 bits can be achieved.

Two arrays are used for noise compensation, as shown in Fig. 5. Such a basic memory module then has a storage capacity of

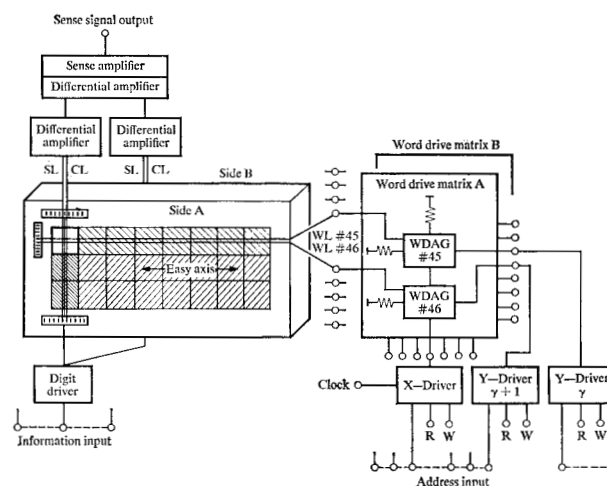
$$2 \times 256 \text{ words} \times 288 \text{ bits} = 147,456 \text{ bits},$$

and a megabit memory can be built up with eight such modules.

Noise compensation is very important. The word noise generated by direct capacitive coupling of word and sense lines is cancelled by an identical coupling of the word line with a compensation line, Fig. 1, and by separating noise and signal in a differential amplifier, Fig. 5.

Digit noise is generated by the strong coupling of digit and sense lines which are parallel throughout the whole memory. The digit noise has large, short pulses which can saturate the sense amplifier, and a long trailing edge due to current spreading in the groundplate. The short noise peaks can be reduced at the sense amplifier input by utilizing directional coupling¹²; the remaining part considerably influences the sense amplifier design. The length of the trailing edge determines the time after the write operation during which no signal can be detected. This recovery time has been considerably reduced by using bipolar digit pulses. However, an additional reduction of the digit noise was still necessary. Two symmetrical memory planes are arranged to have nearly identical digit currents simultaneously on sides A and B (see Fig. 5). The remaining common-mode digit noise is rejected in a differential sense amplifier. The simultaneous application of all the described noise compensation methods finally allows the high speed operation.

Figure 5 Cross sectional test memory model.



Circuits

Drivers and sense amplifiers for magnetic film memories must be designed according to certain basic criteria. Due to the large drive currents (≈ 500 mA) and the weak signals (≈ 1 mV/20 μ A), the circuits must provide about four orders of magnitude in gain to match the magnetic properties of the storage element to the logic circuits of the computer. The risetime of the drive pulses must be < 5 nsec to achieve reasonable sense signals. Therefore, the first criterion is a *maximum gain-bandwidth product*. For optimum compatibility with integrated circuits, mainly transistors and resistors should be employed, while tunnel diodes,¹⁸ transformers, etc. should be avoided. Further, parameter deviations should have small influence on performance and individual adjustments should be unnecessary. These requirements can be met most appropriately by negative feedback and impedance mismatch in transistor amplifiers.¹³⁻¹⁵ The next criterion is *minimum propagation delay* for fast access time, which means that the transistors must be operated in their active region and not be driven into saturation or cut off. This is in contradiction to the requirement for having minimum standby power and a compromise has to be made. High-speed memory operation means high pulse repetition rates up to 50 Mc/sec. Achieving this, the drivers must be decoupled to avoid level shift and they must be carefully designed with respect to heat dissipation.

All circuits have been designed according to these general criteria. The word selection and drive circuits as well as the sense amplifiers will now be discussed in more detail.

The word selection and drive circuits select one out of n word lines and provide drive currents with suitable risetime, width and amplitude at a minimum delay. These requirements would best have been met by individual drivers for each word line. The costs, however, would then be very high. That implies a "tradeoff" between minimum delay and minimum cost. Figure 5 shows a block diagram of the system used as a good compromise.

The word driver is subdivided into an X-driver, a Y-driver, and a word driver AND gate (WDAG, Fig. 6), which is at the crosspoint of the XY-selection matrix. The WDAG drives the word line with the necessary large currents at the coincidence of low current pulses on the X- and Y-lines. The word lines are terminated at their far end with resistors, which are evaporated on silver plates for good heat dissipation.

Both the X- and Y-drivers contain a read/write switch, single-shot circuits for determining the pulse width, and an amplifier similar to that within the WDAG. For addressing, the Y-driver output pulse removes the reverse bias from the emitters of all the WDAG's on the Y matrix line. Propagation delay in the matrix lines and within the drivers, and the variation of this delay, require overlap; i.e. the Y-pulses need to be longer than the X-pulses.

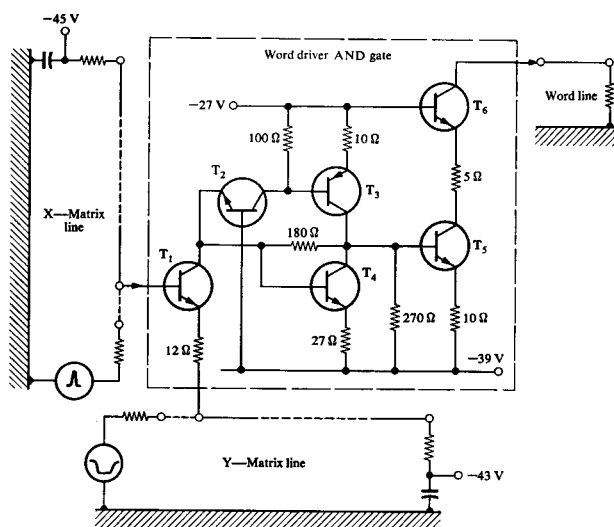
The X-driver provides pulses of different amplitude and width for read and write.

The word drive matrix consists of a multilayer circuit board including planes for the supply voltages. Both the X and Y matrix lines are terminated. Due to capacitive loading by the matrix transistors, the characteristic impedance of the lines is decreased and the propagation delay increased.

It is the major feature of the WDAG, Fig. 6, to match the gain/bandwidth performance of available high-current transistors to the matrix line impedances and the amount of feedback required, and furthermore to keep the capacitive loading of the matrix lines low, even at high output currents.

Other features of the WDAG should be noted: The circuit is direct-coupled, thus avoiding pulse pattern sensitivity. It has negligible stand-by power, it yields both fast leading edges and fast trailing edges which can be controlled independently, and it is compatible with integrated circuit technology. The basic part is a parallel feedback pair T_2, T_3 . Its high loop gain for large bandwidth is ensured by its high source and load impedances. In addition to the AND function, transistor T_1 provides an impedance conversion from the low-impedance matrix drive lines to the current-source type of impedance required for driving the feedback pair T_2, T_3 . T_5 provides current gain and drives the common-base output transistor T_6 . Using T_6 reduces drastically the effect of the Miller capacitance of T_5 . The second output transistor T_6 increases the output voltage available due to its higher collector-to-base breakdown voltage. It also reduces the heat dissipation of T_5 . Without any stand-by current, the trailing edge transients

Figure 6 Circuit of Word Driver AND Gate.



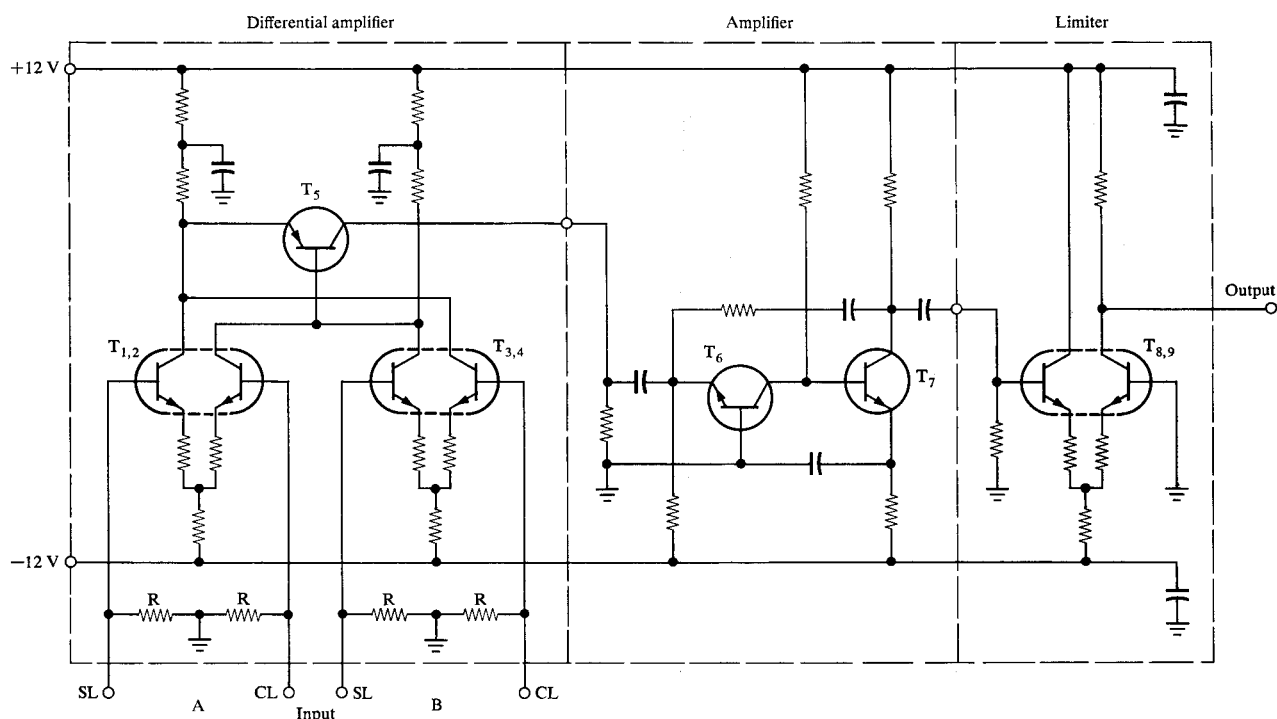


Figure 7 Sense preamplifier circuit.

would be very long. For this reason, transistor T_4 is introduced, which turns on during the trailing edge and makes it fast. Zero stand-by current means increased propagation delay. However, this disadvantage weighs little in comparison to the advantages of bias stability and negligible stand-by power dissipation.

Some of the experimental results achieved with these selection circuits are shown in Figs. 8 and 9; a summary is given in Table 1. In the final experiments with the memory model (Figs. 8, 9), it turned out that the magnetic elements could be operated with somewhat smaller currents, so this table describes the maximum values of which the circuits are capable.¹⁰

The sense amplifier consists of a double differential amplifier for noise rejection, feedback amplifier stages with a high gain-bandwidth product, and digit noise limiters. In Fig. 7 the preamplifier is shown. The experimental results, Fig. 8, are measured at its output terminals.

Sense and compensation lines are terminated with resistors R . At this point, the sense signal is 1 mV; the common mode read noise signal is 2–3 mV. The first differential amplifier rejects this common mode noise. The digit noise during the write operation amounts to about 100 mV with approximately the same waveforms at inputs A and B (Figs. 5, 7) on both sides of the symmetrical memory plate. It is partially cancelled in the differential amplifier transistor T_5 . The remaining peaks due to asymmetry are limited in T_8 and T_9 , thus preventing the succeeding stages from being saturated. The transistors T_6 and

T_7 continue to operate in their active region during noise peaks. They provide the necessary gain as a parallel feedback pair. Level shift in the RC-coupled sense amplifier is kept to a minimum due to the bipolar digit noise. This sense preamplifier has a signal voltage gain of 18. The total sense amplifier, having one amplifier and one limiter stage in addition, has a gain of 70, a bandwidth of 140 Mc/sec and a total delay of 5 nsec.

The digit driver uses a step recovery diode for converting a unipolar pulse into the required bipolar pulse.¹⁷ The rest of the circuit is very similar to the word driver circuit. Appropriate symmetry of the digit currents on both sides of the memory is ensured by driving each digit line with a feedback-controlled current source. The total width of a digit pulse, Fig. 9, is 40 nsec, its amplitude is ± 150 mA, and its transition time is 5 nsec.

Experimental results

A cross sectional test model of a 140,000-bit NDRO memory according to the block diagram, Fig. 5, has been built and is shown in Fig. 10. It is populated by 6 out of 48 of the memory plates of Fig. 1. By mechanically changing the position of the circuits, any arbitrary memory cell out of 5000 on two plates at the far end of the word lines can be tested at high speed. The selection matrix has 64 outputs; tests can be made with any two of them. The results reported refer to word lines 45 and 46.

Table 1 Selection circuit characteristics.

	Output amplitude, mA	Risetime, nsec	Pulse width, nsec	Address input pulses to X- and Y-drivers	Load impedance, ohms	Total delay from clock-input X-driver to word line input, nsec
Read	250	2-2.5	5-6	1 V/20 mA	50	20
Write	500	4	25			

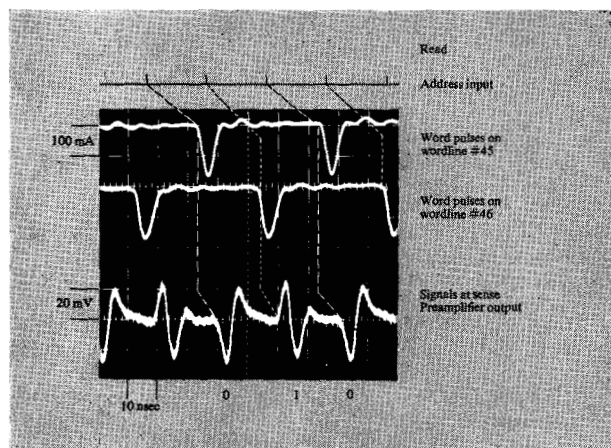


Figure 8 Oscilloscope traces of the read operation.

The first experiment shows the performance of the read operation. The memory can be read out nondestructively as many times as desired. The maximum repetition rate is 50 Mc/sec when reading one word or any two randomly accessed words alternately. This can be seen from Fig. 8, which also shows the sense signals. In word 45 a "0" and in word 46 a "1" have been stored, respectively, in this special case. The access time between address input and sense preamplifier output is 25-30 nsec.

The second experiment demonstrates that the write operation can also be very fast. A write-read program on word lines 45 and 46 has been run. The first oscillogram of Fig. 9 shows the large write and the small read word pulses; the second one shows the bipolar digit pulses in correct timing. The first oscillogram, taken from the signal at the sense preamplifier output, shows the remaining

Figure 9 Oscilloscope traces for a write-read program.

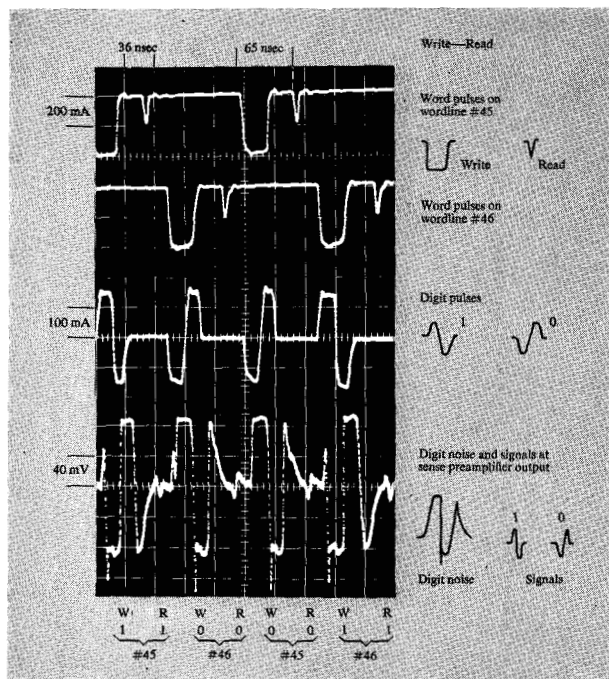
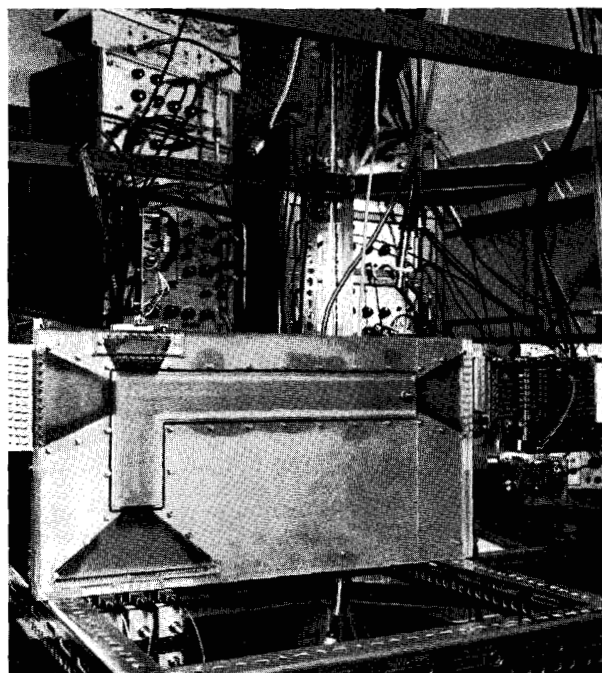


Figure 10 Experimental setup of memory model.



digit noise peaks and between them the signals before being outstrobed. The essential result is that 65 nsec after the beginning of a write operation, the read operation can be started.

Conclusions

It has been demonstrated that a 140,000 bit magnetic film memory can be built, which can be read out nondestructively with a 20-nsec read cycle time and a 30-nsec access time, and which requires 65 nsec for the write operation.

Acknowledgements

The authors gratefully acknowledge the excellent technical work of Messrs. H. P. Gschwind, R. Lüscher, G. Sasso and K. Schwarz.

References

1. W. Dietrich, W. E. Proebster and P. Wolf, "Nanosecond Switching in Thin Magnetic Films," *IBM Journal* 4, 189 (1960).
2. J. I. Raffel et al., "Magnetic Film Memory Design," *Proc. IEEE* 52, 875 (1964).
3. W. Kayser, "Übersicht über Speicherverfahren für Speicher mit dünnen magnetischen Schichten," *Elektron, Rechenanlagen* 4, 60 (1962).
4. W. E. Proebster, "The Design of a High-Speed Thin Magnetic Film Memory," *Digest of Technical Papers, International Solid-State Circuits Conference*, 38 (1962).
5. W. Anacker, G. F. Bland, P. Pleshko and P. E. Stuckert, "On the Design and Performance of a Small 60-nsec Destructive Readout Magnetic Film Memory," *IBM Journal* 10, 41 (1966).
6. G. Kohn, W. Jutzi, Th. Mohr and D. Seitzer, "Design Principles of Nondestructive Read Thin Magnetic Film Memories with Read Cycle Time of 15 Nanoseconds," *Proc. Intermag Conference* 8.3-1 (1965).
7. W. Jutzi, "Nondestructive Readout in Thin Magnetic Film Memories," *Proc. IEEE* 52, 875 (1964).
8. W. Jutzi, "Das elektrodynamische Schaltverhalten dünner Magnetschichten in leitender Umgebung," *Archiv d. el. Übertragung* 19, 178 (1965).
9. H. Chang, "Analysis of Static and Quasidynamic Behavior of Magnetostatically Coupled Thin Magnetic Films," *IBM Journal* 6, 419 (1962).
10. W. Jutzi, "The Eddy Current Resetting Magnetic Field of Switching Thin Magnetic Films in Different Conducting Surroundings," *Proc. Intermag. Conference*, 8.2-1 (1965).
11. W. Jutzi, "Array Design of a Cross Sectional Model for a High Speed Thin Magnetic Film 140k Bit Memory in the Nondestructive Read Out Mode," to be published.
12. G. F. Bland, "Directional Coupling and its Use for Memory Noise Reduction," *IBM Journal* 7, 252 (1963).
13. E. M. Cherry and D. E. Hooper, "The Design of Wide-Band Transistor Feedback Amplifiers," *Proc. IEE* 110, 375, (February 1963).
14. M. S. Ghausi and D. O. Pederson, "A New Design Approach for Feedback Amplifiers," *IRE Trans. Circuit Theory* 8, 274 (1961).
15. D. Seitzer, "Die gegengekoppelte Doppelstufe mit Transistoren und ihre Eigenwerte," *Archiv d. el. Übertragung* 19, 301 (1965). (Also available in English.)
16. D. Seitzer, "Amplifier and Driver Circuits for Thin Magnetic Film Memories with 15 nsec Cycle Time," *IEEE Trans. Electronic Computers* 13, 722 (1964).
17. A. Melmed and R. Shevlin, "Diode-Steered Magnetic Core Memory," *IRE Trans. EC-8*, 474 (1959).
18. D. Seitzer, "Eine Gabelschaltung für Nanosekundenimpulse zur Herabsetzung der Schreibstörung in einem Magnetschichtspeicher," *Archiv d. el. Übertragung* 18, 577 (1964).
19. D. Seitzer, "An Experimental Word Decode and Drive System for a Magnetic Film Memory with 20-nsec Read Cycle Time," to be published.

Received July 5, 1966.

Revised manuscript received August 26, 1966.