

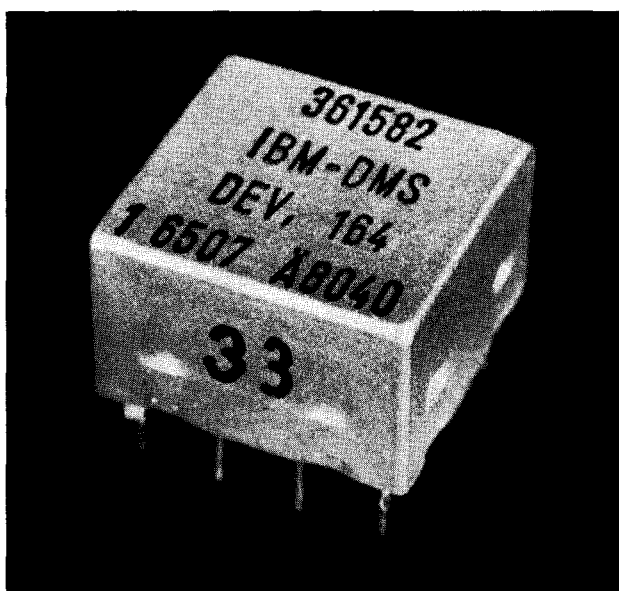
ASLT: An Extension of Hybrid Miniaturization Techniques

Abstract: The hybrid miniaturization technique of applying active and passive components separately to a packaging substrate enables independent customization of components and minimizes stray capacitance between components. Manufacturing advantages result because all components can be pretested, and the critical component joining operation can be performed as a continuous operation. This paper describes IBM's Advanced Solid Logic Technology (ASLT) wherein the capabilities of hybrid circuit technology have been extended to produce a high-speed, high-density digital logic module compatible with automated production. Design considerations and assembly processes are detailed. A development of the power handling capability reviews the various thermal paths within the module.

Introduction

Advanced Solid Logic Technology (ASLT) is a high-density, high-performance extension of IBM's Solid Logic Technology (SLT) electronic packaging system.¹ The increase in density (3 to 5 times that of SLT) is accomplished in part by stacking one ceramic substrate atop the other, and by utilizing both the top and bottom surface of each substrate for mounting circuits. The ASLT module is designed to be compatible with an extremely fast version of current-mode logic circuitry.²

Figure 1 Representative ASLT module.



This paper begins with a discussion of the elements which comprise the ASLT module. It includes a description of fabrication techniques, including such factors as screen printing and firing of electrode and resistor materials, soldering techniques, and encapsulation materials. In a discussion of the overall design, it is shown that high-density fabrication and assembly techniques enable the production of precision components for ASLT modules, resulting in circuits which meet rigorous specified performance criteria. In addition, form factors and interconnection techniques are reviewed with emphasis on manufacturability, testability, and circuit performance. Thermal characteristics are also examined to determine the power handling capabilities of this technology.

A completed ASLT module is shown in Fig. 1. The 0.490 inch square base contains 16 terminal pins on 0.125 inch centers. The module case is 0.290 inches high.

Module components

• Resistors

ASLT resistors are produced by depositing a 75 Ω /sq resistor material on the ceramic substrate and firing to drive off the organic vehicle and sinter the glass binder. The resistivity and resistor drift with life time are sensitive functions of the temperature-time profile of this firing cycle. The resistor paste is a highly stable version of the palladium oxide glaze system used in SLT. Its resistivity is controlled by the semiconductor properties of the palladium oxide and the amount of glass binder used. In accordance with the high life-stability required for ASLT circuits, these resistors have been demonstrated to be stable at power

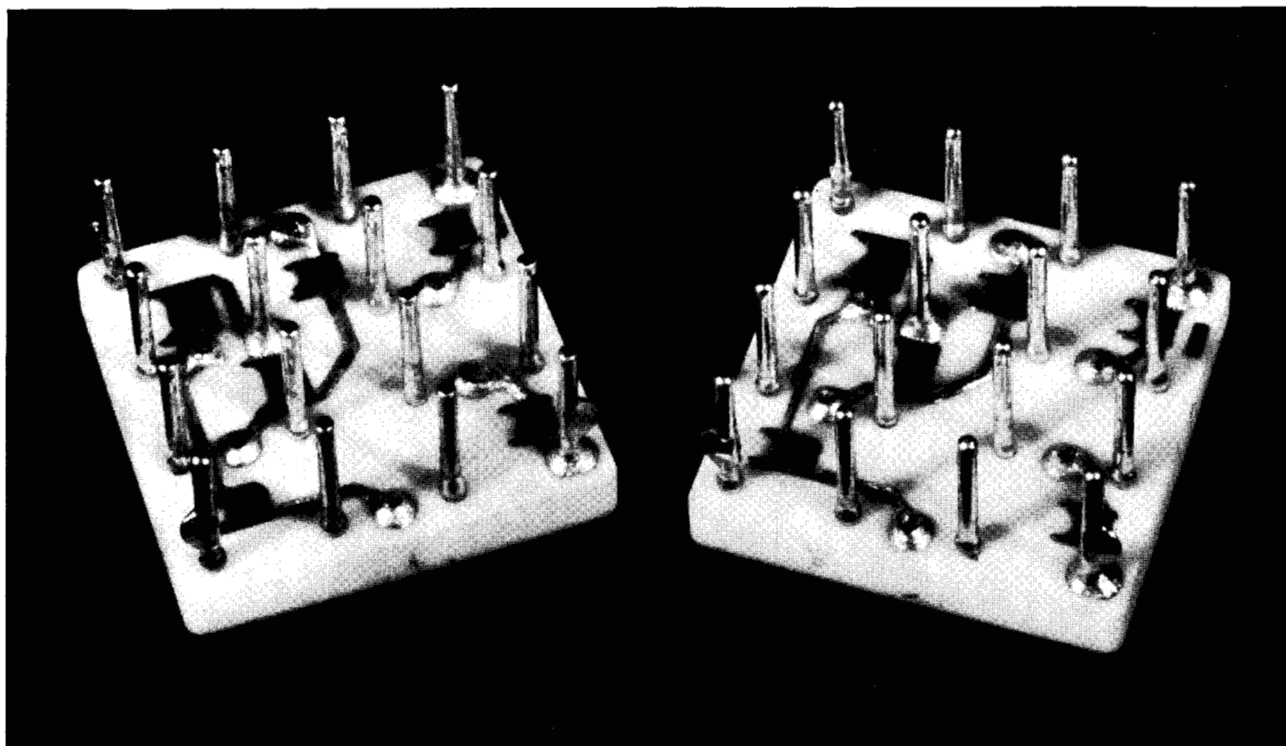


Figure 2 Resistors after trimming.

densities in excess of 200 W/sq in, although they were designed to operate at less than 25 W/sq in.

Once deposited and fired, the resistors are mechanically abraded by sandblasting from air nozzles until the resistors are trimmed to the proper value. A limit is set on the amount of resistor material abraded away during the trimming operation. This fixes the maximum power density and minimizes the effects of surface erosion resulting from scattering abrasive material. The eroded area appears as a halo around the cut edge of the resistor and is known to contribute to resistor drift. By controlling the depth of cut, it is possible to limit this eroded area to a small percentage of the total resistor area. A resilient coating is applied prior to resistor trimming to minimize this effect. To meet the end-of-life requirements of $\pm 4\%$ specified performance, the resistor is initially trimmed to $\pm 0.5\%$. Notice in Fig. 2 that the terminal and via pins* are arranged so that all the trimming nozzles can travel between the pins and trim all resistors from the same direction. It is therefore possible, with four independently controlled abrasive jets, to trim the eight possible resistors in two passes.

• Electrode metallizing

An electrode metallizing system of silver-palladium in a glass binder was chosen because of its minimum contact

resistance with the silver-palladium, palladium oxide resistor material and because its superior soldering qualities permit consistent tinning of the critical 0.010 inch fingers used to connect the semiconductor chips.

• Capacitive element

The capacitive element of an ASLT module is a multi-layer ceramic chip. The capacitor is fabricated by laminating screen-printed metallized sheets of slip-cast green ceramic. Individual capacitor chips are cut from the sheets and fired. End cap metallization is then applied and tinned for contacts.

This type of capacitor was chosen instead of a printed capacitor because it can be pretested to tight tolerances before being mounted on the module. Also, the laminated ceramic capacitor has a much higher capacitance-to-substrate surface ratio than screened capacitors. The latter results partly from the fact that it is not possible to achieve high densities with screen printing deposition of the dielectric material. This lessened density reduces the dielectric constant and, therefore, the capacitance.

Since each plate of the laminated capacitor connects directly to the end cap metallization, the series resistance and inductance are extremely small. In fact, the high-frequency performance of this capacitor is determined primarily by the length of land used to connect it to the module.

* See below, *Module Fabrication*.

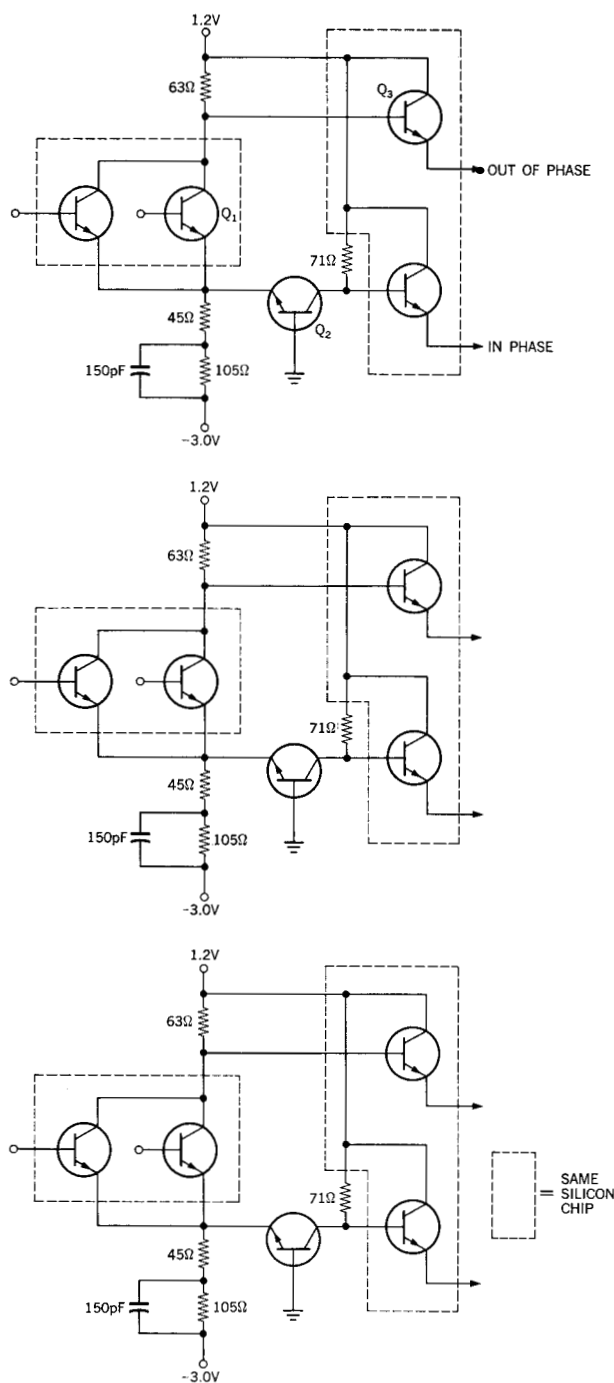


Figure 3 Schematic of typical ASLT module.

• Transistors

Another ASLT element, a high-speed transistor, is described elsewhere in this issue.³ Two contact configurations are used, one having three and the other five contacts. There are two types of five-contact chips: one contains two transistors with a common collector connection; and the other, three transistors with both collectors and emitters

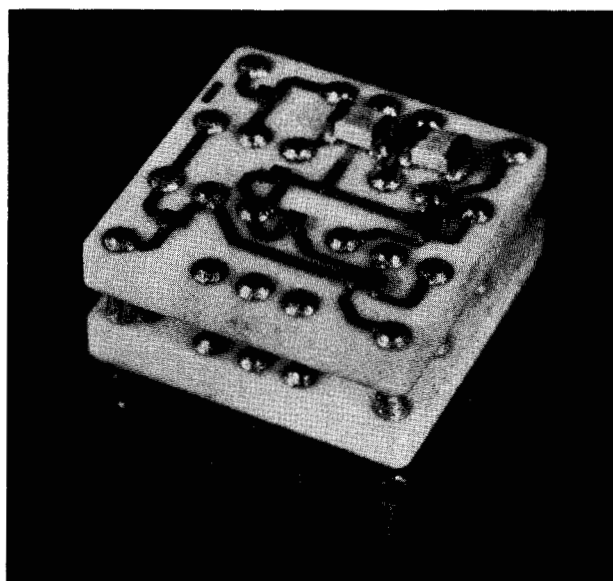


Figure 4 Stacked substrates.

common. Although the techniques for joining chips were demonstrated to be compatible with seven contacts per chip, five proved optimum because of the following considerations:

For production economy it was desirable to limit the number of contact configurations to two. A single transistor chip is always required for the common base transistor (Q_2 in Fig. 3). With five contacts it is possible to have either two transistors with a common collector contact or three transistors with both common collector and common emitter connections. The first configuration is used in the emitter-follower positions and proved optimum since there are never more than two circuits on one substrate (normally only one emitter-follower is used per circuit). The common collector, common emitter connection is used in the input position (Q_1 in Fig. 3). Since few modules call for four inputs, and since the common collector connection can be used when only two inputs are required, the three-transistor group proved to be optimum for this situation.

The size of the silicon chip is determined not by the number of transistors it contains, but by the number of contacts. (Minimum contact sizes and spacing are dictated by the screen printing tolerances on the module.) This was an additional reason for not using more than five contacts.

• Crossovers

Crossover connections are used in certain ASLT circuit configurations. The crossover is simply a pre-formed metal bridge, of height sufficient to provide insulation.

Module fabrication

• Screen printing, firing and pin insertion

Screen printing and firing of electrode and resistor materials on alumina substrates represent the first step of ASLT module fabrication. Terminal pins are automatically inserted in the substrate, then deformed to mechanically fasten them. Note in Fig. 4 that although this is a 16 pin module, 22 pins are used. The extra six pins serve two purposes—to serve as a monitoring terminal during the abrasive trimming of resistors, and to provide the “via” connection between the two surfaces of the module. Since the resistors are located on the bottom surface of the substrate, electrical connections must be made to the top surface during the resistor adjustment process. The automatic pinning equipment uses standard length pins for all locations. The “via” pins and the pins serving to connect the top and bottom substrates are then simultaneously sheared to the correct length. The top substrate does not usually require 16 voltage and signal pins; therefore some of the 16 pins are available for via pins, and the top level of the module can accommodate more components than the bottom level. The pinned assembly is then coated with solder. This provides a good electrical connection between the pins and lands and enhances the mechanical connection. The parts are vibrated during removal from the molten solder to assure a uniform coating.

• Component joining

Solder fingers which accept the semiconductor chips are mechanically flattened to maximize the probability of all joints being made. The semiconductors, capacitors, and crossover are automatically placed on the module and held in position with a high-viscosity flux. All the connections are soldered simultaneously in a continuous-belt furnace. Figure 5 shows a substrate before and after component placement and joining. Note that the electrodes connecting the capacitor terminal pads to the pins are all necked down to 0.010 in. This counteracts the tendency of the large capacitor terminal area to draw solder away from the pin by capillarity during the stacking reflow cycle.

• Substrate stacking process

The first step in the substrate stacking process is to apply a carefully-controlled amount of joining solder to the bottom of the pins on the upper substrate. This was initially accomplished by simultaneously cutting a pre-form from solder tape and applying it to the pin ends. The pre-form was shaped to extend beyond the pin ends to assure contact of joints prior to reflow joining. It was subsequently found that adequate control of solder volume and shape could be accomplished by simply dipping the pin ends (through a mask) into a pumped-solder wave. The high flow rate of the solder assures a uniform and repro-

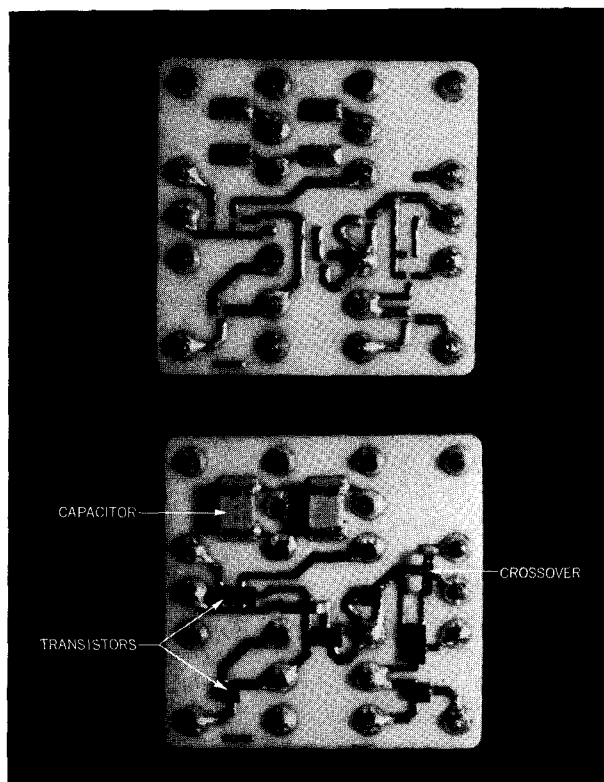


Figure 5 A substrate before and after component attachment.

ducible condition upon exit from the molten solder. Parts are then allowed to cool and are placed atop the lower substrate in a locating fixture. The joints are soldered by running these fixtures through a controlled-profile continuous-belt furnace. This continuous solder-reflow joining enables extremely high throughput at minimum cost with almost 100% yield.

• Solder alloy selection criteria

Three different tin/lead alloys are used on the module. Lands and pins are initially coated with 10% Sn-90% Pb (10/90) for the component-to-substrate joints. Pin ends of the bottom substrate are subsequently dipped in 63/37 (eutectic) since this alloy is used in the module-to-card soldering. Also, the high lead content of the 10/90 alloy would cause lead oxide to form on the pins during subsequent processing, unless coated with 63/37. Lead oxide greatly impairs solderability. It is desirable to stay below the liquid temperature of the 10/90 (310°C) during the stacking operation to avoid disturbing the component joints. Therefore, 20/80 solder is used for the stack joint (liquid at 290°C). Another factor contributed to the selection of this alloy—the percentage of tin was minimized because there is a tendency for the tin to take the silver of

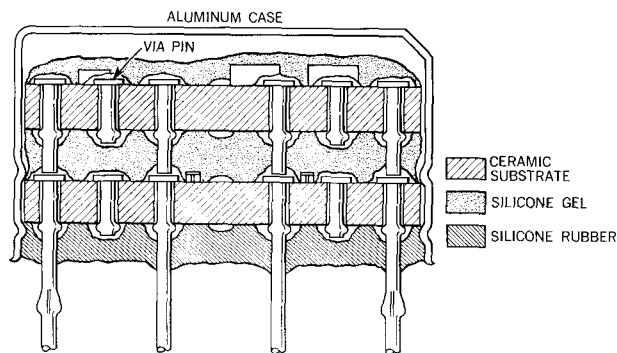


Figure 6 Schematic cross section of encapsulated ASLT module.

the silver-palladium metallizing into solution. This leaching of the silver greatly reduces the bond strength between the metallizing and the ceramic. In fact, if a high tin-content solder is used, a large amount of low tin-content alloy is present, or if the part is held in molten solder for an excessive period, a complete loss of land can result.

• Encapsulation system

Although each semiconductor chip is completely protected from moisture by a glass coating, it is still necessary to provide an encapsulation system that assures mechanical protection and minimizes corrosion of solder lands and semiconductor contacts. Figure 6 is a cross-section view of an ASLT module and shows the various features of the encapsulation. During fabrication, fine needles eject the silicone gel between the stack levels and onto both top surfaces. The substrate assemblies are preheated so that the silicone gel cures on contact, thereby restraining the material from flowing over the edges and interfering with the back seal.

Mechanical protection is afforded by a 0.010 in. thick deep-drawn aluminum case. The aluminum surface is anodized to provide a uniform matte finish. The case is deformed above and below the bottom substrate to hold it firmly in place and accomplish dimensional control from the bottom of the case to the pins. The module is then inverted to accept the automatically dispensed primer and silicone rubber back seal. The back seal provides a strong joint between the case and the substrate, and also greatly reduces the amount of moisture and contaminants that can enter the enclosure. The deformation of the pins as illustrated in Fig. 6 provides a positive standoff between module and card.

General design considerations

Most ASLT modules contain unit-logic partitioning similar to that shown in Fig. 3. That is, the functional inter-connection between logic gates is performed on the second-level package, not on the bottom level. This greatly reduces both the number of module types required and the impact of computer design and logic changes on the module requirements. Electrical testing is also simplified. However, certain constraints of module utilization result from this packaging approach, because any one particular grouping of circuit configurations is not always completely usable in all module locations. In addition, the number of components per module is limited by the input/output pins available.

• Yield

The solder reflow joining of the multi-ball semiconductor chips is one of the most critical assembly operations. Because all joints are made at the same time and faulty joints are not repairable, small variations in the per-joint yield greatly influence the assembly yield. If we assume that the joining defects are random (which appears to be the case in the long run), the per-substrate yield Y is an exponential function of the per-joint (or per-chip) yield X ; i.e., $Y = X^n$ where n equals the number of joints or chips per substrate. A similar trend exists for the electrical test yield, although not to the same degree because many compensating factors exist between various component parameters within a circuit.

It is this yield-factor multiplying which, more than anything else, dictates a stacked module approach in place of higher element densities or larger substrates. (As assembly (and electrical testing) yields increase, it will become economically feasible to go to larger substrates and higher densities.) To realize optimum yield advantages of the stacked substrate approach, it is essential to perform complete testing prior to stacking, thereby avoiding committing good product to defective product. Also, the yield of the stacking operation must be considerably higher than the component joining or electrical test yields.

• Packaging density

Major gains in circuit packaging density have been realized by optimizing screen printing techniques. For example, electrode line widths and spacings between electrodes have both been reduced to 0.010 in. to conserve space. The surface available for components has been doubled by mounting one substrate on another, as illustrated in Fig. 4, yet this results in only a 1.4 $\times$ increase in mounted module volume. In addition, this is a particularly efficient method for increasing overall density in the card-on-board packaging philosophy utilized in the System/360 Model 91. This is because a certain minimum space is re-

quired between cards to accommodate the card sockets, and a double-high module utilizes most of this normally unused space. The ASLT module height is such that no increase is required for connector spacing, yet sufficient space is available for adequate cooling-air flow. By limiting the resistors to the bottom surfaces of each substrate, the number of times the substrate is handled for printing and trimming is minimized.

The use of double and triple common-collector transistor chips economizes on the silicon chip size per transistor and, more significantly, results in considerable reduction of required interconnection space and crossovers on the substrate. Notice in Fig. 3 that the common-collector chip can be used in the input transistor position within a gate or be shared between gates in the emitter-follower position. Although not shown in Fig. 3, when the in-phase output is not used, the collector of the grounded-base transistor is tied directly to ground. In this configuration, the common-collector transistor chips can also be shared between gates in the grounded-base position. From these considerations it is evident that the common-collector chip is used to very good advantage.

- *Form factors and interconnections*

The circuit configuration is the basic determinant of performance. However, when the circuit involves 20 mA current changes in 1.0 nsec with a 0.5 V total signal swing, it is essential that the electrical character of the interconnectors within a module be thoroughly explored. Ten mil electrode lands represent about 17 nH/in. of inductance and, when spaced 0.010 in. apart have a 1.8 pF/in. capacitance. Care was taken in module layout to locate this unavoidable inductance and capacitance where it would least affect circuit speed and stability. For example, it was determined that for optimum circuit stability inductance in series with the emitter resistor of the input transistor (Q_1 , Fig. 3) should exceed that in the collector lead, yet the inductance between the input emitters and the common-base transistors must be kept at an absolute minimum.

Since the input impedance of this circuit can be negative at some frequencies, it is possible to have an underdamped oscillation between the input capacitance and inductance in the input lead. Every effort was made to keep the input leads short. Inductance in the collector lead of the input transistor can cause temporary saturation of the transistor during the positive-going transition. (The voltage developed across the parasitic inductance is of the correct polarity to forward bias the collector-base diode). This inductance also increases the time constant associated with any capacitance at the collector diode. Yet, a relatively large inductance (10-20 nH) can be tolerated in the collector of the emitter-follower since the quiescent voltage on the collector-base junction is 400 mV or more away from saturation. Since there is no decoupling on the

module, pin inductances of the supply circuits are also particularly critical. This circuit is very sensitive to noise generated on the 1.2 V supply; therefore this voltage is brought into the module by two pins to halve the effective lead inductance. The parasitic capacitance appearing at the collector node of the input transistor or the common-base transistor is most detrimental to switching speed. Careful layout keeps this capacitance well below 0.5 pF.

- *Effects of design on testing procedures*

As previously mentioned, the high joining or stacking yield plus complete testing prior to stacking are both essential to achieving high yield of ASLT module fabrication. Since most of the modules have one or more complete logic functions on each level, final electrical test procedures can be implemented prior to stacking without having the test equipment complete the testing function (as would be the case if part of the logic function were located on each level). At these high speeds (approximately 1.5 nsec) the signal delay from the bottom to the top level and back (approximately 180 psec) represents an appreciable portion of the total switching time. The pre-stacking test limits are adjusted to correct for such differences.

- *Thermal characteristics*

The mechanical and solder-metallizing joint of the sixteen 0.020 in. copper pins to the lower substrate provides an excellent heat-conducting path out of the module. Since the connection between the substrate and the module case represents a high thermal impedance, the thermal conductivity of the card and the distance the pins extend beyond the card into the air stream become major determinants of module power-handling capability. This is illustrated by the fact that the thermal resistance between the lower substrate and the pin ends is approximately 4°C/W. Yet, the total external thermal resistance is 70°C/W in high-velocity air (400 linear ft./min.) with about 0.010 in. of pin extending beyond the card.

The thermal ambient inside the module is complicated by a thermal resistance between substrate levels (3°C/W), and by differences between the thermal resistance of the resistors and that of transistors with reference to the substrate. Therefore, the maximum allowable power depends upon the type of circuit and the division of power between top and bottom substrate layers. To provide an indication of module capability, the *effective* internal thermal resistance must be studied. This resistance can be defined as the temperature rise of the most critical (i.e., limiting) component divided by the total module power. This parameter is therefore a function of the type of circuit and the module layout. For the module in Fig. 1 (typical of all ASLT modules), this value is 17°C/W (see Appendix).

If this is added to the 70°C/W external thermal resistance experienced in the System/360 Model 91, we have a

total of 87°C/W. Since the circuits are designed to a maximum junction temperature of 85°C and the maximum ambient air temperature is 40°C, the power-handling capability of these modules in this application is calculated at 515 mW by

$$P_{wr.} = \frac{85^{\circ}\text{C} - 40^{\circ}\text{C}}{87^{\circ}\text{C/W}}$$

Conclusions

The ASLT packaging concept represents a successful program to extend the capabilities of hybrid miniaturization technology to an ultra high-speed, high-density application within the design constraints of a product intended for automated manufacture. Full advantage is taken of the ability to individually tailor components to the requirements of a high-performance circuit.

Acknowledgments

The short time between development and manufacturing of this product required considerable cooperation and contributions from many members of the Systems Development and Systems Manufacturing Divisions of IBM. While it is impractical to cite all of the numerous contributions, special attention should be called to the efforts of T. Palfi, F. Pakulski, R. McGregor, and the late V. Vulcan of the module development department.

Appendix

The components of the internal thermal resistance are:

R_T : Transistor junction to substrate (for double chip)—170°C/W

R_T : Substrate to pins (for this power distribution)—5°C/W

R_T : Top level to pinheads* on lower substrate—3°C/W

The limiting temperature for the module in Fig. 2 is the junction temperature of Q_3 on the top level. The power of each circuit is 80 mW and they are divided, two on the top level and one on the bottom. Q_3 dissipates 16 mW in the worst case. Therefore, the ΔT of $Q_3 = 0.016\text{W} \times 170^{\circ}\text{C/W} + 2 \times 0.080\text{W} \times (5 + 3^{\circ}\text{C/W}) = 4^{\circ}\text{C}$. This gives: Effective $R_{\text{int.}} = \Delta T$ of limiting component/total module power = $4^{\circ}\text{C}/0.240\text{W} = 16.6^{\circ}\text{C/W}$.

* An arbitrary reference for the separation of internal and external thermal drop.

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