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ASLT Circuit Design

Abstract: The full switching-speed potential of high performance transistors is difficult to realize in a current switch configuration because of the instability which exists when many circuits are interconnected in a system. With a phase compensating network in the emitter current source, however, it has been possible to design a stable circuit using 1 Gc/sec transistors. Design techniques and engineering aspects of the circuit which result in a 5-nsec in-the-environment propagation delay are described. Particular attention is given to the dc design, stability analysis, switching performance, evaluation and specification of the circuit.

Introduction

The ASLT circuit family was developed specifically to meet the performance requirements of the IBM System/360 Model 91. These requirements include:

- A propagation time of 5 nsec, in and including the environment.
- Double level logic blocks.
- High fan power.
- Predictable delays.

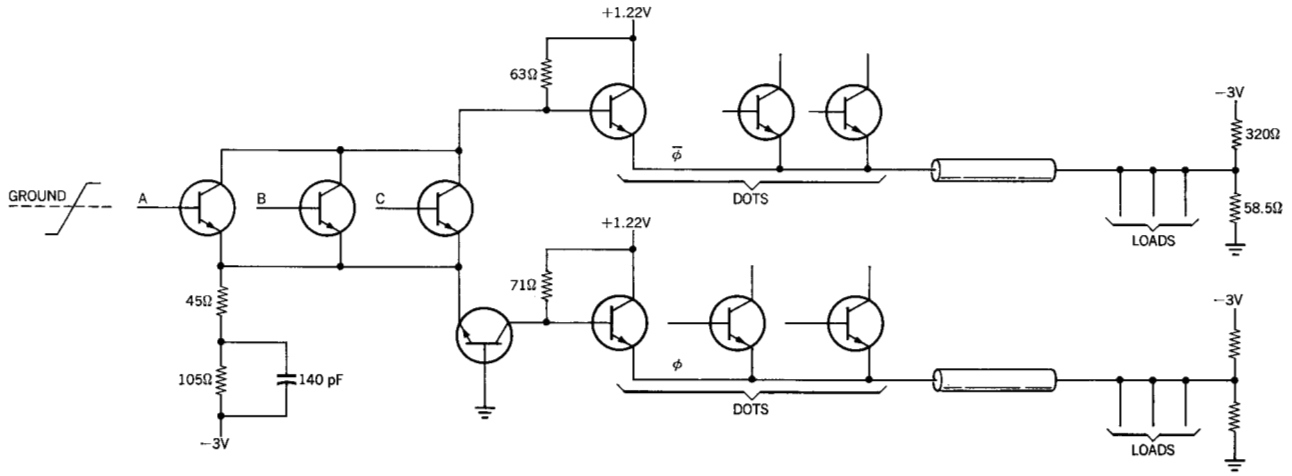
In order to realize these goals, significant effort on the part of device, module, packaging, test equipment and other supporting groups was necessary. A listing of the important achievements which made the design of this circuit family possible would include:

- A stabilizing technique for the current switch circuit.
- High-performance single and multiple chip transistors.
- Packing density of 10–15 circuits per square inch.
- Multi-impedance transmission line system.
- Improvements in power distribution system.
- Improvements in component tolerances.

The ASLT circuit family is implemented by nine different 16-pin stacked (two substrates) SLT modules and associated external resistors (R-pacs). Multiple device chips, together with the stacking feature, permit the use of up to 4 circuits per module.

Figure 1 shows the ASLT circuit with final resistor and power supply values. If the positive level is defined as a logical 1 and the negative level as a 0, the truth table for the circuit of Fig. 1 is as shown in Table 1. The out-of-phase output, $\bar{\phi}$, is the NOR statement while the in-phase output, ϕ, yields its complement, +OR. The connecting of out-of-phase emitter followers (called "dotting") provides

Figure 1 ASLT circuit.



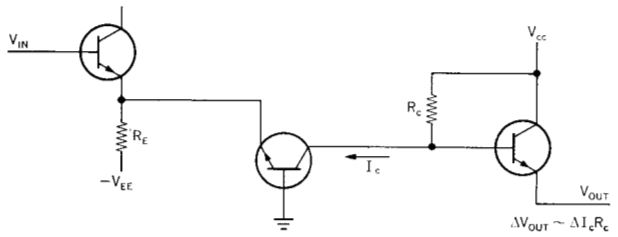


Figure 2 In-phase ASLT circuit for gain optimization.

the double level function $\bar{A}\bar{B} + \bar{C}\bar{D} + \text{—}$. Dotting of in-phase emitters extends the OR. The logic power capability of the ASLT circuit is summarized in Table 2. The design approach for the circuit of Fig. 1 is described below.

DC design

The dc design of the circuit is the adjustment of all nominal component values so that, when component values are deviated to their extremes, operating levels of the circuit are achieved which produce complete switching of similar circuits. The dc design has the following constraints:

1) The output must drive a 50 ohm system with a substantial noise margin.
2) The voltage levels must be such that transistors do not saturate.
3) The circuits must operate with junction temperatures from 35°C to 85°C.

A number of design iterations were necessary to determine that a 150 ohm, maximum current switch resistor, R_E, was nominally required to achieve condition 1. Within the constraints listed above, the maximum value of R_E is used to minimize power dissipation. Once this value was chosen the design could be optimized to give the maximum voltage gain in the switching region. For a given input voltage change, ΔV_{in}, the change in current switch collector current is determined by the device tolerances. The corresponding change in V_{out} is proportional to R_C, the collector resistance (Fig. 2).

Table 1 Truth table for circuit of Fig. 1.*

Input			*Output*	
A	B	C	$\bar{\phi}$	ϕ
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

* $f_1 = \bar{\phi} = \bar{A}\,\bar{B}\,\bar{C}$; $f_2 = \phi = A + B + C$.

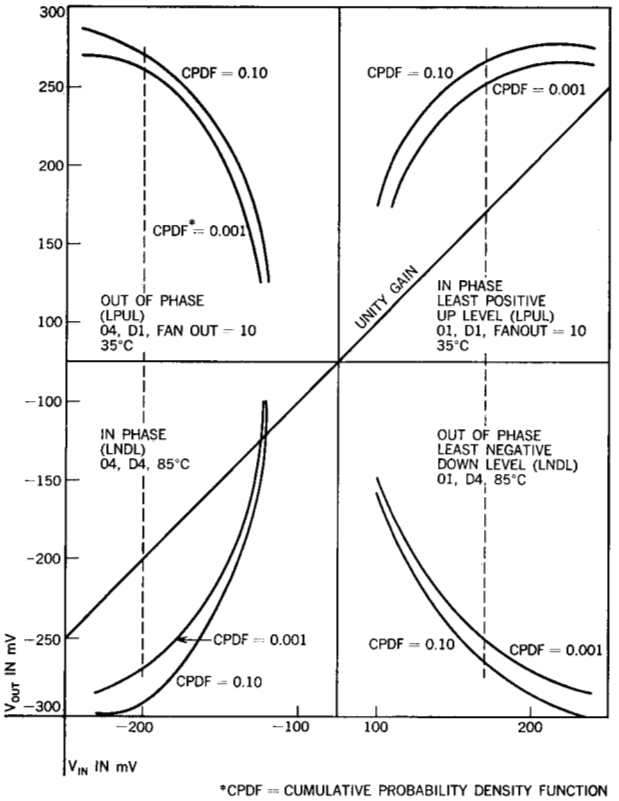
In order to maintain the proper output levels V_{CC} must be increased with R_C. The gain, $\Delta V_{out}/\Delta V_{in}$, is maximized by increasing R_C and V_{CC} until any further increase results in levels which saturate the succeeding stages. Saturation is avoided to minimize circuit turn-off time. The optimization of $\Delta V_{out}/\Delta V_{in}$ provides maximum possible ac and dc noise tolerance and optimum risetime restoration due to the high voltage gain in the switching region.

With this philosophy as a guide, a circuit design can be developed with the aid of a computer program. Worst-case values are utilized for parameters outside the circuit, such as power supplies ($\pm 3\%$) and external resistors, $\left(\begin{smallmatrix}+5\%\\-4\%\end{smallmatrix}\right)$. Device parameters internal to the circuit are assumed to have a statistical distribution. The program employs a Monte Carlo method of circuit analysis, which simulates the statistical behavior of the networks by selecting random combinations of circuit parameters. One hundred thousand calculations are made for each input level. Using this technique the distribution of output voltage values for each input voltage value is calculated.

- *DC gain curves*

The design results are best understood by the use of gain curves, as shown in Fig. 3. It is desirable to consider the

Figure 3 DC gain curves for ASLT circuit.



*CPDF = CUMULATIVE PROBABILITY DENSITY FUNCTION

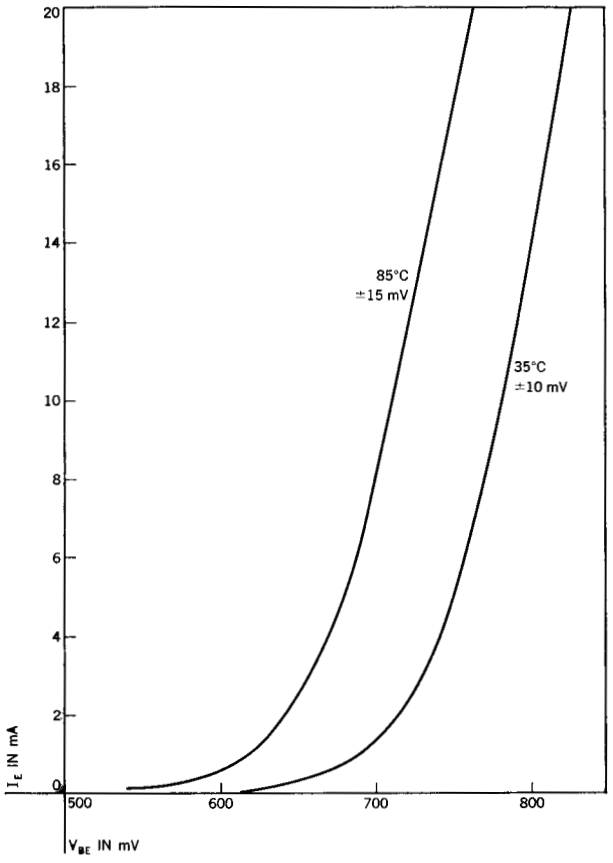


Figure 4 Current switch V_{BE} design curve.

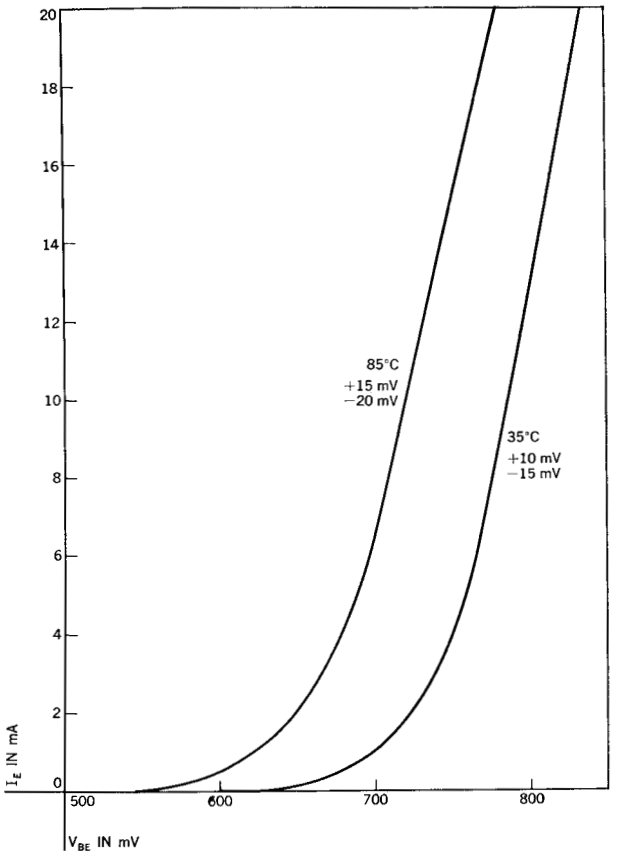


Figure 5 Emitter follower V_{BE} design curve.

output voltage levels over the entire range of input voltage levels, as shown here, in order to detect the maximum noise margin of the circuits. That is, since the circuit generally operates without complete switching of transistors, operating levels are not uniquely defined and can be chosen as those giving the maximum noise margin. The interpretation of the 0.001 curve in Fig. 3 is that, for a given input voltage, in only one case in a thousand will the output voltage be less than the value given on the curve. The high gain in the switching region is apparent from these curves. Also, the circuits have a substantial noise margin. As an example, for $V_{in} = +170$ mV, $V_{out} = +250$ mV for the in-phase circuit. This can be interpreted as follows: In a chain of in-phase circuits with worst case loading and power supply values, 80 mV of noise can be injected at each base in the chain and the output level of the last stage will still be greater than +250 mV.

Device specifications

One of the important advantages of hybrid circuit technology is that the individual components comprising a circuit can be tested and matched before they are connected on the module. This feature was especially important in achieving the dc design goals for the ASLT circuits described in Table 2. Two important features of the design are:
1) The devices can be sorted on the basis of V_{BE} and then matched on the module so that no two transistors in any one current switch differ in V_{BE} by more than 20 mV (Fig. 4). Devices with more resistive V_{BE} characteristics are used as emitter follower transistors (Fig. 5).
2) The resistor distribution is assumed to be Gaussian within $\pm 5\%$ at the $\pm 3\sigma$ points, respectively. In addition, resistors on the same substrate will "track" within 3%

Table 2 Logic power capability.

	In phase	*Out of phase*
Fan-in	4	4
Dots	4	4
Fan-out	10	10

Table 3 DC voltage levels for ASLT circuit.

Parameter	V_{in}	*Fan-in*	*Dots*	*Fan-out*	*Junction temperature (in °C)*	*CPDF** 0.10	0.001	0.00001
Out ϕ LPUL†	−200 mV	1	1	10	35	280 mV	271 mV	268 mV
	−200	2	1	10	35	278	267	264
	−200	3	1	10	35	276	264	261
	−200	4	1	10	35	273	261	258
In ϕ LPUL	+170	1	1	10	35	268	259	249
Out ϕ LNDL‡	+170	1	4	1–10	85	−271	−251	−239
In ϕ LNDL	−200	1	4	1–10	85	−313	−294	−286
	−200	2	4	1–10	85	−310	−290	−282
	−200	3	4	1–10	85	−308	−287	−279
	−200	4	4	1–10	85	−306	−284	−274
Out & In ϕ MPUL§	open	1	4	1	85	+559	+589	+595
V_{sat}	MPUL	1–4	1–4	1–10	85	+562	+654	+680

* Cumulative probability density function
† Least positive up level
‡ Least negative down level
§ Most positive up level

of one another, viz.

$$\frac{\Delta R_i}{R_i} - \frac{\Delta R_j}{R_j} \leq 0.03,$$

where R_i and R_j are any two resistor values arbitrarily selected from the same substrate. Table 3 shows the dc levels attained by the circuit. The 0.001 points are specified for all dc tests. V_{sat} is the forward bias on the collector-base junction of the input transistors under worst case conditions.

Stability

The stability problem associated with current switch circuits is that the optimization of switching speed tends to produce unstable circuits. The introduction of the emitter stabilization capacitor in ASLT has permitted the circuit design and transistor to be optimized for switching speed without instability.

The nature of the stability problem in ASLT circuits can be summarized as follows:

1) Instability, when it occurs, is confined to the steady state operating levels of the circuit. It does not occur during switching, nor does it bear any relationship to previously applied switching signals. The result of instability is an oscillation at high frequency (100 Mc/sec $\leq f \leq$ 750 Mc/sec), superimposed on the normal operating levels.

2) Oscillations, when they occur, are limited in amplitude by the large signal nonlinearities of the circuits; the fact of occurrence, however, can be determined by a small signal analysis of the circuits.

• *Theorems*

A useful stability analysis should be performed in real frequency, $F(j\omega)$ rather than $F(s)$, in order that analytical results can be compared with laboratory measurements. The real frequency requirement suggests the use of Nyquist's criterion of oscillation. Since laboratory equipment is available to measure driving point impedances and admittances, Nyquist's criterion has been employed for these network functions.

The following application of Nyquist's criterion can be stated for a source-free, linear, bilateral circuit, having input impedance $Z(j\omega)$: If the circuit is stable with its input terminals open-circuited, it will be stable with the terminals short-circuited if, and only if, the locus of $Z(j\omega)$ (as ω is varied from $-\infty$ to $+\infty$) has no encirclements of the origin ($Z = 0 + j0$) in the Z plane of an impedance plot.

The apparent difficulty in this theorem, caused by the presence of negative frequency and variations of frequency to $+\infty$, is easily resolved by laboratory measurements. Any circuit under consideration will have one or more narrow ranges of frequency within which stability is a problem, and the critical shape of the network function

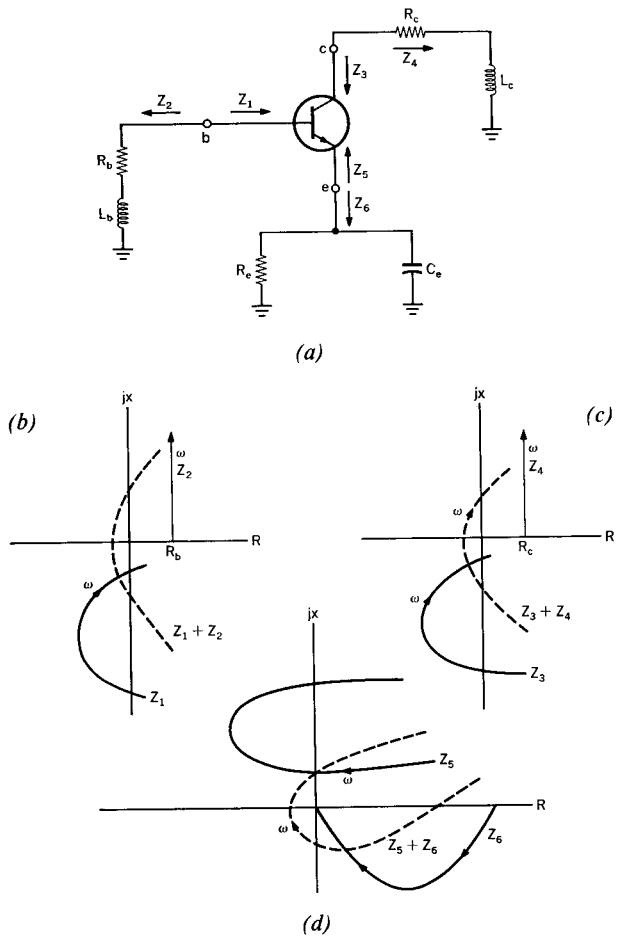


Figure 6 Transistor circuit impedance plots.

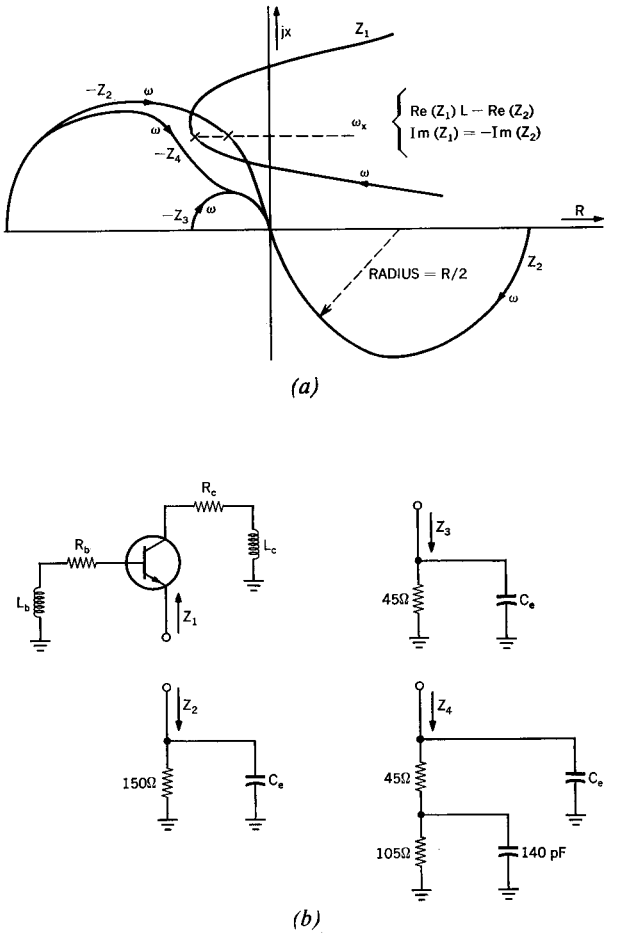


Figure 7 Transistor impedance locus demonstrating effect of stabilization capacitor.

which produces oscillation can be measured. Normally, the presence of one point, $X = 0$, $R < 0$, is used to determine instability.

- *Transistor instability*

The simple transistor circuit in Fig. 6 has bias resistances and critical stray reactance as shown. The circuit is stable with points *b*, *c*, or *e* open-circuited.* The input impedance loci (referred to ground) at each terminal are shown. The short circuit impedance at each terminal is the sum of the input impedance at that terminal and the external impedance connected to it. In general, the stray reactance and resistance values used in ASLT circuits produce an unstable circuit, as shown in the impedance loci sums.

The effect of the emitter stabilization capacitor is shown in Fig. 7. Z_1 is the input impedance at the transistor emitter. The stability of this impedance when coupled with the emitter *RC* network (Z_2) is assured if the locus of the sum of the two impedances does not encircle the origin. An encirclement of the origin would require

$$\text{Re}\,(Z_1) + \text{Re}\,(Z_2) \leq 0, \text{ or, for convenience,} \quad (1)$$

$$\text{Re}\,(Z_1) \leq -\text{Re}\,(Z_2), \quad (2)$$

when

$$\text{Im}\,(Z_1) + \text{Im}\,(Z_2) = 0, \quad \text{or} \quad (3)$$

$$\text{Im}\,(Z_1) = -\text{Im}\,(Z_2). \quad (4)$$

It can be seen from Eqs. (2) and (4) that if the locus of the negative of the emitter *RC* network impedance does not intersect with the locus of the emitter input impedance, stability is assured, whereas an intersection of the two loci will produce instability if the intersecting frequencies overlap.

It is seen in Fig. 7 that the impedance Z_4 has the required dc resistance of Z_2 and the stabilizing effect of Z_3.

* An experimental verification is normally relied upon here. An analytic proof requires determining the location of the poles of $Z(s)$.

Table 4 Transistor parameters.

Symbol	*Definition*	*Transistor value*
β_0	Current gain $(\Delta I_C/\Delta_{IB})_{IE}$	30–50
C_1	One-half the collector junction capacitance external to the emitter	0.5 pF
C_2	One-half the collector junction capacitance external to the emitter	0.5 pF
C_{BC}	Stray capacitance from base to collector	1.0 pF
C_{BE}	Stray capacitance from base to emitter	0.5 pF
C_{CE}	Stray capacitance from collector to emitter	0.5 pF
C_{TE}	Emitter junction capacitance	0.5 pF
C_{TC}	Collector junction capacitance	0.5 pF
H	One-half the emitter width	0.5 mil
F_{L1}	Width of first section used in solution of Z_B	0.025 mil
F_{L2}	Width of second section used in solution of Z_B	0.125 mil
q/KT		$37.77V^{-1}$
R	Base layer sheet resistance under the emitter	1.894 KΩ/mil
R_B	Base bulk resistance external to emitter	8Ω
R_C	Collector bulk resistance	5Ω
R_E	Emitter diode resistance	$(KT/q)I_{RE}$
τ_E	Emitter transient time	0.13 nsec
Z_B	Complex base impedance	function of circuit

• *Quantitative stability analysis*

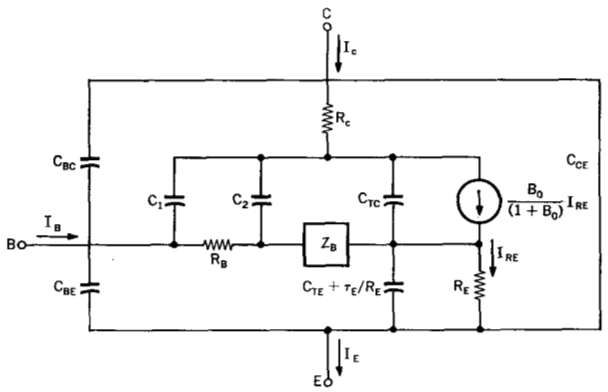
The transistor model used for the stability analysis is shown in Fig. 8a; Fig. 8b is a plot of complex base impedances for this model. A complete discussion of this model, along with the derivation of the equations for the complex base impedance, Z_B, appears in the literature.[1] Table 4 shows the transistor parameters; Fig. 9 shows the module layout; and Table 5 shows module parameter variations.

The primary stability problem is associated with the input transistor (Q_1 in Fig. 9). The output emitter followers are stabilized by their large base resistors (63Ω and 71Ω). The common-base transistor has less severe stability problems than the input transistor because of its small base inductance.

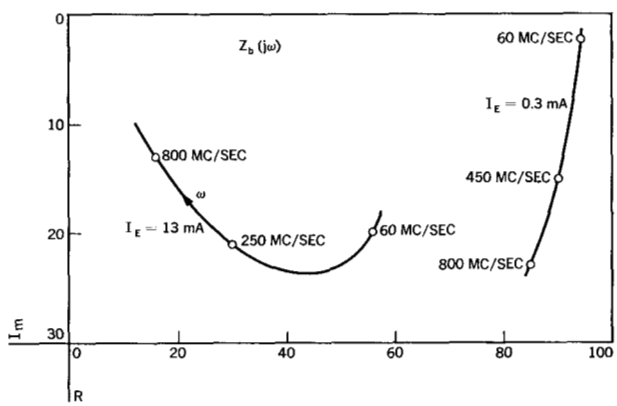
By computer analysis, the circuit parameters can be chosen to produce the most pessimistic input impedance locus (shown in Fig. 10). The impedance locus is separated into two important segments. In region 1, the position of the impedance locus is determined primarily by the value of the emitter stabilization capacitor. The most important point in this section is the point at which the real part of Z_{in}, Re (Z_{in}), becomes positive. This is the frequency above which no combination of such impedances with passive loads can oscillate. The value of the imaginary part of Z_{in}, Im (Z_{in}), at the crossover determines the minimum positive reactance required at the input to produce oscillation.

In region 2, the impedance locus is primarily determined by the stray parameters associated with the module

Figure 8 (a) Model for stability analysis; (b) plot of complex base impedance for model.



(a)



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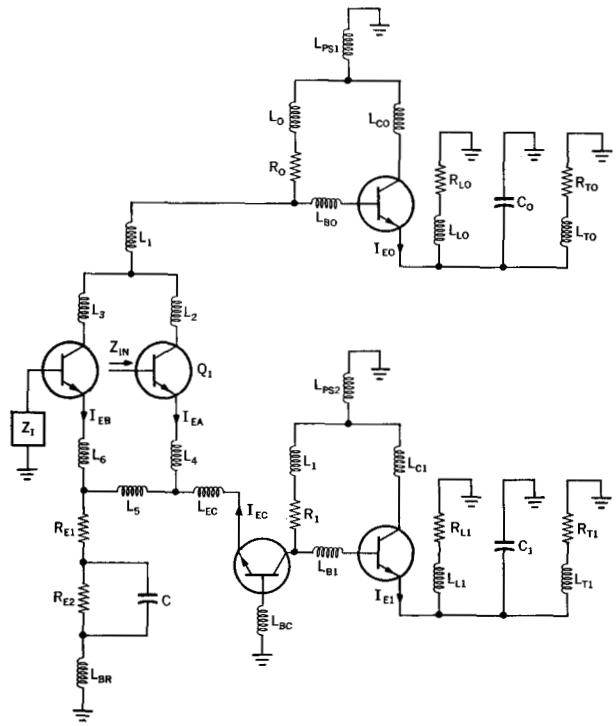


Figure 9 Model of module circuit layout.

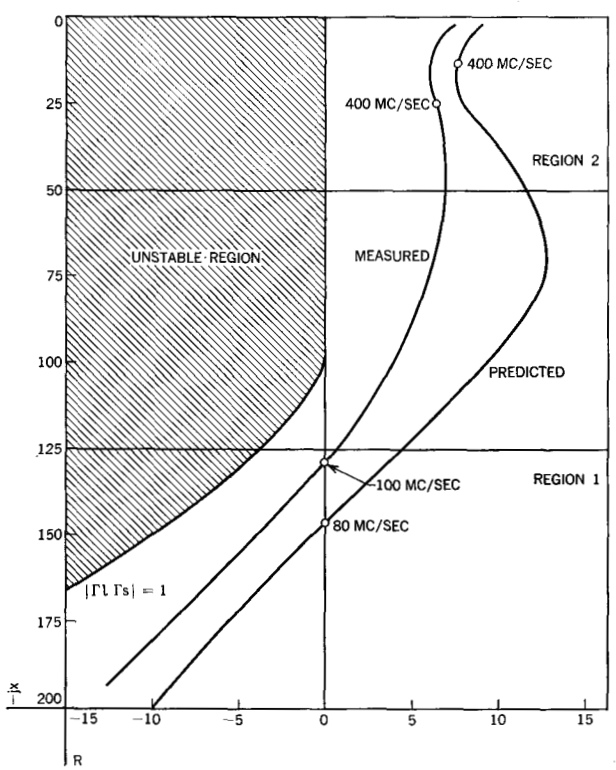
Table 5 Module parameter variations.

Stray components

(1) $L_1, L_2, L_3 \leq 11$ nH; $(L_1+L_2), (L_2+L_3), (L_1+L_3) \leq 12$ nH
(2) $L_4, L_5, L_6 \leq$ nH; $(L_4+L_5), (L_4+L_6), (L_5+L_6) \leq 12$ nH
(3) $1 \leq L_{BR} \leq 20$ nH
(4) $1 < (L_{ps1}, L_{ps2}) < 10$ nH
(5) $1 \leq L_{BO}, L_{CO}, L_O \leq 5$ nH
(6) $L_1, L_{B1}, L_{C1} \leq 1$ nH
(7) $L_{EC}, L_{BC}, 1 \leq L_{EC} \leq 4$ nH $L_{BC} = 1$ nH
(8) $L_{LO} = 5$ nH $= L_{L1}$
(9) $L_{TO} = 1$ nH $= L_{T1}$

Circuit currents	*Components*
(1) I_{EA} 13 − 18 mA	(1) R_{E1} − 42 − 48 Ω
(2) I_{EB} 0 − 6 μA	(2) R_{E2} − 100 − 110 Ω
(3) I_{EC} 10 − 100 μA	(3) 150 ≥ $C \geq$ 75 pf
(4) I_{EO} 0.1 − 6 mA	(4) Z_I − 25 Ω
(5) I_{EI} 18 mA	(5) R_0 − 60 − 63 Ω
	(6) R_1 − 71 Ω
	(7) R_{LO}, R_{LI} − 284 Ω
	(8) R_{TO}, R_{TI} − 50 Ω
	(9) C_0 − 50 pf
	(10) C_1 − 50 pf

Figure 10 ASLT input impedance locus.



layout and the value of the emitter resistor, R_{E1}. It is essential in this region to maintain a positive Re (Z_{in}) because of the low magnitude of Im (Z_{in}). This requirement dictates the maximum value of R_{E1} and restricts the module layout, as noted in Table 5.

As previously noted, it is possible to produce oscillation in ASLT circuits because of the presence of negative Re (Z_{in}) at low frequencies. To demonstrate that this condition is never realized in the ASLT circuit environment, Nyquist's criterion is employed, with reflection coefficient as the network function under consideration.

To perform the analysis a simple network such as that of Fig. 11 is first considered. ASLT circuits Z_ℓ and Z_s, or combinations of such circuits, are interconnected by a transmission line of length ℓ as shown. The signal flow diagram of the network is given in Fig. 12. From this diagram, we may write the transfer function in the complex frequency domain:

$$\frac{e_0}{e_{in}} = \frac{2Z_\ell Z_0 \exp(-sT_0\ell)}{(Z_\ell + Z_0)(Z_s + Z_0)[1 - \Gamma_\ell\Gamma_s \exp(-2sT_0\ell)]},$$

where

$$\Gamma_\ell = \frac{Z_\ell - Z_0}{Z_\ell + Z_0};$$

$$\Gamma_s = \frac{Z_s - Z_0}{Z_s + Z_0}.$$

The network will be stable provided e_0/e_{in} has no poles in the right half s-plane. Sufficient conditions for stability,

therefore, are:

1) $Z_\ell + Z_0$
2) $Z_s + Z_0$
3) $1 - \Gamma_\ell \Gamma_s \exp(-2sT_0\ell)$

} have no zeros in right half s-plane.

Conditions 1 and 2 require that the loads be stable when the inputs are connected through Z_0 (real) to the reference point (ground in Fig. 11). If these conditions are satisfied, then the stability of the network can be determined by plotting the locus of $F(s) = 1 - \Gamma_\ell \Gamma_s \exp(-2sT_0\ell)$ in real frequency ($s = j\omega$). An encirclement of the origin by $F(j\omega)$ is sufficient to assure instability of the net. The condition for stability can therefore be expressed in the following manner:

$$|\Gamma_\ell(j\omega)\Gamma_s(j\omega)| < 1.$$

The impedance locus allowing $|\Gamma_\ell \Gamma_s| = 1$ under most pessimistic interconnection conditions was determined analytically and is plotted in Fig. 10. This curve essentially divides the impedance plane into two parts. If Z_{in} of the circuits comprising the net lies to the right side of the $|\Gamma_\ell \Gamma_s| = 1$ line, the system is stable. Circuits with Z_{in} curves in the shaded region of Fig. 10 may be unstable. Although the predicted and measured curves for Z_{in} differ slightly, they both lie in the stable region of the Z-plane.

• *Specifications*

To detect product variations and inaccuracies in the computer analysis, test procedures are required to assure that ASLT circuits have the desired impedance characteristics.

At the module level, one of two tests is performed, depending on the information desired:

Test 1: The input impedance locus can be measured with a ZDU diagraph. Critical test points are:

(a) $f = 100$ Mc/sec,
$\mathrm{Re}(Z_{in}) > 0$,
$|\mathrm{Im}(Z_{in})| > 125\Omega$.
(b) $f = 400$ Mc/sec,
$\mathrm{Re}(Z_{in}) > 5\Omega$.

} $V_{indc} = +0.22$V
$V_{inac} = 10$ mV, RMS

The power supply and signal line impedances must be specified exactly, as indicated in Fig. 9 and Table 5. These measurements are made only when module layouts or chip specifications are changed.

Test 2: A simple test can be performed to determine that the stabilization capacitor has the proper value and has been mounted properly. This is done by measuring the high-frequency input impedance of the module ($I_B = 3$ mA and $I_C = 0$). The emitter-base diode of the saturated input transistor has a very low impedance in this state and the measurement is dominated by the emitter RC network.

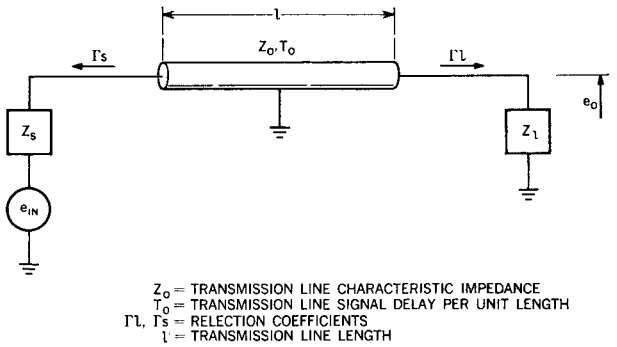
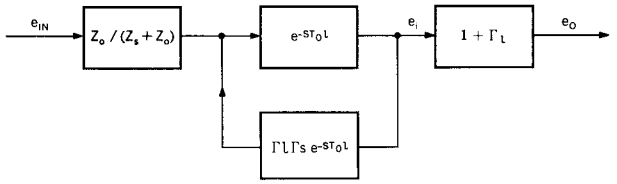


Figure 11 Network for generation of reflection coefficient stability criteria.

Figure 12 Signal flow diagram for network of Fig. 11.



At the chip level, tests are performed on the capacitor and the transistor.

Test 1: To guarantee satisfactory stabilization, the emitter bypass capacitor must have its impedance specified at critical frequencies. The limits are:

at $f = 100$ Mc/sec, $|Z| \leq 16\Omega$, and

at $f = 500$ Mc/sec, $|Z| \leq 5\Omega$.

Test 2: Since transistor instability generally increases as switching delay decreases in a current switch environment, critical performance parameters such as base resistance and gain-bandwidth must be controlled in order to maintain the Z_{in} characteristics described above. A 200 Mc h_{fe} test modified to include the effects of r_{bb} and C_{cb} is specified for the transistor used in this circuit to guard against excessive stability problems at the module level.

Switching performance

The switching performance goals for the ASLT circuit family were essentially achieved with the development of the high performance transistor and the stabilization technique described above. Typical circuit delays and output transitions are 1.8 and 1 nsec, respectively. However, the successful operation of more than 100,000 of these circuits in the Model 91 machine environment requires some additional design considerations, and these are discussed below.

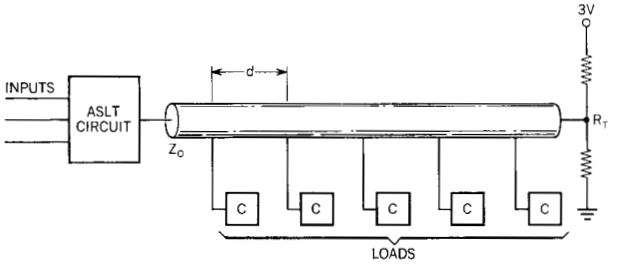


Figure 13 Circuit interconnection method.

• *Interconnection techniques*

When typical interconnections or "wire" lengths are compared with risetimes it is evident that transmission line phenomena will exist in ASLT technology. The basic interconnection scheme for these circuits is shown in Fig. 13.

Since the primary loading effect of the circuit is capacitive, the configuration can be approximated by a transmission line loaded with capacitors, C, distributed over a spacing of d inches. The effective characteristic impedance of the line will then be given by

$$Z = \frac{Z_0}{1 + (C/dC_0)},$$

where Z_0 is the characteristic impedance of the unloaded line and C_0 is the characteristic capacitance of the line. The spacing d is maintained so that the loaded characteristic impedance is within $\pm 25\%$ of the value of the terminating resistor R_T. The reflections resulting under these wiring conditions are tolerable, since the proper dc levels are achieved on the first transient down the line. An uneven distribution of loads will cause reflections that can be serious and will result in the propagation of erroneous data.

An effectively terminated system, $R_T = Z \pm 25\%$, can be maintained by adjusting either the spacing d or the line characteristic impedance Z_0. To cover the wide variety of wiring configurations obtainable in a computer environment, a number of characteristic impedances are desirable. The ASLT package provides 50 Ω and 90 Ω transmission lines. The terminating network is equal to 50 Ω. The wiring configurations required to maintain a characteristic impedance within 25% of the termination impedance are quite restrictive. Greater flexibility is provided by allowing two loads at a node, with transmission line stubs up to two inches in length. The loaded characteristic impedance of the line is maintained by doubling the spacing between these nodes.

Additional wiring flexibility is provided by the use of clustered loads. A clustered load is the presence of three or more loads so spaced that the effective impedance is below the minimum required for the distributed case. The restriction for such a net is that no additional loads can be placed between the cluster and the driver. The reflection from a cluster generates a noise pulse sufficient to cause false switching of the ASLT circuit.

• *Power dissipation and switching performance*

In general, signal delays and transitions are improved as transmission line impedance is decreased. The choice of a 50 Ω system for ASLT was a compromise between performance and power dissipation. To achieve optimum circuit speed when driving 50 Ω, a minimum power level for the circuit is also required.

The effect of circuit power dissipation on circuit speed for fixed drive requirements is shown graphically in Fig. 14. Power supply values are held constant. Therefore, the circuit power dissipation is directly related to the value R_E. An increase in R_E from 150 to 900 Ω is roughly equivalent to a decrease in power by a factor of 4.

Inspection of Fig. 14 shows that at the ASLT power level both output transitions are faster than the input risetime of 1 nsec. This risetime restoration capability of the circuit is extremely important in a system such as the Model 91 where very narrow pulse widths must be transmitted. The basic circuit delays are not as dependent on the power dissipation; however, since the circuit delays are a strong function of the input risetime, t_r, the effect of power on system delay is appreciable. For the current switch emitter follower circuit and a 50 Ω system, this relationship is shown in Fig. 15.

Figure 14 Effect of emitter resistor on circuit transitions.

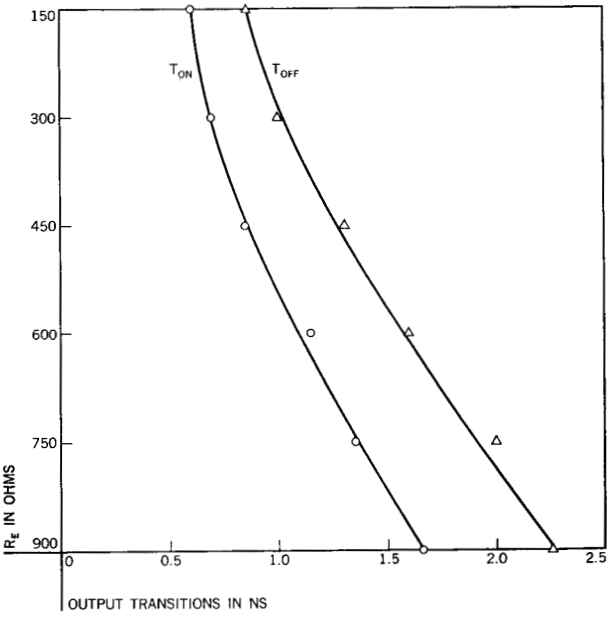


Table 6 Nominal delay circuit equations.

Out of phase delay, nsec	*In phase delay, nsec*
$T_{on} = 1.10 + 0.64\,t_r$ (input)	$T_{on}D = 1.29 + 0.68\,t_r$ (input)
$T_{off} = 1.06 + 0.53\,t_r$ (input)	$T_{off}D = 1.32 + 0.55\,t_r$ (input)
Out of phase transition, nsec	*In phase transition, nsec*
$T_r(_{on}) = 0.40 + 0.20\,t_r$ (input)	$T_r(_{on}) = 0.79 + 0.14\,t_r$ (input)
$T_r(_{off}) = 0.60 + 0.29\,t_r$ (input)	$T_r(_{off}) = 0.63 + 0.18\,t_r$ (input)

For a given input the variation in delay due to device differences is given by the following: $\sigma_D = 0.035 + 0.017\,t_r$ (input).

- *Delay prediction*

To make optimum use of ASLT circuits, an accurate delay prediction technique was required. The goal was to provide a prediction technique with an accuracy of ±10%. For ASLT technology a significant portion of the total delay is associated with the transmission of the signal, or wire delay. Since this is the case, the transient (ac) performance of the system is described by separately specifying the circuit and wire delays.

A set of empirically derived equations describes circuit delays and output transitions into a 50 Ω resistive load. The resulting circuit output transition becomes the input to the transmission line network. The transient performance of this network is likewise described in terms of wire delay and risetime degradation. This waveform becomes the input for the next circuit in the chain, etc. In this manner the path delay through a chain of logic circuits can be determined. The nominal delay equations for ASLT circuits are given as functions of the input risetime in Table 6.

Variations in delay (±0.25 nsec) and transition (±0.15 nsec) result from module layout differences, fan-in, and number of dots. The effects of temperature, power supply tolerances, dc levels, pulse width, etc., are compensating in a chain of circuits and are not used to predict path delays.

The circuit and transmission line equations have been combined into a program for the IBM 7094 computer. This permits the rapid calculation of delays across critical paths in a machine. The delay prediction program was applied to the first two data flow models built with ASLT technology, with the results shown in Table 7.

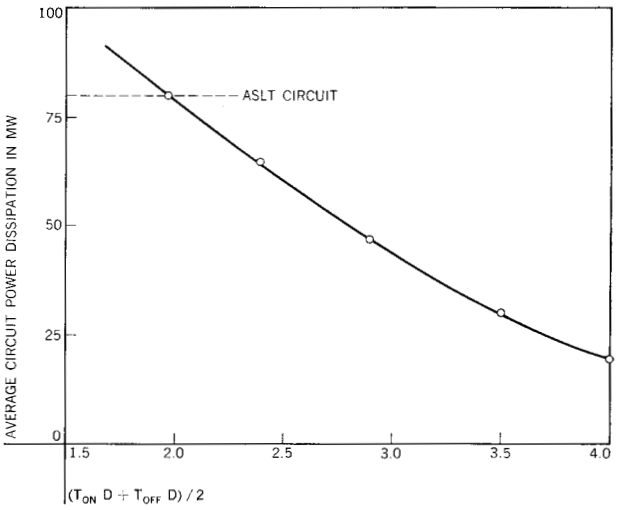
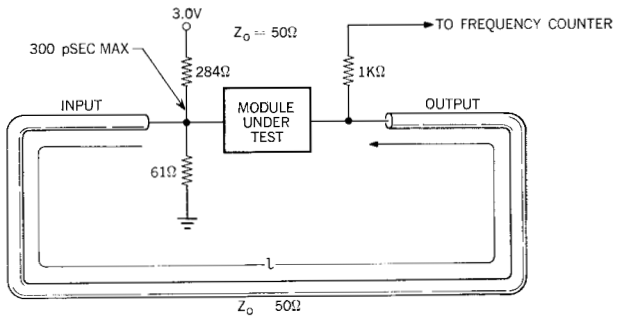


Figure 15 Effect of circuit power dissipation on overall circuit delay.

Figure 16 Circuit switching speed performance test circuit.



To date, more than 500 critical paths of the Model 91 involving more than 4,000 levels have been run with this program. The average predicted time delay per level including wire was 5.62 nsec, about 10% higher than generally measured.

- *Circulating loop test*

Efficient production testing of high speed integrated circuits is a difficult problem. The switching performance specifications for ASLT circuits are checked by means of a unique testing technique, the circulating loop test. The essential features of this test are shown in Fig. 16.

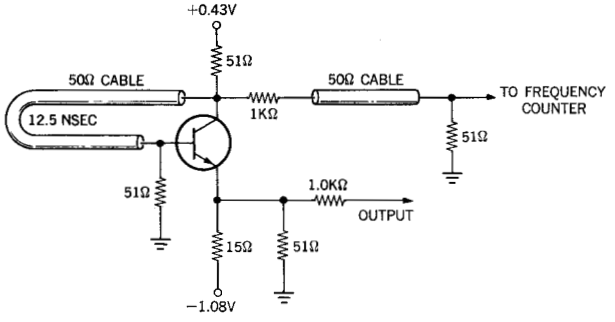
Table 7 Comparison of measured and predicted delays for data-flow models.

Model	*Description*	*Delays, nsec* *Predicted*	*Measured*
Floating-point add data flow model	23 logic blocks, 247.6 inches of wire	108	103
Multiply-divide data flow model	10 logic blocks, 50 inches of wire	57	52.5

Table 8 Effect of loading on circuit delay.

Δf	*Delay from input of line to the 10th base, nsec*		*Risetime at tenth base, nsec*		*Delay from input of line to output of the 10th load, nsec*	
	Positive-going signal	Negative-going signal	Positive-going signal	Negative-going signal	Positive-going signal	Negative-going signal
low	3.7	3.9	3.2	1.0	6.1	5.5
nominal	3.8	4.2	3.3	1.1	6.3	5.7
high	3.9	4.4	3.5	1.2	6.7	5.9
predicted	3.9	4.3	3.3	1.2	7.0	6.0

Figure 17 Transistor switching speed performance test circuit.



The input to the module under test is derived from its own output, ℓ nsec later in time. An out-of-phase circuit (inverter) connected in this manner will drive itself on and off at a frequency which is given by

$$f = \frac{1}{2\ell + T_{on} + T_{off}},$$

where

ℓ = electrical length of the cable in nanoseconds,
T_{on} = turn-on delay of the circuit,
T_{off} = turn-off delay of the circuit.

A transmission line inverter (transformer) in series with the cable permits testing of the in-phase-circuit.

The length of the cable can be adjusted to within ± 25 psec and the frequency of the loop measured to four significant figures with a frequency counter. This test provides a very sensitive, repeatable figure of merit $T_{on} + T_{off}$ for high-speed circuits such as those used in ASLT. Its advantages over standard performance tests are apparent:

- The circuit under test develops its own input waveforms.
- The frequency measurement eliminates the need for oscilloscope measurements with the inherent inaccuracies in this speed range.
- The test exaggerates differences among circuits in switching speed under a fixed input signal.

Another version of the circulating loop test is used to test transistor chips prior to committing them to an ASLT module. This test is shown in Fig. 17. Correlation between circulating frequency of the transistors $T_{on} + T_{off}$ of the corresponding module in a representative system environment appears in Fig. 18.

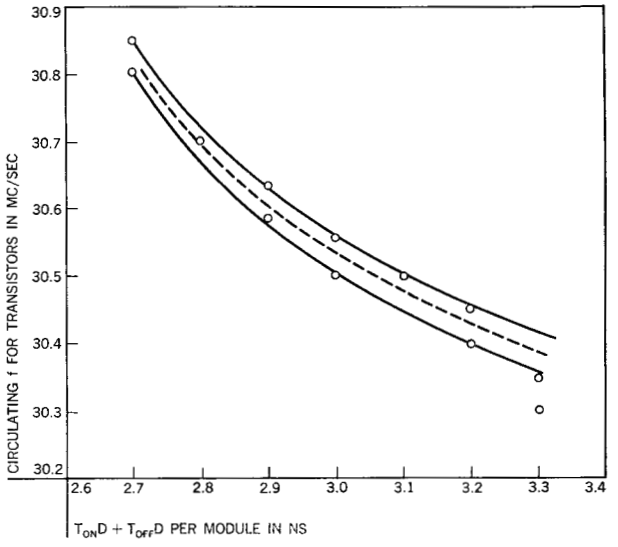
- *Δf test*

The capacitive loading effect described above is another important performance parameter which must be guaranteed to make the system delays predictable. To a first approximation, the transmission time per unit length along a segment of line loaded with C/d pF/in. is given by

$$T = T_0^{1/2}[1 + Z_0(C/d)]^{1/2},$$

where T_0 is the propagation time down an unloaded line of characteristic impedance Z_0. The value of C required for use in this equation is an average value for the circuit

Figure 18 Circulating frequency vs. module delay (from circuit performance test).



over the range of input voltages, and is not readily obtainable on a production basis. A simple method for measuring the loading effect of the ASLT circuit is shown in Fig. 19. A standard module (nominal by dc and $T_{on} + T_{off}$ criteria) oscillates without the module under test in the circuit. Connection of the module under test into the loop causes a decrease in the frequency, Δf, which is proportional to the loading effect C. Three groups of modules selected on the basis of the Δf test were successfully loaded on a 90 Ω ASLT transmission line on 1 in. spacing. The relationship between Δf and the loaded line delay was clearly demonstrated.

Longer line delays were obtained with modules exhibiting higher Δf readings. The risetime deterioration was also more severe with the heavier loads. The differences between the best and the worst case ASLT loads are shown in Table 8.

Conclusions

Achievement of the ASLT performance goals was initially demonstrated in the "floating-point add" data flow design model which was employed as a standard by the system and circuit design groups. More recently, a product test model employing over 2500 ASLT circuits has verified the achievement of the following performance goals:

- Propagation delay of 5-6 nsec in the environment.
- Delay prediction with $\pm 10\%$ accuracy.
- Environment stability independent of circuit placement.
- Adequate dc and transient performance of double level logic blocks with fan-outs up to 10.

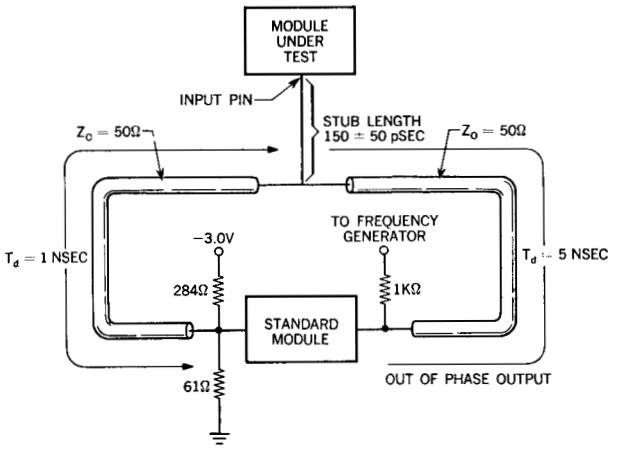


Figure 19 Circuit loading effect performance test circuit.

Acknowledgments

Although significant contributions by a number of people were required to implement the ASLT circuit family, particular mention should be given to J. L. Walsh who was largely responsible for the invention of the stabilization technique.

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Reference

1. H. N. Ghosh, "A Distributed Model of a Junction Transistor and its Application in the Prediction of the Emitter-Base Diode Characteristic, Base Impedance, and Pulse Response of the Device," *IEEE Trans. Elec. Dev.* **ED-12**, 513 (1965).

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