Effects of a Keeper on Thin Film Magnetic Bits

Abstract: When Permalloy films are used for computer storage, a magnetic keeper can improve performance by reducing the following undesirable conditions: stray fields from adjacent lines and from adjacent bits; the effect of current spreading in the ground plane; and trapped flux in the ground plane which opposes switching in the absence of a low reluctance path outside the bit. Theoretical analysis and experimental verification of these important keeper functions are presented in this paper. Through the use of high-frequency pulse techniques, effects of both metallic and non-metallic keepers, at distances from the ground plane ranging from 5 to 30 mils, have been determined. By defining efficiency as the percentage reduction in the average of four worst-case effects, the efficiency factor of a metallic keeper is shown to be 56 and that of a non-metallic keeper, 73. It is suggested that better efficiency is due more to lower electrical conductivity than to any intrinsic magnetic properties.

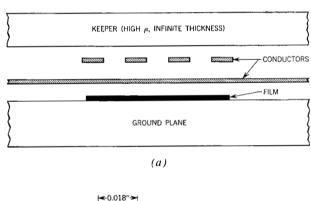
Introduction

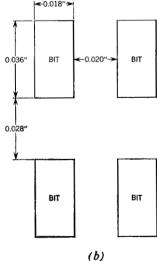
The use of a high permeability backing as a keeper in conjunction with magnetic film arrays has been considered by a number of investigators (e.g., Pohm et al.¹) as a means for reducing demagnetizing effects, worst case ground plane currents, trapped flux and line-to-line interactions. The deleterious effects of these phenomena in memory systems employing conducting ground planes have been demonstrated by Shahan and Townsend.2 In this paper, theoretical analysis and experimental verification are presented for some of the important keeper functions such as (1) augmentation of the field from a strip line at a memory element or bit; (2) diminution of the field at a bit from an adjacent strip line; (3) reduction of the flux from the bit that is trapped in the ground plane during switching; and (4) the reduction in the effect of ground plane current spreading.

In this experimental program, the memory elements, or bits, were evaporated on a thick metallic substrate which served as a ground return path. This arrangement poses two important problems. First, flux from the bit trapped in the ground plane will introduce an adverse bias field during switching for a read-1-write-0 or a read-0-write-1 sequence. Also, the current in the ground plane, which spreads when the word line over the bit under consideration is selected repeatedly and accordingly has an appreciable dc component, reduces the field available for switching.

The other factors that are important in the kind of array under consideration here are disturbing fields from

Figure 1 Cross section of the array.





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adjacent bits, and disturbing fields from adjacent lines. These four factors are referred to as "worst case effects" when conditions are chosen to maximize the adverse effect of each.

A cross section of the array used in this study is shown in Fig. 1. Read and write operations were accomplished by a sequence of word and digit current pulses that are normal for a DRO flat film array. The terminal equipment could be programmed in such a manner that specified adjacent bit orientations could be written in, and the word line over the bit under consideration as well as adjacent word lines could be selected repeatedly. The system had the additional facility of being able to provide successive incremental increases in digit current during a sequence of read-write operations. Under these circumstances the previously described worst case effects could be introduced individually or collectively at will.

Theory

• Field at the ground plane from a strip line

For intermediate frequency range problems, the field from a strip line in the presence of a keeper can be computed from Ampere's law if the keeper is replaced by an image of the strip line current. The image current I' is related to the strip line current I by

$$I' = \frac{\mu - \mu_0}{\mu + \mu_0} I, \tag{1}$$

where μ is the permeability of the keeper.³ In the presence of a conducting ground plane, multiple images must be used because of the electrical images in the ground plane of the strip line current and its aforementioned image. Equation (1) is a convenient way of calculating the effect of the poles on the surface of the keeper resulting from the penetration of the keeper interface by the field from the strip line.

When dynamic fields impinge upon the keeper interface, both transmission and reflection occur. These can be taken into account by changing Eq. (1) to the form

$$I' = I\left(-\rho + \tau \frac{\mu - \mu_0}{\mu + \mu_0}\right), \tag{2}$$

where ρ accounts for the reflected component of the incident wave, and the second term accounts for the surface poles resulting from that portion of the incident wave that penetrates the keeper interface. In these approximations, ρ and τ are reflection and transmission coefficients, and are related by

$$\tau = 1 + \rho$$
.

Using the assumptions that $\mu \gg \mu_0$, $\rho = 0$ and I = I' along with the assumption that no reflection occurs from

the back of the keeper, the field at the ground plane can be derived. Again multiple images must be used because of the presence of the ground plane.

Using Ampere's law and the method of images, and assuming uniform current distribution in the strip conductor, the tangential component of the magnetic field at the ground plane can be obtained both with and without a keeper (Fig. 2 and Eq. (3)). (Other approximations, viz., a mid-frequency addition of potentials approximation, or a four-line current approximation, can also be made. The error introduced by using the uniform current distribution approximation compares favorably with that induced by the other choices. Within the scope of this discussion, all assumptions are equally and acceptably close to the exact solution.)

Without a keeper,

$$\mathbf{H}_{t} = \frac{2I}{\pi L} \left\{ \tan^{-1} \frac{X+L}{2a} - \tan^{-1} \frac{X-L}{2a} \right\};$$

with a keeper,

$$\mathbf{H}_{t} = \frac{2I}{\pi L} \left\{ \tan^{-1} \frac{X+L}{2a} - \tan^{-1} \frac{X-L}{2a} + \sum_{n=1}^{\infty} \left(\tan^{-1} \frac{X+L}{2(2nd-a)} - \tan^{-1} \frac{X-L}{2(2nd-a)} \right) - \sum_{n=1}^{\infty} \left(\tan^{-1} \frac{X+L}{2(2nd+a)} - \tan^{-1} \frac{X-L}{2(2nd+a)} \right) \right\},$$
(3)

where \mathbf{H}_{t} = tangential component of the magnetic field at the ground plane,

X = horizontal distance along ground plane from a point directly under the strip line,

L =width of strip line,

d =distance from ground plane to keeper, and

a =distance from ground plane to strip line.

Equation (3) can be used to compute the field from either the word line or the digit line and forms the basis for a number of correlations with experimental data to be presented subsequently. One of the important results of calculations based upon Eq. (3) is that the field at a bit immediately under the word line is augmented, while that at an adjacent bit is diminished. A numerical solution using Eq. (3) for a particular geometry is shown in Fig. 3. The error induced by the uniform current distribution approximation is within 10% of the exact solution for the same geometry.

• Ground plane current spreading

When any particular word line is repeatedly selected, the word current gains an appreciable dc component. The dc component spreads throughout the ground plane, and

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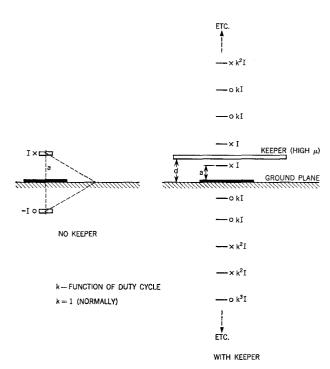
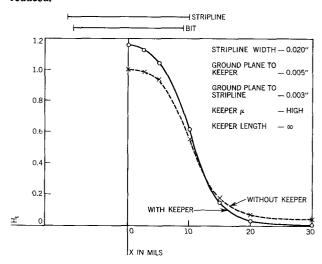


Figure 2 Model for calculating the field at the ground plane.

Figure 3 Plot of \mathbf{H}_t vs distance from center of bit. With a keeper \mathbf{H}_t at x=0 is enhanced and \mathbf{H}_t at x=30 mils is reduced.



the field from the ground plane image at the bit is reduced. With a keeper the effects of ground plane current spreading are diminished. The keeper provides a low reluctance path which tends to keep the H field immediately below the conductor near its original value.

Equation (3) still provides an excellent approximation of the field at the bit if the electrical image in the ground plane is reduced to I' = kI where $k \le 1$ and is dependent

on the duty cycle of the drive line current. The appropriate modification of Eq. (3) to account for the ground plane current spreading is

$$\mathbf{H}_{t} = \frac{I(1+k)}{\pi L} \left\{ \tan^{-1} \frac{X+L}{2a} - \tan^{-1} \frac{X-L}{2a} + \sum_{n=1}^{\infty} (-k)^{n-1} \left[\tan^{-1} \frac{X+L}{2(2nd-a)} - \tan^{-1} \frac{X-L}{2(2nd-a)} \right] + \sum_{n=1}^{\infty} (-k)^{n} \left[\tan^{-1} \frac{X+L}{2(2nd+a)} - \tan^{-1} \frac{X-L}{2(2nd+a)} \right] \right\}.$$

$$(4)$$

Without a keeper $(d = \infty)$ both summations drop out and the value of k has an appreciable effect upon \mathbf{H}_t . With a keeper, the dependence of \mathbf{H}_t upon k is diminished considerably because of partial cancellation by terms of alternating sign in the series. As a result, the presence of a keeper makes the array quite insensitive to ground plane current spreading.

• Trapped flux

When a conducting ground plane is used, that portion of the bit flux which penetrates the ground plane becomes trapped during switching by the long time constant of the eddy currents in the ground plane. When the bit is switched, the lines of B in the ground plane which previously closed their path through the bit must now close in air about the bit, resulting in a bias field opposing the switching which is approximately equal to the demagnetizing field. The presence of a keeper provides a low reluctance flux path for the field from the bit so that little flux penetrates the ground plane. The fractional reduction in the total flux penetrating the ground plane can be computed by replacing the keeper with a magnetic image of the bit. Assuming, as a first approximation, that the bit poles are all located at the ends of the bit, the procedure outlined above results in the following relationship:

$$\delta = \frac{\mu - \mu_0}{\mu + \mu_0} \left\{ 1 - \frac{2}{\pi} \tan^{-1} \frac{2d}{\ell} \right\},\tag{5}$$

where δ is the fractional decrease in ground plane flux, ℓ is the bit length, and d, as before, is the distance from the ground plane to the keeper.

Similar techniques should be applicable to the calculation of the field at a particular bit for neighboring bits, but the result would be too dependent upon array geometry to be of general interest.

Experiment

It should be possible to correlate the theoretical development of the preceding sections with appropriate measurements made upon a conventional flat film DRO array

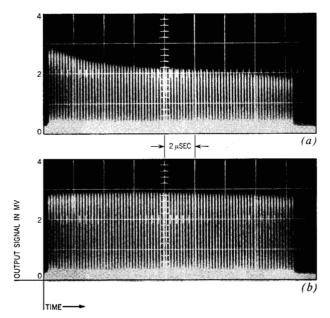


Figure 4 Effect of ground plane current spreading: (a) without a keeper; (b) with a keeper. Clock frequency, 5 Mc/sec; duty cycle, 80%; pulse amplitude, 400 mA; non-metallic keeper.

Table 1 Correlation of calculated decrease in trapped flux with decrease in experimentally observed incremental digit current.

Distance from ground plane to keeper (mils)	Fractional decrease of flux in ground plane* (per Eq. 5)	Fractional decrease in digit current required to overcome trapped flux* bias (using a non-metallic keeper)
5	0.69	0.64
10	0.47	0.49
15	0.35	0.38
20	0.27	0.29
25	0.22	0.25
30	0.20	0.23

^{*} Bit length 36 mils; pulse repetition rate 5 Mc/sec.

Table 2 Worst case effects and keeper efficiency

	Efficiency as a percentage reduction in worst case effects	
Worst case effects	Metallic keeper	Non-metallic keeper
Trapped flux effect	40	64
Ground plane current spreading effect	55	73
Stray field from adjacent bit lines	67	75
Stray field from adjacent bits Overall efficiency	80 56	100 73

(see Fig. 1). In particular, the trapped flux effect can be evaluated by comparing the digit current required for a read-1-write-1 sequence with that required for a read-1-write-0 sequence. In one case, trapped flux aids in writing and in the other case, it opposes writing.

In Table 1, the fractional decrease in trapped flux, as calculated from Eq. (5) with $\mu \gg \mu_0$, is correlated with the observed decrease in the incremental digit current required to overcome trapped flux bias. The correlation is made for various distances from the ground plane to the keeper. The good correspondence between these is expected since the bias field produced by trapped flux varies linearly with the total trapped flux.

Equation (3) can be used to evaluate the field from a strip line at an adjacent bit with and without a keeper. With a keeper the stray field at a distance of 30 mils is reduced by a calculated factor of 93.5% for the particular geometry shown in Fig. 1. Experimentally, the reduction in the stray field at 30 mils for the same geometry is 100% with a non-metallic keeper, and 92% with a metallic keeper.

The effect of ground plane current spreading can be examined by plotting the output signal vs. time for repeated selection of a particular word line. It was predicted qualitatively in a prior section that the keeper should reduce the effect of ground plane current spreading upon the field available for switching the bit. This is verified by the data shown in Fig. 4. For a particular duty cycle the field available for switching the bit is reduced by 15% without a keeper; and with a keeper the reduction is only 5%.

When the various array conditions are chosen to maximize the adverse fields during writing, each of these can be evaluated as before in terms of the incremental digit current required to write in their presence. The fractional reduction in incremental drive current required to overcome these adverse effects is an index of keeper efficiency. A summary of the experimental data is given in Table 2.

Conclusions

Table 2 shows that a keeper improves the performance of the thin film magnetic bits considerably, and that ferrite materials perform more effectively than the metallic keepers. A good correlation between the theoretical predictions and actual measurements has been obtained.

The role of conductivity of the keeper materials at high frequencies was not considered in detail in the discussion above. Therefore, one of the important problems to be investigated will be to determine the explicit effect of conductivity, and permittivity, upon keeper performance. It has been possible to simulate the effect of changing the ac conductivity without changing the magnetic properties of a keeper by mixing various proportions of powdered copper with powdered ferrite. Qualitatively, the increase in the conductivity increases the reflection

from the keeper surface ($\rho \neq 0$ in Eq. (2)). This tends to reduce the field below the keeper and decrease the keeper efficiency. Typically, 10% copper (by weight) mixed with a powdered ferrite will reduce the keeper efficiency from 75% to 45%. This result suggests the role of conductivity on keeper efficiency.

Acknowledgments

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