

On Measures of Logic Performance: Logic Quantum, Factor, and Figure of Merit†

Abstract: A basic logic operation is considered of transferring a logic decision from one point to another point. A certain energy level, W_L , corresponding to decision threshold and a time delay, T_L , are encountered in the transfer process. The product, $W_L T_L$, is a logic quantum, H_L . If the logic transfer takes place through an intermediate device, a logic factor, F_L , can be introduced to describe the reduction in logic quanta that the device can produce under optimum conditions. Optimization is carried out, as for instance with ideal transformers, to "match" the logic source to the device and the device to the logic detector. The condition $F_L = 1$ marks a boundary between a useful and a useless device, and a logic figure of merit, T_{FM} , in units of time corresponds to the fastest source-detector combination such that $F_L = 1$. Logic performance is considered in some detail for a particular linear model of a device. Nonlinear devices and relay devices are considered in less detail, although some numerical calculations are given for a current-switch, two-transistor computer device. The logic figure of merit represents a unique measure of high-speed logic performance and is therefore valuable in comparing devices including associated circuitry on a common basis.

Symbols

A_{WL}	Logic energy amplification
F_L	Factor describing reduction in logic quanta the device can produce under optimum conditions
G_S	Source conductance
H_L	Logic quantum equal to $W_L T_L$
P_S	Available power from logic source
R_S	Source resistance
T_L	Time interval at which detector arrives at logic threshold
T_{FM}	Logic figure of merit
T_d	Device time delay
W_L	Energy level corresponding to logic threshold
W_R	Relay threshold energy

Introduction

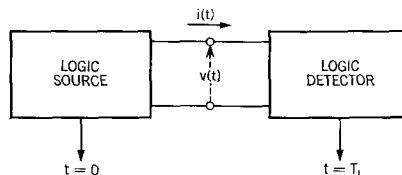
In a computer a number of logic functions are performed. These functions are carried out with the aid of neutral, passive, and active components. For alternate designs or alternate components, the question arises as to which is better. For this purpose, measures of logic performance which relate closely to actual operation are useful. A single measure of performance would be ideal, but such hardly appears feasible in view of the many design requirements. High-speed operation is one of the major design objectives. It is generally found that other design objectives can be

traded off for speed, and so a measure of high-speed performance would appear to be a good single measure of logic performance.

Basic logic operation

Of the many logic functions performed in a computer, the basic logic operation is considered here as that of feed-in and feed-out—that is, combining several logic decisions into one, or distributing a logic decision to a number of loads. This basic logic operation is shown in Fig. 1, where the several logic sources are shown combined into a single source, and similarly the several loads are shown combined into a single load. Thus the basic logic operation is reduced to that of transferring a logic decision from one point to another point.

Figure 1 Basic logic operation.



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† Work performed at Thomas J. Watson Research Center, summer 1964.

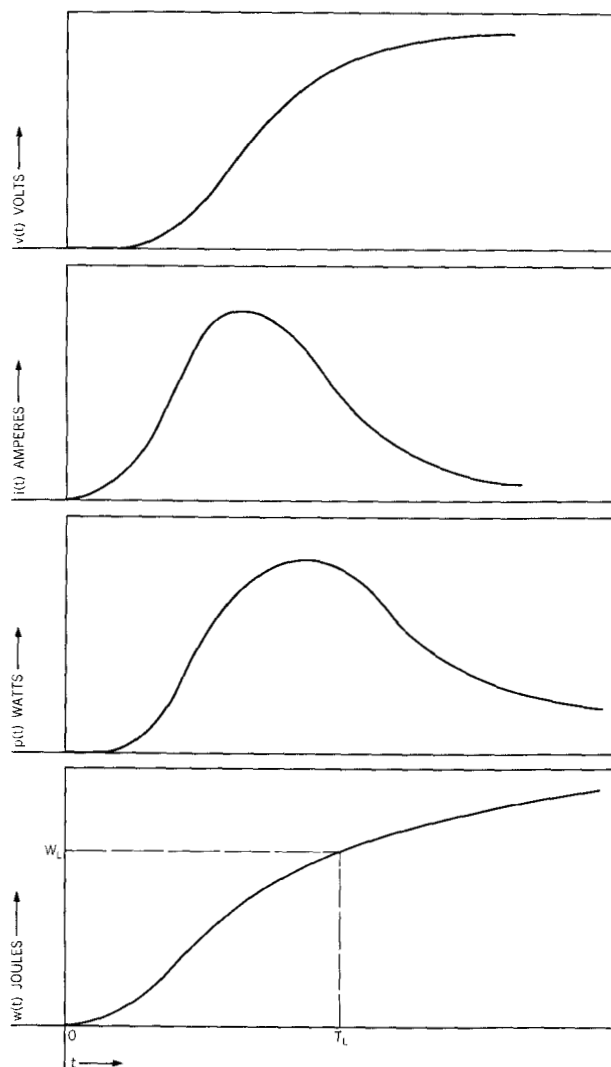


Figure 2 Typical wave shapes of basic logic operation.

At $t = 0$ the logic source originates a logic decision and makes power available to the logic detector to transfer the logic decision. The logic detector receives power until at some logic time, T_L , an energy, W_L , corresponding to a logic threshold is received. At $t = T_L$ then, the logic detector makes its logic decision. Typical wave shapes associated with this basic logic operation are shown in Fig. 2.

Fundamental definitions

In order to make its logic decision, the logic detector has received logic energy, W_L , in the time interval, T_L . We can define a logic quantum, $H_L = W_L T_L$. The use of logic quantum here is closely allied with the quantum associated with an observation, which indeed is what the logic decision is. In an observation, quanta correspond to uncer-

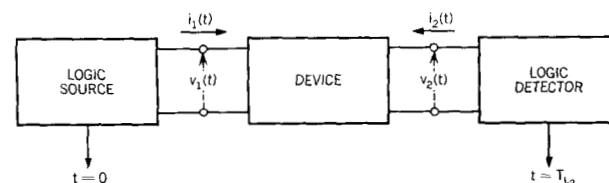
tainties in energy, Δw , and time, Δt , associated with the observation. Similarly, in the logic case, T_L can be considered as an uncertainty in time and W_L an uncertainty in energy. In the limiting accuracy of an observation, Δw and Δt are inversely related and the Heisenberg uncertainty principle establishes the product as approximately the quantum of action, h . Computers as operated today are a long way from the limiting condition¹ although the trend of development is certainly in the direction of reduced logic energy and reduced logic time. Since present operation is a long way from the limiting condition, we can expect that both logic energy and logic time can be reduced simultaneously. Simple means, e.g., by decreasing the size of the logic detector, can be employed to reduce logic energy. Smaller logic energy will generally mean larger frequency of errors, and there exists a trade-off between small logic energy and small frequency of errors. This trade-off situation does not enter into the consideration except as a possible basis for the design choice of a feasible logic energy. This choice then determines, in part, a definite logic factor. Generally the choice of logic energy is made on the basis of worst-case design, but for very small logic energies, statistical probabilities of errors (noise) can become significant.² No *a priori* choice of logic energy is required in formulating the logic figure of merit. Rather, the determination of the logic figure of merit may have associated with it an optimum logic energy.

By "matching" the logic detector to the logic source, we can arrange to minimize the logic quanta. This logic match achieves an optimum value of logic quantum, $H_L|_{op}$. Frequently W_L is fixed so that minimizing H_L is accomplished by minimizing T_L . Otherwise, W_L can be formulated as a function of T_L (or vice versa) and the optimization carried out. In any event, there results an optimum (minimum) logic time, $T_L|_{op}$.

Consider now that a device is interposed between the logic source and detector as shown in Fig. 3. We now have an output logic quantum $H_{L_s} = W_{L_s} T_{L_s}$ delivered to the detector. Depending upon how the device is interposed, we have:

- 1) insertion logic quanta if device is interposed without changes in the source and detector;
- 2) output optimized logic quanta if device is interposed

Figure 3 Logic operation with interposed device.



and detector is logic matched to the device to minimize H_{L_s} ;

- 3) input optimized logic quanta if device is interposed and source is logic matched to the device to minimize H_{L_s} ;
- 4) optimized logic quanta, $H_{L_s}|_{op}$, if device is interposed and source and detector are simultaneously logic matched to the device to minimize H_{L_s} .

If $H_{L_s}|_{op} < H_L|_{op}$, the device has improved the logic situation and for instance we could then expect to fan-out without an increase in logic time. A logic factor, F_L , can be defined to measure the extent to which the device has improved the logic situation.

$$F_L = \frac{H_{L_s}|_{op}}{H_L|_{op}} = \frac{(W_{L_s} T_{L_s})|_{op}}{(W_L T_L)|_{op}} \Rightarrow \frac{T_{L_s}|_{op}}{T_L|_{op}}. \quad (1)$$

The limiting form of F_L is applicable if $W_{L_s} = W_L =$ constant independent of the "matching" operation. In all subsequent work this condition is assumed to hold and the limiting form of F_L will be used. A quantity of related interest is the logic energy amplification, A_{W_L} , defined as

$$A_{W_L} = \frac{\text{Energy delivered to detector at } T_{L_s}|_{op}}{\text{Energy delivered to device input at } T_L|_{op}} = \frac{w_{L_s}(T_{L_s}|_{op})}{w_{L_s}(T_L|_{op})}. \quad (2)$$

In formulating $w_{L_s}(t)$, $w_{L_s}(t)$ and similar quantities, the corresponding values at $t = 0$ are considered as zero reference, so the quantities of interest are actually changes in energy. Design constraints generally will not permit logic matching. This fact in itself does not detract from the usefulness of logic factor as a measure of logic capability. The situation here is quite similar to the usefulness of noise factor as a measure of noise capability and not of actual performance. If desired, ratios of nonoptimized logic quanta can be formulated, but it should be clearly understood that the result is a *measure of actual performance* and not a measure of potential performance.

As the logic energy of the detector, W_L , is reduced, it will be more difficult for the device to effect an improvement in the logic situation and the logic factor can be expected to increase. Similarly, as the available power from the logic source, P_s , is increased the logic factor can be expected to increase. There may be values of W_L and P_s such that $F_L = 1$. In this event, the device is neither improving nor worsening the logic situation; the source could just as well be connected directly to the logic detector to achieve the same logic time. This situation then marks a boundary between a useful and a useless device, and can be employed to obtain a measure of the device

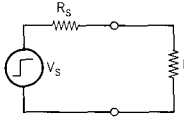
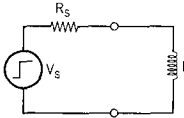
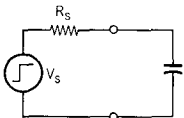
TYPE	IDEAL LOGIC SOURCE-DETECTOR	LOGIC MATCH CONDITION	OPTIMUM LOGIC TIME
RESISTIVE		$R _{op} = R_s$	$T_{L op} = W_L/P_s$
INDUCTIVE		$L _{op} = 3.9W_L/I_s^2$	$T_{L op} = 1.23W_L/P_s$
CAPACITIVE		$C _{op} = 3.9W_L/V_s^2$	$T_{L op} = 1.23W_L/P_s$

Figure 4 Basic ideal logic source-detector types.

utility for logic operation. Thus we can define a logic figure of merit, T_{FM} , for the device as

$$T_{FM} = \frac{W_L}{P_s} \Big|_{F_L=1}. \quad (3)$$

This measure of the device is made unique by indicating that not only do we select values of W_L and P_s such that $F_L = 1$, but additionally we select the optimum value of W_L and P_s such that T_{FM} is minimum.

Ideal source-detector combinations

An ideal logic source is considered to be a step voltage of amplitude, V_s , in series with a source resistance, R_s , such that the maximum power available from the source is $P_s = V_s^2/4R_s$, or equivalently a step current of amplitude, I_s , in shunt with a source conductance, G_s , such that the maximum power available from the source is $P_s = I_s^2/4G_s$. An ideal logic detector utilizes all the energy delivered to it to arrive at the logic decision. Thus a resistive ideal logic detector uses all the thermal energy received to form a logic decision. Approximate examples might be:

- 1) devices that deform suddenly when a threshold temperature is reached, like the "Klixon" device;
- 2) devices containing magnetic elements that have a threshold Curie temperature where the magnetic susceptibility changes discontinuously;
- 3) devices containing superconducting elements that have a threshold superconductivity temperature where the conductivity changes discontinuously.

The logic match of the resistive ideal logic detector to the ideal source (Fig. 4) is the same as for a maximum power match, namely, $R|_{op} = R_s$; then the optimum logic

time is $T_L|_{op} = W_L/P_S$. The variation of energy in the resistive detector is shown in Fig. 5. The construction of T_L and $T_L|_{op}$ associated with a given W_L and P_S is also shown. For a given W_L and P_S , the resistive ideal logic detector is capable of reaching a logic decision in the shortest time so we shall use $T_M = W_L/P_S$ for this minimum logic time.

An inductive ideal logic detector (Fig. 4) uses all the magnetic energy received to form a logic decision. Approximate examples are:

- 1) magnetic relays which close when a threshold current is reached;
- 2) magnetic cores which reverse their direction of magnetization when a threshold current is reached.
- 3) cryotron devices that change their superconductivity state when a threshold current produces a critical magnetic field.

The variation of energy in an inductive detector is shown in Fig. 6. Assuming that $W_L < \frac{1}{2}LI_S^2$, the equation for the logic time is

$$W_L = \frac{1}{2}LI_S^2[1 - \exp(-T_L/T)]^2, \quad (4)$$

where $T = L/R_S$. Introducing $T_M = W_L/P_S$, this can be written as

$$T_M = 2T[1 - \exp(-T_L/T)]^2. \quad (5)$$

We now seek to logic match the inductor to the source by minimizing T_L with respect to L and therefore with

Figure 5 Variation of energy in resistive detector.

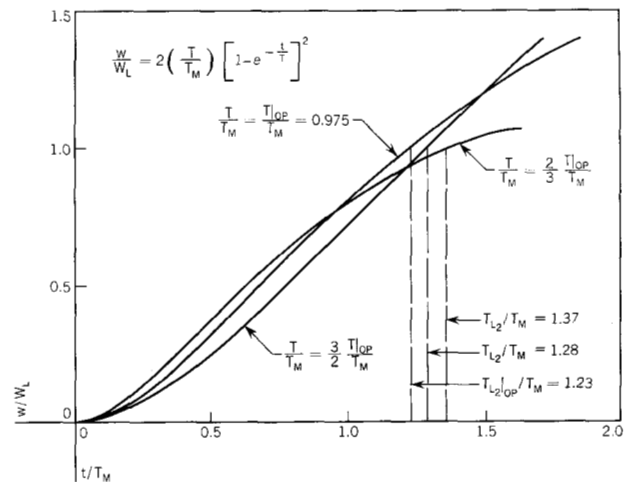
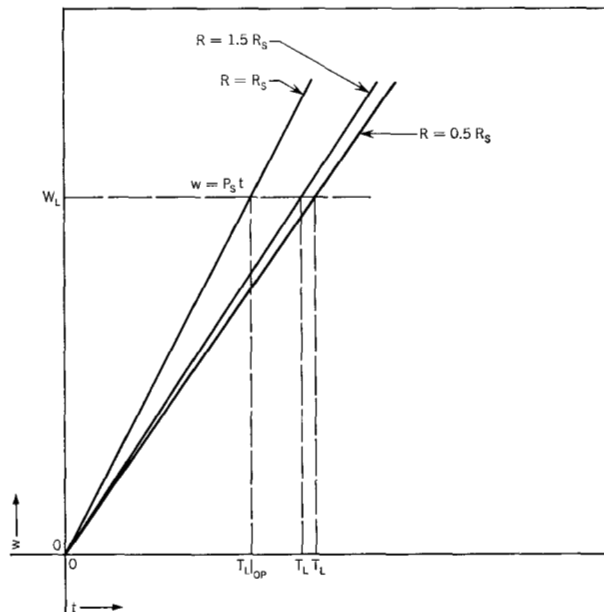


Figure 6 Variation of energy in inductive and capacitive detectors.

respect to T . The resulting equation for $x = T_L|_{op}/T|_{op}$ is $1 - e^x + 2x = 0$. (6)

This has the solution $T_L|_{op} = 1.26T|_{op}$. Additionally from Eq. (5), $T_M = 1.023T|_{op}$, so $T_L|_{op} = 1.23T_M$ and $L|_{op} = 0.975T_MR_S$. The formulation of an optimum value of the inductor is shown in Fig. 6 in relation to three separate values of T/T_M , one of which is the optimum value.

A capacitive ideal logic detector (Fig. 4) uses all the electric energy received to form a logic decision. Approximate examples are:

- 1) gas discharge devices which discharge when a threshold voltage is reached;
- 2) ferroelectric devices which reverse their direction of polarization when a threshold voltage is reached.

The variation of energy in a capacitive detector is identical with that in an inductive detector; Fig. 6 with $T = R_SC$ applies, so the optimum capacitor value is $C|_{op} = 0.975T_M/R_S$.

In the same manner that ideal transformers are employed to provide for power match, ideal transformers can be employed for logic matching any resistor, capacitor or inductor to an ideal logic source.

Logic factor of general devices

If a device is interposed between the ideal logic source and ideal logic detector as in Fig. 3, there will be a new logic time, T_{L_s} . By employing ideal transformers at both input and output of the device, T_{L_s} can be minimized to achieve $T_{L_s}|_{op}$. The logic factor can then be formed as $F_L = T_{L_s}|_{op}/T_L|_{op}$. Note that $T_{L_s}|_{op}$ may be different depending

upon whether the logic change is from state 0 to state 1 or vice versa. There will then be two values of logic factor to be considered.

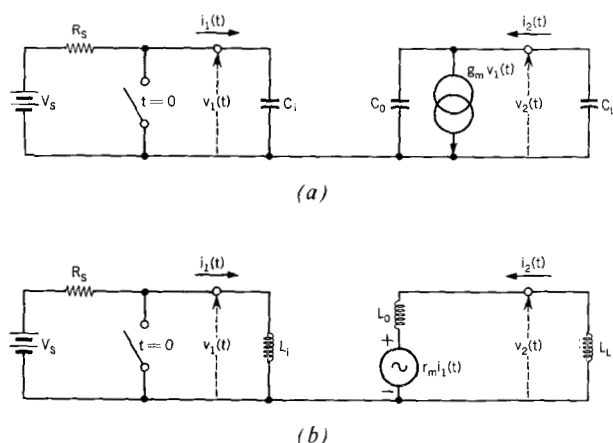
The logic factor for some general devices is:

- 1) If the device is a direct connection, $F_L = 1$.
- 2) If the device is an ideal (no losses, no energy storage) transformer, $F_L = 1$.
- 3) If the device is a resistive network, $F_L > 1$. This follows since, by looking back from the detector, the source-device combination can be replaced via Thevenin's theorem by a new ideal source with less available power.
- 4) If the device is a passive network (including a transmission line), $F_L > 1$. This follows since the dissipative elements of the network will reduce the available power, and the energy storage elements will cause less energy to be delivered to the detector.
- 5) If the device is an ideal delay such that the output signals are the input signals delayed by T_d , $F_L = 1 + (T_d/T_{L_{op}})$. This follows since the delay is directly additive and $T_{L_{op}} = T_{L_{op}} + T_d$.

Logic factor of a linear device

If the device is linear then $v_2(t) = V_s f(t)$. For a capacitor as the logic detector, $W_L = \frac{1}{2} C_L v_2^2(T_{L_s}) = \frac{1}{2} C_L V_s^2 f^2(T_{L_s})$. Then $2C_L R_s f^2(T_{L_s}) = W_L/P_s = T_M$. The quantity T_{L_s} can be minimized with respect to C_L and R_s with the result that $T_{L_s}|_{op} = f_1(T_M)$. Finally, $F_L = T_{L_s}|_{op}/1.23T_M = f_2(T_M)$. Similarly this is true for a resistive or inductive logic detector. This result indicates that for a linear device W_L and P_s will be linearly related for constant values of logic factor as will be shown subsequently in the analysis of the model in Fig. 7a. Stated differently, for a linear device the logic factor will depend only upon the ratio of logic energy and available power. Dividing both by a constant will leave the logic factor unchanged.

Figure 7 Logic circuit with a linear device (a) electron tube—nodal type (b) cryotron—loop type.



The details in the formulation of F_L for a linear device will depend upon the model of the device. A simple model that serves to bring out some of the properties of F_L and problems in forming it is shown in Fig. 7a. This model is applicable to pentode tubes and similar devices. A more complicated model of linear devices is considered in Appendix I.

With $T_1 = R_s C_i$ we have

$$v_1(t) = V_s [1 - \exp(-t/T_1)], \quad (7)$$

$$\begin{aligned} v_2(t) &= -\frac{g_m}{(C_0 + C_L)} \int_0^t v_1(t) dt \\ &= \frac{g_m V_s T_1}{(C_0 + C_L)} \left[1 - \exp\left(-\frac{t}{T_1}\right) - \frac{t}{T_1} \right]. \end{aligned} \quad (8)$$

Then

$$\begin{aligned} \frac{W_L}{P_s} &= T_M \\ &= \frac{2g_m^2 C_L R_s T_1^2}{(C_0 + C_L)^2} \left[1 - \exp\left(-\frac{T_{L_s}}{T_1}\right) - \frac{T_{L_s}}{T_1} \right]^2. \end{aligned} \quad (9)$$

Minimization of T_{L_s} with respect to C_L can be accomplished by maximizing $C_L/(C_0 + C_L)^2$ with respect to C_L . The result is that $C_L|_{op} = C_0$, and Eq. (9) can be written as

$$T_M T_D^2 = T_1^3 \left[1 - \exp\left(-\frac{T_{L_s}}{T_1}\right) - \frac{T_{L_s}}{T_1} \right]^2, \quad (10)$$

where

$$T_D = (2C_i C_0)^{1/2} / g_m. \quad (11)$$

The logic match at the input port can be accomplished by minimizing with respect to R_s or equivalently with respect to T_1 . The resulting equation for $T_{L_s}|_{op} = x T_1|_{op}$ is

$$3x - (1 - e^{-x})(3 + 2x) = 0. \quad (12)$$

The solution is $x = T_{L_s}|_{op}/T_1|_{op} = 2.15$. From Eq. (10), $T_M T_D^2 = 1.60 T_1^3|_{op}$. Therefore $T_{L_s}|_{op} = 1.84 (T_M T_D^2)^{1/3}$ so finally,

$$F_L = T_{L_s}|_{op}/1.23 T_M = 1.495 (T_D/T_M)^{1/3}. \quad (13)$$

This result is shown in Fig. 8. The slope of the radial lines correspond to T_M . The value of T_M for $F_L = 1$ is T_{FM} , the logic figure of merit for the device:

$$T_{FM} = 1.83 T_D. \quad (14)$$

This result³ indicates that the logic time cannot be reduced by this device if the ratio of logic energy to source available energy, W_L/P_s , is less than $1.83 T_D$.

Suppose that the device corresponding to Fig. 7a is followed by a second similar device. Let the two devices be coupled together via an ideal transformer with N turns on the No. 1 device output side and 1 turn on the No. 2 device input side. In this case then

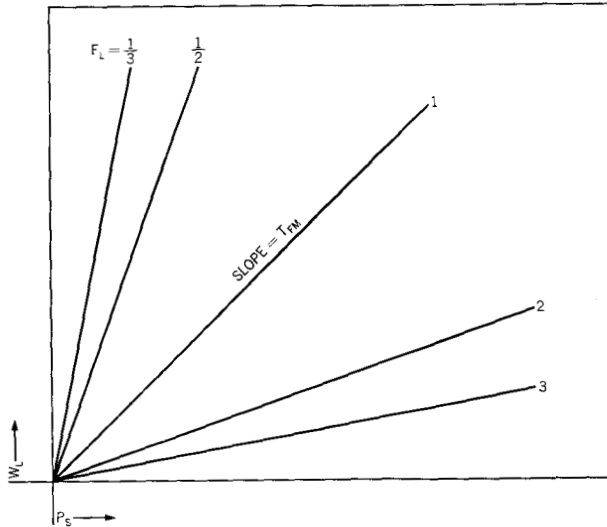
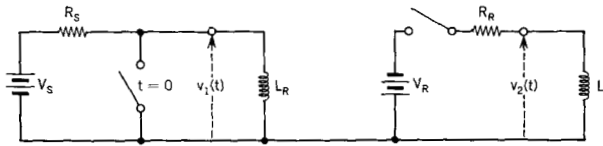


Figure 8 Typical variation of logic energy and available source power for a linear device.

Figure 9 Relay logic circuit.



$$T_M = \frac{2g_{m1}g_{m2}C_L R_S T_1^4}{N^2(C_{01} + C_{i2}/N^2)(C_{02} + C_L)^2} \cdot \left[1 - \exp\left(-\frac{T_{L2}}{T_1}\right) - \frac{T_{L2}}{T_1} + \frac{1}{2}\left(\frac{T_{L2}}{T_1}\right)^2 \right]^2 \quad (15)$$

with $T_1 = R_S C_{i1}$. The minimization of T_{L2} with respect to C_L requires that $C_L|_{op} = C_{02}$; minimization with respect to N requires that $N = (C_{i2}/C_{01})^{1/2}$; minimization with respect to R_S or equivalently with respect to T_1 is provided by the root of

$$3x - \frac{1}{2}x^2 - 5(1 - e^{-x}) + 2xe^{-x} = 0. \quad (16)$$

The solution is $x = T_{L2}|_{op}/T_1|_{op} = 3.105$; also, from Eq. (15), $T_{L2}|_{op} = 2.407(T_M T_{D1}^2 T_{D2}^2)^{1/5}$ with T_{D1} and T_{D2} given by Eq. (11) with 1 and 2 subscripts, respectively. The logic factor and logic figure of merit of the composite device corresponding to the cascade combination of two devices of Fig. 7a are

$$F_L = 1.956 \left[\frac{T_{D1}^2 T_{D2}^2}{T_M^4} \right]^{1/5} \quad (17)$$

$$T_{FM} = 2.322(T_{D1} T_{D2})^{1/5}. \quad (18)$$

These results can be recast in terms of individual device values as given by Eqs. (13) and (14):

$$F_L = 1.207(F_{L1} F_{L2})^{3/5}. \quad (19)$$

$$T_{FM} = 1.27(T_{FM1} T_{FM2})^{1/5}. \quad (20)$$

The composite results are independent of whether device 1 precedes or follows device 2. If the individual devices are identical, $F_{L1} = F_{L2} = 0.855$ is required in order that $F_L = 1$ and then, $T_{FM} = 1.27T_{FM1}$.

Identical results can be obtained for the linear device model shown in Fig. 7b, which is the dual of the device model of Fig. 7a. The model of Fig. 7b is applicable to cryotrons and similar devices. The previous results are generally applicable with the redefinition of $T_1 = L_i/R_i$ and $T_D = (2L_i L_0)^{1/2}/r_m$.

Logic factor of a relay device

A relay is a device that operates ON-OFF and therefore is grossly nonlinear. It is sometimes considered an amplifying device in the sense that a small amount of power can be used to control a much larger amount of power. However, it is not an amplifying device for logic purposes, for, as we shall see, the logic factor is normally greater than unity.

Consider the logic circuit as shown in Fig. 9. An inductor is assumed as the logic detector. The relay coil is L_R and a resistor R_R is shown in series with the relay contacts. Further, the relay is assumed imperfect as there is a fixed delay, T_d , between the time when L_R has threshold energy, W_R , and the time when the contacts begin to close, and the time when contact closure is made. The device input and output operate independently so that optimization for minimum T_{L2} can be made by logic matching at input and output ports independently. The "match" conditions are the same at both ports and are

$$L_R|_{op} = 3.9 W_R R_S^2 / V_S^2, \quad L_L|_{op} = 3.9 W_L R_R^2 / V_R^2$$

A time interval, $T_1 = 1.23 W_R / P_S$, is required before relay threshold energy is reached; an additional interval, T_d , is required before contact closure is made; and an additional interval $T_2 = 1.23 W_L / P_R$ is required before output logic time is reached. Therefore $T_{L2}|_{op} = T_1 + T_d + T_2$, and

$$F_L = \frac{T_{L2}|_{op}}{1.23 T_M} = \frac{W_R}{W_L} + \frac{P_S}{P_R} + \frac{T_d}{1.23 T_M}. \quad (21)$$

Now, normally, at best $W_R = W_L$ since if W_R were less than W_L , the relay could advantageously be used as the detector; as $R_R \rightarrow 0$, $P_R = V_R / 4R_R \rightarrow \infty$. Thus, in the limit of an ideal relay with $R_R = 0$ and $T_d = 0$, $F_L = 1$; the relay device can normally not produce a logic time less than that associated with the source-detector combination.

For the general situation where the relay closure energy might be less than the logic energy, $F_L < 1$ is possible.

The constant logic factor contours are shown in Fig. 10 for the special case when $K = T_d P_R / 1.23 W_R = 0$. As before, the $F_L = 1$ contour is of special interest. For $F_L = 1$, there is some combination of W_L and P_S such that their ratio, T_M is a minimum and equal to the logic figure of merit,

$$T_{FM} = \frac{K^2}{[\sqrt{1+K}-1]^2} \frac{W_R}{P_R} \Rightarrow 4 \frac{W_R}{P_R} \quad (22)$$

The associated values of W_L and P_S are:

$$W_L = (T_{FM} P_R W_R)^{\frac{1}{2}} \quad P_S = \left(\frac{P_R W_R}{T_{FM}} \right)^{\frac{1}{2}} \quad (23a, b)$$

Suppose that the ideal logic source is itself one of the relays; i.e., consider a chain of identical relays. Then $W_R = W_L$ and $P_S = P_R$, so

$$F_L = 2 + \frac{T_d}{1.23 T_M} \quad (24)$$

In a chain operation of identical relays, the smallest logic factor that can be achieved is 2.

Logic factor of nonlinear devices

The formulation of the logic factor of a nonlinear device proceeds along the same lines as for a linear device. For an ideal logic detector with logic energy, W_L , and an ideal logic source of available power, P_S , the input and output are first logic matched for minimum logic time. This can

be done by changing R_S while keeping P_S constant at the input and changing C_L , L_L , or R_L while keeping W_L constant. There results an $R_S|_{op}$ and a $C_L|_{op}$, $L_L|_{op}$ or $R_L|_{op}$ and an associated $T_{Ls}|_{op}$. F_L can then be computed. These steps are then repeated for different values of W_L and P_S . Contours of constant F_L similar to Figs. 8 and 10 can be developed. Then the W_L and P_S values associated with the $F_L = 1$ contour which have the smallest ratio permit a unique figure of merit rating of the nonlinear device.

Because of nonlinearity, the steps as outlined will generally have to be carried out by numerical methods. An example is given in Appendix II for a current-switch circuit employing two transistors. If the nonlinear device is passive, then $F_L > 1$ as for a linear device; if the nonlinear device is active, then F_L may be less than unity if operation is through a region of power amplification.

Arbitrary source-detector combinations

Logic factor and logic figure of merit are useful in evaluating the ultimate logic capabilities of a device. For this purpose it is appropriate to consider the device in conjunction with an ideal source and an ideal detector. In an actual circuit the source and detector will generally be nonideal and logic times will be greater than that indicated by the logic figure of merit. As a figure of merit, T_{FM} serves only as a unique yardstick of comparison and cannot indicate the logic time that can be achieved with arbitrary source-detector combinations.

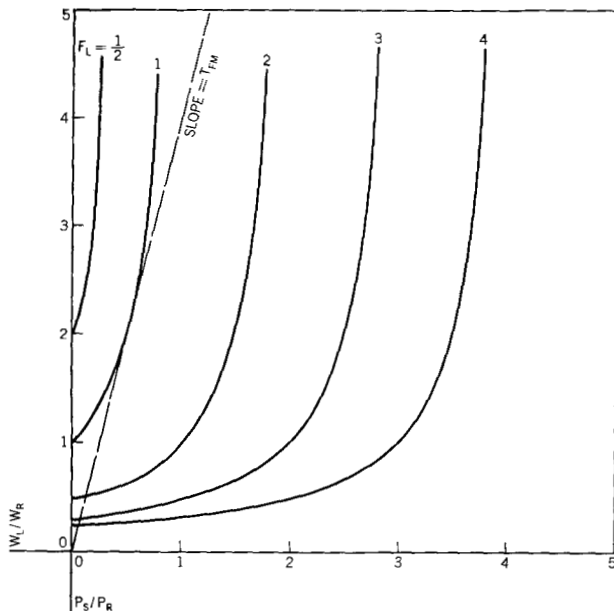
An arbitrary source has extraneous energy storage and additional energy dissipation so the terminal voltage rise is slower and often the $t = 0$ logic time is not well defined. An arbitrary detector also has extraneous energy storage and dissipation so that not all of the energy delivered to the logic detector is useful in reaching the decision threshold. The net effect of an arbitrary source-detector as compared with an ideal source-detector is an added delay in arriving at a logic decision.

If an ideal source and an ideal detector can be isolated in the actual circuit, analysis can be carried out for an actual logic factor, F'_L . This result would be the logic factor of a modified device including the extraneous source and detector elements as part of the device. Otherwise, the actual logic factor can be obtained from measured values of actual optimized logic times with and without the device, $T'_{Ls}|_{op}$ and $T'_L|_{op}$, respectively. The optimization is to be carried out with whatever degrees of freedom there may exist in the source and detector. Then

$$F'_L = T'_{Ls}|_{op} / T'_L|_{op} \quad (25)$$

A comparison of F'_L with F_L serves to indicate the extent to which the actual has approached the ultimate as associated with a specific ideal source and ideal detector. The basis for the comparison is an arrangement as shown in Fig. 11.

Figure 10 Constant F_L contours and logic figure of merit. ($K = 0$)



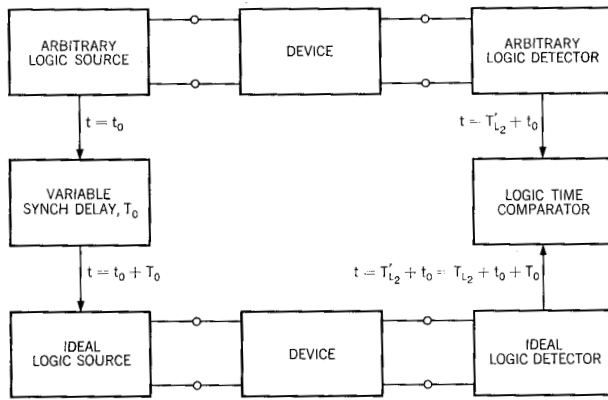
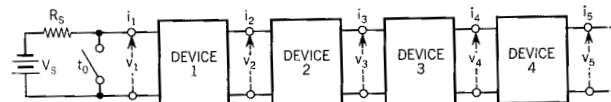


Figure 11 Comparison circuit for arbitrary source-detector.

Figure 12 Chain operation of devices.



A few simple cases of arbitrary sources and detectors are considered in Appendix III.

Chain operation of devices

The chain or cascaded operation of devices is shown in Fig. 12. Arrangements similar to this occur in computer shift registers. The energy delivered successively to each input is indicated in Fig. 13. If the logic energy is small the logic times would tend to increase continuously with additional devices as shown in the figure for W_{L_1} . For an intermediate logic energy, W_{L_2} , the logic times would tend to be the same, and for a larger logic energy, W_{L_3} , the logic times tend to decrease.

If the chain is made up of identical amplifying devices and is long enough, the output signals tend to become equal to the input signals with added delay:

$$\begin{aligned} v_{n+1}(t) &= v_n(t - T_d) \\ i_{n+1}(t) &= i_n(t - T_d) \\ p_{n+1}(t) &= p_n(t - T_d) \\ w_{n+1}(t) &= w_n(t - T_d). \end{aligned} \quad (26a, b, c, d)$$

The situation indicated in Fig. 13 is that of a growing wave. For longer chains nonlinearities will limit the amplitude, growth is terminated, and the steady-state situation as shown in Fig. 14 satisfies Eq. (26). For logic energy corresponding to W_L , the input of the n^{th} device

has a logic time of T_{L_n} and the input of the $(n+1)^{\text{th}}$ device reaches logic decision at $T_{L_{n+1}} = T_{L_n} + T_d$. The increase in logic time per device is T_d . However, T_d has no direct connection with minimum logic time as used in forming F_L . The quantity T_d has closer connection with actual logic time as associated with F'_L . For F_L , a $t = 0$ point would be established by an ideal logic source as for the first device of the chain (Fig. 12). For F'_L , a $t' = 0$ point would be established by the time at which the $(n-1)^{\text{th}}$ device operating as a nonideal logic source reaches logic decision; $t' = T_{L_{n-1}}$ as shown in Fig. 14. Then, $T'_L = T_{L_n} - T_{L_{n-1}} = T_d$; $T'_{L_2} = T_{L_{n+1}} - T_{L_{n-1}} = 2T_d$; and $F'_L = 2$. This result can be compared with the logic factor of chain-operated relays (see Eq. (24)).

Conclusions

The logic figure of merit, T_{FM} , is a better means of evaluating and comparing logic devices than voltage ampli-

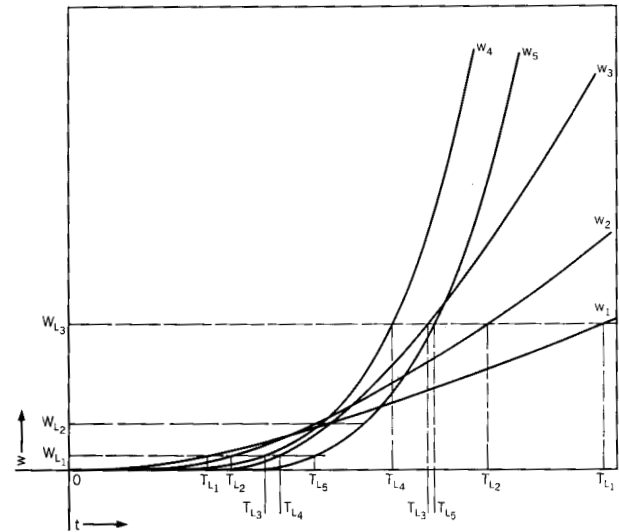
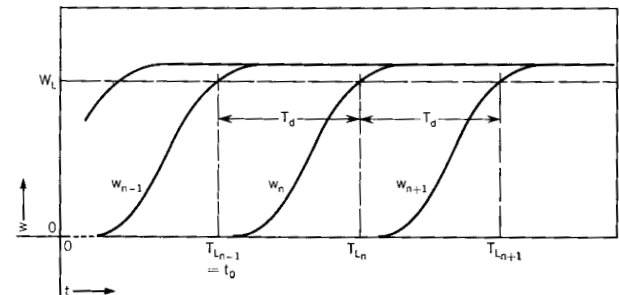


Figure 13 Growing wave of chain operation.

Figure 14 Steady-state wave of chain operation.



fication $\times$ bandwidth or power amplification $\times$ bandwidth. The latter figures of merit are defined only for linear operation, whereas T_{FM} is applicable to both linear and nonlinear operation of various devices. The straightforward formulation of T_{FM} for nonlinear operation is sometimes tedious. Simplifications are sometimes possible, e.g., there is evidence that in some cases T_{FM} for nonlinear operation may be determined from the limiting small-signal (linear) operation.

The basic ideas behind logic factor and logic figure of merit should prove useful and valuable in evaluating logic performance. The logic figure of merit is a unique measure of ultimate logic capability and can be compared with actual logic speed to indicate the possible amount of improvement as perhaps by circuit modifications. Throughout this study the viewpoint has been taken that the device is given and not subject to modifications. With a suitable yardstick for comparison, the important next step would be to inquire as to how the device can be changed for improved logic performance. For this purpose we would start with a model of the device or the device terminal properties and carry out the analytical steps to formulate the logic figure of merit. The proper functional dependency on device parameters would then be in evidence and these parameters could be changed by the correct amount subject to design constraints to produce the smallest logic figure of merit.

For minimizing the logic figure of merit, the device should have the following general properties:

- (1) output signal of correct polarity should follow immediately upon the application of an input signal so time delay should be minimized;
- (2) power amplification should be maximized so as to increase the source available power;
- (3) all energy storage and power dissipation elements should be minimized.

Acknowledgments

This study was carried out during summer consultation with Solid State Electronics, Physical Sciences Department. The ideas presented were rationalized and developed with the aid of discussions with M. Axelrod and H. Yu.

Appendix I. Logic performance of a specific linear device

Consider a specific linear device that satisfies the model as shown in Fig. I-1. The model shown is applicable to logic operation of electron tubes, transistors, and similar devices when represented by their small-signal equivalence. Except for the transit-time delay shown in the g_m generator, the model is that of the hybrid- π equivalent circuit⁴ with resistive elements in shunt with the capacitors

omitted. These resistive elements contribute dissipation and tend to increase the logic time, but if the logic time is short compared to all of the RC time constants, the additional contribution of the shunt resistive elements will be negligible.

The circuit operating equations are

$$\frac{V_s U(t) - v_i(t)}{R_s + r} - (C_i + C_f) \frac{dv_i(t)}{dt} + C_f \frac{dv_2(t)}{dt} = 0, \quad (\text{I-1})$$

$$g_m v_i(t - T_t) - C_f \frac{dv_i(t)}{dt} + (C_0 + C_f + C_2) \frac{dv_2(t)}{dt} = 0. \quad (\text{I-2})$$

Solving for dv_2/dt in the second equation and substituting into the first equation,

$$\begin{aligned} \frac{V_s U(t)}{R_s + r} &= \frac{v_i(t)}{R_s + r} + \frac{g_m C_f}{C_0 + C_f + C_2} v_i(t - T_t) \\ &+ \left[C_i + \frac{C_f(C_0 + C_2)}{C_0 + C_f + C_2} \right] \frac{dv_i(t)}{dt}. \end{aligned} \quad (\text{I-3})$$

This is a linear first-order differential equation which can be solved easily if $T_t = 0$. With the aid of the Laplacian transform variable, s , the solution of Eq. (I-3) can be indicated formally as an inverse transform,

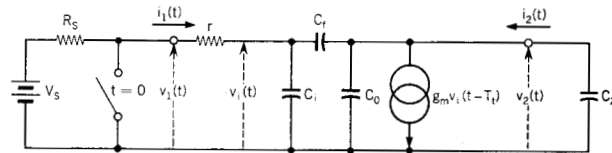
$$\begin{aligned} v_i(t) &= \frac{V_s}{(R_s + r)} \\ &\times \mathcal{L}^{-1} \left\{ \frac{1}{s} \left[\frac{1}{(R_s + r)} + \frac{g_m C_f}{(C_0 + C_f + C_2)} e^{-s T_t} \right. \right. \\ &\left. \left. + \left(C_i + \frac{C_f(C_0 + C_2)}{C_0 + C_f + C_2} \right) s \right]^{-1} \right\}. \end{aligned} \quad (\text{I-4})$$

Then,

$$\begin{aligned} v_2(t) &= \frac{C_f}{C_0 + C_f + C_2} v_i(t) \\ &- \frac{g_m U(t - T_t)}{(C_0 + C_f + C_2)} \int_0^{t - T_t} v_i(t') dt'. \end{aligned} \quad (\text{I-5})$$

If $s T_t$ is small so that $e^{-s T_t} \approx 1 - T_t s$, the solution for $v_i(t)$ is

Figure I-1 Linear device model.



$$v_i(t) = \frac{V_s}{1 + \frac{g_m(R_s + r)C_f}{(C_0 + C_f + C_2)}} \left[1 - \exp\left(-\frac{t}{T_1}\right) \right], \quad (I-6)$$

where

$$T_1 = (R_s + r) \left[\frac{C_i + \frac{C_f(C_0 + C_2) - g_m C_f T_i}{(C_0 + C_f + C_2)}}{1 + \frac{g_m(R_s + r)C_f}{(C_0 + C_f + C_2)}} \right]. \quad (I-7)$$

Also,

$$v_2(t) = \frac{g_m T_1 V_s}{C_0 + C_f + C_2 + g_m(R_s + r)C_f} \times \left\{ U(t - T_1) \left[1 - \exp\left(\frac{T_1 - t}{T_1}\right) - \frac{t - T_1}{T_1} \right] + \frac{C_f}{g_m T_1} \left[1 - \exp\left(-\frac{t}{T_1}\right) \right] \right\}. \quad (I-8)$$

Note that the approximation used for $\exp(-sT_1)$ means that the accuracy of the $v_i(t)$ and $v_2(t)$ solutions will improve as $t \gg T_1$. The quantity $v_i(t)$ will increase exponentially to a limiting value somewhat less than V_s , since for large t there will be a constant current through C_f . Assuming that g_m is positive, $v_2(t)$ will start out with a small positive excursion due to the last term in Eq. (I-8); $v_2(t)$ will then go negative somewhat exponentially as the transit-time-delayed contribution is introduced; for large t ,

$$v_2(t) \approx -\frac{g_m V_s}{C_0 + C_f + C_2 + g_m(R_s + r)C_f} \times (t - T_1 - T_i).$$

T_{L_2} will occur at a time greater than T_1 . Forming $W_L = \frac{1}{2}C_2 v_2^2(T_{L_2})$ and introducing $P_s = V_s/4R_s$ and $T_M = W_L/P_s$,

$$T_M = \frac{2g_m^2 T_1^2 C_2 R_s}{[C_0 + C_f + C_2 + g_m(R_s + r)C_f]^2} \times \left[1 - \exp\left(-\frac{T_{L_2} - T_1}{T_1}\right) - \frac{T_{L_2} - T_1}{T_1} \right] + \frac{C_f}{g_m T_1} \left[1 - \exp\left(-\frac{T_{L_2}}{T_1}\right) \right]^2. \quad (I-9)$$

Next, it is necessary to formulate $T_{L_2}|_{op}$ by minimizing T_{L_2} with respect to C_2 and R_s . These steps will be carried through for different cases representing restricted regions of device properties.

Case I. $r = C_f = T_i = 0$.

This limiting case which was considered in the main text can be solved exactly. The results are

$$C_2|_{op} = C_0, \quad (I-10)$$

$$R_s|_{op} = 0.855(T_M T_D^2)^{1/3}/C_i, \quad (I-11)$$

$$F_L = 1.495(T_D/T_M)^{1/3}, \quad (I-12)$$

$$T_{FM} = 1.828T_D, \quad (I-13)$$

where

$$T_D = (2C_i C_0)^{1/3}/g_m. \quad (I-14)$$

Case II. $g_m R_s|_{op} C_f \ll C_0 + C_f$, $C_f \ll C_i$, $r \ll R_s|_{op}$, and

$$T_i \ll \frac{2C_i(C_0 + C_f)}{g_m C_f}.$$

In this case, the device amplification and coupling effects are small enough that $T_1 \approx (R_s + r)C_i$ independent of C_2 . Then,

$$C_2|_{op} = C_0 + C_f, \quad (I-15)$$

$$R_s|_{op} = 0.855(T_M T_E^2)^{1/3}/C_i - 2r/3, \quad (I-16)$$

$$F_L = 1.495\left(\frac{T_E}{T_M}\right)^{1/3} + 0.583 \frac{rC_i}{T_M} + \frac{0.814}{T_M} \left(T_i + \frac{C_f}{g_m}\right), \quad (I-17)$$

$$T_{FM} = 1.828T_E + 0.778rC_i + 1.085\left(T_i + \frac{C_f}{g_m}\right), \quad (I-18)$$

where

$$T_E = \frac{[2C_i(C_0 + C_f)]^{1/3}}{g_m}.$$

Case III. $g_m r C_f \gg \frac{1}{2}(C_0 + C_f)$, $C_i \gg C_f$, and $T_i \ll C_i/g_m$.

In this case the device amplification and coupling effects are large enough that there is significant current through C_f even after $v_i(t)$ has reached its limiting value. Now, $T_1 = [1/g_m C_f][(C_i + C_f)(C_0 + C_2) + C_i C_f - g_m C_f T_i]$ and is independent of R_s . The input optimization is simply given by $R_s|_{op} = r$. T_1 is large, and generally $T_{L_2}/T_1 < 1$.

Then, using small argument approximations,

$$T_M = \frac{C_2 T_1^2}{8r C_f} \left(\frac{T_{L_2} - T_1}{T_1} \right)^4.$$

Optimization with respect to C_2 and the other results follow,

$$C_2|_{op} = C_0 + C_f, \quad (I-19)$$

$$R_s|_{op} = r, \quad (I-20)$$

$$F_L = 1.931 \left[\frac{r(C_i + C_f)^2(C_0 + C_f)}{g_m^2 T_M^3} \right]^{1/4} + 0.814 T_i/T_M, \quad (I-21)$$

$$T_{FM} = 2.405 \left[\frac{r(C_i + C_f)^2(C_0 + C_f)}{g_m^2} \right]^{\frac{1}{2}} + 1.082 T_i. \quad (\text{I-22})$$

For the next two cases, it is assumed that the device transit-time is so large that the input voltage reaches its limiting value essentially before the output voltage starts to change. In terms of Eq. (I-4), this is equivalent to $\exp(-sT_i) \approx 0$. Eqs. (I-6), (I-7), and (I-8) are still valid, but $T_i \rightarrow 0$ in Eq. (I-7) for T_1 .

Case IV. $g_m r \gg 1$, $C_i \gg C_f$, and $T_i \gg 2rC_i$.

This case is similar to Case III, except for T_i value. Since, when $v_2(t)$ begins to change, $v_i(t)$ is approximately constant, the optimization of C_2 and the other quantities are

$$C_2|_{op} = C_0 + C_f, \quad (\text{I-23})$$

$$R_S|_{op} = r, \quad (\text{I-24})$$

$$F_L = 0.814 \left\{ \frac{T_i}{T_M} + \left[\left(\frac{2T_H}{T_M} \right)^{\frac{1}{2}} + \frac{4rC_iC_f}{g_m T_M^2} \right]^{\frac{1}{2}} \right\}, \quad (\text{I-25})$$

$$T_{FM} = 0.814 T_i + 1.30 (T_i T_H^3)^{\frac{1}{2}} + 1.018 \frac{rC_iC_f}{g_m (T_i T_H^3)^{\frac{1}{2}}}, \quad (\text{I-26})$$

where

$$T_H = \left[\frac{4rC_i^2(C_0 + C_f)}{g_m^2} \right]^{\frac{1}{2}}. \quad (\text{I-27})$$

Case V. $g_m R_S|_{op} C_f \ll C_0 + C_f$, $C_f \ll C_i$, $r \ll R_S|_{op}$, and $T_i \gg R_S|_{op} C_i$.

This case is similar to Case II except for T_i value. The results are the same as both assume small device amplification and coupling. The figure of merit changes since with T_i large, a different approximation is used.

$$T_{FM} = 0.814 \left(T_i + \frac{C_f}{g_m} \right) + 0.583 r C_i + 1.632 (T_i T_H^2)^{\frac{1}{2}}. \quad (\text{I-28})$$

A number of approximations are made in obtaining the results given except for Case I. For those cases where the device does not fall within one of the five classes or, if critical comparison is to be made between devices, the exact formulation with numerical calculations should be used.

These formulas have been used to obtain comparative values of T_{FM} for several existing and hypothetical devices.⁵

Appendix II. Performance of a current-switch device

The current-switch device to be considered contains two transistors in an arrangement shown in Fig. II-1. This is a direct-coupled logic circuit which uses silicon tran-

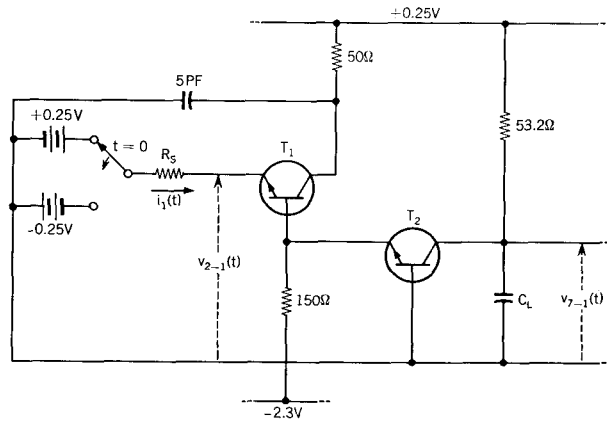


Figure II-1 Current-switch device.

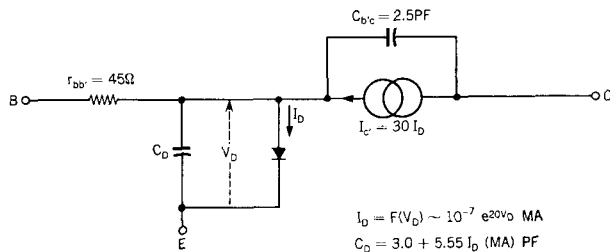


Figure II-2 Large-signal transistor model.

sistors.⁶ For calculation purposes, a large-signal transistor model,⁷ as shown in Fig. II-2, is used. Response signals were obtained by means of a computer program.⁸

For $R_S = 25\Omega$ a set of curves as shown in Fig. II-3 (solid lines) is obtained for the output voltage, $v_{7-1}(t)$, for different values of C_L . The dashed curves are approximate output voltage curves obtained by displacing the computed curves to the left. Using $v_{7-1}(0) = 0.25$ V as the initial zero reference level, $v_{7-1}(T_{L2}) = 0.25 - (2W_L/C_L)^{\frac{1}{2}}$ V can be computed for a given W_L and C_L value. The locus of $v_{7-1}(T_{L2})$ points for constant W_L values are shown also as solid lines in Fig. II-3. It is seen that for each W_L value there is a minimum T_{L2} associated with a $C_L|_{op}$ as corresponding to output logic match operation. Fig. II-4 shows a similar set of curves for $R_S = 100\Omega$. Fig. II-5 is a set of $v_{7-1}(t)$ curves for different R_S values.

The next step in the optimization process would be to vary R_S while keeping P_S constant to obtain a $T_{L2}|_{op}$ with each W_L value. This optimization step implies a change in the source voltage. In usual computer operation the logic voltage levels are maintained constant throughout. Because of this, input optimization which would usually require different logic voltage levels was not admissible. Accordingly, the results to be discussed correspond to

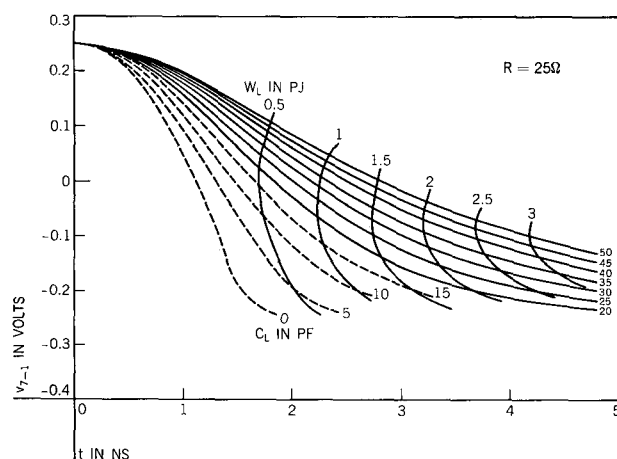


Figure II-3 Output signals for different C_L values.

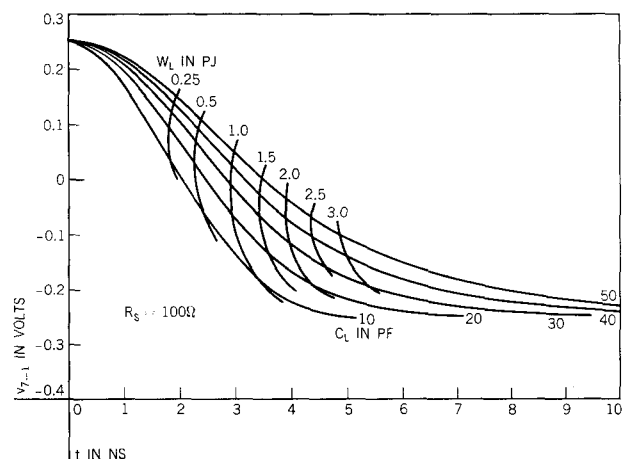


Figure II-4 Output signals for different C_L values.

output optimized performance only, but the notation to be used will be that of fully optimized performance. Accordingly, associated with each $W_L = \text{constant}$ line in Figs. II-3 and II-4 there is a $T_{Ls|op}$ and a $T_M = W_L/P_S$; $F_L = T_{Ls|op}/1.23T_M$. For the paired values, W_L and P_S , a F_L value can be noted as shown in Fig. II-6. With enough F_L values thus spotted, the $F_L = \text{constant}$ contours can be drawn in. For the limited number of F_L values available, the $F_L = \text{constant}$ contours appear to be approximate straight lines at least at the smaller W_L , P_S values.

The smallest T_M value associated with the $F_L = 1$ contour is the logic figure of merit, T_{FM} . In Fig. II-6, the logic figure of merit for this current-switch device is 3.2 ns. If the source-detector available has $T_M = W_L/P_S < 3.2$ ns, the device cannot improve the logic situation.

Up to this point, the source P_S and the detector W_L have been assumed to be fully arbitrary. In actual use, the circuit might typically be driven by a 50Ω transmission line, so $P_S = 1.25$ mW. The detector could be an identical device as in cascade operation. The input response wave shapes as shown in Fig. II-7 are the input voltage, v_{2-1} , input current, i_1 , input power, p_1 , and the input energy, w_1 . These are for a 50Ω source resistance and 50 pF output capacitance. In forming p_1 and w_1 , the $t = 0$ values of v_{2-1} and i_1 are considered as zero reference values. The detector logic time, $T_L = 3.5$ ns, is determined by extrapolating the essentially straight line portion of v_{2-1} to -0.25 V. The associated input energy is the detector logic energy, $W_L = 2.47$ pJ. The resulting source-detector combination has a minimum logic time, $T_M = 1.98$ ns. If the detector were an ideal capacitor, the logic time would be 2.44 ns as compared to 3.5 ns. Also, for a logic voltage of 0.5 V, the equivalent capacitor would be 19.8 pF, to correspond to $W_L = 2.47$ pJ. For $P_S = 1.25$ mW and $W_L = 2.47$ pJ, Fig. II-6 indicates that the device would

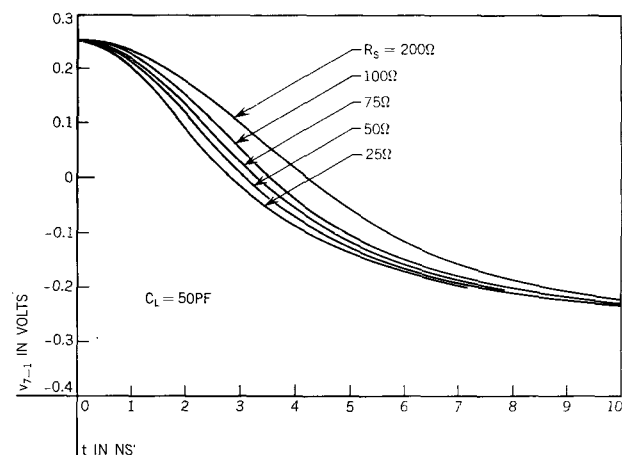


Figure II-5 Output signals for different R_S values.

have a logic factor of about 1.3. This value of T_{FM} indicates that the device can be used advantageously.

In Fig. II-6, the region of major interest has straight-line variation for constant F_L . This result is believed very significant as indicating that even for a highly nonlinear device, the device figure of merit is governed by the linear (small-signal) properties of the device. A proof of the general validity of this surmise would be very useful, since the evaluation of the device could then be correctly made from the small-signal equivalent of the device.

Appendix III. Logic operation of nonideal sources and detectors

Sources and detectors are somewhat less than ideal if there is extraneous energy dissipated or stored in the process of transferring a logic decision. Consider as a

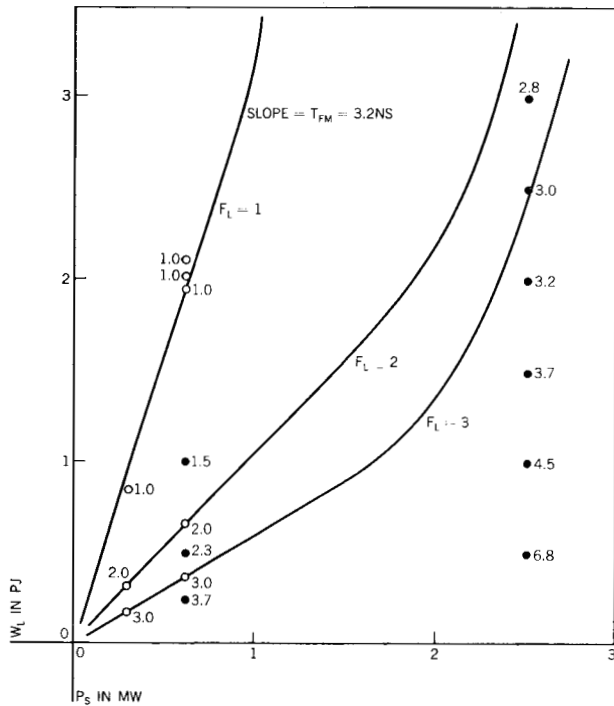


Figure II-6 Constant logic factor contours.

simple example, the situation of Fig. III-1. There are three possible operating conditions:

1) R_D is part of the detector but not useful in forming the logic decision. Logic match is made at the 1-1' port. Then

$$w_L(t) = P_L(t)t = \frac{v_{1-1'}^2(t)}{R_L} t$$

$$= \frac{V_S^2}{R_L R_S^2 (G_S + G_D + G_L)^2} t, \quad (\text{III-1})$$

$$T_M = \frac{W_L}{P_S} = \frac{4}{R_L R_S (G_S + G_D + G_L)^2} T_L, \quad (\text{III-2})$$

$$G_S|_{op} = G_D + G_L, \quad (\text{III-3})$$

$$T_L|_{op} = \left(1 + \frac{R_L}{R_D}\right) T_M. \quad (\text{III-4})$$

2) R_D is part of the source but not associated with available source power. Logic match is made at the 2-2' port. The operation is similar to that of (1) above and

$$G_L|_{op} = G_S + G_D, \quad (\text{III-5})$$

$$T_L|_{op} = [1 + (R_S/R_D)] T_M. \quad (\text{III-6})$$

3) R_D represents a device. Logic match is made at both 1-1' port and 2-2' port. Operation is again given by Eqs.

(III-1) and (III-2) but with $T_L \Rightarrow T_{L_2}$. Logic match at both ports simultaneously can be accomplished by having G_S and G_L become infinitely large. Therefore, $T_{L_2}|_{op}$ is achieved by

$$G_S|_{op} = G_L|_{op} = \infty, \quad (\text{III-7})$$

and

$$T_{L_2}|_{op} = T_M. \quad (\text{III-8})$$

The match conditions for the three cases are identical to the requirements for power match.

Consider next the three possible operating conditions for the circuit of Fig. III-1b:

1) C_D is part of the detector but not useful in forming the logic decision. Logic match is made at the 1-1' port. Then

$$w_L(t) = \frac{1}{2} C_L v_{1-1'}^2(t) = \frac{1}{2} C_L V_S^2 [1 - \exp(-t/T_0)]^2, \quad (\text{III-9})$$

with

$$T_0 = R_S(C_D + C_L). \quad (\text{III-10})$$

Then

$$T_M = \frac{W_L}{P_S} = 2C_L R_S [1 - \exp(-T_L/T_0)]^2. \quad (\text{III-11})$$

The minimization of T_L with respect to R_S requires that

$$R_S|_{op} = 0.975 T_M / C_L, \quad (\text{III-12})$$

and the minimum value of T_L is

$$T_L|_{op} = 1.26 T_0|_{op} = 1.23 T_M [1 + (C_D/C_L)]. \quad (\text{III-13})$$

2) C_D is part of the source. Logic match is made at the 2-2' port. The minimization of T_L requires that $C_L|_{op}$ satisfy the transcendental equation

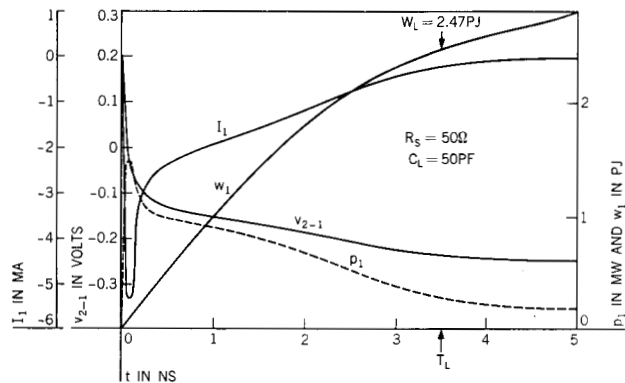


Figure II-7 Input response to voltage source.

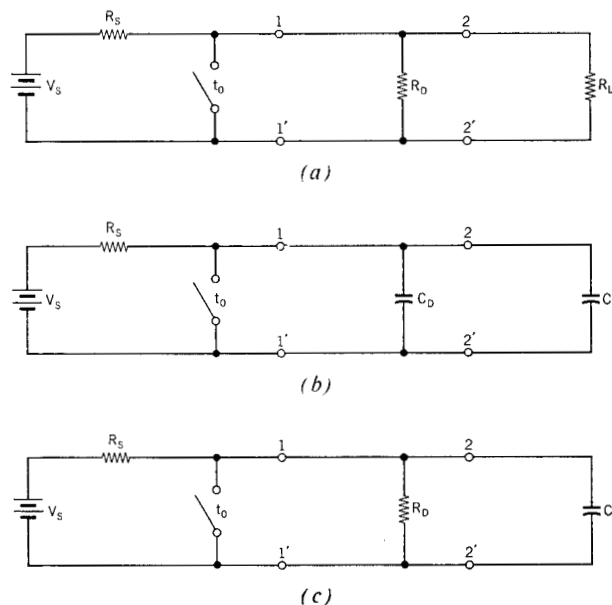


Figure III-1 Ideal source-detector with extraneous shunt element (a) resistive elements (b) capacitive elements (c) resistive and capacitive elements.

$$1 + \frac{C_D}{C_L|_{op}} - 2 \left[1 - \left(\frac{2R_s C_L|_{op}}{T_M} \right)^{\frac{1}{2}} \right] \times \ln \left[1 - \left(\frac{T_M}{2R_s C_L|_{op}} \right)^{\frac{1}{2}} \right] = 0. \quad (\text{III-14})$$

The associated $T_L|_{op}$ is obtained by substituting $C_L|_{op}$ into Eq. (III-11).

3) C_D represents a device. Logic match is made at both the 1-1' port and 2-2' port. Equation (III-11) is applicable but with $T_L \Rightarrow T_{L_s}$. In order to minimize T_{L_s} simultaneously with respect to R_s and C_L , it is necessary that

$$C_L|_{op} \gg C_D. \quad (\text{III-15})$$

With this inequality satisfied, the remainder of the optimization becomes identical with condition (1) above so

$$R_s|_{op} = 0.975 T_M / C_L, \quad \text{and} \quad T_L|_{op} = 1.23 T_M.$$

The arrangement in Fig. II-1(c) involves a combination of a resistive element and a capacitive detector.

1) R_D is part of the detector but not useful in forming the logic decision. Logic match is made at the 1-1' port. Then,

$$w_L(t) = \frac{1}{2} C_L v_{1-1'}^2(t) \quad (\text{III-16})$$

$$= \frac{C_L}{2} \frac{V_s^2}{[1 + (R_s/R_D)]^2} \left[1 - \exp\left(-\frac{t}{T_0}\right) \right]^2,$$

$$\text{with } T_0 = \frac{R_s C_L}{1 + (R_s/R_D)}. \quad (\text{III-17})$$

Also,

$$T_M = \frac{W_L}{P_s} = 2 \frac{T_0}{[1 + (R_s/R_D)]} \left[1 - \exp\left(-\frac{T_L}{T_0}\right) \right]^2. \quad (\text{III-18})$$

The value T_L is minimized when R_s satisfies

$$[1 - (R_s|_{op}/R_D)]y + 2(1 - y) \ln(1 - y) = 0, \quad (\text{III-19})$$

with

$$y = [T_M / 2C_L R_s|_{op}]^{\frac{1}{2}} [1 + (R_s|_{op}/R_D)]. \quad (\text{III-20})$$

The associated $T_L|_{op}$ is obtained by substituting $R_s|_{op}$ into Eq. (III-18).

2) R_D is part of the source but not associated with available source power. Logic match is made at the 2-2' port. Minimization of T_L with respect to C_L is obtained when

$$C_L|_{op} = 0.975 [1 + (R_s/R_D)]^2 [T_M / R_s], \quad (\text{III-21})$$

and then

$$T_L|_{op} = 1.23 [1 + (R_s/R_D)] T_M. \quad (\text{III-22})$$

3) R_D represents a device to be matched at both the 1-1' and 2-2' ports. Equation (III-18) is applicable but with $T_L \Rightarrow T_{L_s}$. In order to minimize T_{L_s} simultaneously with respect to R_s and C_L , it is necessary that

$$R_s|_{op} \ll R_D. \quad (\text{III-23})$$

With this inequality satisfied, R_D drops out and $C_L|_{op} = 0.975 T_M / R_s$, and $T_{L_s}|_{op} = 1.23 T_M$.

References and footnotes

1. As an example, present transistors have $W_L = 1$ picojoule and $T_L = 1$ nanosecond so $H_L = 10^{-21}$ joule-seconds. For comparison, $h = 6.6 \times 10^{-34}$ joule-seconds.
2. See for instance, R. Landauer, "Fluctuations in Bistable Tunnel Diode Circuits," *J. Appl. Phys.* **33**, 2209-2216 (1962).
3. The logic figure of merit is directly relatable to a gain-bandwidth figure of merit, $f_{BW} = 0.823 \times 1/T_{FM}$. See Harold A. Wheeler, "Wide-Band Amplifiers for Television," *Proc. IRE* **27**, 429-439 (1939).
4. L. J. Giacoletto, "Study of P-N-P Alloy Junction Transistor from D-C Through Medium Frequencies," *RCA Review* **15**, 506-562 (1954).
5. L. J. Giacoletto, "Logic Figure of Merit," *Proc. IEEE* **53**, 392-393 (April 1965).
6. D. H. Chung and J. A. Palmieri, "Design of ACP-Resistor-Coupled Switching Circuits," *IBM Journal* **7**, 190-198 (1963).
7. K. G. Ashar, H. N. Ghosh, A. W. Aldridge, and L. J. Patterson, "Transient Analysis and Device Characterization of ACP Circuits," *IBM Journal* **7**, 207-223 (1963).
8. Programming and calculations were carried out by E. Schlig, Thomas J. Watson Research Center, using a routine developed by A. W. Aldridge, IBM Systems Development Division, Poughkeepsie.

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