W. Anacker
G. F. Bland
P. Pleshko
P. E. Stuckert

On the Design and Performance of a Small 60-nsec Destructive Readout Magnetic Film Memory

Abstract: The design of a small very-high-speed magnetic film memory using existing components is summarized. The memory has a capacity of 32 words and 36 bits per word, operates in a destructive-readout mode, and has a cycle time of 60 nsec and an access time of 32 nsec. The storage medium is a continuous sheet of NiFe film. The operational characteristics of the film and the properties of the strip line array are given, with worst case pulse conditions applying to both. The design and operation of the electronic circuitry are also described. A model of the memory, populated with three word-driver circuits and three regeneration-loop circuits for reading, rewriting, and writing, has been built and operated successfully. The paper concludes with oscillograms of waveforms which were obtained in closed regeneration-loop operation with that model.

Introduction

It has been known for several years that thin NiFe film memory elements can be switched in times close to 1 nsec.[1] However, the extent to which their potential can be exploited is limited by the electrical and mechanical characteristics of the systemic environment in which they are immersed. Such limits are imposed, for example, by array noise, signal amplification and consequent delay, limitations in transistor drive capabilities, and organization of the regeneration loop.

This paper presents results from an engineering research program undertaken to advance the realization of this high speed potential through simultaneous and consistent attack on these and other closely interrelated environmental factors. In this program, the storage capacity to be achieved was considered to be of minor importance but a capacity of 1000 bits was taken as a practical lower bound. Specifically, the objective came to be the development of a laboratory model having a capacity of 1152 bits and a cycle time of 60 nsec.

Design features and operational characteristics of a model built to realize that objective are presented below in five principal sections: "Operational mode of the memory"; "Properties of the storage medium"; "Array properties"; "Electronic circuitry"; and "Organization of the memory."

Operational mode of the memory

The memory model contains 32 words with 36 bits per word, is word organized, and operates in a destructive readout (DRO) mode. The storage medium is a thin continuous NiFe sheet which was utilized to achieve the greater simplicity and flexibility of array design and assembly that results from elimination of the need for registering the array lines with discrete locations.

The word and bit fields are orthogonal to each other so as to permit the use of the fast rotational switching mode. One word pulse per cycle is used, the leading edge of which performs reading by inducing bipolar read signals into the sense lines. Writing and rewriting is performed at the end of the word pulse in conjunction with an overlapping bipolar bit pulse.

Properties of the storage medium

The basic memory elements are small areas in a continuous sheet of a 600 Å thick NiFe film with uniaxial anisotropy. The film is evaporated on a 3 in. $\times$ 3 in. silver-copper alloy substrate coated first with a smoothing layer of SiO. The composition of the film is 18.4% Fe, 81.6% Ni. Typical magnetic properties are: $H_k = 4.1$ Oe; $H_c = 3.3$ Oe; and dispersion and skew, $\alpha, = 5°$.

A number of individual storage locations in several bit plates were tested under high speed pulse conditions in

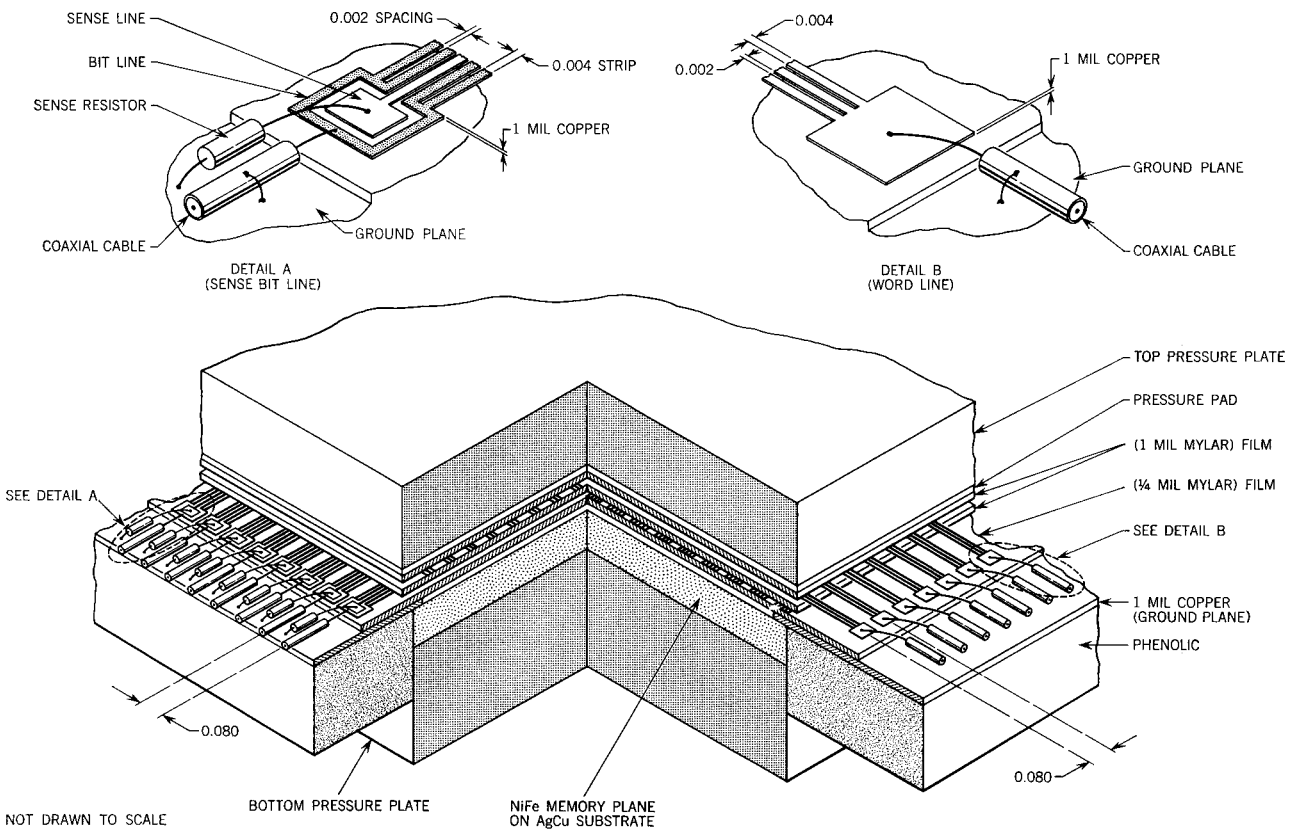


Figure 1 Mechanical structure of the memory plane and the laminated array.

recognition of the fact that low-frequency magnetic properties alone are not adequate to characterize the film for very high speed use. The characteristics of the individual elements, and especially those in a continuous sheet, are highly dependent on environmental conditions, e.g., on the geometric structure and the dimensions of the array, the presence of magnetic material around the individual storage areas, and the presence of the metallic substrate upon which the film is deposited. For this reason, the pulse tests were made with the array that was to be used in the memory. This array is shown in Fig. 1. The dimensions of the strip lines were based on preliminary measurements and estimates of the drive currents and sense signals, taking into account the capabilities of available electronic components.

Before the start of each pulse test, the magnetic material around the individual storage locations was set antiparallel to the magnetization of the area under test by an external magnetic field in order to simulate worst case conditions. Two effects due to the presence of the conducting ground plane and strip lines, known as "trapped flux" and "current spreading,"[2] were accounted for by three cyclic pulse programs, Programs 1, 2, and 3 shown in Fig. 2. All measurements were carried out by subjecting individual elements to word and bit fields using three adjacent word lines and three adjacent bit lines of the array as shown in Fig. 2. The response of the element was tested by measuring the voltage-time integral of the sense signals induced in the sense line by the element under test during the read operation of each program cycle. Since the voltage-time integral of the signal is independent of the rise time of the read word pulse, a 10-nsec rise time read pulse was used. This permits low-distortion amplification to a level which is compatible with commercially available sampling oscilloscope integrators. Typical results are given in Fig. 2, where the integrals of the sense signals are plotted against write-bit currents and disturb-bit currents, respectively. The pulse rate of these test programs is 100 nsec and the number, amplitude, and width of the pulses used are indicated in Fig. 2.

The curves given in Fig. 2a for Program 1 take into account both the counteraction of "trapped flux" and "current spreading" fields during the write operation, and also the reduction of the sense signal that occurs because

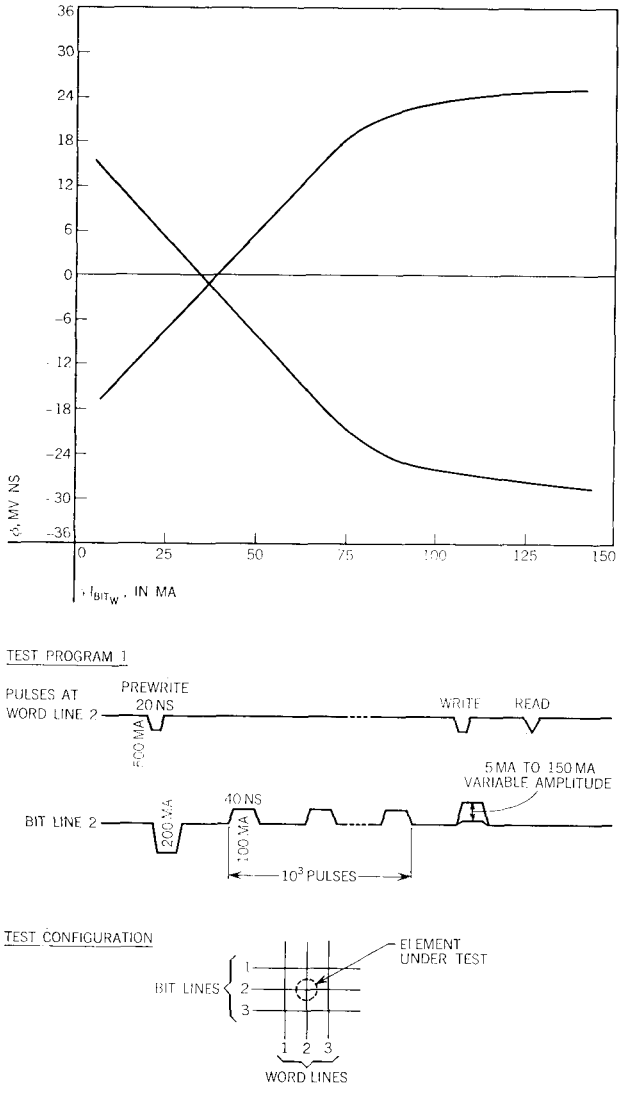


Figure 2a Test Program 1 for read and write test, and the voltage-time integral (ϕ) of the sense signal plotted against writing bit current for the read and write test.

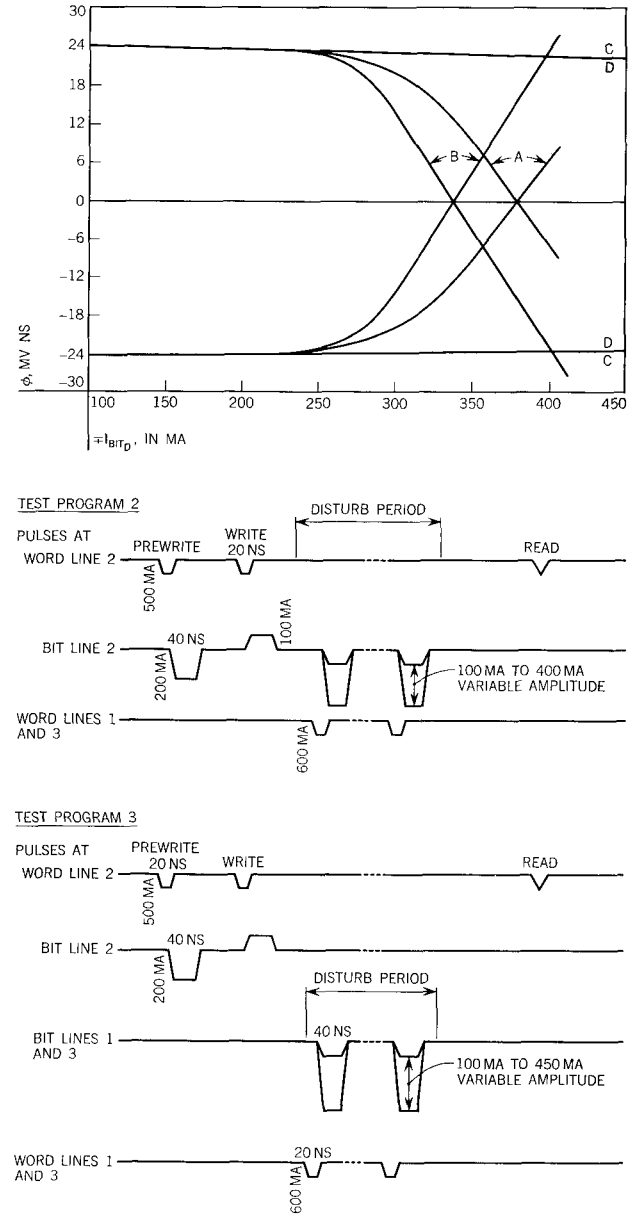


Figure 2b Test Programs 2 and 3 for disturb tests, and the voltage-time integral (ϕ) of sense signal plotted against disturbing bit current for the disturb tests.

of the antiparallel magnetization of the material around the element under test during the read operation. They represent, therefore, actually the worst case test for writing and reading of undisturbed bits. These curves indicate that a bit current of more than 80 mA is needed to switch the magnetization of the element fully into the desired direction, and that the switched flux which determines the sense signal under worst case read conditions is at least 23 mV nsec.

Curves A and B in Fig. 2b show disturb effects due to bit currents in bit line 2 which belongs to the element under test (Program 2) while curves C and D indicate the almost negligible disturb effect when bit currents are flowing in the adjacent bit lines 1 and 3 (Program 3). Curves A and C are obtained by using 10^4 disturb pulses while curves B and D are obtained by applying 10^5 disturb pulses. Both adjacent word lines 1 and 3 were pulsed simultaneously during the entire disturb period to exaggerate the worst case disturb effects.

The resulting curves of Fig. 2b indicate reliable operation for 10^5 disturb pulses as long as the disturbing bit currents in the bit line 2 associated with the element do

not exceed 250 mA, and essentially no disturb effect is seen from bit currents up to 450 mA in adjacent bit lines 1 and 3. Because of the large (0.080 in.) bit line spacing, the same curves of Figs. 2a and 2b are also valid for any combination of bit currents flowing simultaneously in bit lines 1, 2, and 3 during writing and disturbing. This point was verified by experiment.

Unfortunately, the number of disturb pulses was limited to 10^5 pulses by the instrumentation available for these tests, so that the "creeping" effects (for which the difference between curves A and B in Fig. 2b is an indication) could not be measured to their full extent. Hence, a separate test was conducted to verify that "creeping" would not affect reliable operation even for worst case disturb conditions involving current spreading effects and tolerances of bit driver circuits, i.e., low write and high disturb bit currents. This test was performed with a closed regeneration loop; it indicated that no loss of information occurred after 10^9 disturb pulses.

From these tests the following values for operating the memory elements were established:

- A word current of 500 mA (+20%, −0%) with a rise time of 4 nsec.
- Bipolar bit pulse currents of ±100 mA (±10%).
- Minimum sense signals of ±4 mV with a base width of 4 nsec and rise and fall times of approximately 2 nsec each.

Array properties

The array consists of two sets of slotted strip lines photoetched on thin copper-coated Mylar film. The separate sense and bit lines are in a common plane and are placed closest to the film. The word lines are placed on top of the sense and bit lines. The configuration is shown in Fig. 1. The directions of the lines with respect to the film are such that the word fields are parallel to the hard magnetization axis of the film, the bit fields are parallel or antiparallel to the positive easy axis, and the sense lines are linked with the easy-axis magnetic stray flux of the bits. The ground plane for the word-, bit-, and sense-line currents is the metallic substrate.

The magnitude of interline coupling in the array played a critical role in establishing design criteria for the electronic circuits. The effects of this coupling fall under two categories, *read* noise and *write* noise.

- *Read noise*

Read noise is induced in the sense lines by the leading edge of the word pulse and has the same polarity as the word pulse transition. Read noise is superimposed on the information signal and therefore can introduce a high degree of asymmetry between the ONE and ZERO signals, thereby increasing the complexity of the detection circuits over that necessary for symmetrical (bipolar) detection. Since the word and sense lines are orthogonal to each other, the coupling between them is due to the electric field in the vicinity of the crossovers (i.e., the coupling is capacitive). In an array in which the propagation delay of the word line is much less than the rise time of the word pulses, it is possible to reduce the read noise significantly by terminating the word lines in short circuits. This possibility arises from the fact that the reflected leading edge of the word pulse cancels the incident wave at the position of the crossover after a time equal to twice the electrical length of the word line between the crossover and the short circuit. In the model, the maximum read noise was reduced to 1 mV by this technique. The word-pulse rise time is 4 nsec and the electrical length of the word line between the first sense line and the short circuit is less than 0.5 nsec.

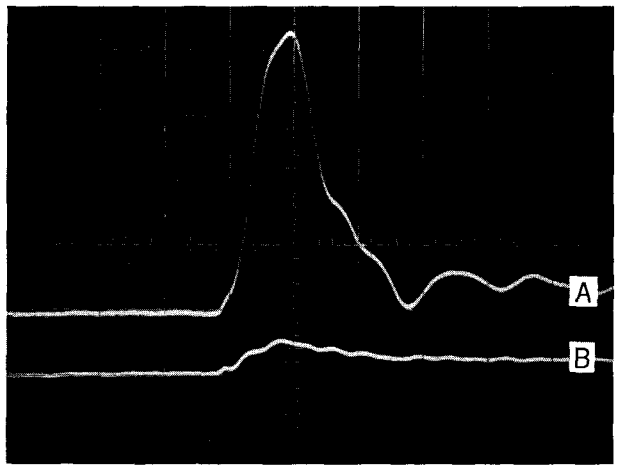
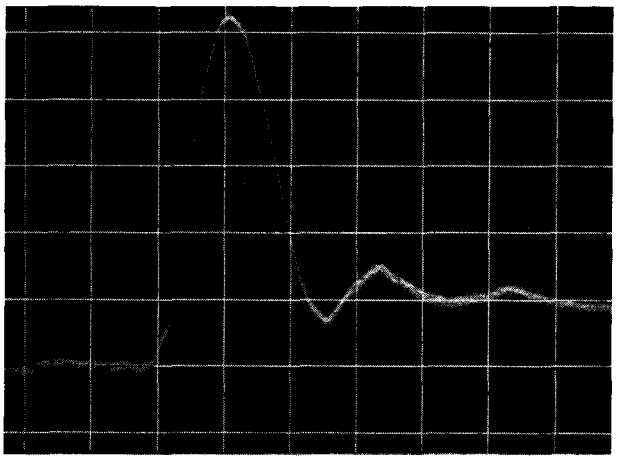


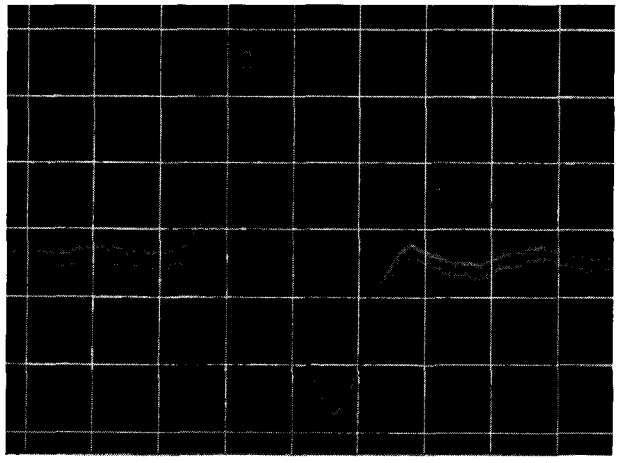
Figure 3 Write noise on a sense line due to a writing pulse of 100 mA on the associated bit line. Trace A shows the noise when bit and sense lines are terminated in short circuits; trace B shows the noise when the bit line is terminated in 15 ohms, the sense line in 50 ohms. Major vertical divisions represent 10 mV; major horizontal divisions, 5 nsec.

- *Write noise*

Write noise occurs when the bit line is pulsed and is due to the coupling between the bit lines and the sense lines. Since the bit lines and sense lines are parallel to each other the coupling is due to both electric and magnetic fields. It is important to reduce this noise as much as possible since it occurs at the end of a rewrite cycle and lengthens the recovery time of the sense amplifier; it therefore increases the memory cycle time. The *major* part of the write noise is due to the coupling between a bit line and the sense line with which it is paired. It is possible to make a signficant reduction in the magnitude of the write noise in this case by taking advantage of the directional properties of the coupling between two parallel transmission lines.[3] To do so it is necessary to place the



(a)



(b)

Figure 4 Write noise on a center line due to identical writing bit pulses of 100 mA each on the associated bit line and the four nearest neighboring bit lines, (a) without, and (b) with, a shorted coaxial cable of proper length connected at the sense line output. The vertical scale is 2 mV per major division; the horizontal scale is 5 nsec per major division.

sense amplifier at the end of the sense line opposite to the driven end of the bit line and then to terminate the two remaining bit and sense line terminals in resistive impedances whose product is equal to a constant. The value of this constant is determined by the electromagnetic characteristics of the bit-sense line structure. Although the value can be calculated directly in idealized situations, experimental determination is generally more satisfactory in memory arrays where deviations from the lossless and homogeneous two-line structures are significant. In the model a bit line termination of 15 ohms and a sense line termination of 50 ohms was found to give the best reduction in noise. Figure 3 compares the write noise observed when the lines were terminated in short circuits with that observed when the proper terminal resistors were

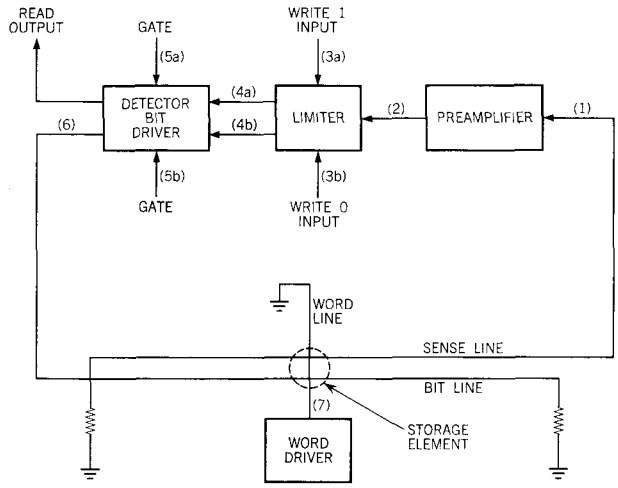


Figure 5a Block diagram of a sense-bit regeneration loop. Numerals in parentheses indicate circuit points cited in the discussion (page 47) and in Figs. 5b and 6.

used. A reduction from 40 mV to 5 mV was achieved in the case illustrated.

Coupling between a sense line and all other bit lines in the array is also a source of write noise. The magnitude of this coupling falls off rapidly with distance and can therefore be reduced by increasing the bit line to bit line spacing. In the model this was not necessary since this coupling contributed only 6 mV of write noise. The total worst case write noise peak amplitude was therefore less than 11 mV, as shown in Fig. 4a. Note that the noise does not return to the baseline after the major noise peak but, rather, remains at an apparent "pedestal" of 2 mV; the decay time of this pedestal is of the order of 1 μ sec. The pedestal is due to the change of the magnetic field distribution with time, this change being caused by the penetration of the fields into the ground conductor as a consequence of resistive losses of the ground conductor. Although the maximum amplitude of the pedestal is only 2 mV it can have a cumulative effect on sense amplifier operation. This effect was obviated by placing in parallel with the sense amplifier input terminals a coaxial cable that is terminated in a short circuit. The delay of the coaxial cable was made equal to the base width of the sense signal; therefore it does not affect the sense signal but reduces the write noise and eliminates the pedestal. The resultant worst case write noise of ± 6 mV, the value finally achieved in the model, is shown in Fig. 4b.

An additional source of noise in the array can be the reactive and resistive discontinuities in the array lines and terminals and in the ground plane. Therefore the mechanical design of the array and its supporting structure was directed towards minimizing these effects. For example, there are only two breaks in the ground plane in the direction of either the sense-bit lines or the word lines.

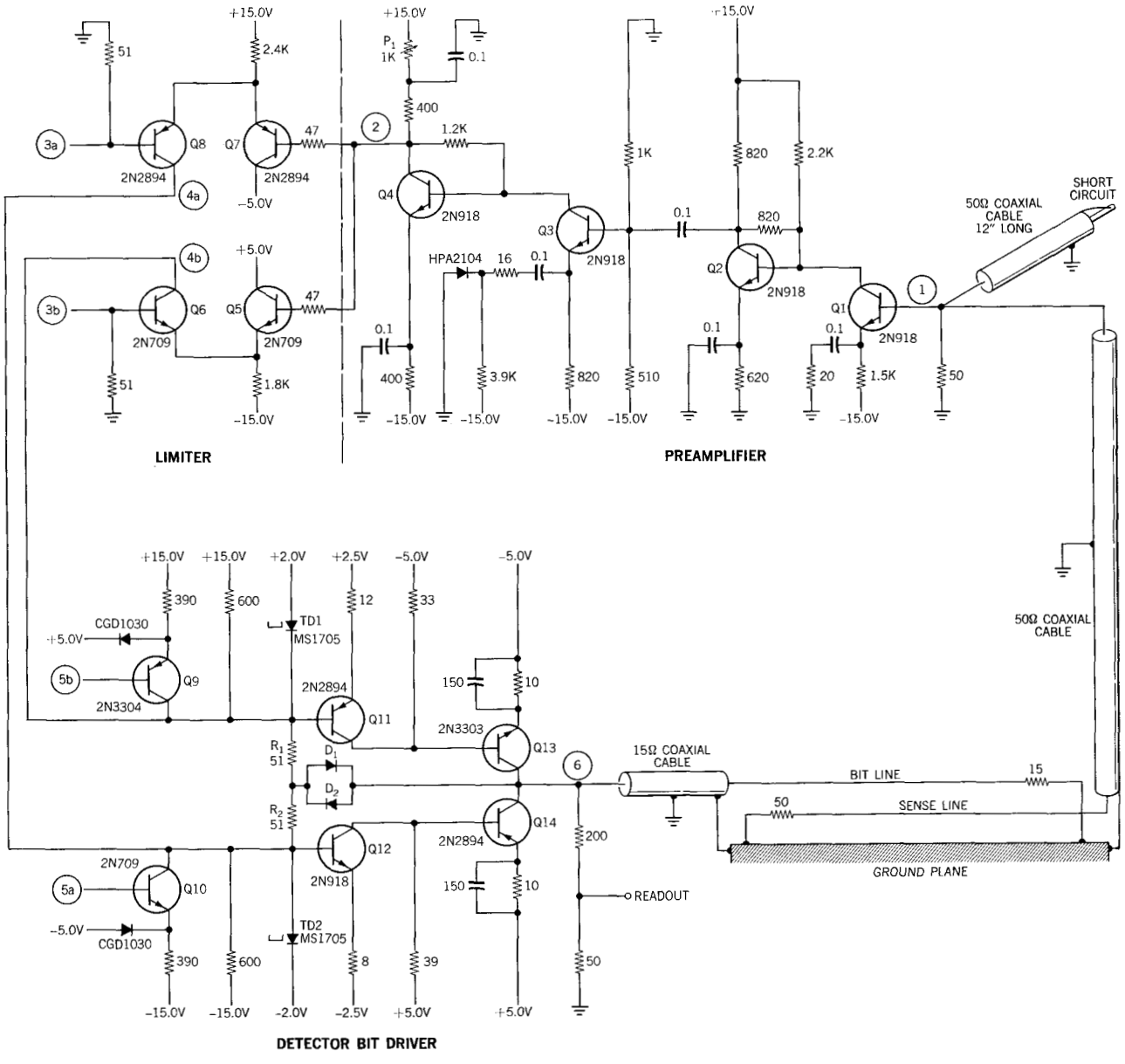


Figure 5b Circuit diagram of the preamplifier, limiter, and detector bit driver circuits.

These breaks occur at the edges of the bit plate where a pressure contact is made between the overlapping ground plane and the bit plate (see Fig. 1). This arrangement permits the removal of the bit plate but also closely approximates a continuous ground plane throughout the entire length of the array lines. In addition, all terminating resistors are soldered directly to the ground plane with leads kept as short as possible to minimize reactance. Coaxial cable is used to connect the array lines to the electronic circuits. Together, these precautions contribute substantially to the reduction of noise and the recovery time of the memory.

Electronic circuitry

The delay and the recovery time of the electronic circuitry, especially that of the sense-bit loop circuits, were minimized by omitting buffer registers from the loops and, instead, combining gated and self-blocking detectors with bipolar bit drivers. Preamplifiers with short rise times were used. In addition, saturation of the amplifiers by write noise was avoided. Further, word drivers with small delay and very fast rise times were designed and employed to speed operation.

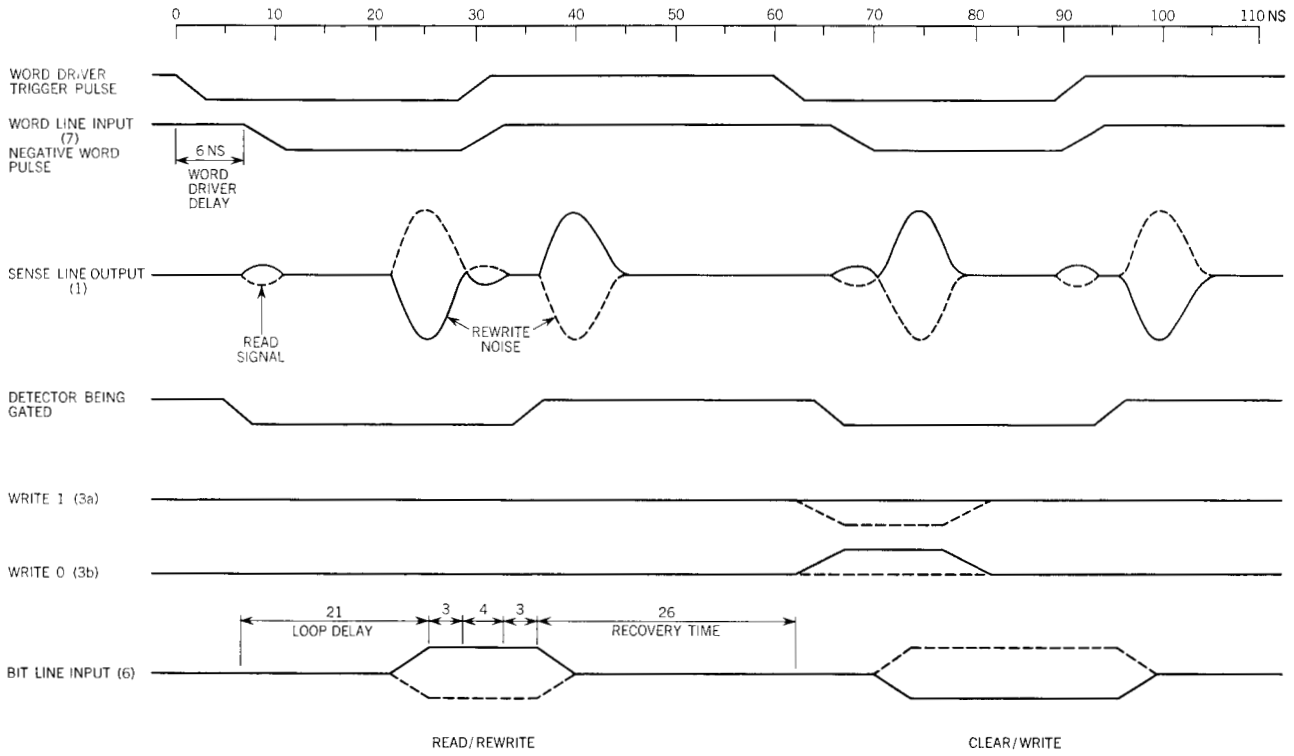


Figure 6 Timing of a read/rewrite and consecutive clear/write cycle.

A block diagram of the sense-bit loop is shown in Fig. 5a and the circuits are shown in Fig. 5b. The circuits are divided in the three sections indicated in both figures as PREAMPLIFIER, LIMITER, and DETECTOR BIT DRIVER. The sense line is connected to the preamplifier input, the bit line to the bit driver output. Typical waveforms and timing are shown in Fig. 6.

The design of the sense-bit loop circuits is based on an assumed minimum read signal of ± 4 mV at the sense line output, and a maximum write noise of ± 20 mV, giving a noise/signal ratio of 5. The ± 20 mV range takes into account the superposition of the coupled write noise and the voltage induced by the rotation of the magnetization of the memory elements during the fall time of the word pulse. The sense line waveforms are amplified by a four-stage preamplifier, of the feedback type[4] which has linear feedback in stages 1, 2, and 4 and nonlinear feedback in stage 3.

The output of the preamplifier is connected to the limiter. The two lines (3a) and (3b) are for writing a ONE or a ZERO, respectively. The limiter pulses one of the two output lines (4a) or (4b) with a current depending on whether a ONE or a ZERO is being read or written. The limiter also reduces the noise/signal ratio from 5 to 1.5.

The tunnel diode detector is conditioned for detection by gate pulses at (5a) and (5b). Depending on the information supplied by the limiter, one of the two tunnel diodes will switch into the high voltage state. The switched tunnel diode turns on a bit driver transistor and holds it in conduction until it is reset by the end of the gate pulse. All noise following the signal during a read/rewrite cycle is rejected by the blocking action of the tunnel diode pair and the nonlinear feedback network composed of D1 and D2. The second pair of complementary transistors in the bit driver is for additional amplification. It supplies bit pulses of either $+100$ mA or -100 mA to the bit line and a readout signal to the output register 21 nsec after the read signal occurs at the preamplifier input.

To write in new information, one of the write inputs is gated before the leading edge of the gate pulse arrives. This causes a current in one of the two output lines of the limiter and its associated tunnel diode; however, this tunnel diode is inhibited from switching by the absence of the gate pulse. When the gate pulse arrives, the tunnel diode switches and blocks the detector before the arrival of the sense signal from the sense line. It thereby rejects both the sense signal and the subsequent write noise.

The circuit diagram of the word driver is shown in Fig. 7. It consists of an input tunnel diode monostable circuit designed to operate from an ACP[5] collector output ($+0.2$V to -0.2V), a grounded emitter stage, an emitter follower stage, and a final grounded emitter stage. The first two stages are operated in the active region while the final stage is driven from cutoff to saturation. The

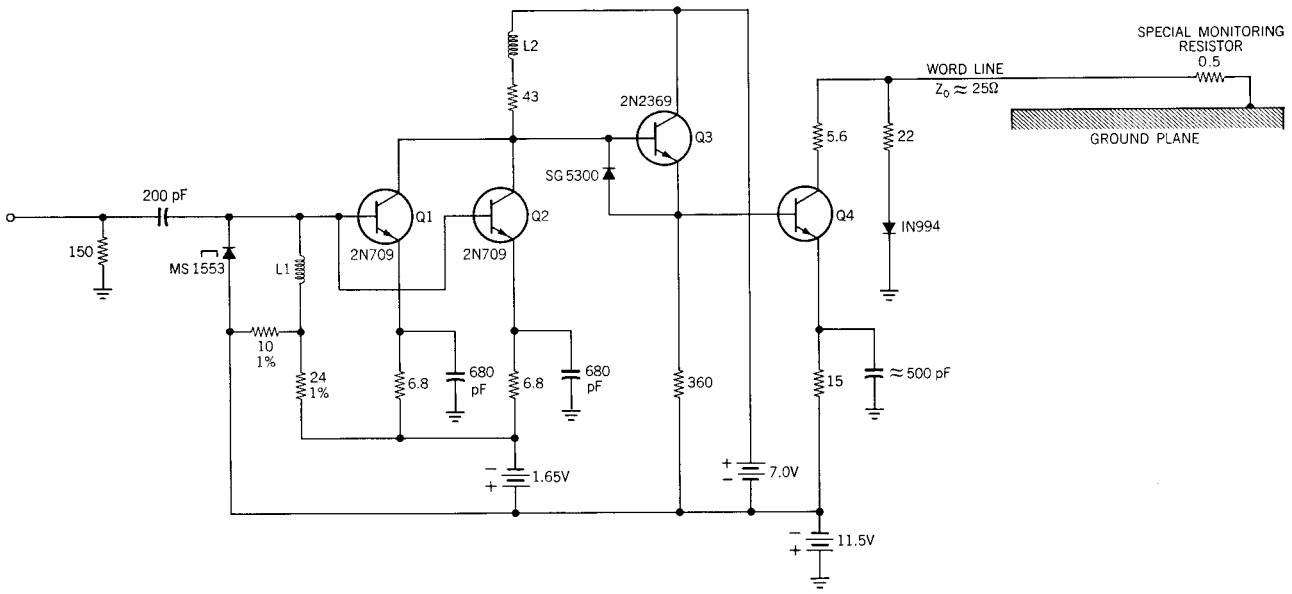


Figure 7 Circuit diagram of the word driver circuit. Element Q4 is an IBM 6B7 experimental transistor.

final stage drives the word line which has a characteristic impedance of 25 ohms and is terminated in a short circuit at the far end. The 5.6-ohm resistor in series with the word line provides a suitable load line for the final transistor. The 22-ohm resistor and the diode in parallel with the word line reduce multiple reflections at the end of the word pulse.

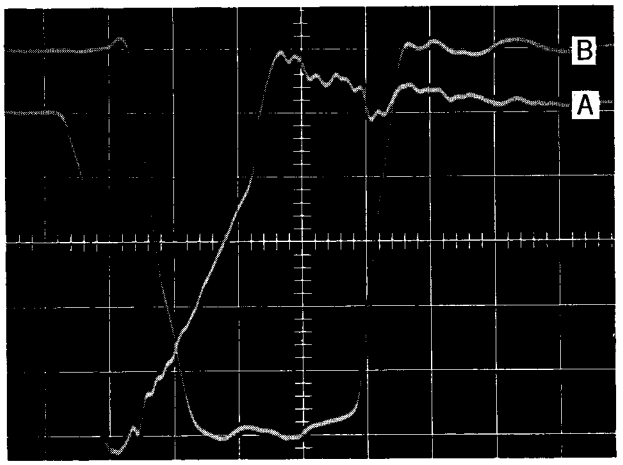
Typical word driver input and output waveforms are shown in Fig. 8, where the input shown is the voltage across the 150-ohm input resistor, and the output is the current in the word line as monitored with a low inductance 0.5-ohm resistor inserted at the end of the word line. The delay of the word driver is 6 nsec. The delay through an ACP 32-word decoder is 5 nsec making a total delay time of 11 nsec.

Organization of the memory

The organization of the memory and its operation in a read/rewrite and a clear/write cycle will be described briefly. The memory bit plate with 32 word lines and 36 pairs of sense and bit lines is shown in Fig. 9. Also indicated are 32 word drivers—one for each word line—with the associated decoder and address registers, and 36 sense-bit loop circuits with the associated input-output registers. The input-output registers are connected to the sense-bit loop circuits by means of "enable read" gates for controlling the read signals and "write" gates for controlling the write signals. Furthermore a gate driver circuit is shown that is common to all 36 sense-bit loop circuits and enables the loop circuits to detect the read and write signals.

The memory cycle is initiated by a "start" pulse which is given after the address register is set and decoded; in the case of writing the input-output registers are also set. The start pulse turns on both the gate driver circuit and one of the word drivers, the output current pulse of which induces read signals in all sense lines, with the polarity of the signals depending on the stored information. The polarity of the read signals is detected in the sense-bit loop circuits which in turn supply readout information and bit pulses of the proper polarity for rewriting.

Figure 8 Wave forms of the word driver circuit. Trace A shows the input trigger pulse (vertical scale: 0.2 V/division); trace B shows the output current pulse (vertical scale: 100 mA/division) as measured across a 0.5-ohm resistor at the end of the word line. The time scale is 5 nsec per division.



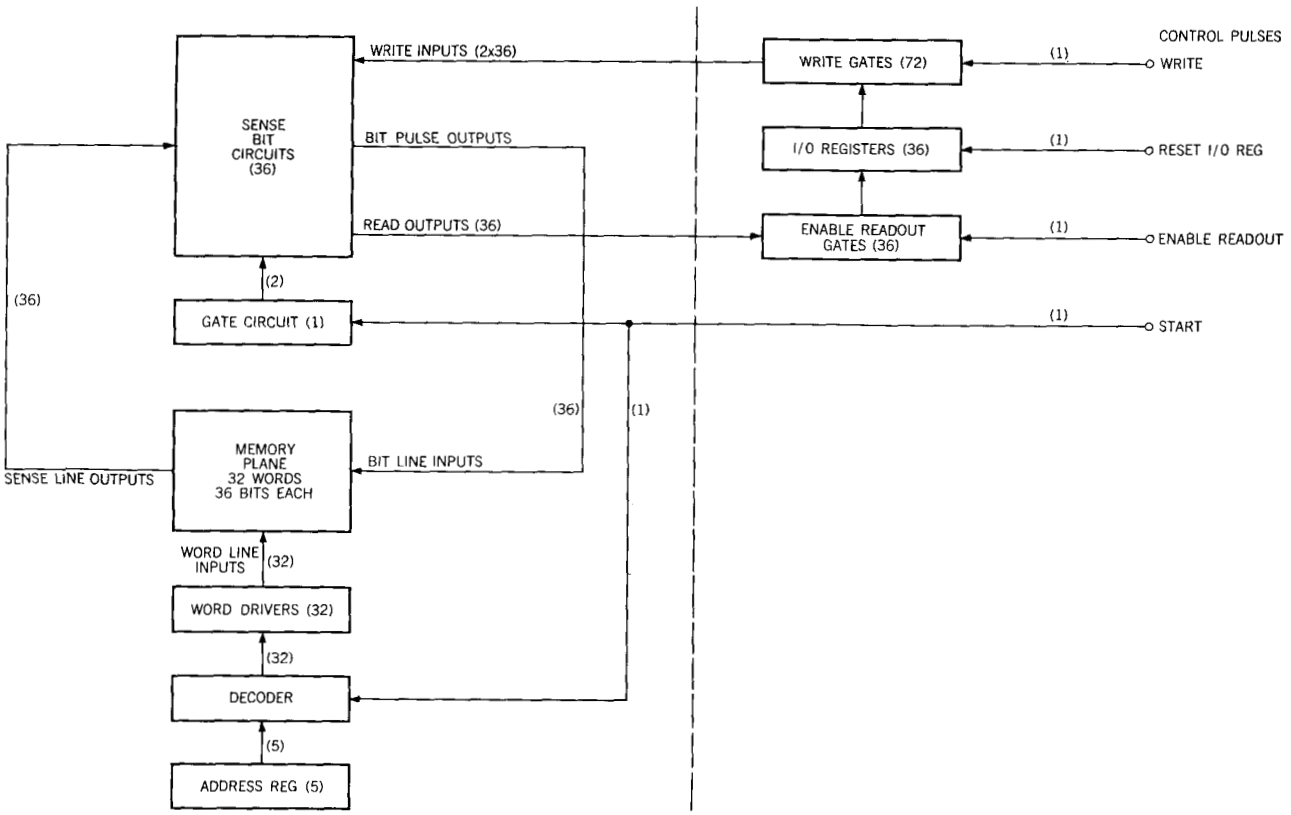
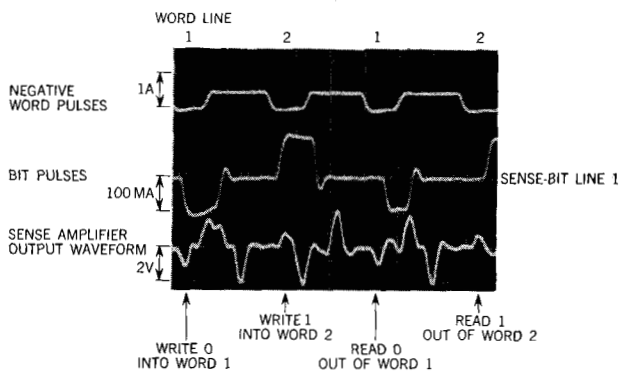


Figure 9 Block diagram of the memory organization.

In order to write new information from the input-output registers into the memory the start pulse is accompanied by a "write pulse". The write pulse transfers the new information via the write gates into the sense-bit loop circuits before the read signals arrive; thus the circuits are blocked not only against the write noise but also against the read signals which are unwanted in this case.

The model was populated with three word driver circuits and three complete sense-bit loops. Oscillograms of two write and two read cycles of this model are shown in Fig. 10 (the second read cycle is displayed only partially). The upper trace shows four word pulses with negative polarity as monitored across a low-inductance 0.5-ohm resistor to which two adjacent word lines (1 and 2) were connected. The center trace displays four bit pulses as monitored at the end of one bit line input and the lower trace shows the wave form at the output of the corresponding preamplifier, this last being the most critical point in the circuit with respect to recovery from write noise. The first two bit pulses indicate write operations while the last two bit pulses belong to read/rewrite cycles. Note that the write bit pulses are wider in time than the read/rewrite pulse. The oscillograms in Fig. 10 clearly show that sufficient overlap exists between word and bit pulses in each cycle and that the voltage at the output of the preamplifier is returned to its quiescent level between consecutive cycles when the memory is operated at a cycle time of slightly less than 60 nsec.

Figure 10 Oscillograms of consecutive clear/write and read/rewrite cycles of the model at 60-nsec cycle time. Upper trace shows negative word pulses in two adjacent wordlines, observed across a common 0.5-ohm monitor resistor; the vertical scale is 1A per major division. Center trace shows write and rewrite bit pulses observed at point (6) of Fig. 5a; the vertical scale is 100 mA per major division. Lower trace shows read signals and write noise as they appear at the preamplifier output (point 2 in Fig. 5a); the vertical scale is 2V per major division. Time scales are 20 nsec per major division.



Conclusion

It has been demonstrated that 1000-bit NiFe film DRO memories with cycle times of 60 nsec and access times of about 30 nsec can be built using existing components. Experience with this model indicates that the design can be extended to allow a significant increase of capacity in a memory having this same cycle time and access time; however, it is felt that to achieve a marked increase in speed will require radical departures from the conventional circuit and array techniques that were employed in the model described here.

Acknowledgment

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