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Glass-Passivated GaAs Chip Tunnel Diode*

Abstract: A novel approach to the fabrication of tunnel diodes is described. The experimental tunnel diode is a gallium arsenide planar device, using a conventional alloyed junction in an epitaxially grown GaAs substrate, and hermetically sealed by a high-temperature glass coating. The tunnel diode is fused to a circuit module using a solder reflow method. This package provides a high degree of mechanical reliability, great reduction in size, and an easy means of interconnection. Another unique feature is that the peak current is tailored electrically to within 1% by altering the impurity distribution near the junction, rather than by the conventional electrochemical etching technique. The resulting gallium arsenide tunnel diodes, having peak currents of 8 mA and capacitances of 5 pF, are suitable for use in a one-nanosecond switching circuit.

Introduction

Since the discovery of the tunnel diode[1] it has been used in numerous experimental high-speed switching circuits, including a 1-nsec circuit that also employs high-speed transistors.[2,3] The present paper describes a new concept for the fabrication and interconnection of tunnel diodes.

Mechanical weakness has been a persistent problem in the design of tunnel diodes.[4] The new structure is designed for better mechanical strength and smaller size than conventional low-peak-current tunnel diodes. Instead of being fabricated in the usual etched-neck configuration, the junction is formed in and is protected by the crystal substrate, providing a strong mechanical structure. Unit size is reduced, and ultimately packing density is thus increased, by passivating the junction with glass and SiO_2 instead of using the bulkier types of hermetic sealing. The small size of the diode unit also minimizes parasitic inductances and capacitances.

As an interconnection method, it was decided to use a solder reflow technique rather than thermocompression bonding. In addition, a single-sided planar configuration was adopted to simplify the soldering procedure.

Because of the contamination sometimes introduced by the conventional electrochemical etching of the junction, causing continued peak-current drift, a different approach was used to adjust the peak current. The adjustment is made by increasing the width of the depletion layer.

GaAs was chosen as the substrate material rather than Ge because GaAs tunnel diodes have a wider voltage swing, have a more linear negative resistance characteristic, have a lower capacitance/unit area for same peak-current density,[5] and can be electrically tailored with relative ease.

Fabrication

• *Crystal substrate*

Instead of growing single-crystal GaAs by the conventional Bridgman method and slicing the crystal into wafer substrates, the experimental tunnel diodes were fabricated on vapor grown GaAs substrates. The GaAs was epitaxially grown on a polished germanium wafer substrate and degenerately doped with zinc during growth.[6] The growth process was not affected because the GaAs heterojunction is not active. The advantages for using such a material are fourfold:

1. *Uniformity of doping.* The uniformity of doping across the wafer substrate is much better in the vapor growth process than in the Bridgman process. The reproducibility in obtaining a desired level of zinc doping in the substrate

* Based on a paper presented at the IEEE Electron Devices Meeting, October 31, 1963, Washington, D. C.

also seems to be much better, as pointed out by Blakeslee.[6]

2. *Size.* The maximum wafer size that can be grown by the Bridgman technique, with the desired degree of doping uniformity, is about $1/2 \times 3/4$ inches. About 150 tunnel diode units can be produced from such a wafer. However, if GaAs is epitaxially grown on a germanium substrate, wafers greater than one inch in diameter can be grown with the desired doping uniformity over the surface of the wafer. More than 1000 tunnel diodes can be obtained from these wafers. Germanium substrates of the size illustrated in Fig. 1 are readily available.

3. *Mechanical strength.* Single crystal GaAs is very brittle and is therefore susceptible to breakage during processing, especially when the wafer is very large. When a germanium substrate is used, the brittle GaAs is mechanically supported by the stronger germanium.

4. *Electrical characteristic.* It has been our experience that vapor grown GaAs yields tunnel diodes with higher peak-to-valley current ratio than Bridgman-grown GaAs.

• *Insulator*

An adherent silicon dioxide film 3000 Å thick is pyrolytically deposited over the wafer surface at 700°C and covered with a glass film two microns thick. This SiO_2 film is necessary to prevent a reaction between the glass and the GaAs, resulting in the formation of an undesirable compound at the glass-GaAs interface. In general the glass film should have the following properties. It should form a permanent bond to the SiO_2 film, should have a thermal expansion coefficient which matches that of the GaAs, and should be easily etchable to a microscale accuracy. In addition it should not adversely affect the tunnel diode characteristic, should be impervious to water molecules or other solvents, should be relatively inert to the various chemicals used in the fabrication process, and should have a high temperature softening point and a low dielectric constant and dissipation factor.

A thin layer of glass meeting these requirements is applied over the surface of the SiO_2 by a technique similar to that described by W. A. Pliskin et al.[7,8] These glassing techniques were developed at IBM and are also used on silicon diodes and transistors.

A standard photolithographic technique is used to produce the pattern for an array of a 0.5-mil-diameter hole (tunneling junction) and two 3-mil-diameter holes (ohmic contact). The holes are etched through the glass and SiO_2 using a special glass etch and buffered HF, respectively. This 0.5-mil-diameter tunneling junction results in a 0.5-pF junction capacitance. The ohmic contacts are actually reverse-biased tunnel diodes with a total peak current at least 20 times that of the tunneling junction.

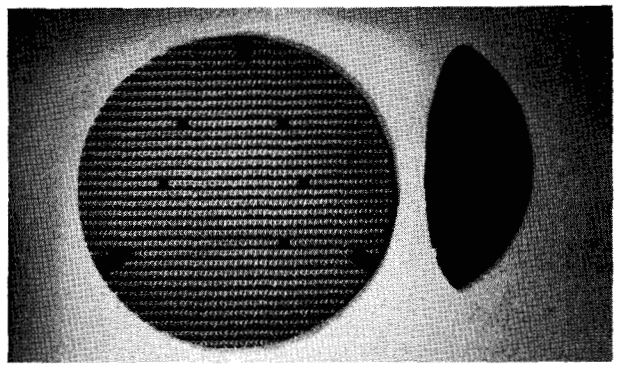


Figure 1 **GaAs single crystal substrates grown by (left) epitaxial method, wafer about one inch diameter, and (right) Bridgman technique.**

• *Alloying*

A tin dot is then evaporated over the holes in the insulator, using a metal mask. The total dot volume is adjusted to obtain good diode characteristics without excessive penetration which might crack the insulator.

The alloy junction is then formed by heating the wafer to 600°C and cooling rapidly. It is found that the alloy temperature has a strong influence on the tunneling peak current. The spread in peak currents over the wafer surface closely resembles a standard Gaussian distribution with 90% of the units within the limits $I_{median} \pm 33\%$. Therefore, since the final peak current is to be 8 mA, the substrate doping is chosen so that the range of peak currents over the wafer surface is 8 to 16 mA after alloying.

The typical spreads in peak current and peak-to-valley current ratios are shown in Figs. 2 and 3. Note that the average peak-to-valley current ratio is 40 to 1, and that the spread in peak current is a factor of two.

• *Contact*

It is desirable to remove the low-melting tin and to replace it with a high-temperature ohmic contact to the regrown GaAs inside the holes. First, the wafer is heated and the molten dots wiped away. Then a high-temperature metallic contact is evaporated over these holes in order (1) to make a good electrical connection to the exposed regrown region, (2) to hermetically seal the active area, and (3) to provide a solderable land to which the electrical connections can be made.[9] This contact adheres tenaciously to both the glass and the GaAs. Sn-Pb solder is subsequently evaporated over these lands.

The interconnection scheme for placing the unit in a final circuit is identical to that described by E. M. Davis et al.[10] Metallic balls 5 mils in diameter are placed over

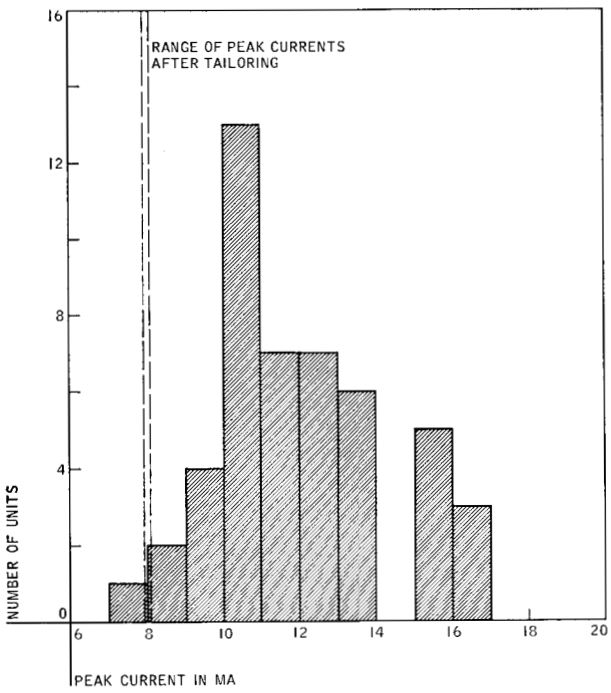
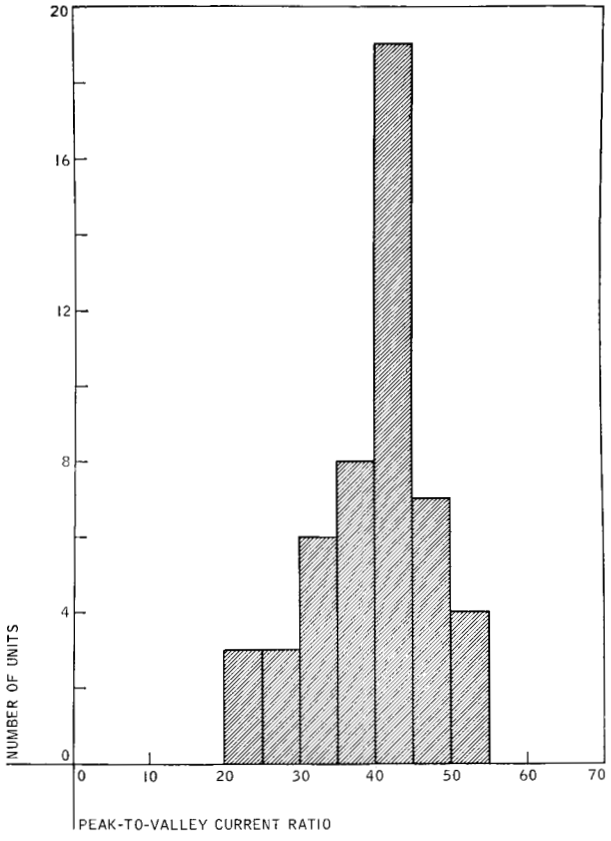


Figure 2 **Distribution of peak currents on epitaxially grown GaAs.**

Figure 3 **Distribution of peak-to-valley current ratios on epitaxially grown GaAs.**



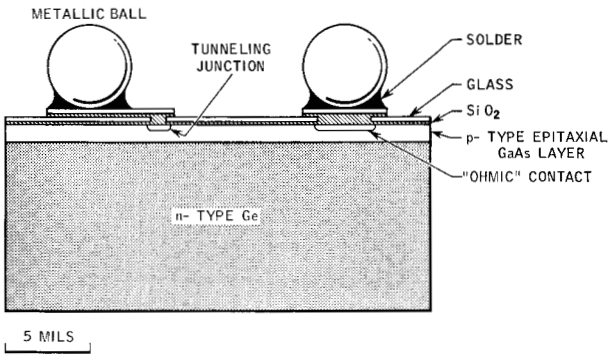
the lands and soldered en masse. To avoid pressure effects on the tunneling junction,[11] the metallic ball rests on the glass at one side of the junction hole and is connected to the regrown region by the thin metallic finger, as shown in Fig. 4. The wafer is then cut into individual devices and these devices are soldered via the metallic balls to metallized lands on an alumina module with pluggable pins.

• *Peak current tailoring*

At this point, the peak currents over the wafer vary up to twice the final desired peak current. The peak currents are tailored to the desired $I_p \pm 5\%$ tolerance by passing a high forward current through the junction at some elevated temperature.[12] Straight line plots of ln I_p vs $\sqrt{\text{time}}$ are obtained (see Fig. 5), implying that the reduction in the peak current is due to some impurity diffusion at the junction.[13] The peak current, I_p, during tailoring can be expressed mathematically as $I_p(t) = I_p(0) \exp -\{\alpha (t_0 + t)^{\frac{1}{2}}\}$, where t is time, α is a function of both temperature and current density, and t_0 represents that amount of tailoring that has taken place during the fabrication of the tunnel diode prior to the tailoring process. The present tailoring is carried out at ~10,000 A/cm^2 at 100°C. Under these tailoring conditions the values of the various other parameters of interest, and in particular the valley current, do not change appreciably. This scheme of tailoring is inherently easy to automate with a high degree of accuracy. A prototype which has the ability to tailor peak currents within 1% tolerance is now in operation.

The slope, α, of the ln I_p vs $\sqrt{\text{time}}$ was found to be a very fast moving function of the current density through the junction, as indicated in Fig. 6. Therefore, although the peak currents decrease rapidly under high bias, they are extremely stable under actual operating bias. To illustrate this, one can relate these α to the time required

Figure 4 **Schematic side view of GaAs chip tunnel diode.**



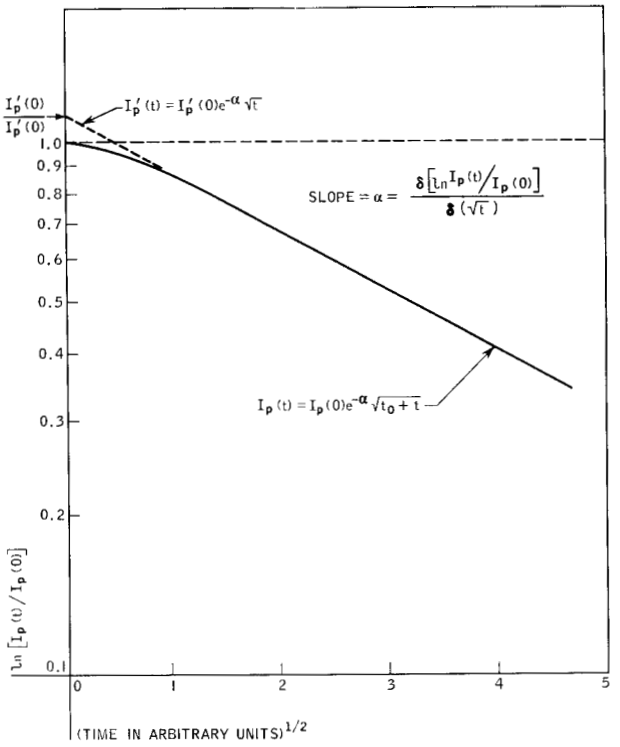


Figure 5 **Reduction of peak current vs time under constant bias conditions during tailoring.**

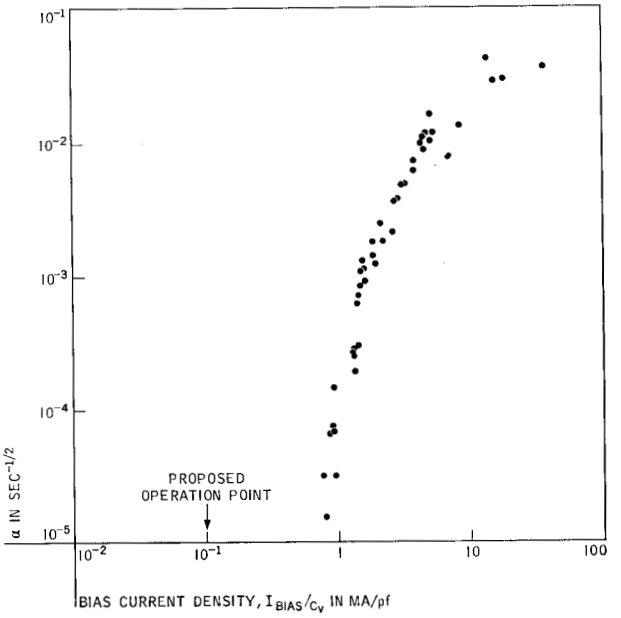
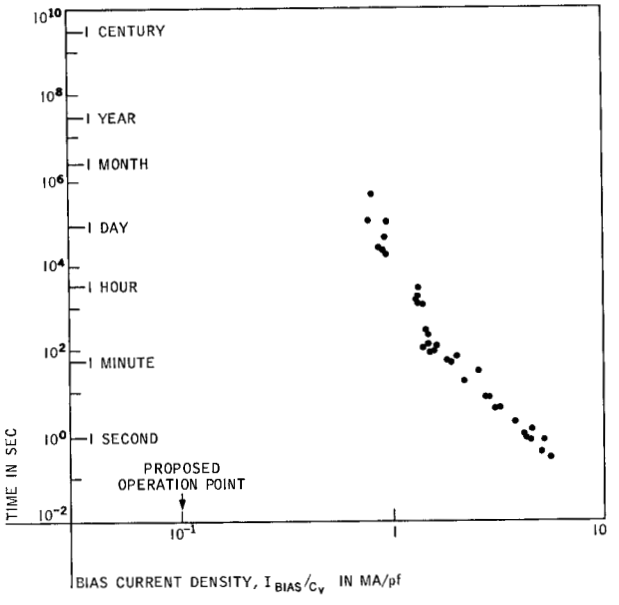


Figure 6 **Dependence of slope, α, on bias conditions I_{bias/c_V}.**

Figure 7 **Time required for 1% change in peak current as a function of bias condition I_{bias/c_V}.**



for a 1% change in the peak current shown in Fig. 7. At 5 mA/pF bias, i.e.,

$$\frac{\text{current bias}}{\text{junction capacitance}} = \frac{5\text{mA}}{\text{pF}},$$

the peak current changes 1% within 1 second; whereas, at 1 mA/pF it takes a few hours to observe such a change. If one can extrapolate this graph, it would take over a century to observe a 1% change in the peak current at 0.1 mA/pF, which is the maximum operating bias to which the diode will be subjected.

Results

Preliminary reliability studies were conducted on a total of 200 GaAs tunnel diodes fabricated in the manner described above. They were subjected to the following test conditions (see tabulation on page 531). Early on life test, three units exhibited an increase in valley current greater than a factor of 2 when subjected to #6 test condition.

Conclusion

This paper has shown how silicon planar technology has been adapted in the design of a new type of tunnel diode. The inherent peak degradation of GaAs tunnel diodes was utilized in the new fabrication method. The experimental high-speed diodes feature mechanical ruggedness and compactness, electrical stability, and ease of fabrication.

One aspect of this tunnel diode design that has not yet been explored is the lower limit of the diameter of the

	Test Conditions			No. of Samples
	Bias	*Temp.*	*Humidity*	
1	None	RT	*	20
2	None	100°C	*	20
3	None	85°C	85% RH	60
4	−50mA (reverse bias)	100°C	*	20
5	0.1 V (bias at peak)	100°C	*	20
6	0.7 V (bias near valley)	100°C	*	60

* Room ambient

holes that can be etched with precision in the glass. This, of course, is important for reproducible characteristics in ultra-low-capacitance units.

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