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Design of ACP Tunnel-Diode-Coupled Circuits

Abstract: The performance of the Advanced Circuit Program (ACP) circuits described by D. H. Chung and J. A. Palmieri[1] can be improved by replacing the coupling resistor with a pair of tunnel diodes. The low impedance and power gain properties of the tunnel diode increase the fan-power and provide better control of signal levels. In addition, the improved rise times increase circuit speeds to the extent that delays of less than 1 nsec per logic function have been demonstrated. Since the tunnel diode pair can be designed to perform AND, OR, or majority logic functions, the logic flexibility of these circuits is greater than that of the resistor-coupled circuits. The design techniques which lead to a consistent set of logic circuits and to binary full adders are discussed.

The very fast rise times generated by the tunnel diode pair require the use of transmission lines as the interconnection medium. The techniques used to minimize the effects of noise and reflections on circuit performance are discussed.

Introduction

The circuits described in this paper employ the transistor circuit configuration described previously[1] but develop the output voltage by means of a tunnel diode pair - resistor combination. The presence of this additional nonlinear device makes significant changes in the design, as well as the performance, of these circuits. The tunnel diodes enable greater fan-power, provide better control of the signal levels, decrease the delay significantly by improving the rise time by a large factor, and increase the logic flexibility of the circuits.

The goal of the design techniques described in the following sections is to obtain the optimum steady-state performance, while arbitrarily selecting a minimum number of circuit parameters. Other constraints, such as tolerances and transient considerations, force certain parameters to fall into a specified range. The nonlinear methods used to evaluate these unknowns in the design of the actual circuit family will be shown.

In the design of any circuit involving a large number of components, it soon becomes apparent that a strict worst-case design is so pessimistic that the circuit performance must suffer. It is so with these circuits. Therefore, in order to improve the performance, while still maintaining a satisfactory reliability level, the fan-in, fan-out evaluation utilizes statistics. These statistical techniques are quite simple, and the designer can insure that any error introduced by approximation leads to a more conservative reliability figure.

In order to demonstrate the flexibility provided by the tunnel diode pair, a binary adder will be described.

Current switch and cascode inverter design

The circuit configurations to be designed are shown in Fig. 1. Table 1 lists the various parameters and the method by which they will be determined. It is clear that an uncommonly large number of parameters are determined by the design techniques.

The objective of the following design procedure is to determine the emitter resistors, R_1 and R_2, and the voltage levels, V_{up} and V_{down}, which will optimize the circuit per-

[1] D. H. Chung and J. A. Palmieri, "Design of ACP Resistor-Coupled Switching circuits," *IBM Journal* 7, 190 (1963).

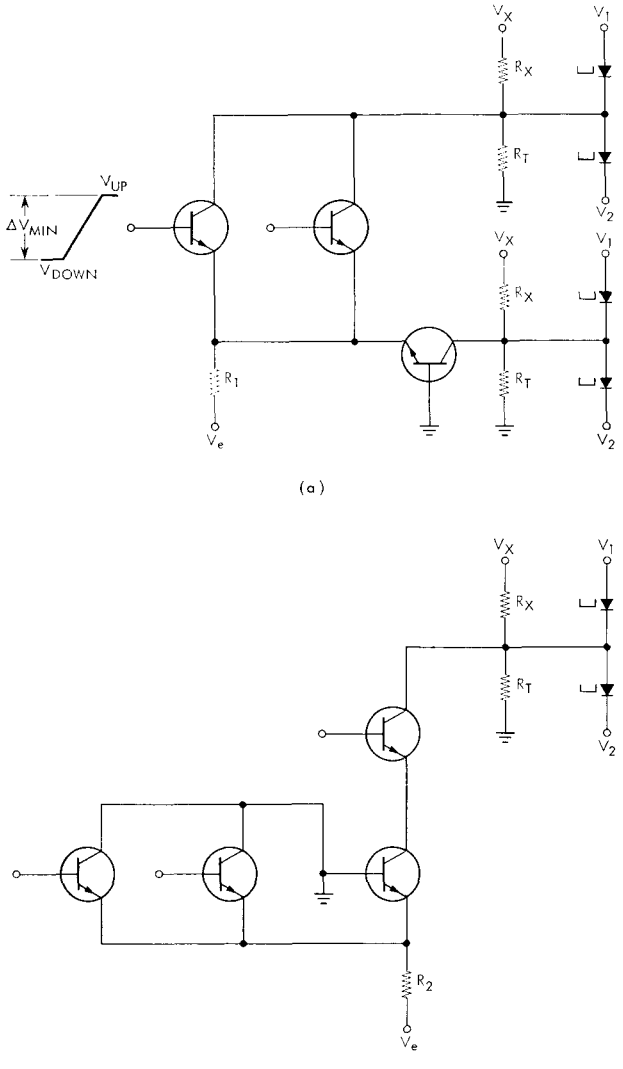


Figure 1 **The circuit configurations for tunnel-diode coupled circuits.** (*a*) *current switch,* (*b*) *cascode circuit.*

Table 1 **Parameters to be determined for circuits in Figure 1**

Parameter	*How Determined*
V_X	design
V_1	design
V_2	design
V_e	selected at −3.0 v
R_X	design
R_T	set by 50-Ω interconnections
R_1	design
R_2	design
V_{up}, V_{down}	design
ΔV_{min}	transient considerations and design
Transistor	specified
Tunnel diode	specified
Tunnel diode peak current	transient considerations
Junction temperatures	specified
Resistor tolerance	specified
Power supply tolerance	specified, and distribution system
Fan-power	design

Table 2 **Voltage and resistor tolerances.**

Component	*Tolerance*
Resistors	±1%
±3 v supply	$\pm 1\%, {}^{+14}_{-26}$ mv, on magnitude
Small (0.2 v) supplies	$\pm 1\%, {}^{+4}_{-6}$ mv, on magnitude

formance for a certain minimum signal swing. Optimum performance, in the steady state sense, simply means the maximum fan-power.

Any particular output node is loaded with both bases and collectors, which draw current. These "collectors" may be groups of collectors with their emitters in common, collectors of entirely separate circuits, or any combination of the two. To avoid confusion, the points indicated by I_1, I_2, and I_3 in Fig. 2 will be referred to as "outputs." The current drawn at the outputs forms an unwanted leakage except when an output is full on; then the current must switch the output diode pair. The output ON currents, the output OFF currents, and the base currents are functions of R_1, R_2, V_{up}, and V_{down}.

A figure of merit that is the difference between the minimum ON current of one output and the maximum leakage current of four outputs and four bases is used in this optimizing procedure, since approximately equal balance between outputs and bases is desired. This difference will be maximum for a certain set of R_1, R_2, V_{up}, and V_{down}. This figure of merit also indicates the allowable worst-case variation in the tunnel diodes and resistors at the output node.

• *Output currents*

The minimum necessary fan-in capability of each circuit type is determined by logic studies. Figure 2 shows the fan-in for the two circuit types which results in adequate logic flexibility.

The first step in the design is to obtain data for the currents I_1, I_2, and I_3 as a function of V_{in}, R_1, and R_2. The specified transistor parameters and tunnel diode parameter tolerances are listed in Ref. 1. Other tolerances

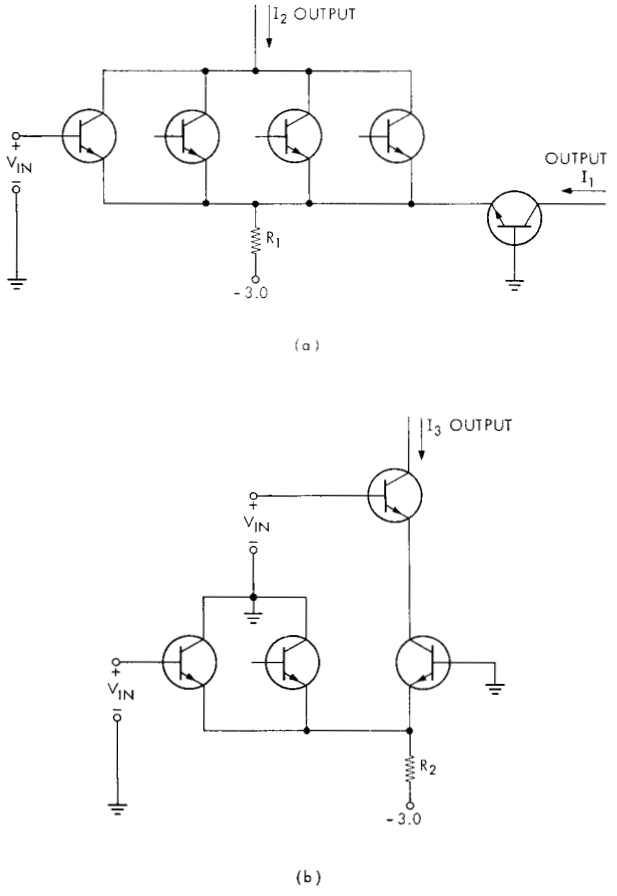


Figure 2 **Fan-in for two circuit types to give adequate flexibility of logical operations.** *(a) 4-input current switch. (b) 3-input cascode* IMPLICATION *circuit.*

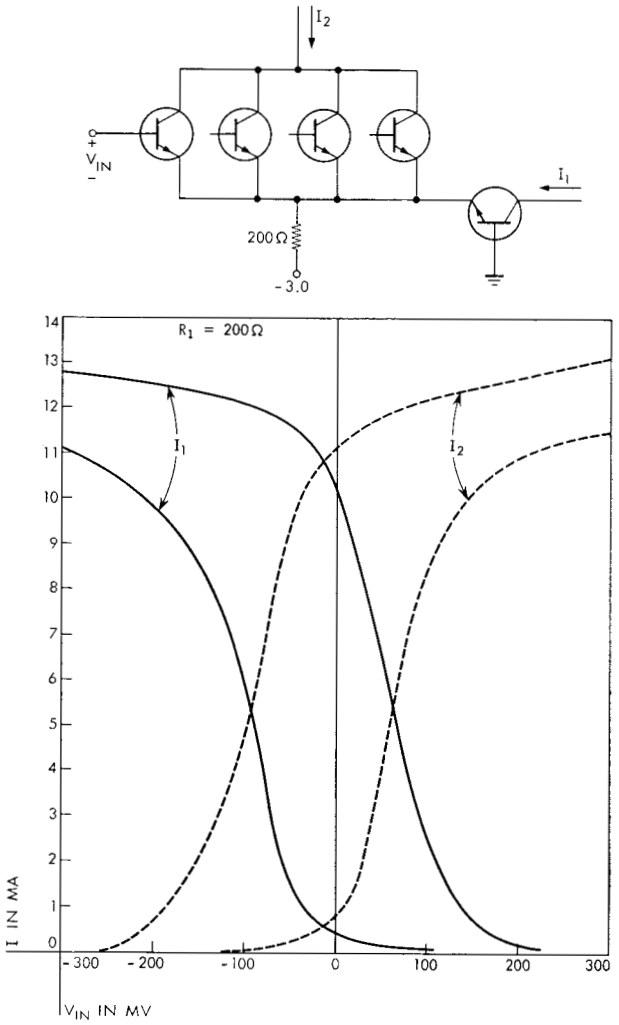
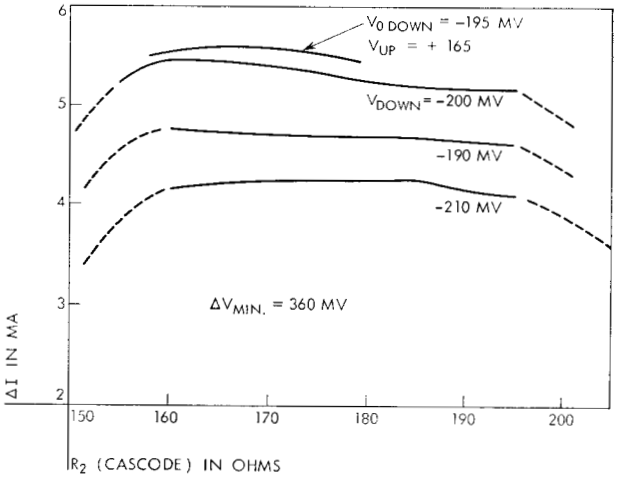


Figure 3 **Collector currents I_1 and I_2 as function of V_{in}, with R_1 as a parameter.**

Figure 4 **Plot of I (net switching current) vs R_2 for given V_{min} and with V_{down} as a parameter.**



may be found in Table 2. It is now a straightforward procedure to obtain curves of V_{in} vs I_1 and I_2, with R_1 as a parameter. Graphical analysis of the emitter node is one method. Figure 3 shows one such resulting curve. To give the proper tolerance picture, the maximum currents are obtained at 50°C while the minimum currents are obtained at 25°C.

Inspection of this typical curve shows that a signal swing in the neighborhood of 400 mv enables what could be called "full switching" of the output currents. Because of restrictions imposed by the series resistance of a 50-ohm stripline and the characteristics of the tunnel diode pair, the minimum signal swing is taken at 360 mv. The reasons for this choice will be given later.

Using transfer function curves similar to those shown in Fig. 3, the various minimum-ON currents and maximum-OFF currents are assembled as functions of the emitter resistors R_1 and R_2 and the input voltage levels. At a particular least-negative down level, emitter resistor, and with a constant swing, the quantity $\Delta I = I_{min-on} - 4(I_{off} + I_b)$ is found. This quantity is plotted as a function of R_2 and

the least negative level, as is shown in Fig. 4 for the cascode circuit. From this graph the optimum emitter resistors and input levels are determined. The resulting parameters are:

Least-positive up level = 165 mv
Least-negative down level = −195 mv
R_1 = 185 ohms
R_2 = 170 ohms
I_{min-on} = 10.25 mA
I_{max-on} = 13.6 mA

We now have sufficient information to design the output node. Prior to designing this, a description of the interconnection technique is in order.

Interconnection method

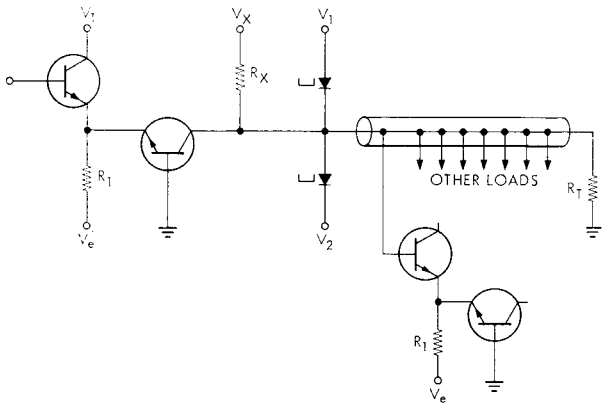
Since the tunnel diodes can be expected to generate rise times less than 1 nsec, practical interconnections will invariably behave as transmission lines. Consider the circuit of Fig. 5. We can expect that the loads, which have been placed on the line, would disturb its characteristics in some degree. Measurements of the input capacitance of the current switch as a function of the input (dc) voltage give the results shown in Fig. 6.

Empirical results have shown that for the purposes under consideration, the average capacitance may be used with good results. There is, of course, a resistive component, but it may be neglected without serious error. What we have, then, is a transmission line with 10-pF loads distributed along it. If we assume that these loads are distributed uniformly, the results are a transmission line of new characteristic impedance given by

$$Z_0' = \sqrt{\frac{L_0}{C_0 + C_b}},$$

where $L_0 = (Z_0/c)\sqrt{\epsilon_r}$, $\quad C_0 = \sqrt{\epsilon_r}/Z_0 \cdot c$,

Figure 5 **Circuit showing the ACP interconnection technique.**



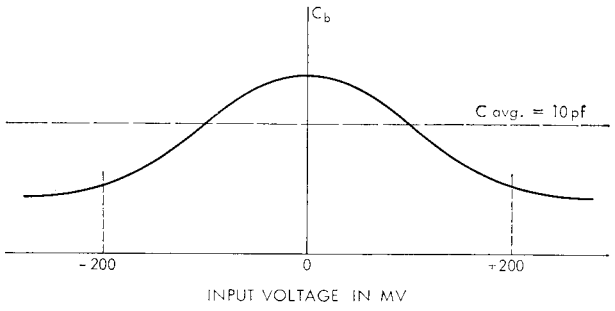
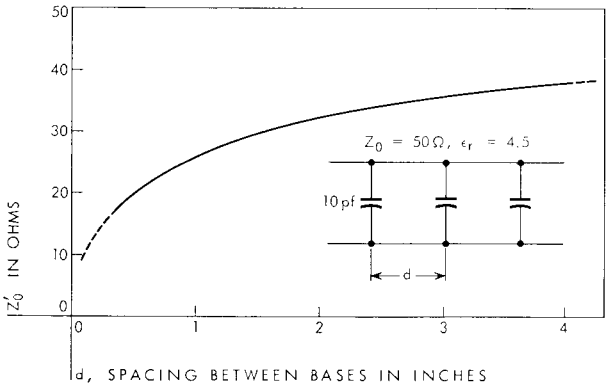


Figure 6 **Current switch input capacitance vs input voltage.**

Figure 7 **Plot of Z_o' as function of distance between bases.**



and Z_0 is the characteristic impedance of the unloaded line, ϵ_r is the relative dielectric constant, c is the velocity of light, and C_b is the average circuit input capacitance. In order to determine the range of impedances which must be driven, we plot Z_0' as a function of the distance between bases in Fig. 7. Empirical results have shown good agreement with this postulated line behavior over the range of spacings from 0.3 inch to about 4 inches. This range is expected to handle most situations which would occur in a large machine using the package techniques described.

The lowest impedance which the diodes must drive is the impedance of one line loaded with bases every 0.3 inch, namely, 15.7 ohms. When the circuits are connected in a machine, care is taken to avoid an impedance lower than 15.7 ohms and to properly match the loaded lines.

Output node design

Figure 8 shows a composite diode pair with specified tunnel diodes and 500 mv difference across the two diodes. The two straight lines represent the lowest resistance the diode pair can drive. The distance between the lines is the ΔI_D for diode tolerances. Then $R_p = (R_x R_T)/(R_x + R_T)$,

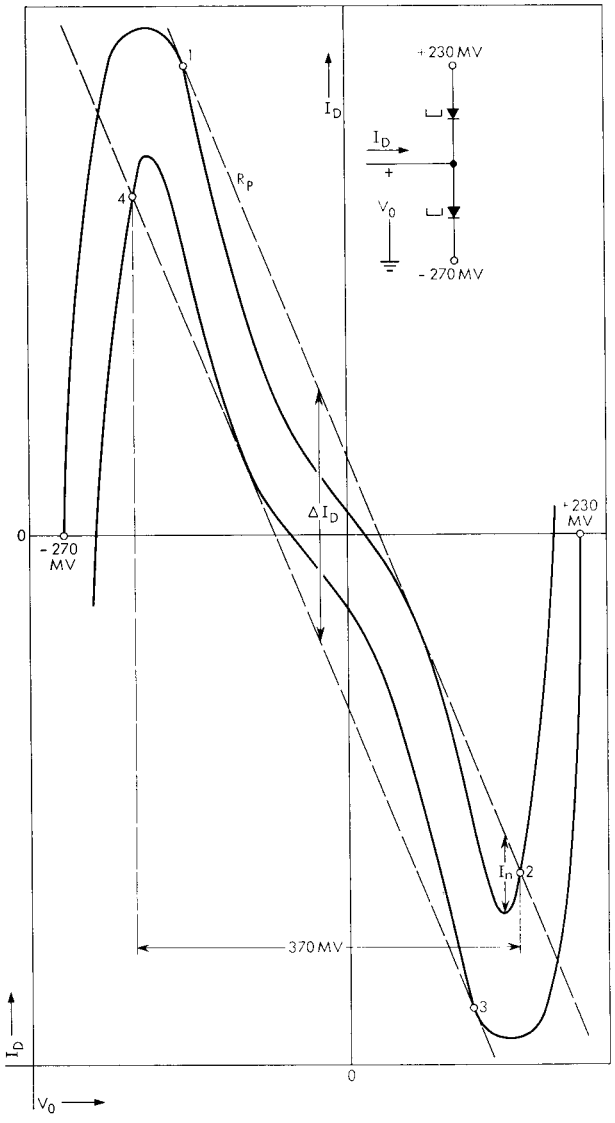
where R_T = 15.7 ohms, and R_x is the bias resistor (see Fig. 10).

Assuming that the current axis scales directly when the peak current, I_p, changes, data for R_p vs I_p and R_p vs ΔI_D are obtained. This information is plotted on Fig. 9.

If R_x is sufficiently large so that R_p = 15.7 ohms, a peak current of 13 mA for the tunnel diode is indicated. Actually a choice of a 13.4 mA peak current is a better selection. Now, if R_x = 500 ohms, R_p = 15.2 ohms is assured, and the possibility of operation in the negative resistance region is eliminated.

The points (1), (2), (3), and (4) shown in Fig. 8 represent the boundaries of satisfactory operation. Points (2) and (4) are the least-positive level and least-negative level,

Figure 8 **Plot of V_o vs I_D for composite diode pair with 500 mv across pair.**



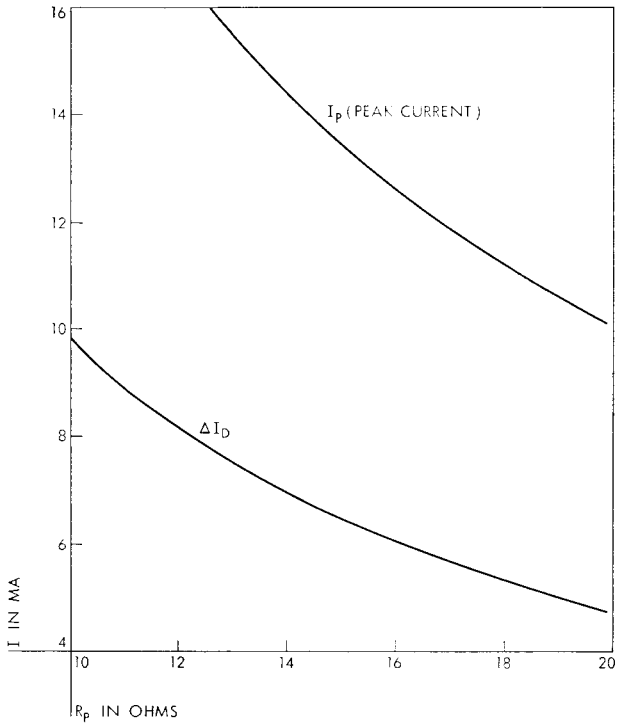


Figure 9 **Peak current and spread of I_D vs I_p (see text).** *500 mv across specified diode pair.*

respectively. The voltage from (2) to (4) is 370 mv. Of this swing 10 mv is lost in the voltage divider created by the series resistance (0.25 ohm/ft) in the stripline and by the terminating resistor.

We choose the diode power supplies such that points (2) and (4) will be +170 mv and −200 mv. For convenience, the bias supply is chosen at +3.0 v. The network to be designed is shown in Fig. 10. Equations are written to guarantee proper operation under load [points (1) and (2) are not violated], and proper switching with the minimum-ON current [points (3) and (4)]. The effects of power supply noise and line crosstalk are included in

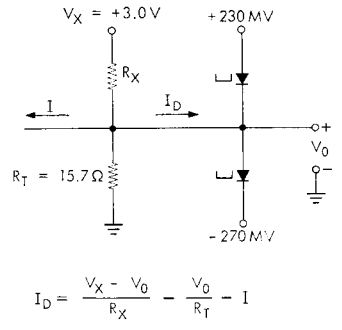


Figure 10 **The circuit from which equations are written to design the output node.**

these equations. Solutions to these equations provide the value of the bias resistor and the load current which can be tolerated. These are $R_x = 530\ \Omega$ and fan-power current = 3.15 mA.

Logic circuit fan-power

In the Appendix of the paper by Chung and Palmieri[1] are discussed the statistical tools that are used in determining the fan-power. This Appendix also demonstrates how the distributions of base current and collector current are obtained. Figure 11 shows the pertinent collector OFF current distributions for this design. Table 3 summarizes the information obtained from these distributions, based on the computations from the Chung-Palmieri Appendix, that

for 2 collectors $m_2 = 3b/4$
$\sigma_2 = 3/8b$
$\therefore\ m_1 = 3b/8$
$\sigma_1 = 3b/8\sqrt{2},$

for 4 collectors $m_4 = 4b/3$
$\sigma_4 = 8b/5(3.1)$
$\therefore\ m_1 = b/3$
$\sigma_1 = 4b/5(3.1),$

where b is the maximum current of one collector.

Table 3 **Summary of data obtained from collector OFF current distributions.**

	b	*1 to 4 outputs*		*Over 4 outputs*	
		m	σ	m	σ
I_1	0·5	0·1875	0·133	0·167	0·129
$I_2/4$	0·175	0·263	0·0928	0·233	0·0903
I_3	0·6	0·225	0·159	0·2	0·155

The mean and deviation of the base current are found to be $m_b = 0.21$ mA and $\sigma_b = 0.08$ mA.

The maximum allowable failure rate was defined to be one case in a thousand. Whenever the fan-power was such that the failure rate was higher than this, a base or output was eliminated until the failure rate was less than 0.001. Two sample calculations will determine how the figures in Table 4 were generated.

For two outputs and eight bases:

$$\underbrace{N_c m_c + N_b m_b}_{m_T} + 3.1\sqrt{\underbrace{N_c\sigma_c^2 + N_b\sigma_b^2}_{\sigma_T}} \leq 3.15\ \text{mA}. \tag{22}$$

since $m_T + 3.1\ \sigma_T$ corresponds to the point where the failure rate is 1 in 1000.

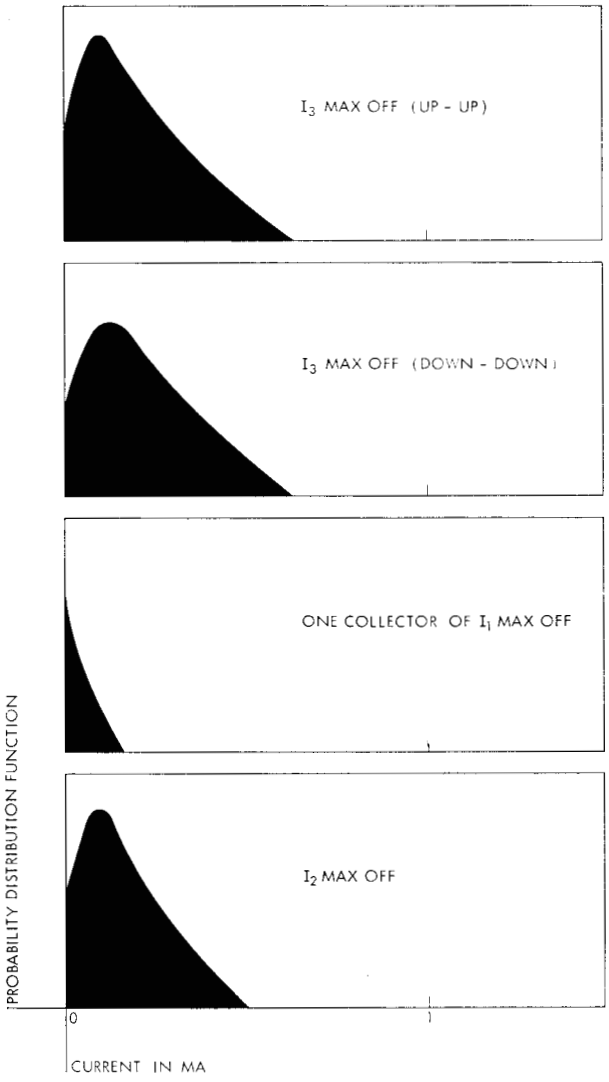


Figure 11 **OFF current distributions for current switch (185Ω) and cascode (170Ω).**

Equation (22) becomes

$$2(.225) + 8(.21) + 3.1\sqrt{2(.159)^2 + 8(.08)^2} \leq 3.15\ \text{mA}$$

or $$3.12\ \text{mA} \leq 3.15\ \text{mA}.$$

Therefore, this fan-power is allowed. The actual maximum failure rate is found as follows:

$$m_T + y\sigma_T = 3.15\ \text{mA}$$

$$y = \frac{3.15\ \text{mA} - m_T}{\sigma_T}$$

$$y = \frac{3.15\ \text{mA} - 2.13}{.319\ \text{mA}} = \frac{1.02}{.319} = 3.2.$$

The probability when $y = 3.2$ is found from a table to be 7 cases in 10,000.

For two outputs and nine bases:

$$2(.225) + 9(.21) + 3.1\sqrt{2(.159)^2 + 9(.08)^2} \leq 3.15 \text{ mA}$$

$$3.36 \text{ mA} \nleq 3.15 \text{ mA}.$$

Therefore, this fan-power is not allowed.

To summarize, we again stress the point that what we have found and used are actually worst case distributions.

Because of the great complexities of combining a large number of random variables, we have consistently made worst-case simplifications. Although only elementary statistical techniques are used, the results justify greatly increased fan-powers.

With 3.15 mA of available current we could have a worst case fan-power of 2 outputs and 4 bases. But we have a fan-power of 2 outputs with 8 bases, and still we are being very conservative.

Table 4 **Fan-power tabulation**

Bases	*Outputs*	*Maximum Probability of Failure**
1	7	1×10^{-4}
2	7	9
3	6	6
4	5	3
5	4	1
6	3	2
7	2	1
8	2	7
9	1	2

* Probability of Failure = Prob [$I_{off} \geqq 3.15$ mA]

• *Circuit performance*

Figure 12 shows the waveforms through four circuit levels which are a mixture of inverting and noninverting circuits, each driving a total of eight circuits. The average delay is 1.75 nsec.

Since two levels of logic may be performed in this time, the delay per logic function is well under 1 nsec.

Adder logic block

The circuits described previously have all been designed to switch with one unit of collector current. By "prebiasing" the tunnel diode network many other useful logic functions may be obtained. To illustrate this, a binary full adder will be described which has controls to permit it to perform the EXCLUSIVE OR, AND, and OR functions as well as generate the SUM and CARRY functions.

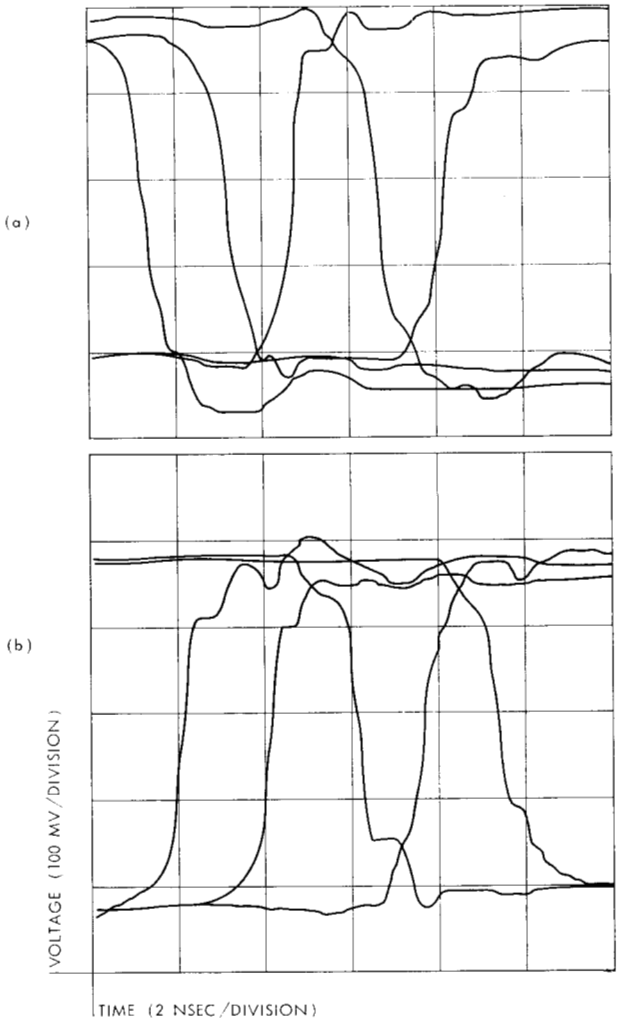


Figure 12 **Waveforms through four circuit levels, each driving a total of eight bases.** (*a*) *Leading edge,* (*b*) *trailing edge.*

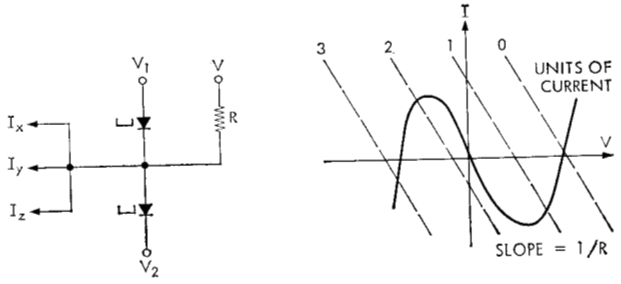


Figure 13 **Circuit for implementing Eq. (23).**

• *Binary full adder*

We begin by noting that the CARRY function C can be written as the following function of the three inputs x, y, z.

$$C = yz + x(y + z). \tag{23}$$

This function can be implemented by the circuit shown in Fig. 13. If I_x, I_y or I_z can be either 0 or 1 unit of current,

the V vs I load-line diagram of the tunnel diode pair shown in Fig. 13 results. It takes two units of current flowing from the node to change the output from its positive to negative voltage.

The circuitry to provide the proper current switching at the node of the tunnel diode pair is shown in Fig. 14.

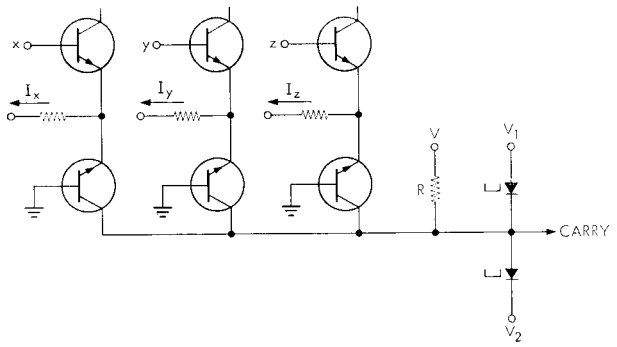


Figure 14 **Circuit for CARRY function.**

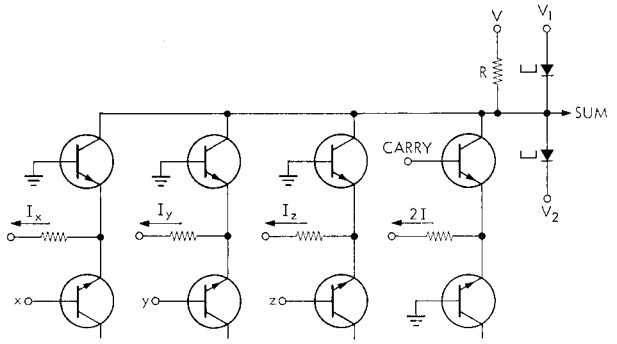


Figure 15 **Circuit for SUM function.**

The SUM function can be written as

$$\text{Sum} = \bar{C}(x + y + z) + xyz. \tag{24}$$

Since C is ONE when xyz is ONE, we can rewrite this equation as

$$\text{Sum} = \bar{C}(x + y + z) + Cxyz. \tag{25}$$

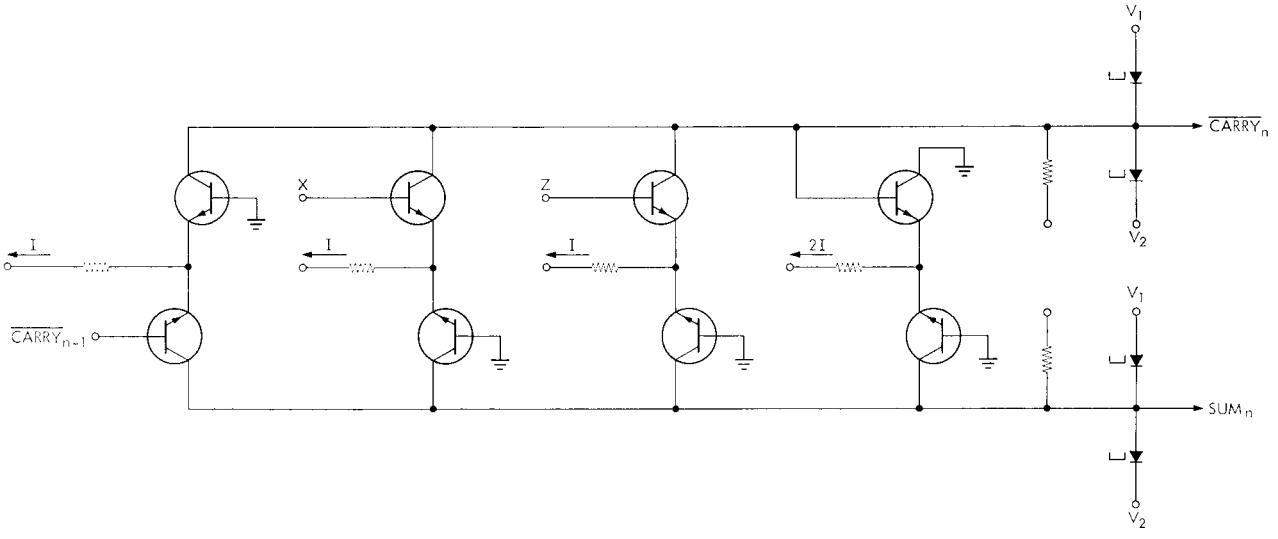
The form of the expression suggests the same procedure that was used to generate the CARRY function. Assume that one unit of current flows for each element (I_x, I_y, I_z) when the corresponding input equals a ONE and I_c flows when C equals a ZERO; furthermore, assume that I_c takes on the value of 2 units of current when it flows. With the aid of a truth table we can determine the total current (I_T).

Now note from Table 5 that when $I_T = 2$ units, the sum = 0 and when $I_T = 3$ units, the sum = 1. Therefore, another V vs I load-line diagram could be drawn which would require 3 units of current flowing from the node to change the output from its positive to negative states. Figure 15 represents the circuitry obtained for the SUM

Table 5 **Truth table for determination of I_T.**

x	y	z	*sum*	I_T *carry*	I_T *component*	I_T *units*
0	0	0	0	0	$I_c + 0$	2
0	0	1	1	0	$I_c + I_z$	3
0	1	0	1	0	$I_c + I_y$	3
0	1	1	0	1	$I_y + I_z$	2
1	0	0	1	0	$I_c + I_x$	3
1	0	1	0	1	$I_x + I_z$	2
1	1	0	0	1	$I_x + I_y$	2
1	1	1	1	1	$I_x + I_y + I_z$	3

Figure 16 **Methods of merging circuits obtained for SUM and CARRY (see text).**



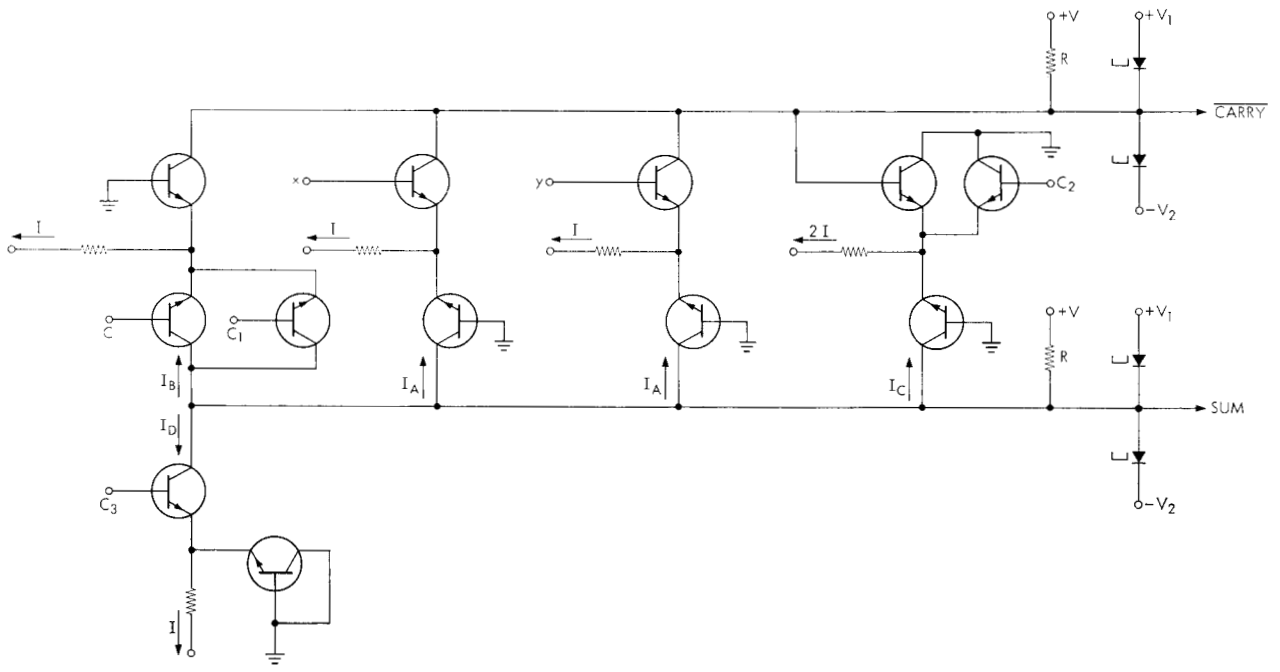


Figure 17 **Adder logic block schematic.**

and CARRY. This can be accomplished if we invert one of the functions. If we also invert one input we get the circuit of Fig. 16, which is now useful for a multistage adder.

Logic adaptation

When $z = 1$, the sum output has the property of an EXCLUSIVE OR circuit relative to the x and y inputs. Therefore, by paralleling the z (carry) input transistor, this logical function can be accomplished. (See Fig. 17). When the C_1 input is negative, the circuit operates as a binary full adder; when the input is positive, it acts as an EXCLUSIVE OR and is independent of the carry input.

A study of Table 5 and the components that make up the current I_T shows that if I_c is inhibited, three units of current flow only when I_x, I_y and I_z are all ONE$_s$. By adding the control C_1 (above) I_z can be made to appear as a ONE regardless of the actual input condition. Therefore, if I_c can be forced to remain zero, then the sum output would represent an AND circuit between the x and y inputs. The insertion of the parallel transistor with input control C_2 (Fig. 17) serves to inhibit I_c for all conditions.

Once the AND circuit is established, conversion to an OR circuit can be made by pre-biasing the tunnel diode pair with one unit of current. Then when x or y are a ONE, the sum output will be the OR of the two inputs. This pre-bias is established by the addition of the current switch and control C_3 (Fig. 17).

Conclusions

ACP tunnel-diode coupled circuits possess high logic flexibility and exhibit delays per logic decision under 1 nsec. These characteristics would permit system performance superior to that possible with any other circuit family published to date. Very reliable operation is the result of careful design techniques, which account for the nonlinearities of the semiconductor devices, and the use of conservative statistical techniques.

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