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Chemical and Ambient Effects on Surface Conduction in Passivated Silicon Semiconductors*

Abstract: **The effect of processing variables on the surface conduction properties of passivated silicon junction devices has been studied. Insulated gate field-effect transistors fabricated in *p*-type silicon were used as an experimental tool. Varying the metal used as the gate electrode is shown to strongly influence the surface conductivity of the field-effect device. The effects of heat treatments in various ambients and variations in the insulators used are also discussed. Surface conduction is shown to be a complex function of materials, thermal history and processing.**

The surface conductivity of semiconductor devices is of great importance in the fabrication of silicon transistors and diodes. The formation of *n*-type conducting layers on oxidized *p*-type silicon surfaces is a significant problem in current silicon device fabrication.[1] The *n*-type surface layer is commonly referred to as an inversion channel. In *npn* junction transistors, the existence of an *n*-type channel across the *p*-type base region is highly undesirable, resulting in high emitter-to-collector leakage and increased collector-base area and capacitance. Similar problems involving leakage currents and capacitance occur on *pnp* transistors and on diodes. These surface channels, while deleterious in conventional bipolar transistor fabrication, are the basis of insulated gate field-effect device operation. The operation of the insulated gate field-effect device is based on the ability to control the current flowing between source and drain regions (the channel current I_{sd}) by varying the voltage applied to the gate electrode. When the gate is biased positive, electrons are drawn to the *p*-type surface, inducing an *n*-type region at the silicon-silicon dioxide interface thus creating a surface channel.

In order to establish guide lines for processing of silicon devices, we have studied some of the factors that influence the formation of conducting surface channels. The effect of different metals, ambient thermal treatments and insulators have been investigated. Insulated gate field-effect devices have been used as an experimental tool in these investigations.

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Experimental technique and results

Field-effect devices were fabricated in 1 ohm-cm *p*-type silicon having the structure shown in Fig. 1. Source and drain regions were formed by diffusion, using conventional silicon dioxide masking with a P_2O_5 source held at 300°C. Deposition time was 15 min at 1000°C, followed by diffusion at 1060°C in dry oxygen (10 min), steam (40 min), and dry oxygen (10 min). Contact holes were then etched through the silicon dioxide layer grown during diffusion. Junction depths were approximately 2.5 microns with $C_0 \cong 3 \times 10^{21}$ atoms/cc. Thickness of the silicon dioxide layer was ~5000 Å over the diffused areas and ~8000 Å

Figure 1 **Field-effect device geometry.**

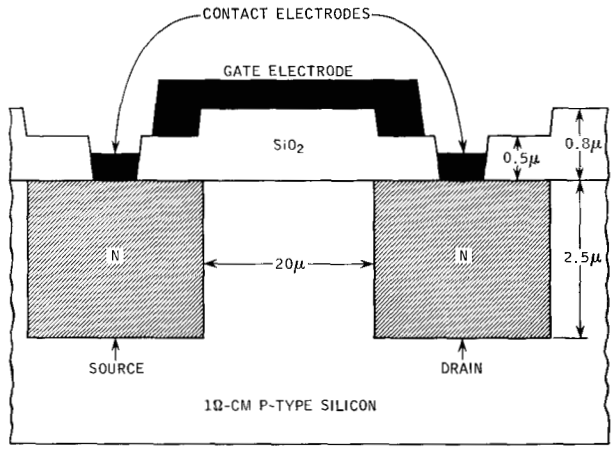


Table 1 **Effect of metallurgy on the channel conduction in oxidized field-effect devices. Values quoted are for the gate voltage corresponding to 10 μA source-drain current, at 25 V source to drain.**

Metal	Initial voltage	Degrees Centigrade 200°	300°	400°	450°	500°	550°	600°	700°	800°
Al	83	81	50	7	−5	−13	−140	−140	80	—
Mg.	92	86	86	7	−60	−10	7	25	—	—
Ti	82	78	66	43	−70	−61	4	35	80	80
Cr	90	88	85	21	−12	−25	−9	25	80	78
Si	90	77	60	25	−16	−30	0	20	80	82
Ag	88	88	86	47	29	−8	−7	25	87	90
No Metal	88	88	85	50	29	−4	−4	24	88	88
Au	88	88	87	53	31	0	−5	25	85	88
Cu	86	86	82	23	8	8	13	22	85	85
Zn	87	85	81	40	16	10	13	27	83	—
Pt	84	82	75	46	21	7	18	25	86	88
Pd	87	86	85	49	20	8	22	26	84	85
Ni	93	92	92	76	51	26	20	25	86	88
Mo	94	94	81	59	40	27	20	25	86	90

Measurements were made at room temperature after 15 min treatment at the temperature indicated. A negative voltage indicates that the current at $V_G = 0$ was in excess of 10 μA. Measurements on nonmetallized devices were made using an external mechanical probe shaped to conform to the gate electrode geometry. The data cited for the 700° Al condition was obtained on a separate experiment with no intermediate heating, because of the occurrence of gate-to-substrate shorts with repeated high-temperature treatment in this system. The same is true for the 600° Mg data. Each value cited represents an average for ~25 devices.

Table 2 **Effect of metallurgy on the channel conduction. Values quoted are for channel conductance in mA at 25 V source to drain and with gate floating.**

Metal	Initial current	Degrees Centigrade 200°	300°	400°	450°	500°	550°	600°	700°	800°
Al	0.00015	0.00015	0.00015	0.00027	0.011	0.66	10.2	9.5	0.00017	——
Mg	.00014	.00014	.00015	.00035	5.3	4.0	0.007	0.00068	——	——
Ti	.00015	.00015	.00015	.00020	5.7	4.1	.007	.00065	.00017	0.00017
Cr	.00011	.00011	.00011	.00015	0.009	0.60	.020	.00070	.00016	.00016
Si	.00013	.00013	.00013	.00017	.007	.62	.010	.00068	.00018	.00017
Ag	.00017	.00017	.00016	.00017	.00031	.015	.015	.00064	.00018	.00018
No Metal	.00014	.00014	.00014	.00015	.00035	.012	.014	.00069	.00017	.00017
Au	.00015	.00015	.00015	.00015	.00035	.014	.016	.00066	.00016	.00016
Cu	.00011	.00011	.00012	.00012	.00079	.00081	.00065	.00055	.00016	.00015
Zn	.00013	.00013	.00013	.00014	.00031	.00071	.00062	.00057	.00019	.00016
Pt	.00014	.00014	.00014	.00014	.00029	.00065	.00060	.00049	.00017	.00014
Pd	.00014	.00014	.00015	.00014	.00030	.00065	.00061	.00048	.00017	.00015
Ni	.00014	.00014	.00014	.00014	.00020	.00026	.00052	.00049	.00017	.00017
Mo	.00014	.00014	.00014	.00014	.00017	.00021	.00045	.00050	.00018	.00015

Measurements were made at room temperature after 15 min treatment at the temperature indicated. Data cited for the 700°C Al and the 600° Mg condition were obtained on separate samples with no intermediate heating. The cited values in the table represent an average for about 25 devices.

elsewhere as a result of the diffusion masking. Channel width of the devices was ~20 μ and the length of the channel was ~250 μ.

• *Metals*

The effect of using different metals as the gate electrodes of the field-effect device was studied. The same metal was used for source and drain electrodes. The metals were evaporated at room temperature through a metallic mask. The critical area for the metal application is the gate region which overlaps the two junctions, at which the metal covers the channel region between the source and drain areas. Metal film thicknesses ranged from 0.4 to 0.6 microns.

After metallization, measurements were made of the channel currents with the gate floating and, in addition, the gate voltage (V_G) needed to alter the channel current to 10 μA was measured. A channel current of 10 μA was selected as a current level that would be deleterious to circuit performance. For these measurements the source

and substrate were grounded and the gate voltage was applied relative to the substrate. The drain voltage was +25 V. After initial measurements the devices were given successive 15-min thermal treatments, with all contacts floating, at increasing temperatures (up to 800°C) in dry nitrogen. The channel current measurements were made again after each thermal treatment. All current measurements were made at room temperature.

The results obtained and cited in the tables are on wafers cut from one crystal. All wafers were processed together up to the point of metallization. Table 1 lists the metals studied and the gate voltages needed for a 10 μA channel conductance as affected by thermal treatment. Table 2 lists the channel conductance with gate floating for the different metals.

Examination of the data in Tables 1 and 2 shows that all of the devices studied have low channel conductance at temperatures below 400°C, which increases as a result of thermal treatment between 400° and 600°C, and returns to a low value after thermal treatment above 600°C. The magnitude of the peak in conductance varies substantially with the metals used, being extremely high for the active metals such as Al and Mg, intermediate for Ti and Cr as shown in Fig. 2, and low for noble metals such as Au and Cu. It is interesting to see that a small peak in conductivity occurs even without the presence of a metallic gate. The negative values of gate voltage in Table 2 indicate that the silicon surface becomes highly *n*-type when Al, Mg, Ti, Cr, and Si gate electrodes are heated in contact with the oxide. The positive values of gate voltage on first impression suggest the presence of a *p*-type surface. However, Cheroff et al[2] have shown that the surfaces are not necessarily *p*-type. In Fig. 2 the results for Ti and Cr gate electrodes are presented. These data show that the peak in conductivity occurs on cooling as well as on heating. Additional thermal cycling between 400° and 800°C gave results similar to those shown in Fig. 2. All systems investigated behaved this way.

In Table 3 we show the effect of holding the devices at

Table 3 **Average channel currents of each 100 devices after thermal treatments in nitrogen with gate floating.**

History[a]		Channel Current in mA
No Treatment		10^{-5}
500°C	15 minutes	10
300°C	15 minutes	8.5
300°C	4 hours	1.5
300°C	100 hours	0.7
300°C	500 hours	0.1
300°C	1000 hours	0.1

[a] These were aluminum metallized devices.

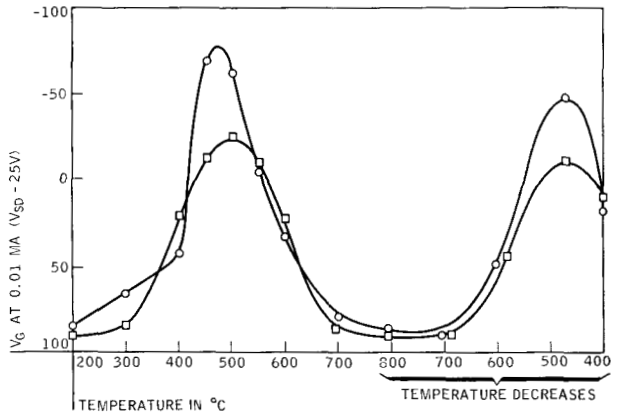
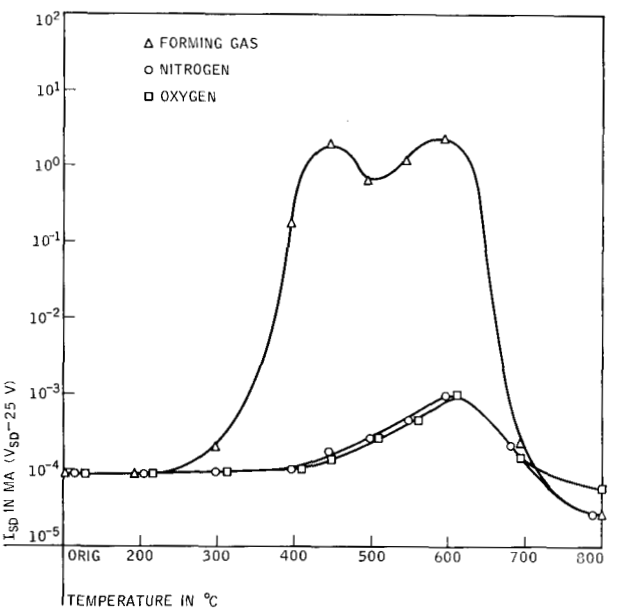


Figure 2 **Gate voltage for 0.01 mA channel conductance as a function of thermal treatment.** *The data were taken with increasing temperature to 800°C followed by decreasing temperature to 400°C. Fifteen min thermal treatments in nitrogen were carried out at each temperature denoted by an experimental point.* ○ *and* □ *indicate titanium and chromium, respectively. Each point represents an average for about 25 devices. Source-to-drain voltage was 25 V.*

Figure 3 **The effect on conductance of ambient thermal treatment for nonmetallized devices.** *Fifteen-minute thermal treatments were carried out at each temperature denoted by an experimental point. Each point represents an average for about 25 devices. Source-to-drain voltage was 25 V.*



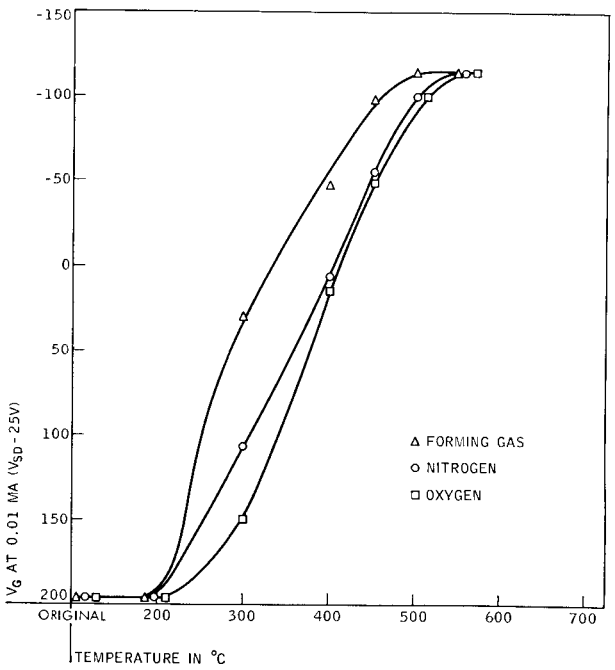


Figure 4 **Gate voltage for 0.01 mA channel conductance as a function of ambient thermal treatment for aluminum metallized devices.** *(Thermal treatment and number of devices were the same as in Fig.3) Source-to-drain voltage was 25 V.*

300°C after attaining a peak conductivity at 500°C. It is evident from the long time required for the conductivity to decrease that the data in the tables and curves may not be the equilibrium values. The heating effect is also slow as shown by Cheroff et al.[2]

A large number of wafers from several crystals were studied and the results confirmed the effects described above in Tables 1, 2, and Fig. 2.

- *Effects of various ambients*

Field-effect devices with and without aluminum gates were heated in oxidizing, reducing, and inert ambients. Oxygen, forming gas (10% H_2 and 90% N_2) and nitrogen were used as the respective ambients. The effect of the forming gas was particularly large, resulting in a peak channel current greater than one mA, as shown in Fig. 3, for the nonmetallized devices. The effects for nitrogen and oxygen were much smaller. Even with the aluminum present (see Fig. 4) the effect of the forming gas is evident. There appears to be, in this case, a difference between the effects for oxygen and nitrogen.

- *Effects of various insulators*

Experiments were conducted to determine whether the presence of the silicon dioxide layer was necessary in order for excess leakage current to occur. After diffusion of source and drain regions, the silicon dioxide layer was removed from one half of the field-effect devices on a wafer. After measurement of channel current, the wafer was then subjected to thermal treatment in forming gas at 400°C. All of the oxidized devices developed conducting channels within two hours of thermal treatment. No excess leakage current was observed on any of the non-oxidized devices even after 100 hours of thermal treatment. The number of units for this experiment was about 200 devices divided equally between the oxidized and non-oxidized structures. Complete removal of the silicon dioxide layer on the devices with the conducting channels resulted in the elimination of the channel. Partial removal of the oxide layer had no effect on the observed channel conductance. As in all other cases, these measurements were made in air at room temperature.

An experiment was run to determine whether there was a minimum thickness of silicon dioxide necessary for excess leakage to occur. After device diffusion, the silicon dioxide layer was removed and very thin oxides 25, 50, 100, 250, 500, and 1000 Å were regrown using anodic oxidation.[3] (Estimates of oxide thickness are based on anodic forming voltage, not physical measurement). After measurement of channel conductance of 50 devices from each sample, the devices were subjected to thermal treatment in forming gas at 400°C. They were cooled to ~100°C in the forming gas ambient and measurements were made at room temperature in air. After 30 min heating in forming gas, all of the devices with oxide thicknesses greater than 25 Å showed conducting channels. No excess leakage was observed on any of the devices which had only 25 Å of oxide even after 100 hours of thermal treatment.

The effects observed with thermally grown and pyrolytically deposited oxide[4] (from the pyrolysis of tetraethoxysilane Si $(OC_2H_5)_4$) were similar to those reported above for the anodically grown oxide.

The substitution of sedimented glass films for the oxide layer was also studied. After device diffusion, the oxide layer was removed and sedimented glass films applied to the field-effect devices.[5,6] After measurement of the channel current, the devices were subjected to thermal treatment in forming gas at 500°C. No channeling was observed on any of the approximately 500 devices studied. The glassed devices were also insensitive to metals such as Al that cause excess leakage on oxidized devices. Many glasses were studied and all behaved similarly. This is in agreement with observations reported by Kerr.[7]

Discussion and conclusions

The formation of surface conducting layers on *p*-type silicon coated with silicon dioxide has been shown to be a complex phenomenon dependent on materials and thermal treatments used in device fabrication. The use of

"reducing" metals (i.e., Al, Mg, Ti) and ambients increases the magnitude of these leakage effects by several orders of magnitude.

There is a rough correlation of the magnitude of the peak channel conduction with the electrochemical reduction potential of the metals (aqueous solution values) used for the gate electrodes. There is also a correlation with the free energy of formation of the oxides and this suggests the important reaction may be of the following type:

$$M + SiO_2 \rightarrow MO_x + SiO_{2-x}.$$

A similar reaction with Si may occur at the silicon-silicon dioxide interface,

$$xSi + SiO_2 \rightarrow Si_{(1+x)}O_2.$$

Both of these reactions lead to an oxygen-deficient SiO_2. A reducing gas such as forming gas apparently behaves like the reducing metals.

Models[8,9] for the mechanism of channel formation in the metal-oxide-silicon system have been proposed. There is at present no satisfactory explanation for the existence of the conduction maximum observed between 400° and 600°C in all oxidized devices studied.

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