G. Cheroff
F. Fang
F. Hochberg

Effect of Low Temperature Annealing on the Surface Conductivity of Si in the Si-SiO_2-Al System

Abstract: Studies on insulated-gate field effect devices fabricated on both n- and p-type Si have shown the existence of inversion layers on p-type surfaces and of accumulation layers on n-type surfaces. The degree of inversion or accumulation was characterized by measuring the total series capacity of the SiO_2 gate and the underlying Si as a function of an applied dc potential. The initial surface conductivity, as measured by the source to drain conductance g_{sd} at zero gate bias, indicates that most of the surface charge is immobile. Prolonged heat treatments at 350°C on p-type substrates have resulted in a two order-of-magnitude increase in g_{sd} accompanied by little or no change in the total surface charge density N_t. On n-type substrates, however, the same treatment results in a factor of 5 decrease in N_t. The effects of these treatments on the surface uniformity as well as on appropriate device parameters are reported.

Introduction

Initial attempts at this laboratory to fabricate insulated gate field effect transistors (FET's)[1] by silicon planar techniques resulted in devices with wide spreads in their electrical properties. Devices with extremely low source to drain conductance, ($g_{sd} \sim 10^{-5}$ mhos) were often found. However, it had already been established by the authors and others[2] that the total charge was in most cases greater than 10^{11} electronic charges/cm^2 on silicon surfaces prepared by the same process as was used for the devices. This high surface charge density is inconsistent with a low surface conductance. In addition, the small signal transconductance g_m was found to be very low, too low in fact to be explained by the reduction of the bulk mobility by surface scattering mechanisms.[3-7]

However, annealing at 350°C markedly changes and stabilizes the surface conductance. For example, upon this treatment, the channel conductance of the p-type substrate at zero-gate voltage may increase two orders of magnitude and stabilize at that value. It has also been established by the authors and others[8] that this effect depends on the presence of Al over the SiO_2. Consequently, the motivation of the present work has been to understand the nature and causes of the surface conductivity changes brought about by heat treatments. To characterize the effects properly, the surface charge as well as the conductance was monitored following heat treatments of different durations.

Method of characterization

The major properties of an insulated-gate field effect transistor[1,9,10] are determined by the nature of the Si-SiO_2 interface. For example, on a p-type silicon wafer the mode of operation is determined by the presence or absence of an inversion layer (negative charge) at the silicon surface when no external field is applied. When an inversion layer is present on p-type silicon, the device operates in a depletion mode and negative gate voltages are required to turn the device off.

In a depletion mode device of this type the magnitude of the built-in field in the oxide is related to the total surface charge by

$$N_t q = E_{ox} \epsilon_o K_{ox}, \quad (1)$$

in the MKS system, where N_t is the total surface charge density at zero gate voltage, E_{oz} is the built-in field in the oxide, ϵ_0 is the permittivity of the free space, and K_{oz} is the dielectric constant of SiO_2.

The amount of mobile charge N_m is defined by

$$N_t = N_m + N_i \tag{2}$$

where N_i represents the immobile charge.

For a small applied source drain voltage V_{sd}, such that the device is operating below pinch-off, the small and large signal channel conductances, g_{sd} and G_{sd}, are then given[11] by

$$g_{sd} = G_{sd} = (W/L)qN_m\mu_s \tag{3}$$

where W/L is the width-to-length ratio of the channel, q is the charge on the electron, and μ_s is the carrier mobility at the Si surface.

A convenient method for obtaining N_t, and hence E_s and E_{oz}, is to measure the total capacitance C from gate to substrate as a function of an applied dc potential. This technique is commonly designated as an MOS (metal-oxide-semiconductor) measurement. It has been shown[12–14] that C decreases to a minimum value when the surface undergoes a transition from accumulation to depletion conditions. For large surface charge densities, i.e., in the range 10^{11}–10^{12} electronic charges/cm^2, N_t is given to first order by

$$N_t q = E'\epsilon_0 K_{oz} \tag{4}$$

where E' is the field which must be applied from gate to substrate to reach minimum capacitance.

In addition to these measurements of capacitance and conductance, we may measure the small signal transconconductance g_m, which is defined by

$$g_m \equiv \left.\frac{\partial I_d}{\partial V_g}\right|_{V_{sd}} = V_{sd}\frac{\partial G_{sd}}{\partial V_g} = \frac{W}{L}q\frac{\partial(N_m\mu_s)}{\partial V_g}, \tag{5}$$

where V_{sd} is the dc voltage applied between the source and drain electrodes.

Experimental technique

- *Method of device fabrication*

Figure 1a is a plan view and Fig. 1b is a cross section showing the geometry of the circular device used in this work. Some pertinent dimensions are: $W/L \sim 50$ and $L = 12 \times 10^{-4}$ cm; the oxide thickness is ~5700 Å.

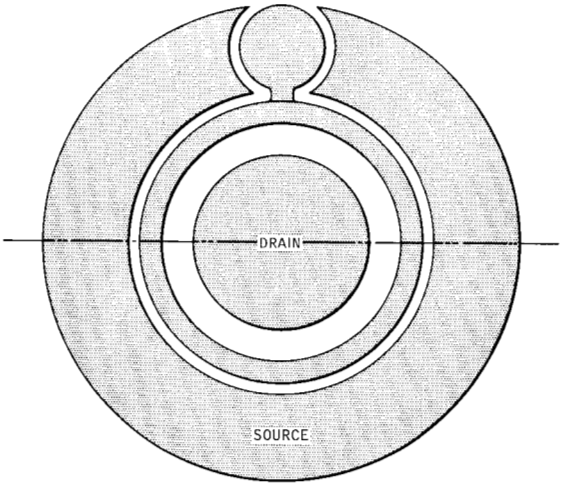
Standard methods from planar silicon technology were used in the fabrication of the structures. Dry oxygen rather than steam was used in the thermal growth process for the SiO_2 which served as both a diffusion mask and gate material. The Al electrodes (gate, source, and drain) were evaporated on the wafer with no intentional heating of the substrate and it is estimated that the devices did not exceed a temperature of 200°C during the electrode deposition. After the Al electrode pattern was established by photolithography and subtractive etch methods, the wafers were subjected to successive heat treatments in air at 350°C.

A p-type control wafer was heated in air at 350°C for 3 hours *before* the Al deposition. Since the resulting devices could not be distinguished from those measured initially (before the heat treatment sequence), involvement of the Al electrode in the conductivity changes is clearly indicated.

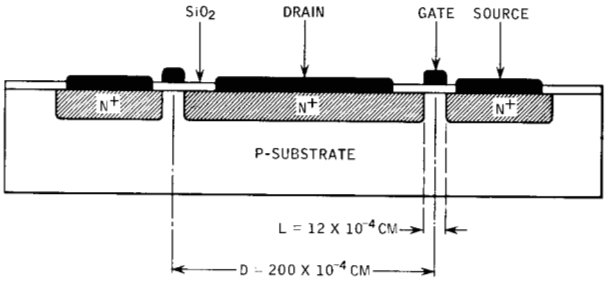
- *Measurement techniques*

All measurements were taken at room temperature after various time increments during the 350°C heat treatment. A Kulicke and Soffa semiautomatic probe coupled to an

Figure 1 **An insulated gate field effect transistor (a) a plan view and (b) a cross section.**



(a)



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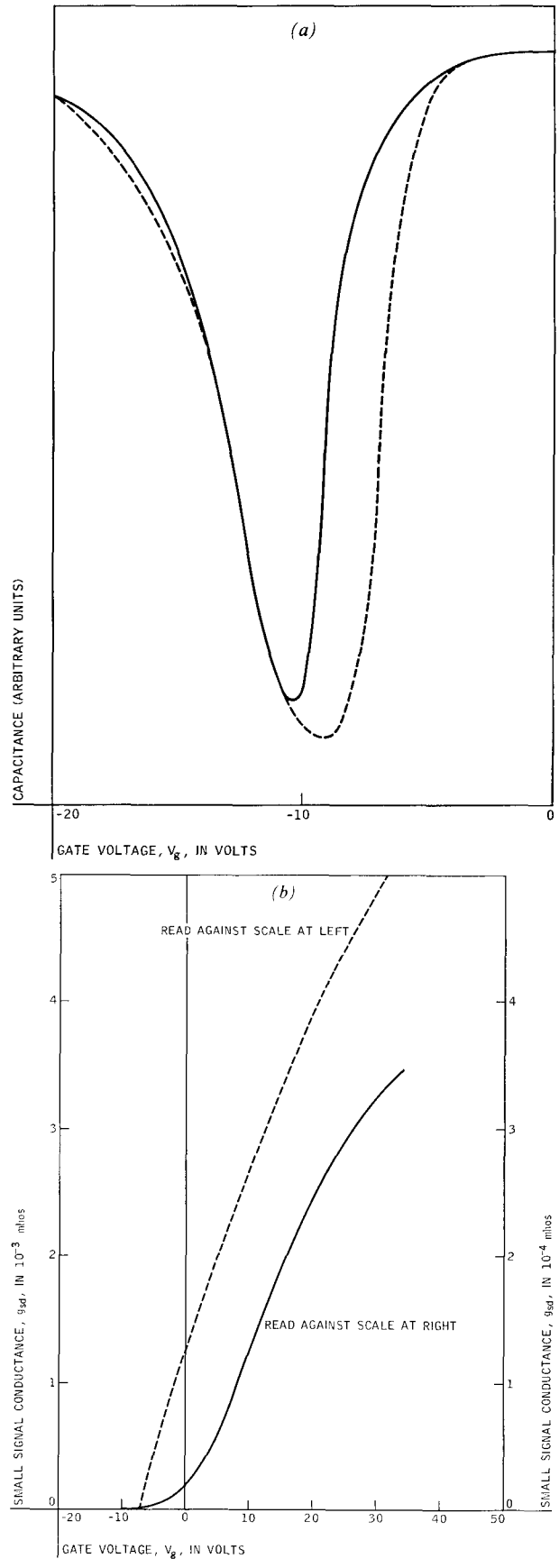


Figure 2 **Typical effects of heat treatment on the relationships between (a) gate-to-substrate capacitance and gate voltage, $C(V_g)$, and (b) small-signal conductance and gate voltage, $g_{sd}(V_g)$, for a field-effect transistor on a 10 ohm-cm p-type substrate.** *The broken lines apply to the heat treated samples; the solid lines to the sample before heat treating.*

automatic data-taking system measured the dc current between the source and drain electrode, I_{sd}, for various values of V_g and V_{sd}. The data was processed by computer to obtain statistical information of both measured and computed parameters. The large signal transconductance G_m was computed by dividing I_{sd} by V_g. (The example of G_m reported in the next section will be for the case where V_g varies from 0 to +10 volts.) The data that was processed encompassed a sampling of approximately 200 devices from each wafer (out of 800 devices per wafer); a total of 12 wafers were measured. A typical result from 1 wafer is used in this paper.

The measurements of capacitance, of small signal conductance g_{sd}, and of g_m that are reported here are based on a smaller sampling than that of the above dc data. (The capacitance measurement has already been described in the section, "Method of characterization"). The g_{sd} is measured by inserting a small ac source v'_{sd} (10,000 cps) in the source-drain circuit, where the ac current i_{sd} is measured by means of a small series resistor. The g_{sd} is then obtained from

$$g_{sd} = \frac{i'_{sd}}{v'_{sd}}. \tag{6}$$

The g_m is measured by inserting the ac source v'_g in series with the gate and electrode source and is obtained from

$$g_m = \frac{i'_{sd}}{v'_g}. \tag{7}$$

The above two parameters are measured as a function of a dc voltage inserted in the gate-source loop. For the cases of g_m reported in this paper, V_{sd} is held at a fixed value of 0.5 volts.

Results

- *p-type substrates*

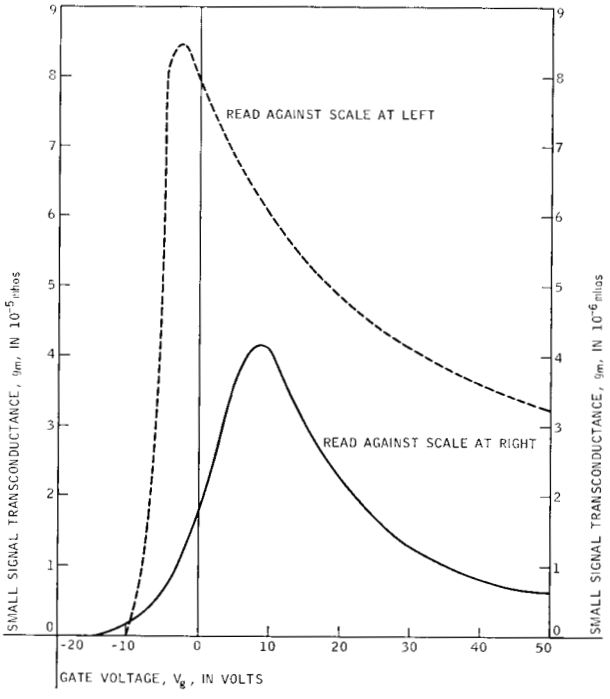
Figures 2a and 2b show, respectively, typical plots of gate to substrate capacitance and g_{sd} versus V_g of a transistor (10 ohm-cm substrate) before and after heat treatment of 3 hours at 350°C. The minimum capacitance for an untreated transistor occurs at about —11 volts. The built-in surface charge density N_t is approximately 4.6×10^{11}

electronic charges/cm^2. From Eq. (3) we calculate the expected g_{sd} at $V_g = 0$ to be 1.6×10^{-3} mhos, assuming all the surface charge to be mobile, and using the typical effective surface mobility value of ~500 cm^2/volt sec.[7,15] The g_{sd} is about one order of magnitude lower than the calculated value. After heat treatment the minimum capitance remained at approximately the same position, indicating that no change in the total built-in surface charge had taken place. However, g_{sd} is now 1.2×10^{-3} mhos, close to the previously calculated value. Figure 3 is a plot of g_m vs V_g before and after heat treatments, respectively; it is seen that heat treatment has resulted in a large increase in g_m at all operating gate voltages.

The dc measurements of I_{sd} and G_m (calculated) illustrate other features of the thermal treatments. Figure 4 shows values for I_{sd} (averaged over 200 devices for $V_{sd} =$ 10 volts and for $V_g = 0$) plotted as a function of heat treatment time. Figure 5 is a plot of the average $G_m(\overline{G_m})$ vs treatment time. Error flags are used to indicate the standard deviations at each point.

The data presented in Figures 4 and 5 are typical of the 12 *p*-type wafers that were investigated, and demonstrate that the effect of increased I_{sd} and G_m saturates in about 120 minutes. The standard deviations indicate that good uniformity has been obtained over the surface properties of Si wafers. The saturation effects would promise device stability (under nonoperating conditions) in this temperature range.

Figure 3 **A plot of g_m vs V_g before and after heat treatment of a typical FET on a 10 ohm-cm p-type substrate.** *The broken line applies to the heat treated sample; the solid line to the untreated sample.*



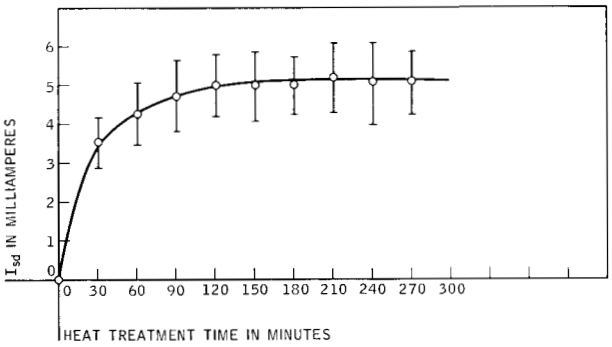


Figure 4 **A plot of I_{sd} vs annealing time for FET's on a 10 ohm-cm p-type substrate.**

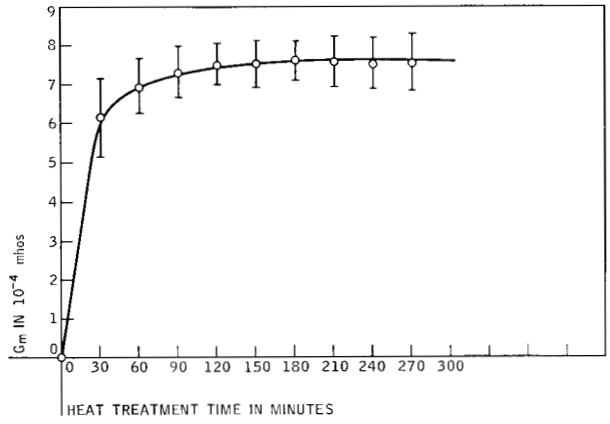


Figure 5 **A plot of G_m vs annealing time for FET's on a 10 ohm-cm p-type substrate.**

- *n-type substrates*

It has also been established by MOS measurements[2] that *n*-type surfaces have a built-in accumulated charge of approximately 10^{11}–10^{13} electronic charges/cm^2. In Fig. 6, C and g_{sd} of a *p-n-p* device are plotted as a function of V_g before and after thermal treatments of three hours at 350°C. The minimum capacitance, as well as the onset of channel conductance, occurs at approximately −35 volts, indicating a built-in accumulated charge of 1.4×10^{12} electronic charges/cm^2 before heat treatment. For devices examined after the heat treatment, the minimum capacitance is shifted to approximately —7 volts, indicating a reduction of the built-in charge to 2.8×10^{11} electronic charges/cm^2.

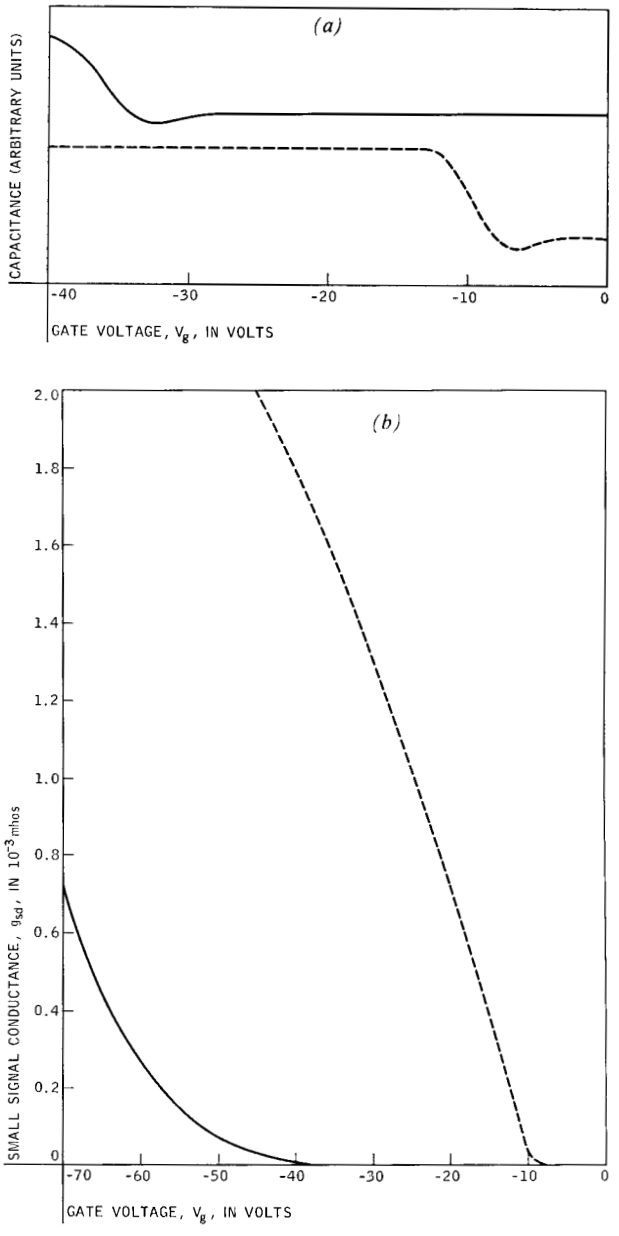


Figure 6 **Typical effects of heat treatment on the relationships between (a) gate-to-substrate capacitance and gate voltage, $C(V_g)$, and (b) small-signal conductance and gate voltage, $g_{sd}(V_g)$, for a field-effect transistor on a 10 ohm-cm n-type substrate.** *The broken lines apply to the heat treated samples; the solid lines to the sample before heat treating.*

Figure 7 shows the relationship between g_m and V_g for the two cases above. The behavior of g_m is quite different from that for the *p*-substrate previously described in that the value of g_m after heat treatment extrapolates to the initial g_m value at high V_g.

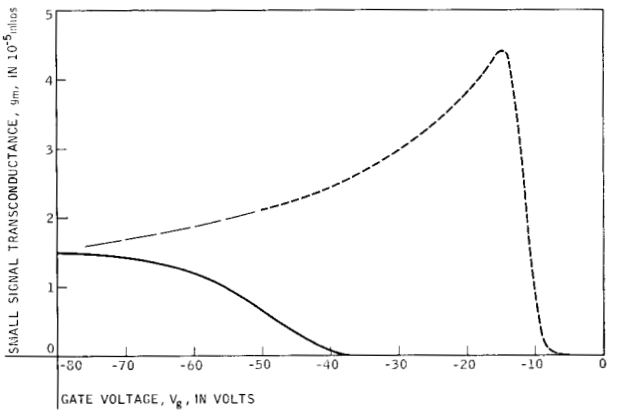


Figure 7 **A plot of g_m vs V_g before and after heat treatment of a typical FET on a 10 ohm-cm n-type substrate.** *The broken line applies to the heat treated sample; the solid line to the untreated sample.*

Discussion of results

For the case of *p*-type materials, we have considered the following mechanisms as possible explanations for the increase in G_{sd} with constant N_t: (1) changes in resistance of source or drain contacts; (2) junction effects; (3) change in the surface mobility; and (4) release of immobile charge.

There is evidence which leads one to believe that (1) is not likely. For example, I. Ames and H. Seki[16] of this laboratory have independently evaluated contacts which had been fabricated by the same process used for the transistors. The largest contact resistance they observed for comparable contact areas was approximately 10 ohms. It is to be noted that this resistance is more than two orders of magnitude below the values for $1/g_{sd}$ that pertain to the devices reported on in this paper. In addition, Ames and Seki have fabricated FET *n-p-n* devices with the geometry arranged such that the Al contact to the n^+ region was far removed (30×10^{-3} inches) from the FET channel. The same increase in G_{sd} with subsequent heating at 350°C was observed. Further, they observed no change in G_{sd} when their devices were heated without Al over the channel. Thus there has been independent confirmation of the results discussed earlier in the section on methods of device fabrication.

With respect to (2) above, it should be remarked that in an *n-p-n* structure an anomalously accumulated *p*-type surface between the diffused region and the channel is not at all anticipated.

A change in μ_s may be a factor to consider more seriously, since the curves in Fig. 4 demonstrate a marked change in g_m. Trapping effects, however, could account for the initial low value of g_m. In this case, one expects the g_m to be frequency dependent.[17] Although we have not

as yet found such a dependence, its existence must not be ruled out. Hall measurements[15] on similar structures have ruled out trapping effects only on heat treated samples. Measurements are in progress on the low conductance type samples to permit this question to be resolved. At this point we do not feel it is reasonable that an order-of-magnitude change in μ_s is sufficient to explain the observed increases in g_{sd} or in g_m.

In view of the above, it is the release of immobile charge that is proposed as the most reasonable mechanism by which to explain the observed effects on *p*-type Si. If the states where immobile charges reside are not completely filled, the trapping effects observed for the initial g_m are to be expected. Relaxation effects in g_m, however, have not been observed by the authors at frequencies up to 10^7 cps. States with time constants less than 10^{-7} sec. are more likely to be found in the Si rather than the SiO_2 bandgap.

For the case of the *n*-type substrates, the change in the total surface charge can be explained either by a change in the surface state density on the Si, or by a change in the total space charge in the insulator. The latter is thought to be due to the transport of ions across the Si-SiO_2 and/or Al-SiO_2 interfaces.[18] The fact that effects more pronounced than those reported in this paper are observed under gate bias conditions[18,19] seems to support the argument of ionic motion.

Summary

A particular process, annealing at 350°C, has been described which, when used in the fabrication of insulated gate field effect devices, results in a highly reproducible device that is capable of improved performance. For the case of *p*-type substrates, plausible arguments are used to establish the initial presence of immobile charges residing in trapping states within the Si bandgap. However, no direct evidence for the existence of such states has been given. It is important that later work account for the role of the Al electrode in these particular effects. Thomas and Young[19] have postulated the presence of a space charge in the insulator due to oxide-ion vacancies brought about by electrode reactions with the SiO_2 and the system proposed by Seraphim et al[18] involves a number of such reactions. However, both models require an observed change in total charge as the systems are moved from one state to another; thus neither can be used in explaining the changes in surface conductivity described in this paper for *p*-type Si.

Finally, it is shown that the use of transport measurements (i.e., G_{sd} on field effect structures, or leakage measurements on diodes or bipolar transistors), or MOS capacitance measurements alone is not always adequate to establish the relationship between the degree of surface inversion and various process parameters. By carefully correlating these measurements together with their time or frequency dependence, the Si-SiO_2 interfaces may be better understood.

Acknowledgements

The authors wish to thank D. P. Seraphim for his constant encouragement and valuable criticisms, and G. E. Brock for his critical reading of the manuscript.

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Received June 17, 1964.