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Electrochemical Phenomena in Thin Films of Silicon Dioxide on Silicon

Abstract: A study has been made of the effect of chemical additives and of annealing and electrical biasing procedures upon the state of charge of silica films grown on silicon. A model, proposed to account for the observations, is based on the assumption that phosphorus, aluminum, and boron, when present, substitute for Si in SiO_2. The resulting species may be represented as PO_2^+, PO_2^-, AlO_2^-, or BO_2^-. The mobile charge carrier in the silica under the conditions investigated here is assumed to be an oxide-ion vacancy. Under certain conditions electrolysis is accompanied by deviations from Faraday's laws and changes the net charge in the oxide; under other conditions only the charge distribution in the oxide is changed. The experiments leading to the development of the model, which were done with metal-oxide-silicon structures, have been supplemented with experiments with field effect transistors. Field effect transistors of the *n-p-n* type have been made to operate in the enhancement mode.

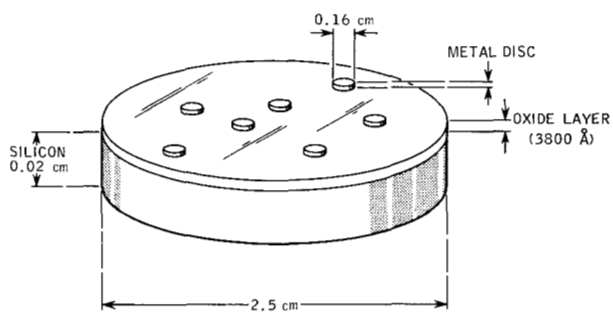
1. Introduction

Thin films of silica glass, deposited or grown on silicon circuit elements, are useful for achieving a degree of isolation of the silicon from external electrical and chemical influences. However, a prevalent difficulty is that the surface potential of the silicon is determined by the presence of nearby charges and it is difficult to prepare silica films that are free of such charges. The work reported here uses the electrical properties of the silicon as a sensitive index of the changes in state of charge of the silica produced by chemical, thermal, and electrochemical treatments. A systematic experimental study of these effects has been made and correlated with an electrochemical model that has been developed to provide a molecular interpretation.

The remainder of this introductory section gives a more detailed description of the MOS (metal-oxide-silicon) systems studied and follows with a simple account of the relation between the state of charge of the silica and electrical measurements actually made on the MOS. The electrochemical model is described in Section 2, the experimental techniques and the principal results are discussed in Section 3, and the results are interpreted in terms of the model in Section 4. Results from these MOS studies have been tested by extending their implications to the treatment of field-effect transistors. This aspect of the work is described in Section 5.

All observations were on the system metal-SiO_2-Si, chiefly with the structure shown in Fig. 1. (Techniques by which such structures are made are discussed in Section 3.) The subsystem comprising one metal disc and the oxide and silicon directly below it is called an MOS structure. The total capacitance-voltage [$C(V)$] characteristic of an

Figure 1 **A wafer of silicon supporting several MOS systems.**



MOS structure fabricated with p-type silicon commonly has one of the two forms shown in Fig. 2. The theoretical basis of these characteristics is well-known,[1] to the extent that the shape of the curve has been calculated by L. M. Terman[2] and, in greater detail, by P. M. Marcus[3] for dc response, and by S. H. Liu[4] for ac response. The difference in shape of the two curves in Fig. 2 has been related to recombination processes at the surface[4] which, although sensitive to surface conditions, are not easily related to the state of charge of the silica. The feature of each $C(V)$ characteristic we shall use is the voltage at which the capacitance changes. This voltage, V_m, is indicated by arrows in Fig. 2.

In general, we may write total voltage V on the MOS as

$$V = V_s + V_d, \tag{1.1}$$

where V_s is the potential rise in going from the interior of the semiconductor to a region in the oxide immediately adjacent to the semiconductor surface, and V_d is the potential rise in going from that surface to the interior of the metal electrode. According to this division of V we may write

$$1/C = 1/C_s + 1/C_d, \tag{1.2}$$

where C is the total MOS capacitance, C_s corresponds to V_s, and C_d corresponds to V_d.

The main effect of this division is that V_s and C_s are, respectively, the potential and the capacitance of the space charge, including surface states, in the semiconductor near the O|S (oxide-silicon) interface. At a temperature of approximately 25°C, at which $C(V)$ is determined in the present work, the term C_d is independent of V. On the other hand, C_s depends on V only through V_s.[3]

Marcus[3] calculated $C_s(V_s)$ (i.e., the dependence of C_s on V_s) as well as contributions to V_d from various surface potential terms. Here we consider an additional contribution to V_d, namely, that from the state of charge of the oxide.[5] First we point out that V_d is an experimentally accessible quantity: at V_m the value of C_s is $C(V_{s,\,\mathrm{min}})$. We have chosen to report V_m rather than the actual point at which $V_s = 0$. (Under our experimental conditions the difference between V_m and the point at which $V_s = 0$ is approximately one volt.[3]) Then from Eq. (1.1) we find

$$V_m = V_d. \tag{1.3}$$

Now suppose that we have a fixed positive charge density, σ_+, (charges/unit area) in the oxide. Then at $V = V_m$ this charge must be neutralized by an equivalent charge in the metal at the M|O interface, otherwise it would contribute to $V_{s,\,\mathrm{min}}$. Then σ_+ makes a contribution to V_d

$$V_+ = -\sigma_+ l_+/\epsilon, \tag{1.4}$$

where l_+ is the average distance of the σ_+ charge from the M|O metal-oxide interface, and ϵ is the permittivity of the oxide. (See Thomas and Young[6] for a more complete calculation of this effect.)

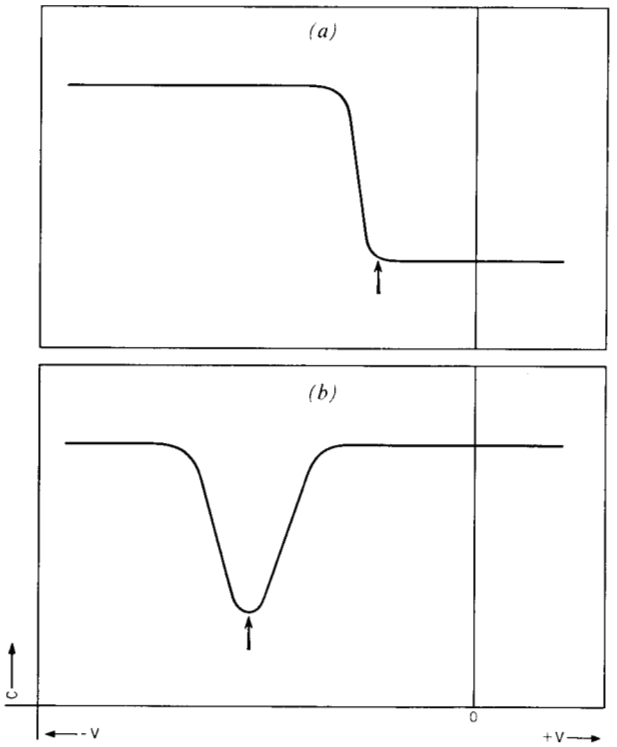


Figure 2 **Two forms of capacitance-voltage characteristics of an MOS structure fabricated with p-type silicon.** *The small-signal capacitance is measured at 10 kc/sec. Vertical arrows indicate voltages at which capacitance changes.*

It is proposed that the σ_+ charge arises in deviations from Faraday's laws in electrochemical processes in the MOS system at elevated temperatures during preparation. The magnitude of the deviations is very small, being about 10^{11} to 10^{13} electronic charges/cm^2, or 1.6 to 96 $\times$ 10^{-8} Coul/cm^2. (A basis for the systematic discussion of these effects is offered in the following Section.) Another contribution to V_d may arise from polarization of the oxide. Such polarization may be thought of as a sheet of positive charge of magnitude σ_+ separated by distance $l_\pm$ from an equal and opposite sheet of negative charge. These sheets are assumed to be parallel to the M|O interface and to exist as sheets only in the sense that there is an average separation of positive and negative charge in a polarized system. The contribution of this polarization to V_d is the sum of two terms of the type shown in Eq. (1.4), one being negative and one being positive. The over-all effect is positive if the positive sheet is closer to the M|O interface than the negative sheet.

2. Electrochemical phenomena in silica

The experimental results described in the following Sections will be discussed in terms of a model having the following key features:

1. The changes that various annealing and electrical biasing procedures produce in V_m reflect changes in the content and the distribution of charged species in the silica.
2. The silica phase is continuous right up to the silicon surface on one side and to the metal surface on the other, and various components introduced into the silica by electrode processes or other treatments enter either substitutionally or interstitially.

These features simplify our interpretation of the various annealing experiments. Other features essential to our model arise from the requirements of conservation of charge and of atomic species in chemical processes, even at electrodes.

We use the following reactions[7] to show how, while respecting the requirements of conservation of charge and of atomic species, we can generate oxide-ion vacancies, V^{++}, in electrode processes:

$$\mathrm{Al(Al)} \rightarrow \mathrm{AlO_2^-} + 2\mathrm{V^{++}} + 3e^-\mathrm{(Al)} \qquad \text{Reaction (1)}$$

$$\mathrm{B(Al)} \rightarrow \mathrm{BO_2^-} + 2\mathrm{V^{++}} + 3e^-\mathrm{(Al)} \qquad \text{Reaction (2)}$$

$$\mathrm{Si(Si)} \rightarrow \mathrm{SiO_2} + 2\mathrm{V^{++}} + 4e^-\mathrm{(Si)} \qquad \text{Reaction (3S)}$$

$$\mathrm{Si(Al)} \rightarrow \mathrm{SiO_2} + 2\mathrm{V^{++}} + 4e^-\mathrm{(Al)} \qquad \text{Reaction (3M)}$$

$$\mathrm{P(Al)} \rightarrow \mathrm{PO_2^+} + 2\mathrm{V^{++}} + 5e^-\mathrm{(Al)} \qquad \text{Reaction (4)}$$

$$\mathrm{PO_2^-} \rightarrow \mathrm{PO_2^+} + 2e^-\mathrm{(Al)} \qquad \text{Reaction (5)}$$

$$\left[\begin{matrix}\text{Normal}\\ \text{structure}\end{matrix}\right] \rightarrow \mathrm{O_2}(g) + 2\mathrm{V^{++}} + 4e^-\mathrm{(M)}. \qquad \text{Reaction (6)}$$

In addition, we use the following equations to represent the processes occurring in the high-temperature doping treatment of the oxides:

$$2\mathrm{V^{++}} + \mathrm{P_4O_{10}}(g) \rightarrow 4\mathrm{PO_2^+} \qquad \text{Reaction (7)}$$

$$\mathrm{B_2O_3}(g) \rightarrow 2\mathrm{BO_2^-} + \mathrm{V^{++}}. \qquad \text{Reaction (8)}$$

In the equations above, $\mathrm{V^{++}}$ represents an oxide-ion vacancy, i.e., a small region in the silica phase that is representative of the normal silica structure except that an oxide ion $\mathrm{O^=}$ is missing, Fig. 3. This is not to imply that $\mathrm{O^=}$ is necessarily present as such in the normal structure but only that

$$\mathrm{V^{++}} + \mathrm{O^=} \rightarrow \text{normal silica structure.} \qquad \text{Reaction (9)}$$

Parenthetically, in this equation and others to follow, chemical species written without further specification are species in the silica phase; in other cases the phase is indicated in parentheses after the formula. For example, Si(Si) means Si in the crystalline silicon phase and B(Al) means B in the aluminum phase.

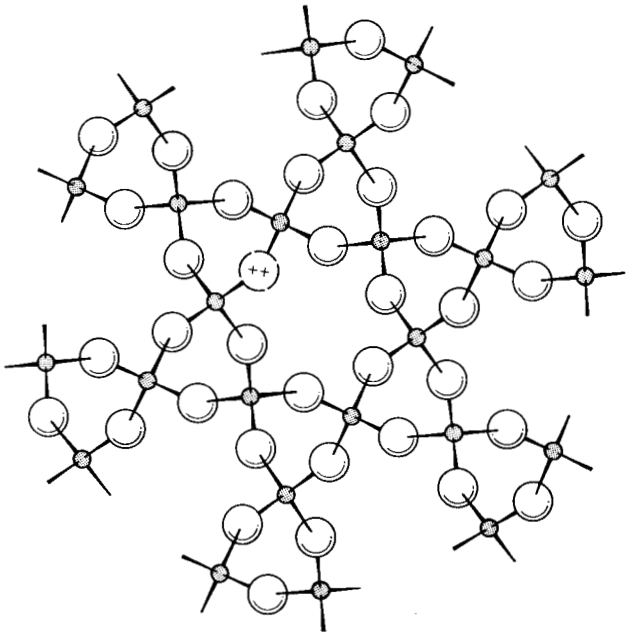


Figure 3 **A possible structure for V++, an oxide-ion vacancy, is shown in the network of silicon atoms (small solid circles) and oxygen atoms (larger open circles).***

Taking the first electrode reaction, Reaction (1), as an example for detailed explanation, we note that we have written the aluminum-containing product as $\mathrm{AlO_2^-}$ to indicate that it substitutes for an $\mathrm{SiO_2}$ unit in the normal silica structure. This implies a structure for the $\mathrm{AlO_2^-}$ species corresponding to what is obtained if, in a normal silica structure, one replaces a silicon atom in oxidation state +4 by an aluminum atom in oxidation state +3. This reaction accounts for the requirement of two oxygen atoms in oxidation state −2 to extend the silica lattice by one $\mathrm{SiO_2}$ (or $\mathrm{AlO_2^-}$) unit. In other words, to obtain enough oxide ions to form the $\mathrm{AlO_2^-}$ species it is necessary to remove oxide ions from some part of the silica lattice, leaving vacant sites. These are effectively positively charged.

Reaction (2) clearly cannot go as an oxidation (i.e., to the right) if the metal electrode is pure aluminum. However, even in this case the corresponding reduction [Reaction (2) to the left = Reaction (—2)] can do so and we find that this is needed to interpret certain observations.

*Adapted from A. F. Wells, *Structural Inorganic Chemistry*, Oxford University Press, Oxford and New York, 1945.

Although the equations for Reactions (1) to (6) are balanced according to the usual criteria for electrode reactions, we note that in one important aspect they are not balanced. This is most easily explained using Reaction (3S) as an example: There is a large volume change associated with this reaction, essentially because it involves the replacement of a certain number of Si-Si bonds on the left by the same number of Si-O-Si bonds on the right. In contrast to the case with familiar electrode reactions involving a liquid solution, the volume change may here be hard to accommodate because the site of this reaction is the interface between two relatively rigid phases. On this basis it would make sense to include the volume change in the bookkeeping of balanced reactions by introducing an appropriate symbol to represent an amount of "space" corresponding to the molar volume change in the reaction. In the interest of simplicity this has not been done here, but it might be necessary in applying the model to the process of growth of the silica phase or to any other case in which it is crucial to investigate the possibility that diffusion of "space" to or from a reaction site is rate-controlling.

The foregoing discussion completes the description of our model; although its applications are to be demonstrated in the subsequent sections, the following general features may be noted here:

(A) A process like Reaction (7) or Reaction (8), acting by itself, conserves charge in the oxide. Therefore, any changes in the charge associated with these processes must also involve electrode reactions that occur during or after the time that the metal electrode of MOS is applied.

(B) A normal electrochemical couple such as Reaction (1) + Reaction (−3S),

$$4\,Al(Al) + 3\,SiO_2 \rightarrow 3\,Si(Si) + 4\,AlO_2^- + 2V^{++},$$

is based on the assumption that for electrochemical systems Faraday's laws are obeyed exactly. We propose here that the observed changes in the charge in the oxide in MOS annealing experiments may come from small deviations from Faraday's laws, in that the charge transferred through one electrode is not equal to that transferred through the other.

As an example, consider the system $Al|SiO_2|Si$, with the Al electrode positive with respect to the Si. If Reaction (1) proceeding at the Al electrode is somewhat faster than Reaction (—3*S*) proceeding at the Si electrode, then a positive charge (excess V^{++}) will accumulate in the oxide, balanced by a negative charge in the remainder of the system, silicon and metal. If the bias is held fixed, the accumulation of excess V^{++} in the silica will tend to slow and stop because the accumulation of V^{++} tends to retard Reaction (1) and accelerate Reaction (—3*S*).

The important advantage of the reactions as written is that they represent chemical changes among species that are *possible* in the light of current knowledge. They represent only changes that conform to conservation of charge and conservation of atomic species, and they enable the problem at hand to be treated with the help of many well-developed concepts taken from the study of more familiar electrolyte solutions. Different formulations are possible; for example, an alternative to Reaction (1) would be $Al(Al) \rightarrow Al^{+++} + 3e^-(Al)$ with Al^{+++} present interstitially in the silica. Then species other than V^{++} may have the role of the principal charge carrier, but at this time the formulation given in detail seems to be the simplest that fits the observations.

3. Experimental techniques

• *Polishing and etching*

The silicon wafers used in these studies were one-inch diameter disks cut with a diamond saw from 100 Ω-cm, *p*-type, oxygen-free silicon ingots with the [111] direction normal to the wafer surfaces. For a few of the experiments 10 or 1 Ω-cm *p*-type silicon was used instead. After being lapped with aluminum oxide (12 microns), the wafers were cleaned by degreasing, rinsing with distilled water, ultrasonic cleaning in acetone, and ultrasonic cleaning in methyl alcohol; finally, they were dried in air. There followed an 8-minute etching treatment in a rotating bath composed of 3 parts (by volume) nitric acid, 2 parts acetic acid, and 1 part hydrofluoric acid; this treatment was terminated by quenching the wafers in distilled water and rinsing. Finally, the wafers were dried on bibulous paper. At the end of this procedure the wafer thickness was 0.008 in.

• *Oxidation*

The wafers were oxidized at 975°C in a silica tube through which dry or wet oxygen was passed at a rate of 0.5 liter/min. The dry oxygen used was obtained from a commercial supplier and had the following analysis: N = 0.05%, A = 0.45%, H_2O < 5 ppm. Wet oxygen was prepared by passing dry oxygen through water heated near 100°C and then directly into the heated quartz tube. Unless otherwise indicated, the oxidation process used here was a sequence of dry, wet, and dry oxidations lasting 65, 45, and 60 minutes, respectively.

At the end of the oxidation process the wafers were cooled to room temperature within 4 minutes after being removed from the oxidation furnace. The oxide film so produced was 3800 Å thick, with ≤ 100 Å variation from wafer to wafer.

• *Boron treatment*

The oxide was doped with boron oxide in a zirconia tube at 1250°C. The boron source was placed towards the

Table 1 **Effects of various annealing procedures on V_m, the voltage at which capacitance changes.**

	System I Al|SiO_2|SiO_2	*System II* Al|P_2O_5, SiO_2|Si	*System III* Al|B_2O_3, SiO_2|Si	*System IV* Au|SiO_2|Si
Treatment A: Quenched from ~1000°C.	-20 ± 10 V	-10 ± 1 V	-17 ± 3 V	-20 ± 10 V
Treatment B: Sample from Treatment A annealed 30 min., open circuit.	-14 ± 3	-3 ± 1	-10 ± 1	-14 ± 3
Treatment C: Sample from A annealed 30 min. while M is biased V_a volts positive.	-90 ($V_a = 2$)	-3 ($V_a = 50$)	-60 ($V_a = 6$)	-90 ($V_a = 2$)
Treatment D: Sample from A annealed 30 min. while M is biased 30 volts negative	-6	-20	$+30$	-6

entrance of this tube in a platinum boat at 900°C. The boron source material was a mixture of 50% B_2O_3 with SiO_2. A carrier gas (99% nitrogen, 1% oxygen) flowed over the source and the sample at a rate of 2 liters per minute. This doping process lasted one hour. With the above conditions, a two-hour treatment was just sufficient for boron to penetrate through an oxide thickness of 3800 Å into the underlying silicon, as determined by observation of the magnitude of the capacitance change at V_m, which depends on the impurity concentration in the silicon.[3]

• *Phosphorus doping*

The oxide was doped with phosphoric anhydride in conditions similar to those used for the boron treatment: In a silica tube at 1050°C the wafer was treated with a gas stream prepared by passing N_2 over P_4O_{10} in a silica boat at 300°C at a rate of 2 liter/min. With these conditions 4 to 6 hours were required for phosphorus to penetrate the 3800 Å film and enter the silicon. In this work the standard duration of the phosphorus treatment was 1/2 hour.

• *Capacitance structure*

The oxide on one side of the silicon wafer was removed by etching with hydrofluoric acid to expose the bare silicon surface. Contact was made to this surface by means of conductive silver paint. To form the electrodes the desired metal was evaporated from a suitable source in a vacuum chamber (10^{-6} mm Hg) and condensed on the opposite (unetched) oxide layer as an array of dots 0.16 cm in diameter. The location of these was fixed by a mask during the evaporation.

Table 2 **Values of V_m for annealing procedures involving Si of various resistivities. The treatments are as specified in Table 1.**

	Resistivities of Si, in Ω-cm		
	1	10	100
For the System Al|P_2O_5, SiO_2|Si:			
Treatment A	-7 ± 1V	-9 ± 1V	-10 ± 1V
Treatment B	$+2 \pm 1$	-3 ± 1	-3 ± 1
Treatment D	-13	-20	-20
For the System Al|B_2O_3, SiO_2|Si:			
Treatment A	-12 ± 3	-17 ± 3	-17 ± 3
Treatment B	-5 ± 1	-6 ± 1	-10 ± 1
Treatment D	$+19$	$+25$	$+30$

• *Annealing*

Subsequent processing of the wafers is referred to in this paper as annealing. This involves a treatment at 325°C in a helium atmosphere for periods of several hours. As part of this process the wafer may be connected to a dc voltage supply with the metal electrode positive (anodic) and the silicon negative, or vice versa. Lehman[8] and Gregor[9] have found that the outcome of the annealing process is dependent upon the ambient atmosphere. However, pure helium and other inert gases do not appear to affect V_m.

• *Data*

The principal experimental results are given in Tables 1

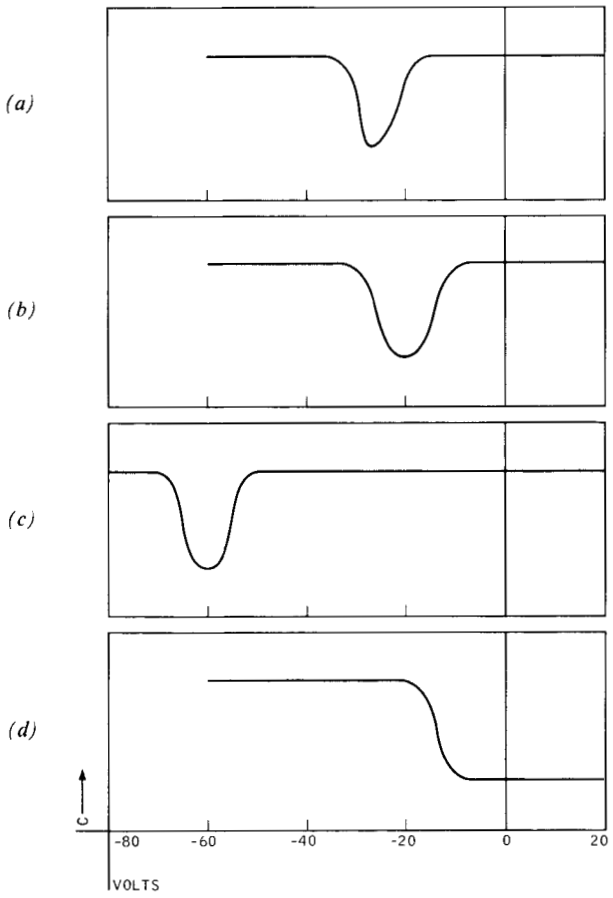


Figure 4 **The capacitance-voltage characteristics of Al|SiO_2|Si structures:** (a) *before annealing,* (b) *after annealing 30 minutes at 320°C,* (c) *after annealing for 2 minutes at 320°C with the* Al *electrode biased 30 volts positive, and* (d) *after annealing 30 minutes at 320°C with the* Al *electrode biased 30 volts negative.*

and 2, and some typical $C(V)$ characteristics are shown in Fig. 4. These data, which are representative of many tests on different wafers and of three to six tests at different positions on each wafer, support the following generalizations:

1. With p-type silicon the V_m of an MOS is always negative before annealing, indicating positive space charge in the silica.
2. Annealing the MOS without bias makes V_m less negative.
3. Annealing the MOS while it is biased so that M is anodic makes V_m more negative unless P_2O_5 is present.
4. Annealing the MOS while it is biased so that M is cathodic gives positive values of V_m if B_2O_3 is present.

An interpretation of these results in terms of the model discussed in Section 2 is given in the following section, together with a description of certain experimental results that were obtained to test the model more completely.

4. Discussion

One general result is that the silica film, as grown by the dry-wet-dry process and quenched to room temperature, contains a large built-in potential (see Section 1) with $V_d = 10$ to 20 volts. The same conclusion has been reached by a number of other investigators.[5,6,8] To the extent that it is based on MOS measurements, one might have suspected that this potential depends on processes at the M|O interface when the M electrode is laid down, as well as on processes at the O|S interface. However, painted-on metal electrodes are found to give MOS having the same characteristics; a more telling observation is that effects corresponding to large negative V_m are found in experiments with field-effect transistors even before the gate electrode is laid down. (See Section 5).

In terms of our model the simplest interpretation of this observation seems to be that during the growth of SiO_2 on Si, Reaction (3S) proceeds to the right to polarization equilibrium, i.e., until the potential of the space charge of V^{++} blocks the reaction. It is then the same space charge that makes V_m negative in the subsequent MOS capacitance measurement. Another way of stating the effect is that the oxidation reaction at the silicon surface causes the SiO_2 to be deficient in $O^=$, and some of the oxide sites are vacant. At the present time, we cannot tell whether the observed kinetics of oxidation are consistent with our hypothesis on the source of large positive space charge in the silica and hence negative V_m.

At this point we consider another problem that arises here and indeed, with slight modification, in every stage of the discussion in this Section. In the present case it is: How can values of V_m in the order of -10 to -20 volts be caused by an electrode process having a potential whose order of magnitude is near 1 volt? It is possible to answer this question providing one assumes that the space charge in the oxide is not uniformly distributed. Then a qualitative discussion is most easily given in terms of a sheet of space charge of concentration σ_+ (charges/unit area). As was pointed out in Section 1, this space charge, at a distance l_+ from the M|O interface, makes a contribution to V_d of amount $-\sigma_+ l_+/\epsilon$. However, during the growth process one need only consider the effect of this space charge on the reaction at the O|S interface, corresponding to the effect of a potential of amount $\sigma_+(l—l_+)/\epsilon$, where l is the total thickness of the oxide. If $l - l_+$ is small compared to l, as seems consistent with the hypothesis of electrode reactions, then V_d can indeed be much larger than the potential of the polarized Si/SiO_2 electrode. A detailed

calculation of this magnification effect has been given by Thomas and Young.[6]

In Treatment A (quenching), Table 1, the presence[10] of P_2O_5 or, to a smaller extent, B_2O_3 results in more reproducible and less negative V_m. It is seen that Reaction (7) or (8) of P_2O_5 or B_2O_3 with SiO_2 occurring at the outer surface of the growing oxide film, followed by diffusion of V^{++} through the film, will affect the final state of the polarization equilibrium in the SiO_2-Si reaction, Reaction (3*S*), achieved at the end of the quenching process.

The results of Treatment B (annealing without bias), Table 1, are negligible except in the system $Al|P_2O_5$, $SiO_2|Si$. Here it is suggested that the interstitial $O^=$ from P_4O_{10} provided by Reaction (9) acts as a sink for the V^{++} which were, in the first place, produced by the oxidation of Si, Reaction (3*S*). In this process the net charge in the oxide is conserved but the initial state in which the net charge is V^{++} near the O|S interface proceeds to a final state in which the net charge is PO_2^+ near the M|O interface. In terms of the calculation of V_d we have used, this reduces l_+ and thus reduces V_d. The fact that the change in V_d is relatively small suggests that this process is not carried to completion under the conditions of these experiments.

Support for the foregoing interpretation is provided by experiments in which the system P_2O_5, $SiO_2|Si$ is annealed *before* the M electrode is deposited, V_m is the same after annealing either with or without the presence of a metal electrode. Hence we infer that the change in charge configuration is not at the outside surface. In these experiments, the M electrode has been deposited both by vacuum evaporation at temperatures below 200°C. (M = Al) or by painting on a conductive suspension of silver particles.

In Treatment C of Table 1, (annealing with anodic bias), we propose that for System I (pure SiO_2), and System III (B_2O_3 doped SiO_2), Reaction (1)—the formation of metal oxide at the M|O interface—proceeds faster than does Reaction (−3S)—the reduction of Si from SiO_2 at the O|S interface. Thus there results a net accumulation of charge in the oxide until the changed potential brings the two reactions to a common rate. In the limit where the Si/SiO_2 electrode is completely polarized (i.e., Reaction (−3S) has zero rate) the extra charge accumulates near the O|S interface and large negative values of V_m may result from much smaller values of the bias used during annealing.

It is remarkable that the same result is found when M is the inert metal gold since neither the reaction $Au(Au) \rightarrow Au^+ + e^-$, with Au^+ interstitial in the oxide, nor any other reaction of gold seems possible with an oxidation potential only a volt less positive than the oxidation potential of Reaction (3S). It seems more likely that Reaction (6) is the anode reaction which produces V^{++}. It may be noted that Reaction (6) or (−6) occurring at a noble metal electrode was assumed by Jorgensen[11] in interpreting his electrochemical studies of the silica growth process.

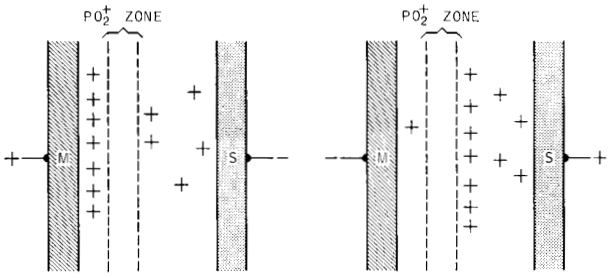


Figure 5 **Schematic representation of the charge distribution in the $Al|P_2O_5$, $SiO_2|Si$ system under conditions of anodic bias (on the left) and cathodic bias (on the right) of the Al electrode. The symbol + represents V^{++}.**

The behavior of the system $Al|P_2O_5$, $SiO_2|Si$ in Treatment C (Al biased positive) is most remarkable. The model proposed here requires that P_2O_5 near the M|O interface should inhibit Reaction (1). The following mechanism for this is suggested: The primary effect, independent of the bias, is the one used above to interpret the behavior of this system when annealed without bias, namely, interstitial $O^=$ bonded to the PO_2^+ acts as a sink for some of the V^{++} originally present near the O|S interface. Furthermore, from consideration of the doping process, we expect that the PO_2^+ produced by the high-temperature doping of Reaction (7) is localized in a zone parallel to and near the M|O interface. In this zone the $O^=$ concentration is presumably very high so that the zone acts as a barrier to the flow of V^{++}, preventing them from concentrating at the O|S interface.

For the system $Al|P_2O_5$, $SiO_2|Si$ in Treatment D (Al cathodic) the zone of high PO_2^+ concentration again acts as a barrier to the flow of V^{++} and this species tends to accumulate on the side of this zone near the O|S interface. The V^{++} concentration in this region increases as the Si is oxidized. Thus the existence of such a zone can account for the outcome of both the reduction of space charge in Treatment C and the increase in space charge in Treatment D provided the zone is some fraction (perhaps 1/4) as thick as the entire oxide film and is near the M|O interface, Fig. 5. It is found that with this system further annealing (open circuit) following either anodic or cathodic treatment (Treatment C or D) has no effect on V_m.

For Systems I and IV of Table 1 (that is, for Al and Au with pure SiO_2 in Treatment D, metal cathodic) it is proposed that we have Reaction (−3M), the reduction of Si at the M|O interface, and Reaction (3S), the oxidation of Si at the O|S interface. Since the first is essentially the reverse of the second, both should proceed at similar

rates and the resulting distribution of V^{++} is only slightly shifted toward the M|O interface, when compared to that in Treatment B (annealing without bias). Indeed, when the product of Treatment D is annealed with open circuit, there is no further change in V_m.

For the remaining system, $Al|B_2O_3$, $SiO_2|Si$, in Treatment D, Al cathodic, the result is very different. Now at the M|O interface the reduction must be Reaction (—2), reduction of boron, which presumably has nearly the same standard potential as Reaction (—3M), reduction of Si, but is apparently much faster. As a result the net positive charge V^{++} in the oxide tends to decrease and to be swept away from the polarized Si/SiO_2 electrode where only the slow Reaction (3S), oxidation of Si, can occur. This moves V_m to positive values. Positive V_m means that there is negative space charge, BO_2^-, in the silica. When the MOS is annealed with open circuit the V_m is found to shift slowly to negative values, presumably under the influence of the built-in potentials.

5. Application to electrothermal treatment of transistors

A field-effect transistor with insulated gate electrode (IGFET) is illustrated in Fig. 6. The source and drain for this *n-p-n* type device are diffused *n*-type regions about 2 microns deep, separated by a *p*-type region (called the channel) of from 8 to 20 microns in width. The metallic gate, an evaporated film, is insulated from the silicon in the channel by 2000 Å to 8000 Å of thermally grown silicon dioxide. A voltage applied to the gate controls the type (i.e., holes or electrons) and density of the current carriers at the surface of the channel.

Characteristic curves for a typical *n-p-n* "depletion mode" device are shown in Fig. 7a. The surface of the channel is *n*-type, as is expected from the behavior of SiO_2 in contact with Si and metal electrodes. This is demonstrated both by capacitance measurements of V_m, as have been described, and by the fact that there is ohmic contact, through the channel region, between one diffused *n*-type junction and the other. A voltage applied to the gate electrode that is negative relative to the source decreases the density of electrons at the surface, returns the surface to *p*-type, and turns off the device. This turn-off voltage corresponds to V_m.

Characteristics for a typical *n-p-n* "enhancement mode" IGFET are shown in Fig. 7b. The surface of the channel in this case is *p*-type and this produces a typical *p-n* junction between the channel and the diffused *n*-type contacts at the source and drain. To turn on this enhancement-mode device a positive voltage is applied to the metallic gate relative to the source and *n*-type carriers are brought into the surface of the channel.

The initial oxidation for these devices was performed in a "post" boron furnace, i.e., a furnace used for oxidizing silicon that is highly doped with boron. Thus, the oxide is contaminated with boron as well as with P_2O_5, the latter entering the oxide during the diffusion of the source and drain electrodes. From the model discussed in Section 2 we would expect Reaction (—2) to proceed when the gate electrode is cathodic at 300°C. Also, to be consistent with results presented in Table 1 for Al/B_2O_3, SiO_2/Si, we would expect the turn-on voltage, i.e., V_m, to shift to large positive values. We would further expect to convert the *n*-type surface of the silicon to a *p*-type surface and to change the electronic characteristics of the transistor from the depletion to the enhancement mode. Figure 7b shows the enhancement-mode characteristics which were in fact achieved by making the gate electrode cathodic while holding the device at 300°C; Fig. 7a illustrates the characteristics prior to the electrothermal treatment.

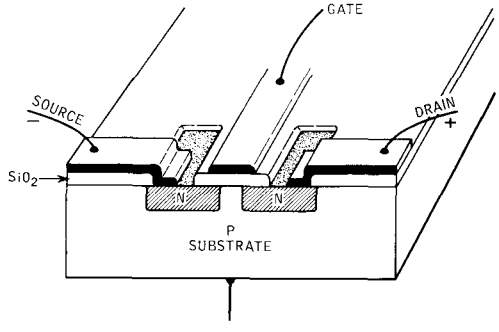
The rate of conversion was determined by periodically observing V_m for the gate-substrate capacitance. Results of typical experiments, Figs. 8 and 9, show that the reaction proceeds very rapidly at first and then in most cases appears to stop. According to the model proposed here, it appears that the reaction is retarded by the space charge that accumulates because the anodic Reaction (3*S*) is slower than the cathodic Reaction (—2). This charge tends to bring these reactions to the same rate. For large applied voltages V_m should increase, just as Fig. 9 illustrates.

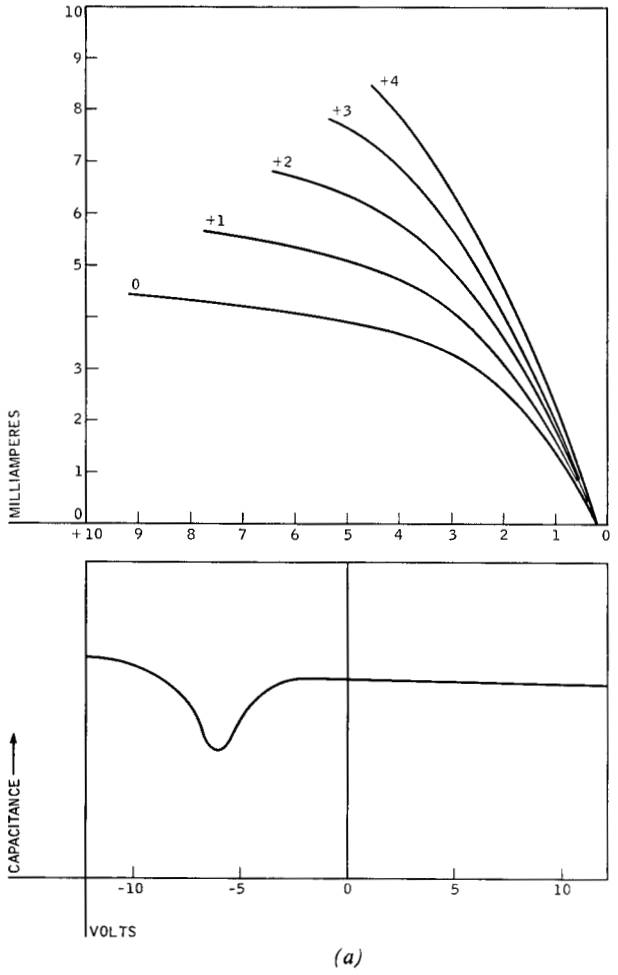
During annealing with Al biased anodic, V_m is observed to shift to large negative values faster than it shifts to positive values in the Al-cathode treatment.

6. Summary

A model based on the generation and motion of a charged species, oxide-ion vacancies, has been developed to account for the effects of positive space charge in SiO_2 on silicon, and of negative space charge in the surface of the silicon. Changes in the space charge have been caused

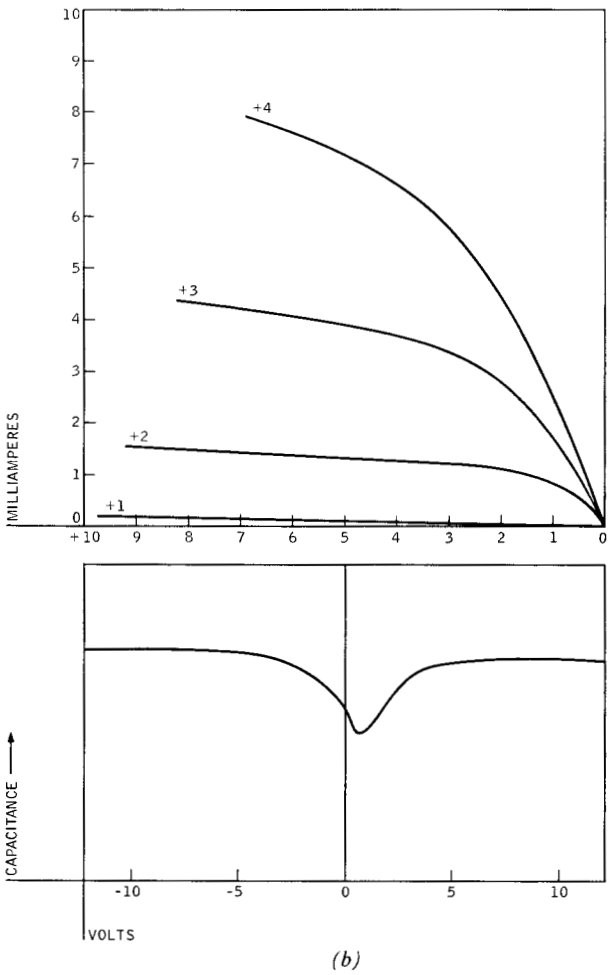
Figure 6 **The structure of an insulated gate field-effect transistor.**





(a)

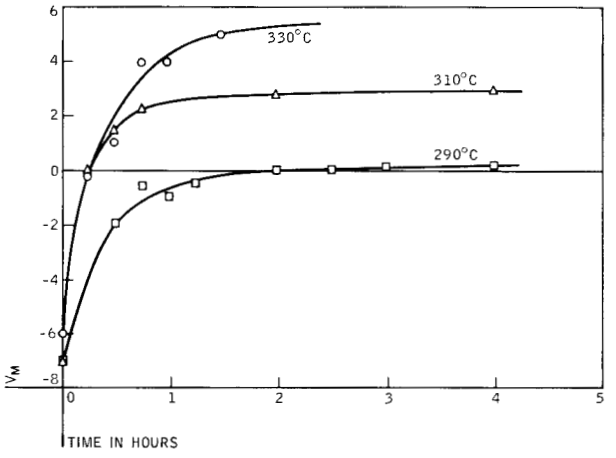
Figure 7a **The source-drain current of depletion-mode insulated gate field-effect transistors is shown (above) as a function of source-drain voltage for gate voltages of 0, 1, 2, 3 and 4 volts. Appearing below is the gate-substrate capacitance as a function of gate-substrate voltage for the same device.**



(b)

Figure 7b **Curves showing characteristics corresponding to those in Fig. 7a for an insulated gate field-effect transistor that has been converted from depletion mode to enhancement mode.** *(See the procedure described in the text.) This normally-off device requires positive gate voltage to turn it on.*

Figure 8 **The room-temperature turn-on voltage (V_m) of an insulated gate field-effect transistor as a function of the duration of annealing treatments at various temperatures with the gate biased at —40V relative to the substrate.**



by annealing and by electrical bias procedures and by doping the SiO_2 with P_2O_5 and B_2O_3. These changes have been explained by the generation or removal of oxide-ion vacancies, by electrochemical processes at the metal-oxide and oxide-silicon interfaces, and by distribution of the vacancies in the SiO_2. A special result is that positive

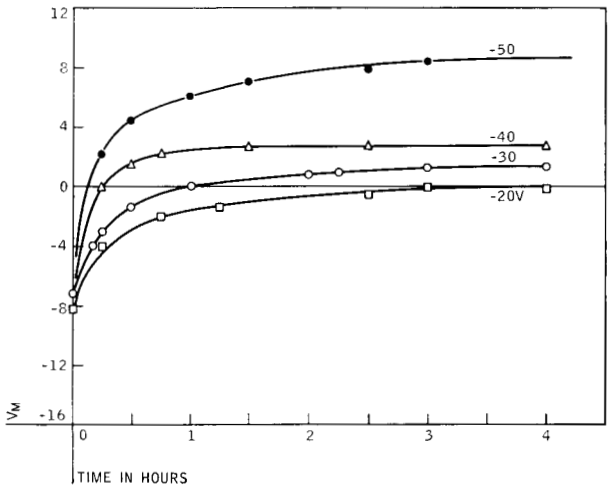


Figure 9 **The room-temperature turn-on voltage (V_m) of an insulated gate field-effect transistor as a function of the duration of an annealing treatment at 310°C with various values of the bias of the gate relative to the substrate.**

space charge can be developed in silicon surfaces when the SiO_2 is doped with B_2O_3 and is then electrically biased.

Although the model has demonstrated predictive value in the course of this work, we regard the more specific details of the electrochemical reactions as being tentative because of the special assumptions about the relative rate of various processes that are required to secure concordance of the model and observations. The most likely way to test those assumptions, as well as other aspects of the model, appears to be by electrical measurements on metal-oxide-silicon systems at the annealing temperature. In particular, extended measurements of the sort described by Kerr et al.[10] and by Yamin and Worthing[12] are likely to be very useful.

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