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Effect of Temperature and Bias on Glass-Silicon Interfaces*

Abstract: New technologies for deposition of thin glass films on silicon substrates have generated interest in the resulting glass-silicon interface potentials and the interface stability under conditions of bias and temperature that might be experienced in device operation.

Experiments are described which show accumulation of space-charge layers at glass-silicon interfaces under combined conditions of electric field applied normal to the surface, and elevated temperature. The glasses studied are lead-alumino-borosilicates and zinc-alumino-borosilicates and were applied in films several microns thick by sedimentation techniques. Measurements were made on metal-glass-silicon capacitor structures. The silicon at the interface may be shifted strongly n-type or strongly p-type, depending on applied field direction, during a heating cycle of a few minutes. Surface charge densities up to 10^{13} electronic charges/cm^2 have been observed. The temperatures required for such shifts vary over the range 100° to 300°C, depending on glass composition. Conductivity through the films during the combined bias-temperature treatment is compared with interface charge build-up. The data suggest a mechanism in which the bias-temperature combination causes movement of ions (possibly sodium) with a resultant build-up of space charge in the glass near the interface. The long-term stability of this "locked-in" charge indicates that interface potential with the more stable glasses may be permanently tailored to a desired value by bias-temperature treatment

Introduction

Techniques for depositing thin glass films onto silicon substrates by sedimentation techniques have recently been developed.[1,2] Since such films could be used for surface passivation of semiconductor devices or as dielectrics in insulated-gate field-effect devices, the surface potential at the glass-silicon interface and the stability of this potential under device operating conditions are of considerable interest.

The purpose of this paper is to describe experiments on potential shifts at such interfaces that occur under the combined conditions of elevated temperature and of electric field applied normal to the surface.† The glasses studied are lead-alumino-borosilicates and zinc-alumino-borosilicates. The metal-insulator-silicon (MIS) capacitor has a small-signal capacitance versus bias voltage (C-V) characteristic which indicates the interface charge per unit area in the silicon at zero bias. The interface potential may then be determined since it is a known function of the space charge in the silicon. The MIS device has been used for this study because of its relatively simple fabrication and ease of testing. Differences in C-V measurements before and after the combined bias-temperature treatments indicate the interface instability at a particular temperature.

Both positive and negative space-charge layers in the silicon have been induced at the glass-silicon interfaces for all glasses tested. The composition of the glass and the temperature of bias-temperature treatment appear to be the most important variables in determining stability. The dc conduction through the glass films during bias-temperature treatment has been measured also and correlates, to some extent, with build-up of interface charge, as indicated by C-V data.

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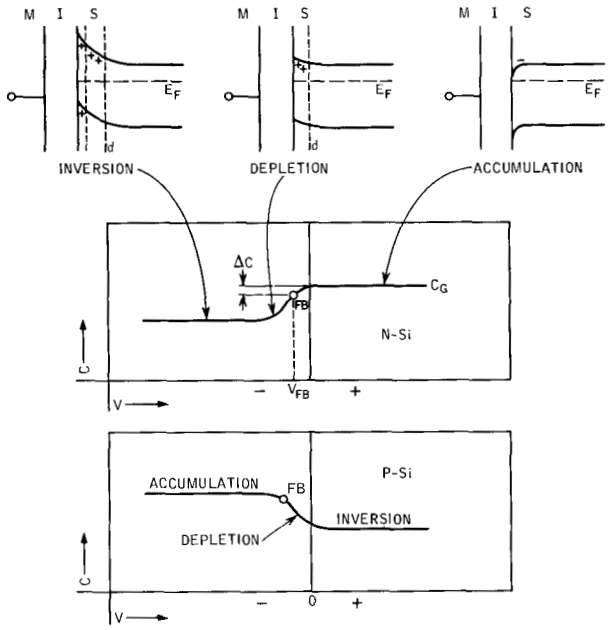
† This stress combination is hereafter referred to as *bias-temperature treatment.*

The theory of the metal-insulator-silicon capacitor and interpretation of *C-V* traces will first be reviewed. The experimental techniques will be described, and the data will be presented and discussed. Finally, the applications of effects reported in this paper will be discussed.

Theory of MIS capacitor

The MIS capacitor has been analyzed in detail in the literature[3-5] and will be reviewed here only briefly. The simplest equivalent circuit for such a device is a fixed capacitance per unit surface area C_G, corresponding to the glass dielectric layer, in series with a variable capacitance C_S due to the space-charge layer of the semiconductor surface. The behavior of such a device in terms of the semiconductor band structure may be qualitatively understood by referring to Figure 1. The illustration is for *n*-type silicon with a uniform donor impurity concentration. When the bias on the metal electrode is varied, the majority carrier concentration near the insulator-silicon interface can be accumulated above the concentration in the bulk of the silicon, depleted below the bulk concentration, or inverted (giving a *p*-type surface in this example). A band diagram is given for each of these conditions. Bias polarity throughout this paper is defined as the potential of the metal electrode with respect to the bulk of the silicon. Considering first the diagram for accumulation, the electron charge induced lies very close to the interface, and the device capacitance reaches a maximum level determined by the thickness and permittivity of the insulator. As bias is decreased, the surface is depleted. The high-frequency induced charge fluctuation occurs at the edge of the depletion region, and the increased distance between the electrode and the induced ac charge results in a capacitance decrease. As the bias is made more negative, the silicon surface inverts. The hole charge induced by the bias now occurs in a very thin layer near the interface, but this layer has a charging time constant sufficiently long that charge fluctuations at frequencies of 1 kc or higher generally occur at the inner depletion layer edge. Since charge induced by the dc bias goes into the hole layer, the position of the depletion layer edge is now nearly independent of bias, and the capacitance saturates at a low value as shown. Similar reasoning for *p*-type silicon leads to a complementary characteristic as shown in the lower curve of Fig. 1.

Figure 1 **Silicon energy-band diagram for three regions of the *C-V* characteristic of a metal-insulator-silicon capacitor.** *The band diagrams and upper C-V characteristic are for n-type silicon, and the lower C-V characteristic is for p-type silicon. E_F is the Fermi level and d indicates the depletion layer edge.*



When the conduction and valence bands are flat out to the glass-silicon interface, there is zero space charge within the silicon. The capacitance per unit area of the silicon surface at this "flat-band" point is given by[3]

$$C_{SFB} = q(\epsilon_s n/kT)^{1/2},$$

where q is the electronic charge, ϵ_s is the permittivity of silicon, and n is the bulk carrier concentration. This capacitance in series with the glass capacitance C_G gives a fractional device capacitance decrease of

$$\frac{\Delta C}{C_G} = \frac{C_G}{q(\epsilon_s n/kT)^{1/2} + C_G}$$

in going from the maximum capacitance of the accumulation region to the flat-band point. This point is indicated by *FB* in Fig. 1, and the bias required is denoted V_{FB}.

By Gauss's law, the space charge per unit surface area in the silicon Q_S is always equaled by a net external charge of opposite sign. External charge here includes charge on the metal electrode, insulator space charge, and charge in interface states (which may be filled or empty, depending on their energy relative to the Fermi level at the interface). With insulator space charge present but interface states absent, the application of V_{FB} affects only Q_S, reducing it to zero. The flat-band electrode charge is then equal to the zero-bias Q_S (in magnitude and sign). In the presence of interface states some of the charge induced by V_{FB} goes into interface states, and the zero-bias Q_S is somewhat less than the flat-band electrode charge. A treatment creating insulator space-charge near the insulator-silicon interface will shift the *C-V* characteristic along the voltage axis, while the creation of interface states will cause a broadening of the *C-V* transition along

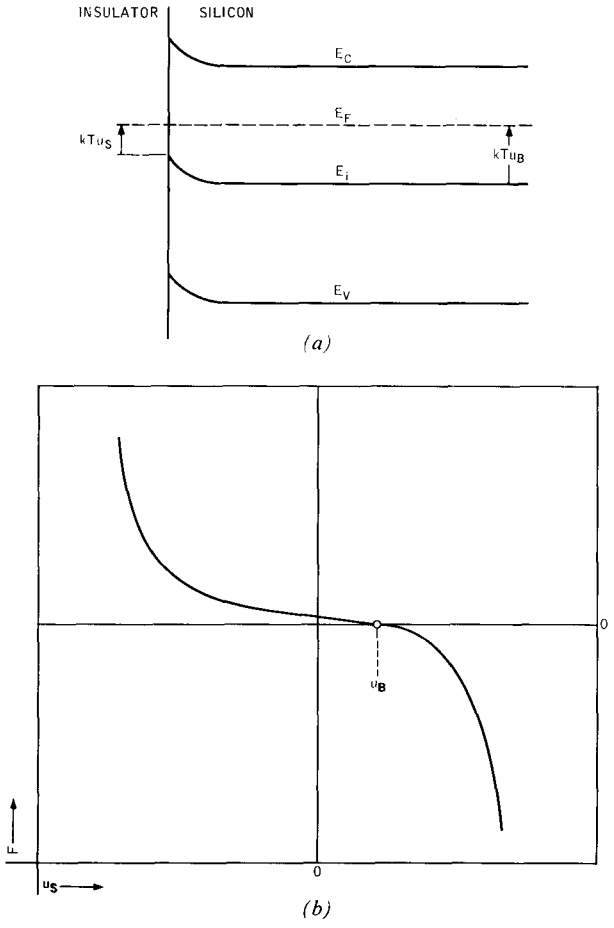


Figure 2 *a) Band diagram for silicon surface defining interface potential u_S.*
b) Illustration of behavior of the function F versus u_S for a positive bulk potential u_B.

the voltage axis. A mathematical treatment describing effects of space-charge build-up at insulator-silicon interfaces is given in an accompanying paper.[6]

Interface states[7] cause an equivalent series *R-C* branch shunting the silicon surface capacitance C_S. The effect of this capacitance on the measured capacitance is negligible if an angular frequency above the reciprocal of the time constant of the states is used. A frequency of 10 kc/sec was found to be sufficiently high for our samples.

The interface potential is defined as u_S in Fig. 2a, where kTu_S is the distance, on the energy band diagram, from the intrinsic Fermi level E_i at the interface to the Fermi level. The illustration is for a depletion space-charge layer on *n*-type silicon. The silicon space-charge per unit area is given by[8]:

$$Q_s = (2n_i\epsilon_s kT)^{1/2} F(u_S, u_B),$$

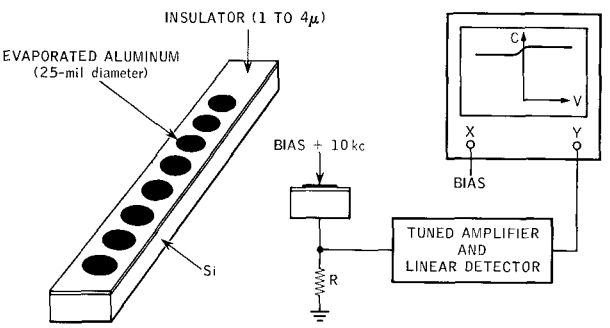
where n_i is the intrinsic carrier concentration. The function $F(u_S, u_B)$ has been tabulated for various u_S and u_B values,[8,9] and its behavior vs u_S for a positive u_B is illustrated in Fig. 2b. The interface potential corresponding to a measured silicon charge may thus be determined. The flat-band condition is defined by $u_S = u_B$ and we note, as mentioned previously, that this corresponds to $Q_S = 0$.

Experimental techniques

Both *n*- and *p*-type silicon wafers with resistivities in the range of 5 Ω-cm were used as substrates. This resistivity is required for flat-band capacitance decreases of several percent with glass film capacitances on the order of 3×10^{-9} F/cm^2. The wafers were chemically etched and thin films of powdered glass were deposited by a sedimentation technique.[2] The glasses were fused into homogeneous films by firing for a few minutes at temperatures in the range 570° to 770°C. Film thicknesses were measured by a light interference technique.[10] Aluminum electrodes with areas approximately 3×10^{-3} cm^2 were then evaporated onto the glass films to complete the MIS structures. Aluminum was also evaporated onto the backs of the wafers for ohmic contact to the silicon. The wafers were not heated during evaporation. The wafers were then scribed into strips, each containing eight MIS devices, so that bias-temperature runs could be made subsequently at several different temperatures.

Figure 3 shows a sample strip and a simplified diagram of the *C-V* measurement equipment. A 10 kc/sec signal (<1 V amplitude) is superimposed on a dc bias and applied to one of the devices on the strip. The termination resistor *R* is a much lower impedance than the capacitor, and the voltage appearing across it is thus proportional to the MIS capacitance. This signal is converted to dc and applied to the vertical channel of an *X-Y* recorder. The bias voltage is electronically swept around any desired average value such that a *C-V* curve is traced in

Figure 3 **Sample strip of MIS devices and diagram of *C-V* measurement equipment.**



about 100 sec. The magnitude of the maximum capacitance and electrode area are measured so that C_G and $\Delta C/C_G$ may be calculated. The flat-band electrode charge density N_{FB} is given by

$$N_{FB} = C_G V_{FB}/q,$$

where flat-band bias V_{FB} is taken from the *C-V* curves. The samples used for the data presented in this paper are described further in Table 1. The N_{FB} values given are from measurements before any bias-temperature treatment.

The bias-temperature jig is constructed such that arbitrary biases may be applied to four devices on a contact strip after it is raised to temperature. The bias-temperature treatments were done in a nitrogen ambient to prevent jig oxidation, but the data were not dependent on the ambient gas. Runs were terminated by cooling in a few minutes to room temperature with bias applied. *C-V* traces were again made and compared with initial curves. Figure 4 is a reproduction of the *C-V* curves for glass #182 before and after bias-temperature at 200°C. Note that the curves are shifted with little distortion along the voltage axis. The shift of the flat-band voltage ΔV_{FB} was -30 V for devices biased at $+10$ V and was $+25$ V for devices biased at -10 V.

The measurements of currents during bias-temperature were made in a low-leakage, shielded cell which, with an electrometer, permitted measurement of dc current as low as 10^{-13} amp through a single MIS unit. The output of the electrometer was fed to a recorder to give a record of current versus time.

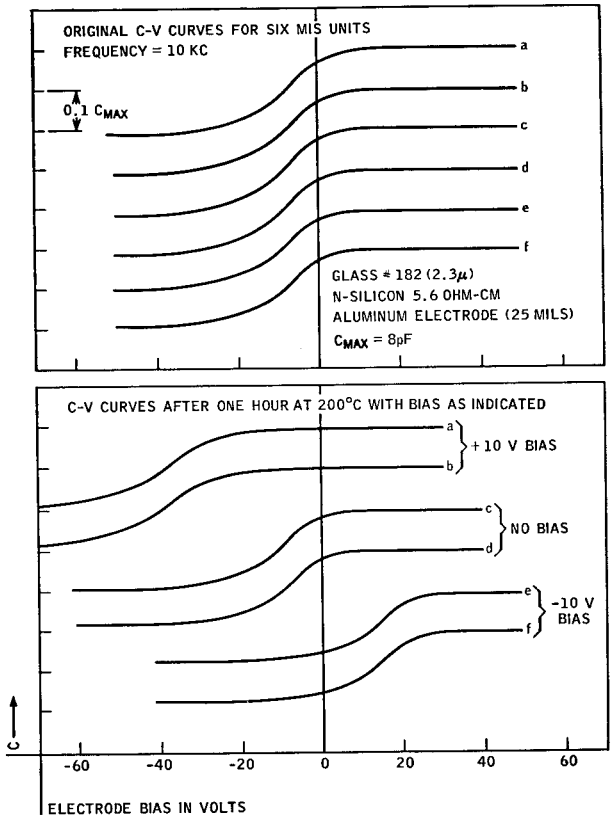


Figure 4 **Typical *C-V* traces before and after bias-temperature treatment.** *For convenience, the zero suppression on the vertical scale is varied between units.*

Table 1 **Sample parameters.**

Glass No.	*Glass composition*	*Silicon resistivity (ohm-cm)*	*Glass thickness (microns)*	C_G (10^{-9} F/cm^2)	$\Delta C/C_G$ (%)	N_{FB} (10^{11}/cm^2)
760[a]	Lead-alumino-borosilicate	4.7-*n*	2.4	2.2	2.3	−1.4
1527[b]	Lead-alumino-borosilicate	6.2-*n*	1.6	5.5	6.8	−2.7
182	Lead-alumino-borosilicate	5.6-*n*	2.3	2.8	3.2	+0.2
P16	Zinc-alumino-borosilicate	5.5-*p*	2.1	3.1	2.2	−0.6
P18	Zinc-alumino-borosilicate	7.3-*p*	3.8	1.8	1.4	−1.1

[a] Available as X760LZ from Corning Glass Works.
[b] Available as E1527 from B. F. Drakenfeld and Company, Inc.

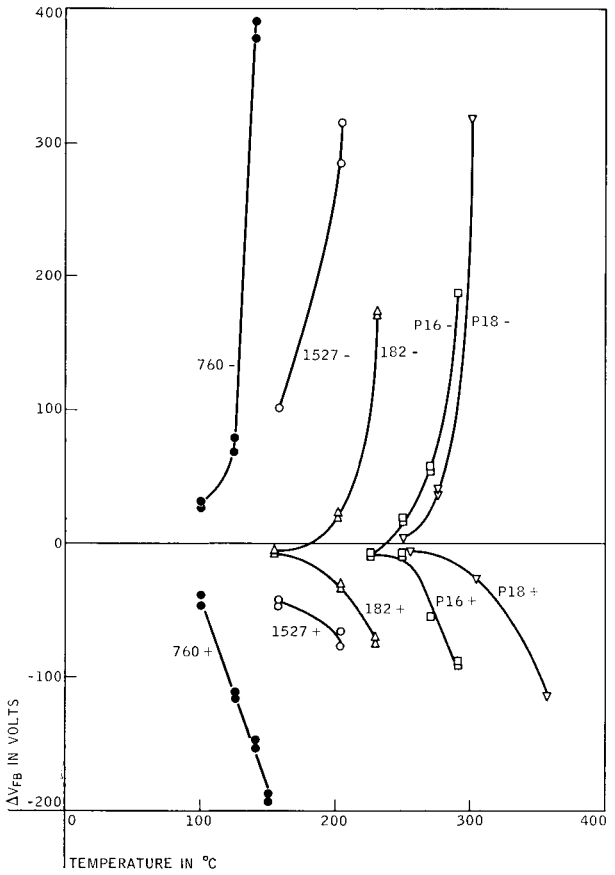


Figure 5 **Shifts in flat-band bias ΔV_{FB} versus temperature used in one-hour bias-temperature treatment of metal-glass-silicon devices.** *Plus and minus signs after glass numbers indicate polarity of 10 V bias applied to metal during bias-temperature.*

Results

- *C-V Shifts*

The ΔV_{FB} shifts resulting from runs at various temperatures for the five wafers listed in Table 1 are shown in Fig. 5. All data are for runs of 60 min with bias of +10 V and −10 V. The general procedure was to bias two units on a sample strip positively and two negatively for each run at a given temperature. As shown in Fig. 5, the *C-V* shifts of units with identical bias usually differed by less than 10 V. Note that all the glasses tested will give large ΔV_{FB} shifts in either direction, but that the temperatures required vary greatly with glass composition. The data indicate that the zinc-alumino-borosilicates #P16 and #P18 should be considerably more stable than the lead-alumino-borosilicates for surface passivation at device operating temperatures less than 150°C. Data of the type shown in Fig. 5 have been taken for similar glass films on both *n*- and *p*-type silicon, and no significant dependence on doping type was observed. Samples of #760 glass with evaporated silver electrodes were also tested and no significant differences between aluminum and silver were observed.

The ΔV_{FB} data may be converted to electrode charge density by multiplying by the glass capacitance from Table 1. Since ΔV_{FB} values of greater than 100 V were observed for all samples, the changes in flat-band electrode charge densities corresponding to ΔV_{FB} values of 100 V are given in Table 2. The highest charge density obtained from the data of Fig. 5 is 10^{13} charges/cm^2 for the positive shift of glass #1527 at 200°C.

Interface charge densities indicated by Fig. 5 could be explained by migration of sodium ions within the glass. Sodium migrating as a positive ion has been often blamed for conductivity and space-charge development in glass.[11,12] The glasses tested here have sodium atom concentrations on the order of 10^{19} cm^{-3}, except for glass #1527, which has about 10^{21} sodium atoms/cm^3 as an intentional additive.[13] These would give densities of 10^{15} cm^{-2} and 10^{17} cm^{-2}, respectively, for glass films of one micron. A small fraction of this sodium migrating to the interface region under positive bias at elevated temperature would cause positive space-charge densities on the order of 10^{13} cm^{-2}. Cooling to room temperature presumably renders this glass charge immobile. Under zero-bias conditions, it induces a negative space charge in the silicon. A large negative bias must then be applied to reduce this silicon space charge to zero and observe the flat-band capacitance. Combined bias-temperature treatment with negative bias could deplete sodium ions from the glass near the interface, leaving a negative space charge. The facts that #1527 is more stable than #760 and that wide differences between glasses are evident in Fig. 5, suggest that mobility of sodium ions

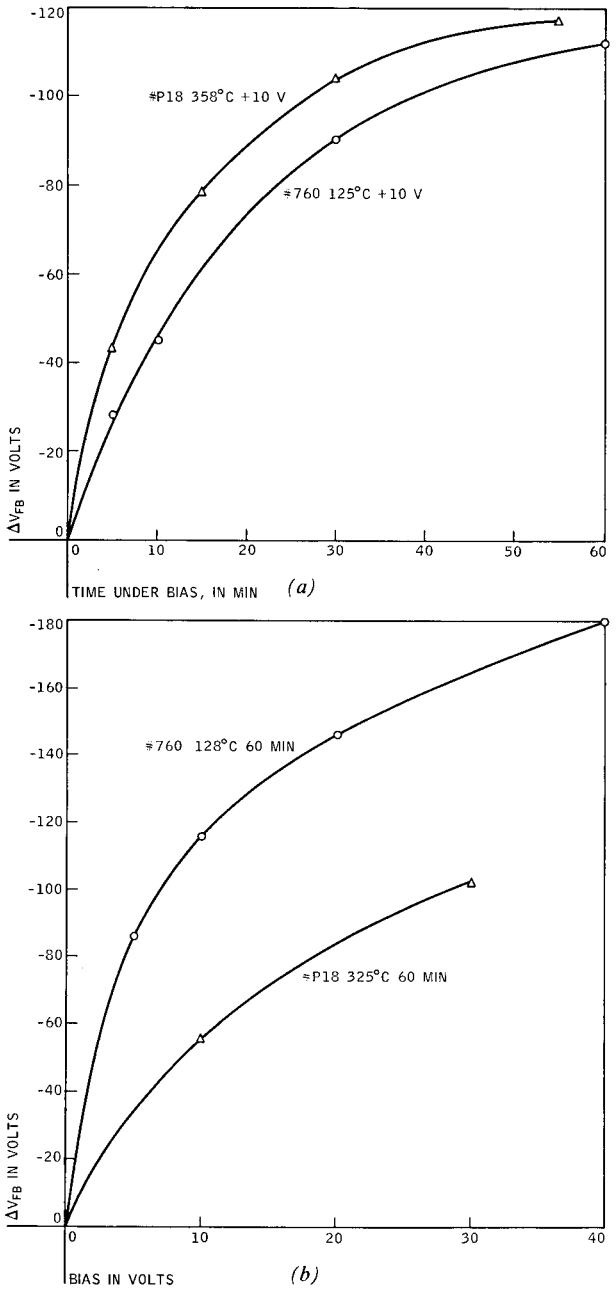
Table 2 **Constants for conversion of ΔV_{FB} data to electrode-charge data.**

Glass No.	*Change in flat-band electrode charge density corresponding to ΔV_{FB} = 100 V (10^{-7} coul/cm^2)*	*(10^{12} electronic charges/cm^2)*
760	2.2	1.4
1527	5.5	3.4
182	2.8	1.7
P 16	3.1	1.9
P 18	1.8	1.1

is more important than sodium concentration in determining glass stability.

The time and bias dependence of the ΔV_{FB} shifts for two of the glasses are shown in Fig. 6. The shifts are seen to be a saturating function of both time and bias. The probable causes of this will be discussed later. A few experiments in which a sample with #760 glass was given a sequence of bias-temperature treatments, differing only in the bias polarity, indicate that bias-temperature shifts are completely reversible. The reversal rates are comparable to initial charging rates (i.e., a 60-min treatment with reversed bias will generally reverse the sign of charge induced in an initial 60-min treatment at the same temperature).

Figure 6 **a) Time dependence of ΔV_{FB} shifts. b) Bias dependence of ΔV_{FB} shifts.**



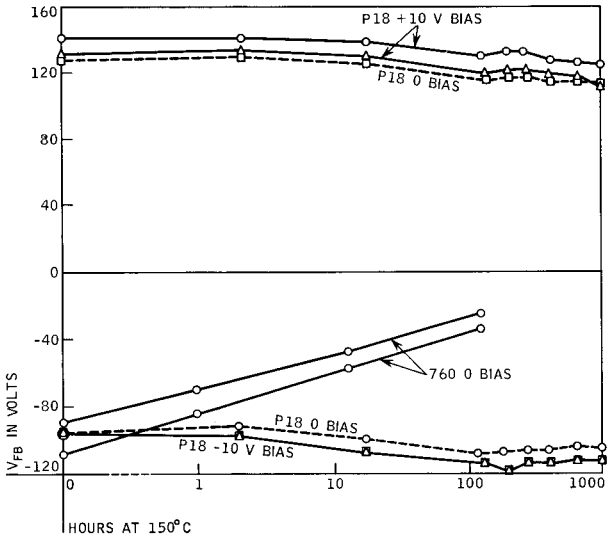
- *Stability after bias-temperature shifting*

From inspection of Fig. 5, one might expect that a glass such as #P18 could be bias-temperature treated in the region of 300°C to give a desired "locked-in" interface charge that would not decay at temperatures of 150°C or less. Trapped charge with #760 glass would be expected to decay rapidly at 150°C, however. Results of an experiment to check this are shown in Fig. 7. Samples with #760 and P18 glasses were stored in air at 150°C after an initial bias-temperature treatment and removed periodically for measurement of the flat-band voltage. The #760 samples were stored with zero bias, while the P18 samples were held at both zero bias and at bias tending to drive V_{FB} towards zero. It is seen that the #760 samples decay to one-half their initial values in about 20 hr, which is much longer than the time required for initial shifting at 150°C, +10 V bias. The P18 samples appear to have good stability of the trapped charge at 150°C. No difference is seen in samples with and without bias at this temperature.

- *Conductivity measurements*

Current measurements with 10 V bias were taken in the

Figure 7 **Long-term stability of V_{FB} at 150°C after initial shifting of interface potential by combined bias-temperature treatment.**



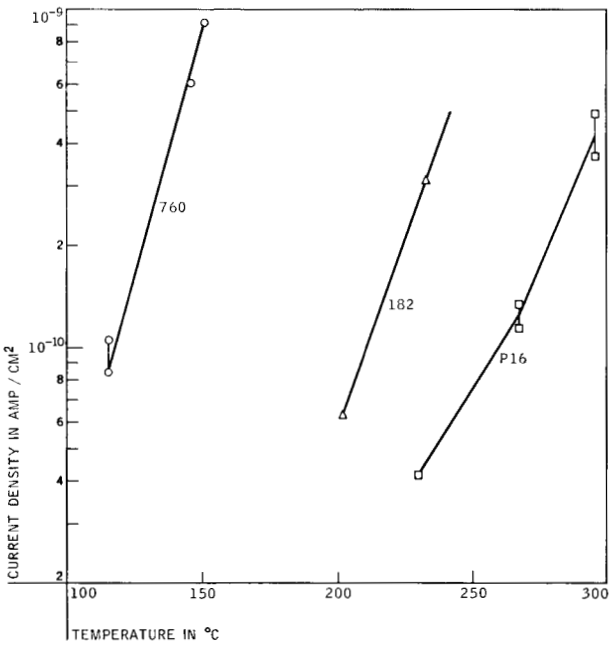


Figure 8 **Current density in glass films 200 sec after application of 10 V bias.**

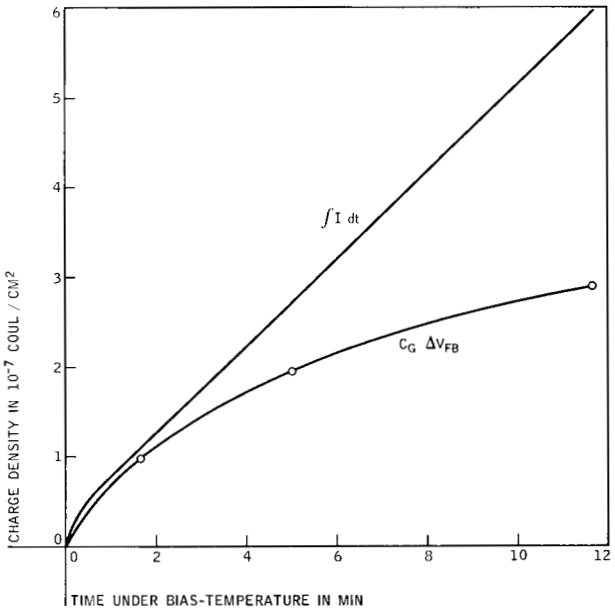


Figure 9 **Comparison of charge conducted and flat-band charge ($C_G\Delta V_{FB}$) for glass #760 biased at + 10 V, 150°C.**

same temperature range as the temperature-bias runs for *C-V* data (100° to 300°C). In all cases the current decayed within the first 100 sec after application of bias to a value which was then nearly time-independent. No asymmetry with bias polarity was noted. Reproducibility of current between units from the same wafer and measured at the same temperature was generally within 25%. The reproducibility and the observed temperature dependence make any explanation of the currents based on electronic leakage through pinholes very unlikely. Figure 8 shows current density 200 sec after applying 10 V bias for three of the glass films at various temperatures. Again a great variation with glass composition is observed which correlates qualitatively with *C-V* shift data of Fig. 5. Based on this data, we might expect a ΔV_{FB} shift of several tens of volts after one hour at bias-temperature conditions, causing current density of 10^{-10} amp/cm^2.

It is interesting to compare the currentdensity—time integral with $C_G\Delta V_{FB}$, which is indicative of insulator space charge near the glass-silicon interface. This comparison is made in Fig. 9 for #760 glass biased at 150°C. Three devices were biased for three different time periods and then *C-V* measurements gave the ΔV_{FB} values. The steady-state current gives a linear current-time integral after the first minute. If we postulate a model in which bias drives positive ions toward the glass-silicon interface, the $\int I\,dt$ curve indicates the number of atoms accumulated at the interface, while the $C_G\Delta V_{FB}$ curve gives the number of these atoms remaining charged. We note that in the first few minutes nearly all the charge transferred is stored at the interface. The saturation of ΔV_{FB} after the first few minutes, seen here and in Fig. 6a, indicates a neutralization of ions as space charge builds up. This could be due to electrons tunneling from the silicon into the glass.

Applications

The combination of *C-V* measurements and bias-temperature treatments on MIS devices should prove to be a useful tool for evaluating the interface charge and stability of insulator-silicon interfaces. The primary advantages are the very simple device fabrication and the short testing time required. An insulator suitable for passivation layer use will give no *C-V* curve shifts under combinations of bias and temperature to be experienced by the device in question. These techniques have also been used in studying the stability of the silicon dioxide-silicon interface.[14]

The data of Fig. 7 show that, with a suitable glass, bias-temperature treatment can "lock-in" an interface charge that will not decay at device operating temperatures. This technique may be useful as a device tailoring step. The gate characteristic of an insulated-gate field-effect transistor may be shifted along the voltage axis. An example is shown in Fig. 10. The device here is an experimental majority-carrier field-effect transistor with an *n*-type epitaxial layer on a *p*-type substrate. The gate

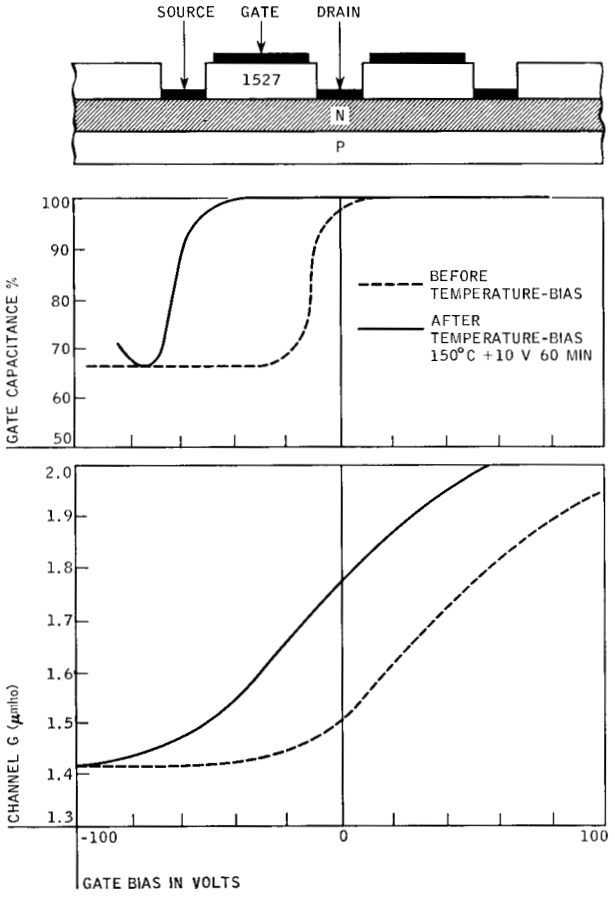


Figure 10 **Tailoring of the gate characteristic of an insulated-gate field-effect transistor by bias-temperature treatment.**

dielectric is #1527 glass and a circular electrode geometry is used. Small-signal channel conductance and gate capacitance are plotted versus gate bias. It is seen that bias-temperature treatment shifted both curves by equal amounts without shape changes. The interface has been shifted from a nearly flat-band condition at zero bias to strong accumulation. These data are presented merely to illustrate the principle of interface adjustment, and a more stable glass would normally be used with a resulting higher adjustment temperature. The breakdown voltage and leakage current of passivated planar silicon junctions are known to be affected by charge applied to external gate electrodes.[15] Gain of planar transistors may also be controlled by a gate.[16] By use of glass passivation layers one or more of these device parameters might be optimized by "locking-in" an interface charge with bias-temperature.

Conclusion

This work has shown that the silicon at a glass-silicon interface may be driven strongly *n*-type or strongly *p*-type depending on applied field direction during a heating cycle of a few minutes. The important variables in the process are glass composition, temperature, applied bias, and time under bias-temperature. Unimportant factors are silicon doping type, electrode metal, and ambient atmosphere. For the glasses measured, the temperatures required for large interface shifts vary over the range 100° to 300°C. The data suggest a mechanism in which the combined bias-temperature treatment causes space charge to build up in the glass near the interface. This charge is probably due to migration of sodium ions within the glass, although proof has not been given here. The long-term stability of this "locked-in" charge indicates that interface potential with the more stable glasses may be permanently tailored to a desired value by bias-temperature treatment.

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