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Stabilization of SiO_2 Passivation Layers with P_2O_5*

Abstract: Measurements are reported on the stability of planar, npn silicon transistors with and without a phosphosilicate glass layer over the SiO_2 passivation layer. The phosphosilicate layer forms during the emitter diffusion from a P_2O_5 source, and the data show that, to insure stability, it must not be removed in subsequent processing steps. The units tested were of conventional geometry except for a gate electrode over the base region, which provided additional information on the surface condition. The transistors were subjected to temperatures of 150° and 200°C with either gate-bias or junction reverse-bias. Production transistors, without gates, which had failed on life test were shown to have no phosphosilicate layer because it had been removed by excessive etching during fabrication. Additional evidence for the stabilization by P_2O_5 has been obtained using metal-oxide-silicon capacitors with and without P_2O_5 treatment of the SiO_2 layer. Both dc conduction through the insulator and stability of the capacitance-voltage characteristic were measured. These experiments suggest that the transistor degradation with unstabilized SiO_2 is caused by an accumulation of positive space-charge in the silicon-dioxide. This charge accumulates when an electric field (directed toward the silicon) is applied to the SiO_2 at temperatures in the range of 150°C.

Introduction

Since the original work by Atalla, Tannenbaum and Scheibner,[1] SiO_2 formed by thermal oxidation has been used extensively for passivating silicon devices. It is well known that SiO_2 forms a chemically stable coating that reduces the sensitivity of devices to external ambient effects. It is also generally recognized that the presence of SiO_2 on Si tends to make the surface of the silicon *n*-type, independent of the bulk conductivity type. This tendency has caused difficulties in *npn* transistors arising when the *p*-type base region is inverted at the surface.

Electrical conductivity measurements on SiO_2 have been made by Yamin and Worthing,[2] and by the authors, showing that ionic conductivity can occur in SiO_2 at temperatures as low as 150°C. This is a surprising observation since much higher temperatures are normally required before diffusion effects are observed.

Extensive experience has shown[3] that the presence of a thin phosphosilicate glass layer on the outside of the SiO_2 results in improvement in the stability of device characteristics. This layer is frequently formed during the fabrication of transistors since SiO_2 is used as a diffusion mask for phosphorus diffusion. A sharp compositional boundary exists between the glass and the unreacted SiO_2, and the movement of this interface through the SiO_2 layer is diffusion controlled.[4] The present work shows that if the phosphosilicate layer is completely removed by subsequent processing steps the device will be unstable, even under the usual accelerated life testing, which is also performed in the temperature range of 150° to 200°C.

In the following sections, data is presented that show the remarkable effect that P_2O_5 has on the electrical stability of SiO_2. In companion papers, Thomas and Young[5] and Seraphim et al.,[6] suggest models for explaining the effects that have been observed.

In the first section below, careful measurements are

* Presented in part at IEEE Solid State Device Research Conference, Boulder, Colo., July 2, 1964.

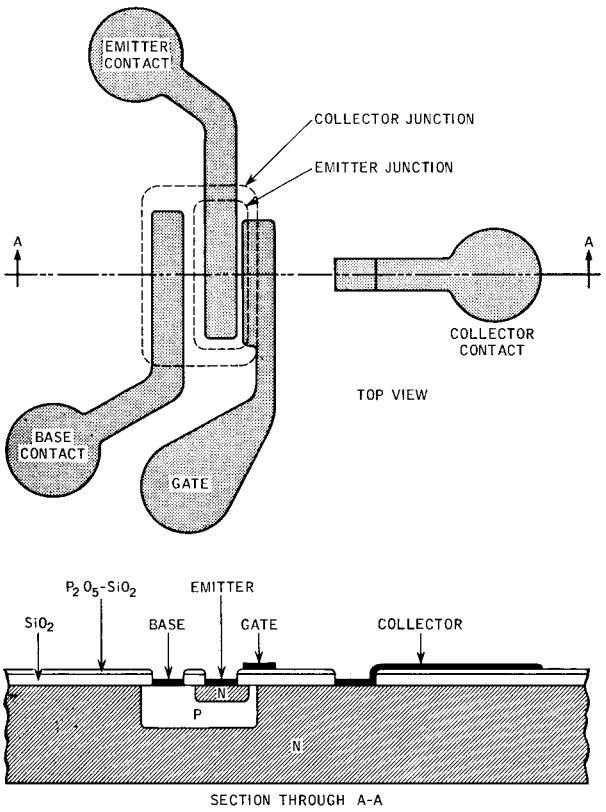


Figure 1 **Gated transistor geometry (with phosphosilicate layer).**

reported of the details of the degradation, with and without phosphosilicate layers, which occurs when *npn* silicon transistors are subjected to temperature and voltage stress. The next section describes the technique for determining the presence or absence of the phosphosilicate layer on completed devices and shows that devices selected at random after life testing have a strong correlation between survival and presence of the phosphosilicate glass layer. The variation in the thickness of the phosphosilicate layer in production devices is related to the clean-up etching used just before aluminum metallization.

The next section of the paper gives detailed studies of surface potential changes in SiO_2-insulated MOS capacitors under temperature and voltage stress, with varying thicknesses of phosphosilicate glass under the metal electrode. This section also presents the differences in electrical conduction through the SiO_2 which relate to the presence or absence of the phosphosilicate layer.

Gated transistor experiments

A transistor electrode structure was designed (Fig. 1) with a gate electrode covering both emitter and collector junctions, in order to provide a means of applying an electric field at the surface of the base region. The gate voltage necessary to induce a given level of conduction between collector and emitter was used as an indicator of surface condition in the base region, allowing detection of surface instability before base inversion actually occurred.

Planar *npn* transistors were made by conventional oxide masking and diffusion processes that resulted in a layer of phosphosilicate glass approximately 2000 Å thick over the entire wafer as determined by an etching technique.[7] Total insulator thickness over the base region was approximately 8000 Å. At this point, half of each wafer was etched in "*p* etch"[7] long enough to completely remove the phosphosilicate glass layer. Then aluminum was applied by evaporation with the substrate held at <200°C. The contact structure of Fig. 1 was obtained by normal photolithographic techniques. Some of the wafers received a 500°C treatment followed by a glass overcoat fired at 570°C. These process variables resulted in four different kinds of devices labeled *A*, *B*, *C*, and *D* in Table 1. Devices of each type were mounted on gold-plated headers and wire contacts attached for testing. The mounting process involved a heat treatment for a short time ($\approx$30 sec) at temperatures above the gold-silicon eutectic temperature of 370°C.

Table 1 **Experimental variables and wafer designations.**

Metals, temperature, and overcoat	*Insulator type*	
	Phosphosilicate glass present	*Phosphosilicate glass removed*
Cold Al contacts, no overcoat	*A*	*B*
500°C, sintered aluminum contacts, and glass overcoat	*C*	*D*

- *Test conditions and measurements*

The transistors were subjected to several stress conditions, but the most common one used was that of collector and emitter junctions reverse-biased at 12 V and 4 V, respectively, and held at 200°C. In this case, the gate electrode was held at the emitter potential, simulating an extension of the emitter contact connection. This test, called *junction stress*, was designed to approach as closely as possible ordinary transistor accelerated-life-test conditions.

A second stress condition at 200°C was positive voltage (30 V) applied to the gate electrode with all other connections grounded. This *gate stress* condition tests the surface stability under the influence of an externally applied field, as opposed to the stability in the presence of the fringing field of the junction.

At intervals during stressing, the transistors were cooled to room temperature with the bias voltages on. The currents listed below* were then measured as functions of the gate-to-base voltage. The measurements were designed to distinguish between collector-to-emitter channel formation, and junction leakage increase.

1. I_{CEX}, defined as:
   Collector current at $V_{CB} = +6.0$ V
   $V_{EB} = -350$ mV, V_{GB} = variable
2. I_{ECX}, defined as:
   Emitter current at $V_{CB} = +6.0$ V
   $V_{EB} = 0$, V_{GB} = variable
3. I_{CBO}, defined as:
   Collector current at $V_{CB} = +6.0$ V
   $I_E = 0$, V_{GB} = variable
4. I_{EBO}, defined as:
   Emitter current at $V_{EB} = +1.5$ V
   $I_C = 0$, V_{GB} = variable

• *Results*

It was found that, of all the quantities measured, I_{CEX} was the most sensitive to both kinds of stress, but that the other quantities moved in the same direction as I_{CEX}. Therefore, to avoid redundant information, only the measurements of I_{CEX} will be presented.

Sample curves of I_{CEX} vs gate bias for type *A* and *B* devices are shown in Fig. 2. In general, the results of both stress conditions were that the I_{CEX} curves moved across the axis for *B* devices (phosphosilicate glass removed) and remained essentially constant for the *A* devices (phosphosilicate glass present). This result is indicated in Fig. 2, where the curves for *A* devices are practically identical before and after treatment, as opposed to the large shift in *B* devices. Tables 2 and 3 summarize the numerical results for all four types, representing a total of 24 devices. (Five of each type in Table 2, and two each of types *A* and *B* in Table 3). In general, no significant difference in stability between the glassed and unglassed units could be found.

A movement of the I_{CEX} curve across the axis means that at zero gate voltage, large leakage currents are observed. These were interpreted as device failures. Thus the results indicate that it is necessary to retain the phosphosilicate glass if device failure at elevated temperature and reverse-bias is to be avoided.

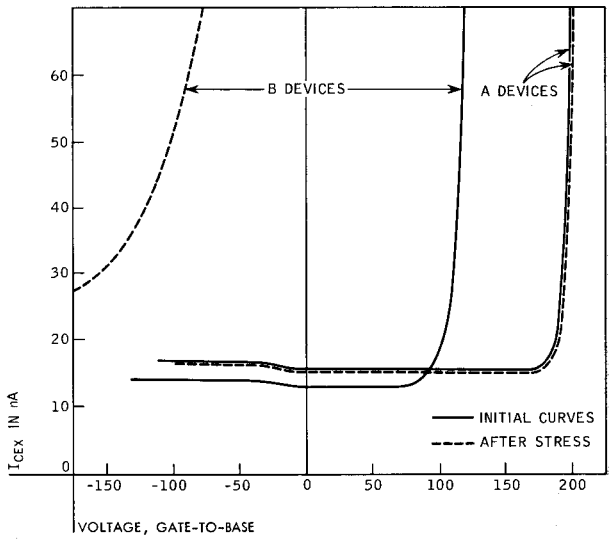
Other devices from these wafers were tested at lower temperatures (150°C) and it was found that devices with phosphosilicate glass present never failed, whereas instability and failure usually occurred on devices with the phosphosilicate glass removed.

Examination of glassed devices

The importance of the phosphosilicate layer for transistor stabilization has also been shown by the examination of production transistors after life tests. The transistors were planar *npn* glass-covered transistors of the type described by Davis et al.[8] Following the phosphorus emitter diffusion, the wafers are reoxidized without removal of the phosphosilicate layer. The final phosphosilicate layer above the pure silicon dioxide is approximately 2000 Å thick as determined by etching techniques.[7] After the reoxidation, holes are opened in the emitter, base, and collector areas by conventional Photo Resist* masking and etching methods. After removal of the Photo Resist, and immediately prior to evaporation of the metal contact lands, the wafer is subjected to a slight ammonium fluoride-HF buffer etch to insure removal of all oxide in the hole area and subsequent proper ohmic contact, but without appreciable removal of the phosphosilicate layer from other regions of the wafer. After evaporation of the metal contact lands the wafer is glassed by special sedimentation techniques[9,10] and contacts to the emitter, base, and collector regions are attained with solderable metal balls.[11]

* Photo Resist is a Trade Mark of the Eastman Kodak Company.

Figure 2 **I_{CEX} curves before and after stress.**



• The letter symbols used here are consistent with "IRE Standards on Letter Symbols for Semiconductor Devices," *Proc. IRE*, **44**, 934-937. Subscripts used are: *C* for collector, *B* for base, *E* for emitter, and *G* for gate.

Table 2 **Results of 200°C junction-bias stress.**

Transistor type	*Gate Voltage to Induce 100 na I_{CEX}*		
	Initial	*1/2 Hr*	*~70 Hr*
A (No Etch)	Avg. +200	+204 V	+215 V
	Range +173 to +209	+194 to +216	+202 to +240
B (Etched)	Avg. +97	<0	<0
	Range +64 to +127		
C (No Etch)	Avg. +156	+161	+128
	Range +146 to +162	+151 to +170	+77 to +149
D (Etched)	Avg. +120	−135	−73
	Range +98 to +135	−50 to −200	−24 to −114

Table 3 **Results of 200°C gate-bias stress.**

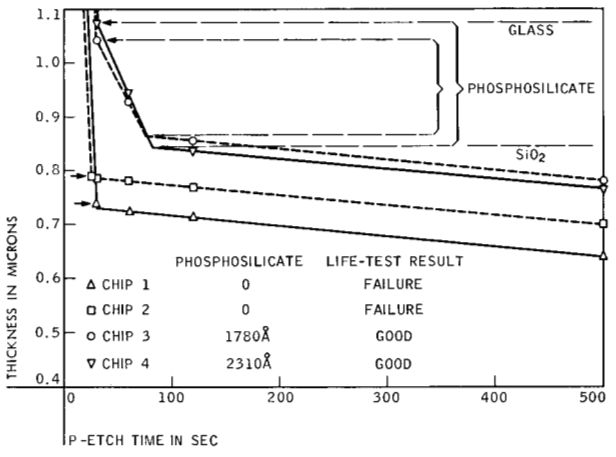
Transistor type	*Gate Voltage to Induce 100 nA I_{CEX}*			
	Initial		*1/2 Hr*	*70 Hr*
A (No Etch)	Unit 1	197	197	193
	Unit 2	173	175	179
B (Etched)	Unit 1	64	<0	<0
	Unit 2	95	<0	<0

Transistors manufactured by the above process were then subjected to reverse-bias testing, similar to that described in the previous section, at 150° or 200°C for various periods. Devices are considered to be failures if they exhibit high leakages at room temperature within any time period of the test. On prolonged life testing the leakages usually return to low levels but the devices are still considered failures. The high leakages are generally observed within 24 hours of life testing.[12] If the devices are produced properly, they will show very low leakages ($I_{CBO} < 1$ nA at 3 V). However, if in the process of manufacture the phosphosilicate layer is removed from the surface prior to metal evaporation, the devices will, in general, fail the high temperature reverse-bias test.

Some particular examples which had been observed on transistors are illustrative. Several transistors which had been subjected to the high temperature reverse-bias test were examined for the presence of phosphosilicate using the "*p* etch" technique.[7] This etch was originally developed for the delineation of glasses on oxides. In this technique the transistor chip is etched for various periods of time in "*p* etch." After each etch period, the chip is examined microscopically and the film thickness determined by a special interference microscope called "Vamfo."[13] The film thicknesses are plotted against etch time. Since the various components in the film system have significantly different etch rates, demarcation of the interfaces is easily determined. The etch rates at 25°C are 2 Å/sec for SiO_2, ~40 Å/sec for the phosphosilicate layer, and ~500 Å/sec for the glass sealing film.

Etch-rate plots for four of the transistors are shown in Fig. 3. These plots show that both good transistors have a significantly thick phosphosilicate layer above the SiO_2. In these plots, arrows correspond to the points at which the etch had just barely removed all the glass sealing film and thus indicates its interface with the phosphosilicate or the SiO_2. Of the seven transistors examined in this early

Figure 3 **Etch-rate plot of glassed transistors with and without a phosphosilicate layer.**



study, all five that failed the reverse-bias tests contained no phosphosilicate; whereas those that passed the test showed a significant amount of phosphosilicate. The absence of phosphosilicate was apparently due to poor control of the previously mentioned buffer etch prior to the metallization. Occasionally, devices from a wafer with phosphosilicate will fail the reverse-bias test for other reasons, but device failures are nearly always observed if the phosphosilicate is removed.

Measurements on MOS devices

• *Bias-temperature effects on C-V characteristics:*

We have studied the stability of accumulation and inversion layers in SiO_2-insulated silicon as influenced by the combination of elevated temperature and electric bias applied across the oxide layer. The method used is the comparison of capacitance-voltage (*C-V*) curves for metal-oxide-silicon capacitors before and after bias-temperature treatments.

The MOS capacitor has been described in the literature[14–16] and a review of its operation is given in an accompanying paper.[17] Typical *C-V* (small-signal capacitance versus dc bias) traces for MOS devices with *n*-type and *p*-type silicon are shown in Fig. 4. The carrier concentration in a thin layer of silicon near the oxide-silicon interface may be varied by the bias voltage *V* applied across the oxide (bias polarity being defined here as metal electrode potential with respect to the silicon bulk). As the interface condition is varied from accumulation of majority carrier concentration above the bulk concentration to depletion of majority carriers, the capacitance goes through a characteristic decrease due to the surface depletion-layer capacitance in series with the oxide layer capacitance. If the bulk silicon doping and the oxide capacitance are known, a capacitance decrease, ΔC in Fig. 4, may be calculated,[17] which determines the device capacitance when the space charge in the silicon is zero. The silicon conduction and valence-band edges are flat out to the interface at this point, and the measured bias required for this "flat-band" condition is denoted V_{FB}.

As seen in Fig. 4, the flat-band bias is normally negative. This indicates a negative space-charge layer in the silicon at zero bias, which may be caused by positive charge either in interface states or fixed space-charge in the oxide near the interface.

The effect of bias-temperature treatment on an MOS device is shown in Fig. 5. These devices were fabricated by growing a 6800 Å layer of SiO_2 by an oxygen-steam-oxygen cycle at 970°C on a 6.5 ohm-cm *n*-type silicon wafer. Aluminum electrodes (approximate area of 3×10^{-3} cm^2) were then evaporated onto the oxide without heating the wafer. A large-area aluminum electrode was evaporated onto the back of the wafer to provide ohmic contact to the silicon. Bias was swept at a rate of about 5 V/sec and capacitance was measured at 10 kc/sec. Room-temperature *C-V* curves were traced out on an *X-Y* recorder before and after bias-temperature treatments in nitrogen. Bias was maintained during cooling to room-temperature at the completion of the bias-temperature treatment. It is seen in Fig. 5 that a typical unit before bias-temperature had a flat-band bias V_{FB} of −28 V. After 70 min at +12 V bias and 100°C the *C-V* trace was shifted in a negative direction to give a V_{FB} of about −107 V. With zero bias or negative bias, the same temperature treatment gave no shifting of the *C-V* characteristic. Higher temperatures with zero or negative bias tend to shift the curve to the right as shown in the dotted trace, but such shifts appear to be a function of time and temperature and not bias. V_{FB} may typically approach −10 V for thermally grown oxides of thickness on the order of

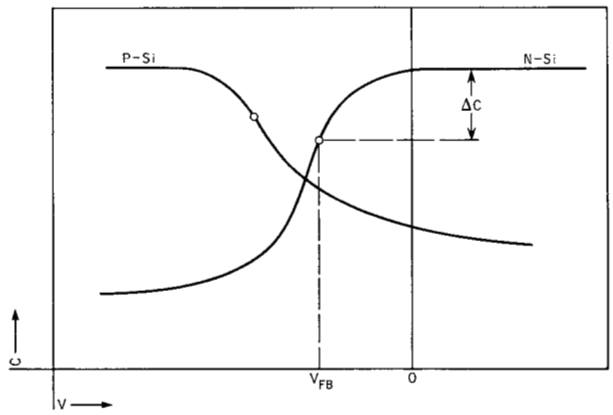


Figure 4 **Typical *C-V* traces of MOS capacitors for n-type and p-type silicon.**

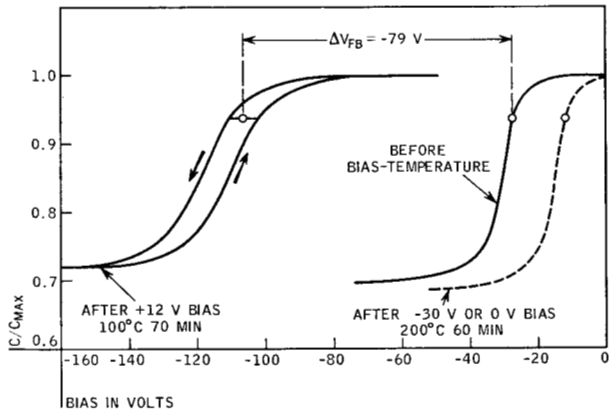


Figure 5 ***C-V* traces before and after bias-temperature treatments.** *Wafer #257:n-type silicon, 6.5 ohm-cm. SiO_2, 6800 Å; $C_{max} = 5.1 \times 10^{-8}$ F/cm^2.*

5000 Å, and positive V_{FB} values have not been observed with bias-temperature combinations as high as −30 V and 450°C.

The negatively shifted curve of Fig. 5 suggests that the treatment under positive bias has built up a positive space-charge in the oxide near the oxide-silicon interface. This causes the silicon surface to be more strongly *n*-type at zero bias, and the negative bias V_{FB} required for zero silicon space-charge to be greatly increased. A physical model for this process based on migration of oxygen vacancies through the silicon dioxide is discussed by Thomas and Young[5] and the effect is described in terms of electrode processes by Seraphim et al.[6] The hysteresis seen in the curve of Fig. 5 would be explained by limited migration of space charge within the oxide at room temperature during tracing of the *C-V* curve. The broadening of the *C-V* transition indicates an increase in interface-state density also as a result of bias-temperature. An alternate explanation for this is a nonuniformity of the interface shift over the device area.

Large negative shifts of *C-V* curves with bias-temperature have been observed with *n*- and *p*-type silicon, and with oxides grown in steam and oxygen. The ΔV_{FB} shifts at a given bias-temperature combination are observed to vary as much as a factor of two between devices on a given wafer. Temperature of bias-temperature treatment is an important variable, and ΔV_{FB} shifts beyond the oxide breakdown strength (≈300 V for 5000 Å films) are commonly achieved at temperatures below 200°C. The roles of various oxidation parameters in determining stability have not yet been fully established. Oxidation in dry oxygen generally produces a more stable film than steam. The temperature required for a given *C-V* shift in an oxygen-grown film is typically 50° to 100°C higher than that required for a similar shift in a steam-grown film.

An experiment in which electrodes of aluminum, silver, chromium and platinum were evaporated onto the same wafer indicates that the electrode material is not an important variable. The substrate for this experiment was 6 ohm-cm *p*-type silicon with a 2800 Å oxide grown in oxygen at 1050°C. Initial V_{FB} values were about − 6 V there being no variation with electrode metal. Two devices of each metal were bias-temperature treated at +30 V, 125°C, 60 min. All V_{FB} values then fell in the range −30 to −80 *V*, and no significant correlation with electrode metal was evident.

- *Stabilization by* P_2O_5

It was found that large *C-V* shifts caused by positive bias and temperature could be completely avoided by exposing the oxidized wafer to a phosphorus diffusion cycle before application of electrodes. An experiment was performed to examine the dependence of P_2O_5 stabilization on the thickness of phosphosilicate glass. Wafers of 5.3 ohm-cm *n*-type silicon were oxidized at 970°C with an oxygen-steam-oxygen cycle to give a 6100 Å film. Diffusions were done in a conventional two-zone, open-tube furnace using a P_2O_5 source and also by a single-zone process from a PH_3 gas source with an oxygen ambient.[18] The diffusion conditions and phosphosilicate glass thicknesses are given in Table 4. The phosphosilicate thickness was determined by the method described in the section on glassed devices. Electrodes for these samples were evaporated aluminum. Flat-band voltages before bias-temperature are also given in Table 4, and comparison of this voltage for the samples with and without a phosphorus diffusion treatment shows that the diffusion treatment tends to reduce the "built-in" interface charge. The average dielectric constants of the films were unaffected by the diffusions ($\epsilon_r \approx 4$).

The ΔV_{FB} shifts resulting from bias-temperature runs on these samples are shown in Fig. 6. All data are for +30 V bias during a 60-min heating cycle in nitrogen. We observe that stability is greatly improved by the phosphorus diffusion treatment. No gross variation of stability with phosphosilicate layer thickness or with the diffusion source (P_2O_5 or PH_3) is observed. The positive shifts (15 V or less) occurring in the stabilized samples at 200°C and higher are independent of bias, occurring also with zero bias and −30 V bias. A small negative shift was ob-

Table 4 **Diffusion treatments and initial flat-band voltages.**

Wafer No.	*Source*	*Silicon temp.* (°C)	*Diffusion time* (*min*)	*Phosphosilicate thickness* (Å)	SiO_2 *thickness* (Å)	V_{FB} *before bias-temp.* (*volts*)
351	P_2O_5	800	60	900	5350	−18
353, 355	P_2O_5	925	60	2150	4500	−15
357	P_2O_5	1035	60	4300	3000	−20
364	PH_3	925	7	700	5500	−30
366	PH_3	925	29	1200	5200	−20
361, 362	—	no diffusion	—	—	6100	−60

served for wafer 357 after bias at 400°C, but this is well above normal device operating temperatures.

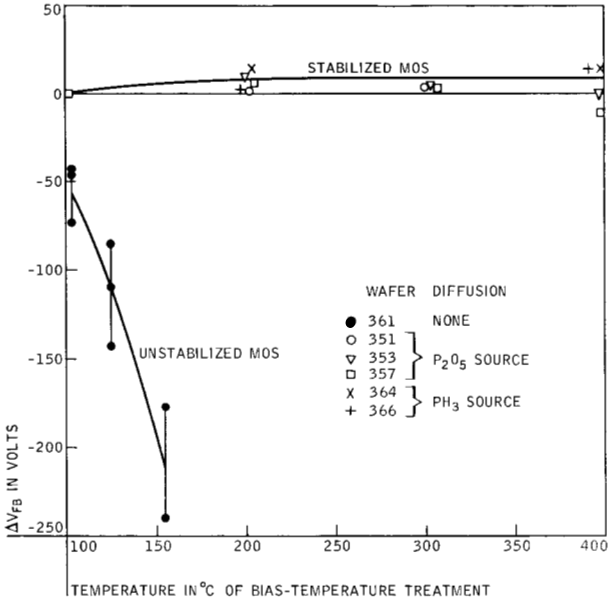
Data on *p*-type wafers with and without P_2O_5 diffusion is essentially the same as that of Fig. 6. Additional experiments were performed in which the phosphosilicate layer was etched away before application of electrodes. These devices gave large negative shifts under bias-temperature which were characteristic of the oxide before phosphorus diffusion.

- *Electrical conductivity*

In an MOS device under bias at elevated temperatures, current flow takes place between the metal and the semiconductor through the insulator. The behavior of this current was investigated as the temperature was gradually raised from room temperature to 300°C. By using a consistent rate of temperature climb from sample to sample, it was possible to make qualitative comparisons of the current-temperature curves for various devices. Peaks in the curves indicate various thermally activated space-charge or electrode polarization and annealing processes, their relative magnitudes, and the temperature ranges where these processes might be observed.

The measurements were made using an enclosed cell with a nitrogen ambient. A large platinum block which supported the device served as both an electrical contact and a thermal mass. The block was heated by a heater cartridge powered by a variable autotransformer. A chromel-alumel thermocouple was spot-welded to the platinum block adjacent to the sample. Temperature was monitored by an *X-Y* recorder which also monitored the current via a Keithley Model 610 electrometer-amplifier. Bias was provided by a constant voltage source. The heating rate was adjusted so that the temperature interval from 25° to 300°C was covered in 8 min. In most instances, preconditioned devices were used for the measurements. This treatment, which improved reproducibility of the data, was performed by placing the device adjacent to the one being measured, thereby providing a preliminary temperature cycle to 300°C without bias.

Figure 6 **Bias-temperature shifts occurring in MOS devices fabricated with and without phosphorus diffusion treatments.** *Specimens were n-type silicon, 5.3 ohm-cm. Contacts were aluminum.*



The current-temperature curves for P_2O_5 stabilized and unstabilized SiO_2 are shown in Fig. 7. Each curve represents the average of some three or four different devices. All of the measurements shown in the Figure were made on devices which had received the 300°C preconditioning. One first notes the striking asymmetry with bias polarity in the curves for the unstabilized oxide (Wafer #362). The polarization peak with positive bias is two orders of magnitude larger than that with negative bias. This large polarization current accounts for the previously described large negative shifts observed in the *C-V* transitions following bias-temperature treatment. Accordingly, since some polarization occurs with negative bias, one would expect a small positive shift in the corresponding *C-V* transition. A slight positive shift was observed for these devices, but this was attributed to a thermal effect since it could be produced without bias. The polarization peaks for the nonthermally conditioned devices were slightly higher than those for the conditioned ones and they were shifted toward higher temperatures. The second current increase, observed at temperatures above those of the polarization peaks, may be either a nonpolarizing conduction current or a very slow polarization.

The extraordinary stabilization effect of P_2O_5 on SiO_2 that was shown in the bias-temperature *C-V* measurements is again borne out in the current-temperature curves for wafer #355 (2150 Å phosphosilicate glass), which show markedly reduced polarization peaks. There seems to be very little difference between positive and negative biasing, indicating device symmetry. It is interesting to note that the current slopes for this wafer above 150°C are quite different for the heating and cooling portions of the curves. A closer match of these slopes is observed at high temperatures for the unstabilized oxide with either bias polarity. This difference for the stabilized oxides suggests that a slow polarization is taking place after the initial peak. If this is the case, one might expect instabilities to appear at higher temperatures with stabilized oxide. Furthermore, since the currents for both positive and negative bias appear to be equal in magnitude and

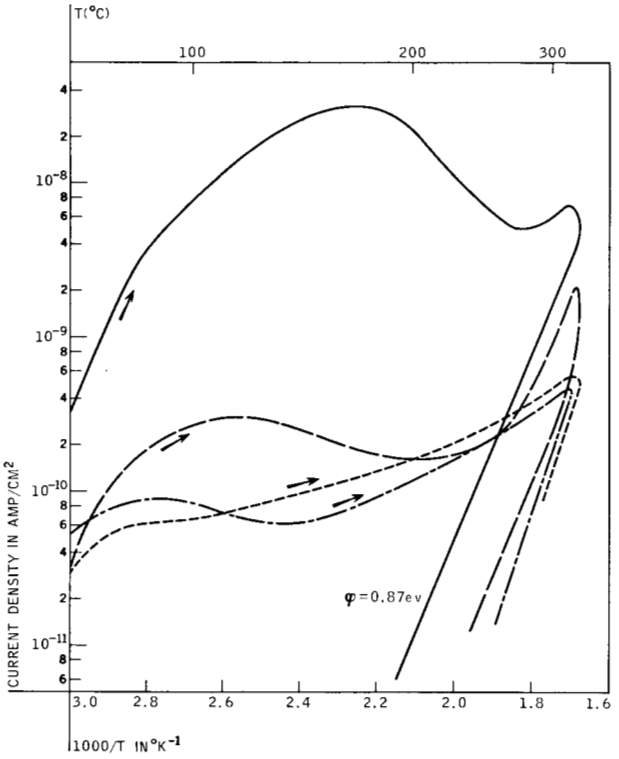


Figure 7 **Current-temperature behavior of stabilized and unstabilized MOS devices (arrows indicate temperature cycle).**

		Wafer
——— SiO_2	+30V	362
— — — SiO_2	−30V	362
— ·— • — P_2O_5 -SiO_2	+30V	355
---------- P_2O_5 -SiO_2	−30V	355

have the same temperature dependence, the high-temperature instability should also be expected to be symmetrical with bias. The bias-temperature *C-V* data of Fig. 6 shows no instability below 300°C, however. As shown in Fig. 7, all devices showed a fairly linear behavior of log I versus $1/T$ during the cooling period. The measured activation energy is approximately 0.9 eV.

A link between the current measurements and the *C-V* measurements can be had by comparing the total charge passed, as measured from integrated current, and $C\Delta V_{FB}$ for the *C-V* transition. A number of measurements were made on unstabilized MOS devices at 100°C using a bias of +30 V. Current was permitted to flow for various time intervals after which the device was removed from the cell and the *C-V* flat-band shift was measured. A comparison of the integrated current (Q_I) and the $C\Delta V_{FB}$ charge (Q_{CV}) is shown in Fig. 8. The oxide used was particularly unstable and, because of the large *C-V* shifts for the longer time intervals, a considerable amount of scatter was encountered. Much of this was due to the broadening of the *C-V* transition as well as its relaxation during measurement.

Q_{CV} includes only the charge which contributes to space-charge, whereas Q_I results from these displacement currents as well as currents which do not contribute to the *C-V* shift. Thus Q_{CV} must always be less than or equal to Q_I. During the first 40 or 50 min, Q_{CV} is very nearly equal to Q_I in Fig. 8, indicating that nearly all of the current flow consists of the polarization currents. The linear increase in Q_I after this time represents a steady-state current which does not produce space charge. Figure 8 indicates that the *C-V* shift reaches a limiting value in a time determined by the polarization rate.

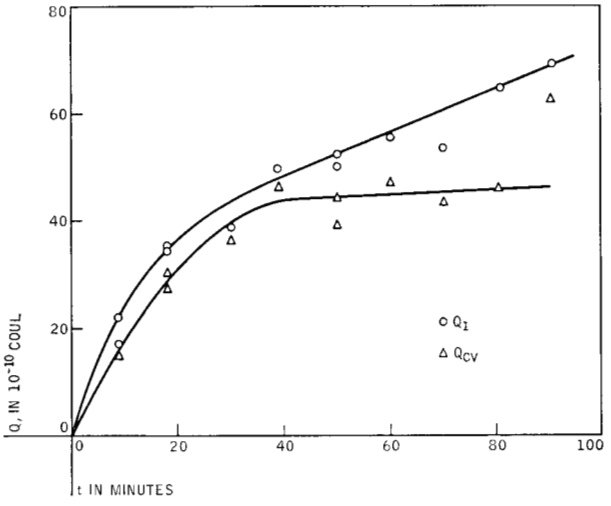
Conclusions

A variety of independent experiments have led to the conclusion that the presence of a phosphosilicate layer over the Si-SiO_2 system has a remarkable stabilizing effect on the electrical properties of the insulator and the insulator-silicon interface. As a consequence of these effects, the surface-controlled properties of junctions are also stabilized. Ing et al.[19] have reported improved stability of silicon planar diodes after gettering treatments with P_2O_5 applied directly to the backs of silicon wafers. Our experiments suggest that their treatment, in addition to gettering impurities from the silicon, created a phosphosilicate layer over the SiO_2 passivated junctions, with resultant improved stability.

The principal pieces of evidence which summarize our experiments are:

1. Severe instability is observed in planar junction transistors with reverse-bias and elevated temperature, when

Figure 8 **Comparison of Q_I and Q_{CV}.** *Wafer #362. Unstabilized SiO_2; T = 100°C; bias = +30 V.*



the phosphosilicate layer has been deliberately removed. This is contrasted to the insensitivity to stress of transistors which are identical in all respects except for the presence of the phosphosilicate layer.

2. Specially developed chemical etching techniques have made possible the physical detection of the phosphosilicate layer and measurement of its thickness. This measurement has shown good correlation between device failure and the absence of a phosphosilicate layer.

3. MOS capacitance measurements before and after bias-temperature stress show that the presence of a phosphosilicate layer inhibits the apparent build-up of positive space charge near the insulator-silicon interface up to temperatures of the order of 400°C.

4. Electrical conduction through MOS devices, with the electric field directed toward the silicon, has been found to be far smaller with the phosphosilicate layer over the SiO_2 than without it.

These experiments have shown the stabilizing effects of phosphosilicate layers ranging in thickness from 700 to 4300 Å. We have not measured the phosphorus concentration of all of these layers nor have we attempted to systematically vary this concentration. Although it appears that the stabilizing effect is rather insensitive to the concentration and/or thickness, it is quite probable that there are limits to these variables. These limits remain to be established by further experiments.

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