A. J. Anello
A. C. Ruocchio
W. D. Van Gieson, Jr.

A New Digital Method of Bit Synchronization Derived from an Analog Theory

This paper discusses a new method of bit synchronization derived from an analog theory to solve the problems involved in receiving a serial train of bits from a remote data communication source. Test results show that accurate frequency and phase information can be derived from the received serial data. The Analog Derived Clock to accomplish this bit synchronization is described, and applications in two-wire (half duplex operation) and four-wire (full duplex operation) communication systems are discussed. Speeds up to 2 Mc/sec using existing digital circuit technology were achieved. The special advantage of the Analog Derived Clock over present clocking techniques is an increase in speed and a reduction in circuitry.

Introduction

The new timing source described in this paper was designed for high-speed data transmission equipment. In all communication systems there exists a clock that decides when a new bit is to be placed on the transmission line. This results in a period for each bit, be it MARK or SPACE (ONE or ZERO), that is theoretically the same. Distortion introduced by the elements of a total system will cause these periods to be longer or shorter than the theoretical length.

At the receiver there exists an optimum time for sampling the line to decide whether the received bit is a ONE or a ZERO. In data transmission systems this time is a fraction of the total bit time and is confined to an area around the center of the bit.

Present communication systems use a digital counting system to maintain this optimum sampling time. An examination of present digital clocking techniques using existing technology showed the speed to be limited to about 200 kilobauds. Therefore, in view of potential improvements in communication facilities, it was evident that improved clocking techniques would ultimately be required. It was decided that a clocking system with a maximum speed capability of about 2 Mc/sec should be sufficient to satisfy both present and future needs of data communications.

This proposed clock must perform as well as present clocking systems, that is, with respect to operation in the presence of dc bias distortion, ac jitter, frequency variations and noise.

Position of strobe relative to transition time

A method of sensing the position of the *receive strobe time** is obtained from the following analysis:

When the received data line changes from a MARK to a SPACE condition, the signal is integrated to generate a ramp. At the time of the receive strobe, the integration is ended, and the level that has been accumulated is then held. When the received data line changes from a SPACE to a MARK condition, the line signal is integrated and added to the value reached on the first integration. At the next receive strobe, the integration is ended and this level is held. The accumulated level is now compared to a reference level. If the accumulated level is over the reference level, the strobe must be advanced in time; if it is under the reference level, the strobe must be retarded in time.

One of the major problems for the high-speed operation of the system just described is the necessity of comparing

* The receive strobe time occurs at the negative transition of the clock signal.

levels and of resetting the final accumulated level before the next MARK-to-SPACE transition occurs.

A method of resetting the accumulated level is to subtract a similarly integrated signal that is character-related to the incoming signal. This character-related signal is generated by a one-bit memory buffer (receive line trigger) which stores the contents of the received data line and changes state, as required, at each strobe time. It is now possible to use this relatively distortion-free signal to derive the required character-related integration.

Figure 1 illustrates this approach for the undistorted and zero-phase-error condition. "Zero phase error" means that the strobe time occurs at the exact center of the incoming data bits. The integrated line trigger represents the character-related level that is subtracted from the integrated data signal received. These two signals are combined to form the sum signal.

Figures 2 through 9 show similar relationships for all the possible combinations of distortion and phase error conditions.

Each of the sum signals, shown in Figs. 1 through 9, has a reference level error which varies with bit pattern. In addition, those in Figs. 2, 3, 4, 5, 7, and 8 exhibit an increasing or decreasing reference level error as a function of time.

Correction signal

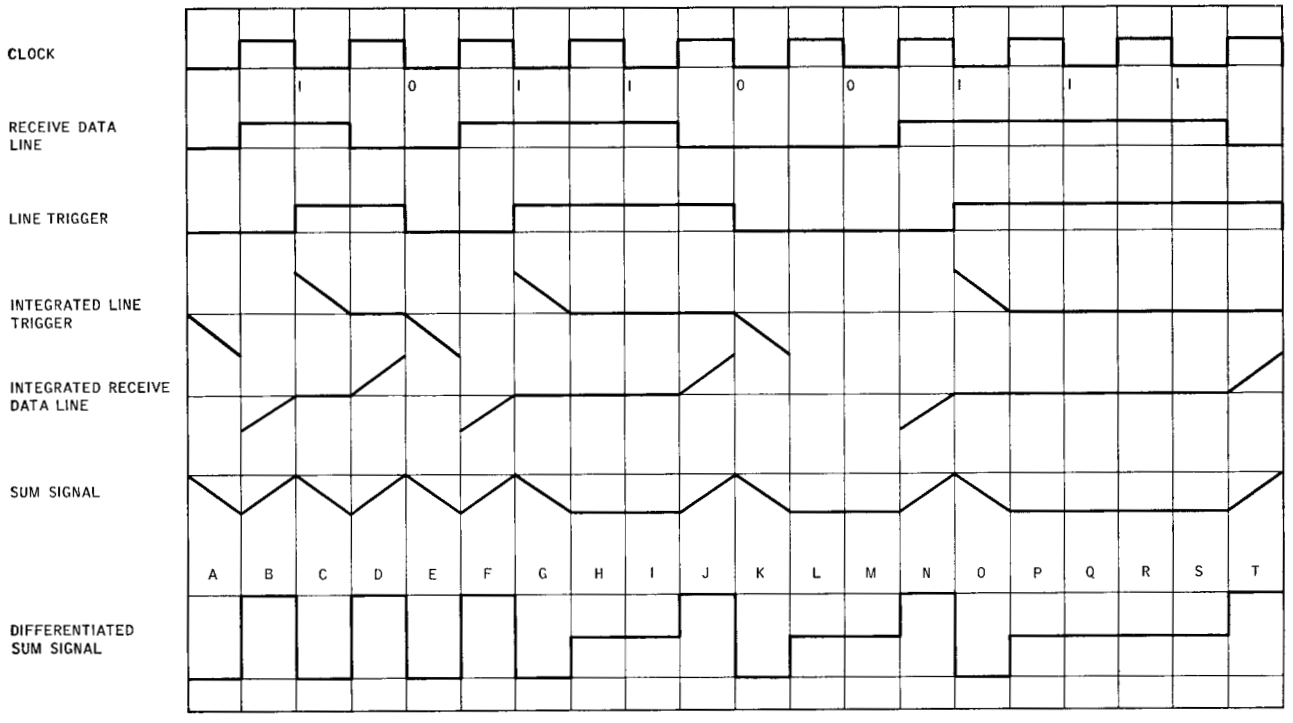
Many methods of combining integrated line trigger signals and integrated receive line data signals have been tried, and all have introduced problems because of varying reference level with bit sequence.

If the sum signal is differentiated (Figs. 1 through 9) the undesirable level is removed. The differentiated signal, when filtered to remove high-frequency components (data fundamental frequency and its harmonics), will produce a signal which varies in value about a fixed zero reference. This signal contains accurate correction information and will be referred to as the *correction signal.*

The correction signal contains the information which dictates the direction and amount of phase correction necessary to align the receive strobe for reliable sampling of the received data line. The correction signal for a centered strobe condition has a zero average value. A condition with the strobe left of center produces a negative average value, and with the strobe right of center, a positive average value. This information will permit the alignment of the receive strobe by a frequency correction to the receive oscillator.

(*Figures 2 through 9 appear on the following four pages. The text is continued on page 324.*)

Figure 1 **Clocking technique for deriving optimum sampling time. Data condition for one = zero in time, clock centered.** (*Figures 2 through 9 show similar relationships for all combinations of distortion and phases error conditions.*)



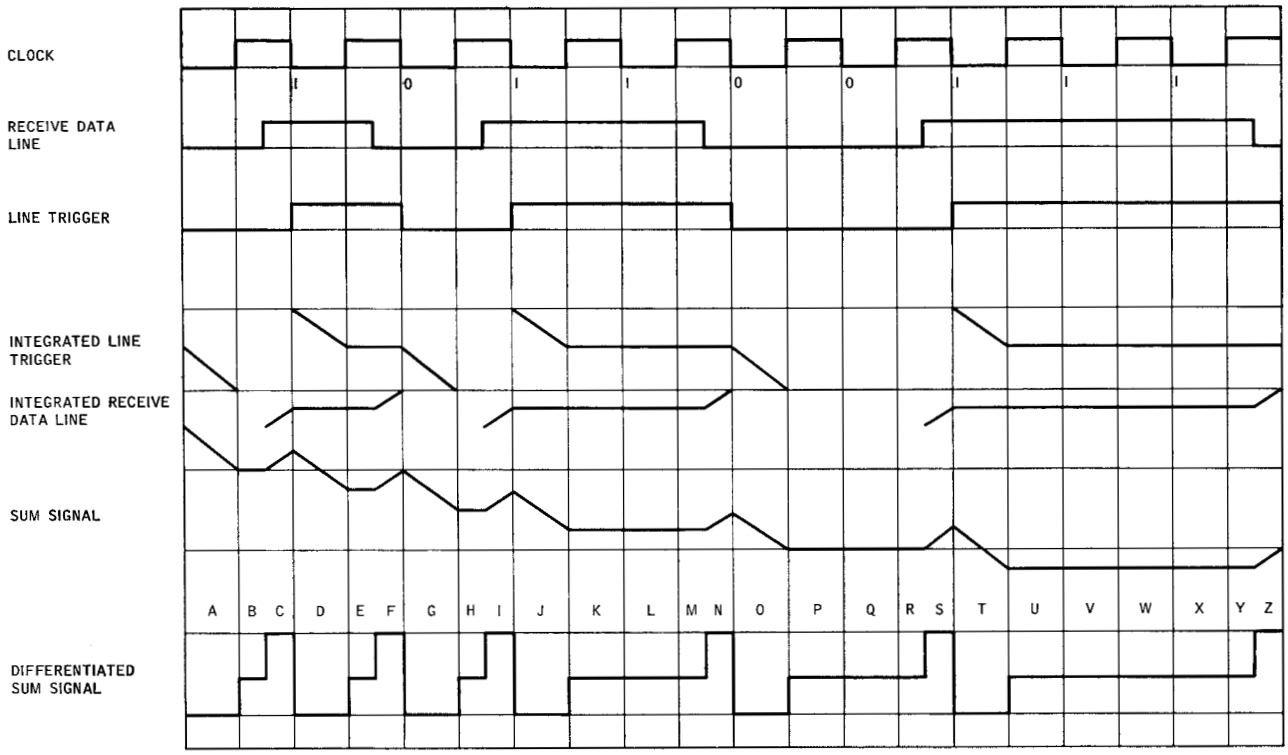
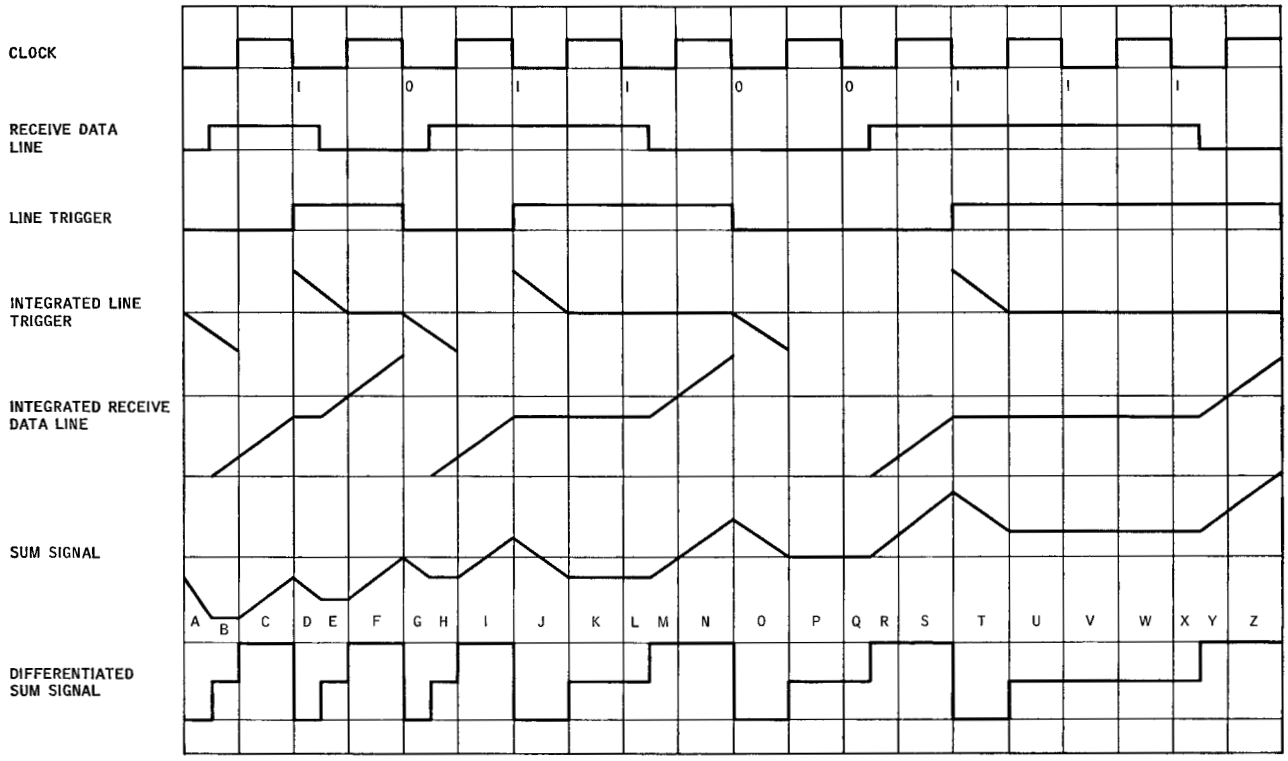


Figure 2 **Possible data condition: Clock to left, one = zero in time.**

Figure 3 **Possible data condition: Clocked to right, one = zero in time.**



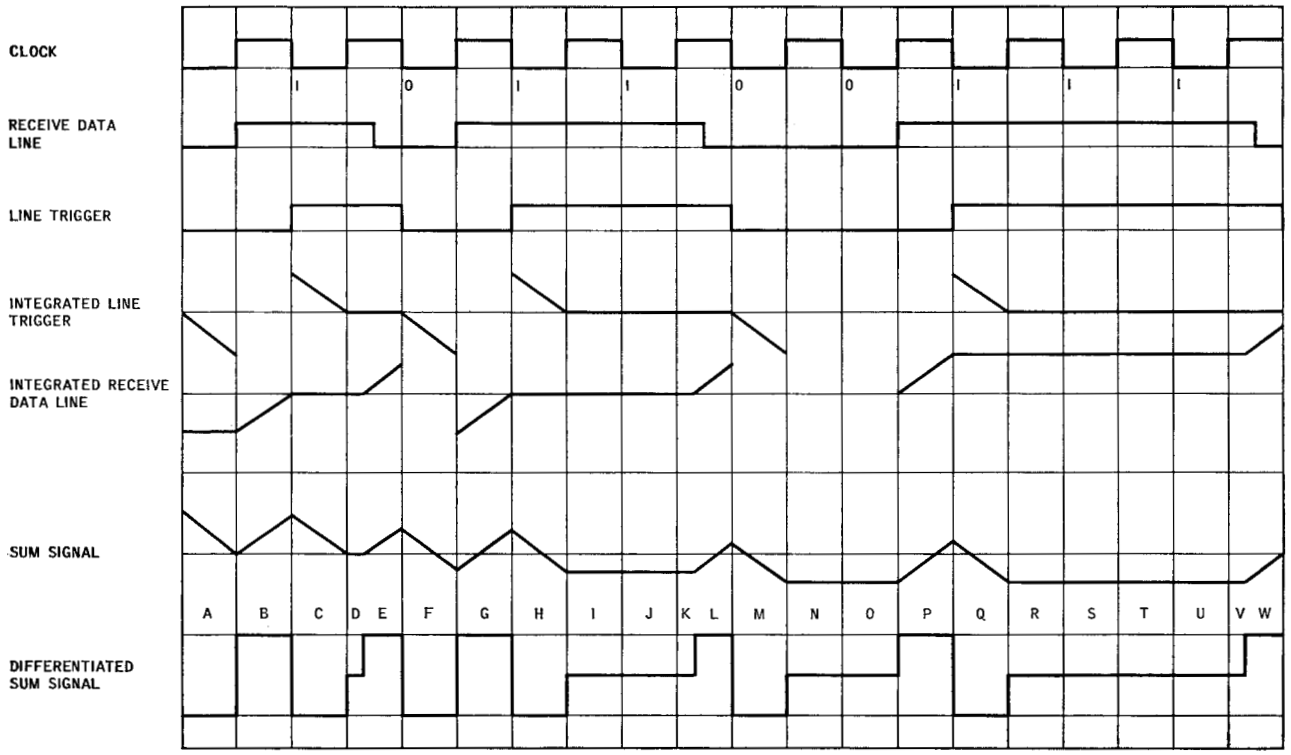
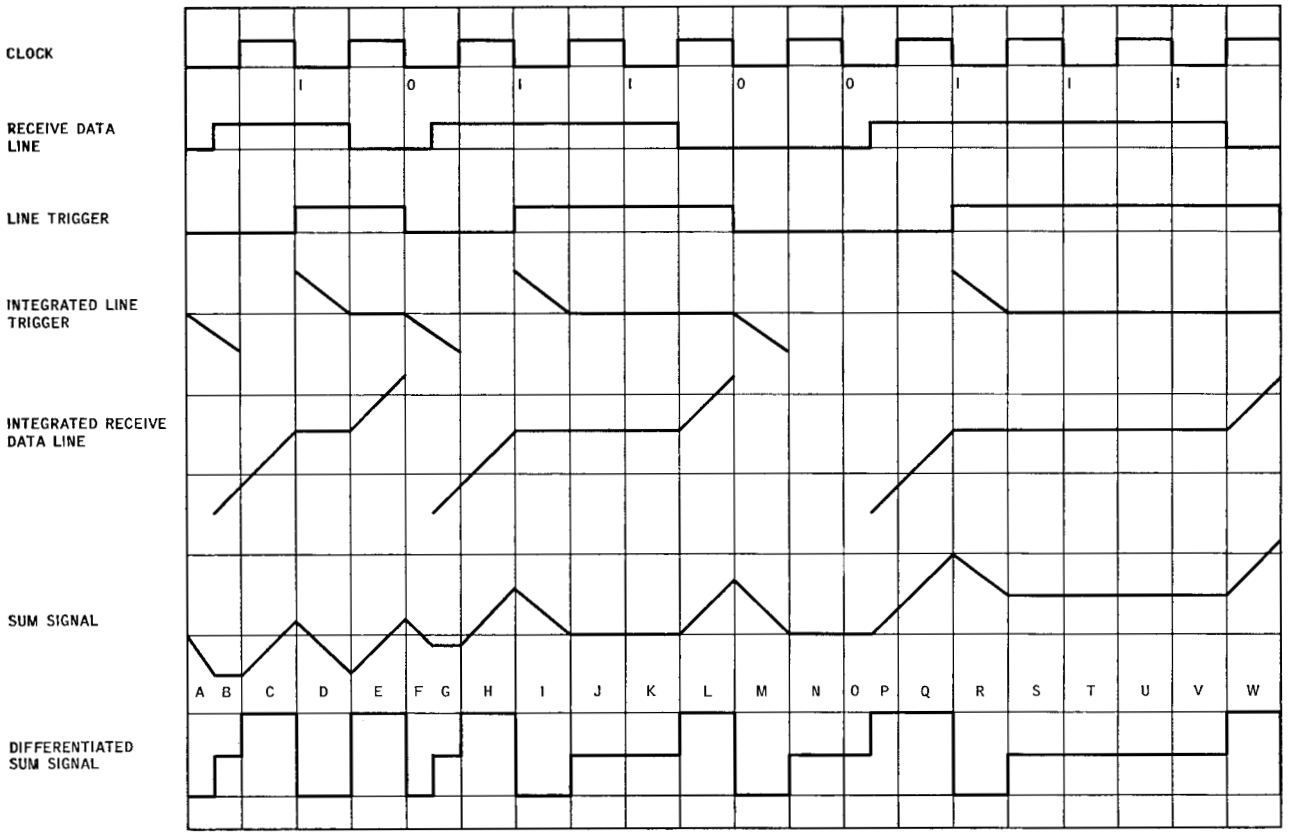


Figure 4 **Possible data condition: Clock to left, one > zero in time.**

Figure 5 **Possible data condition: Clock to right, one > zero in time.**



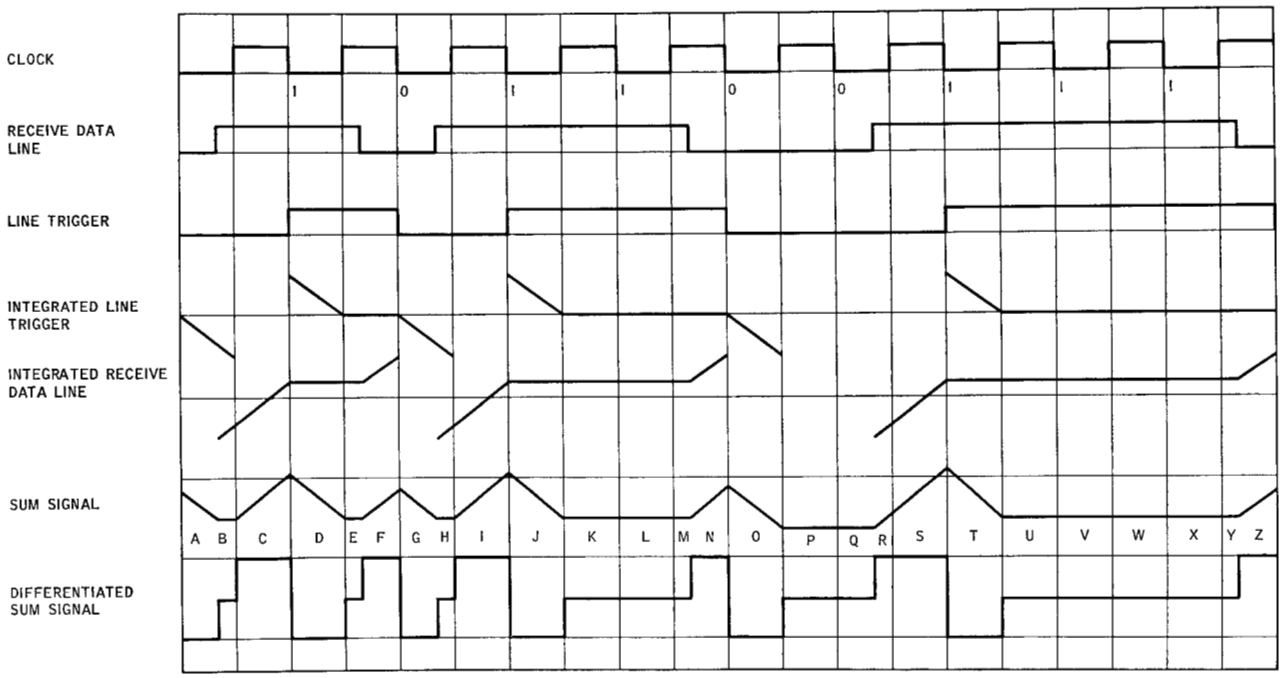
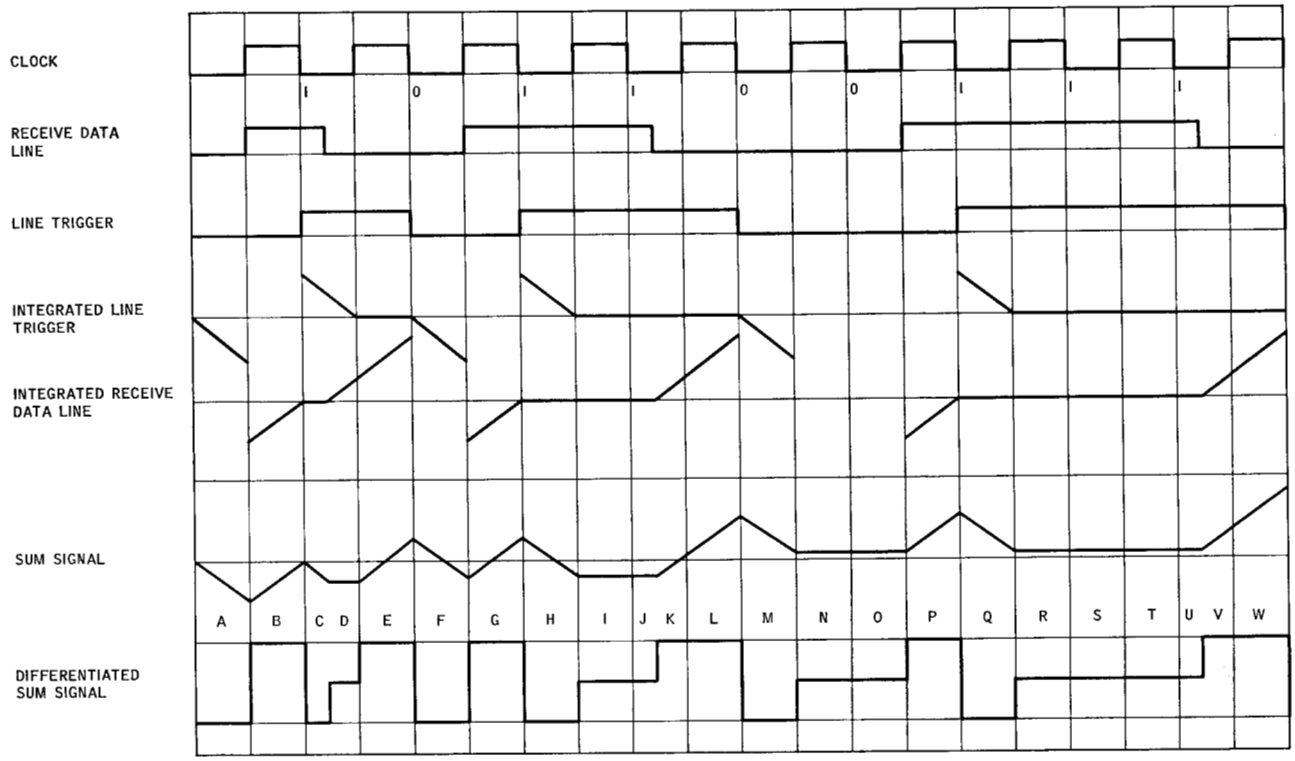


Figure 6 **Possible data condition: Clock centered, one > zero in time.**

Figure 7 **Possible data condition: Clock to right, one < zero in time.**



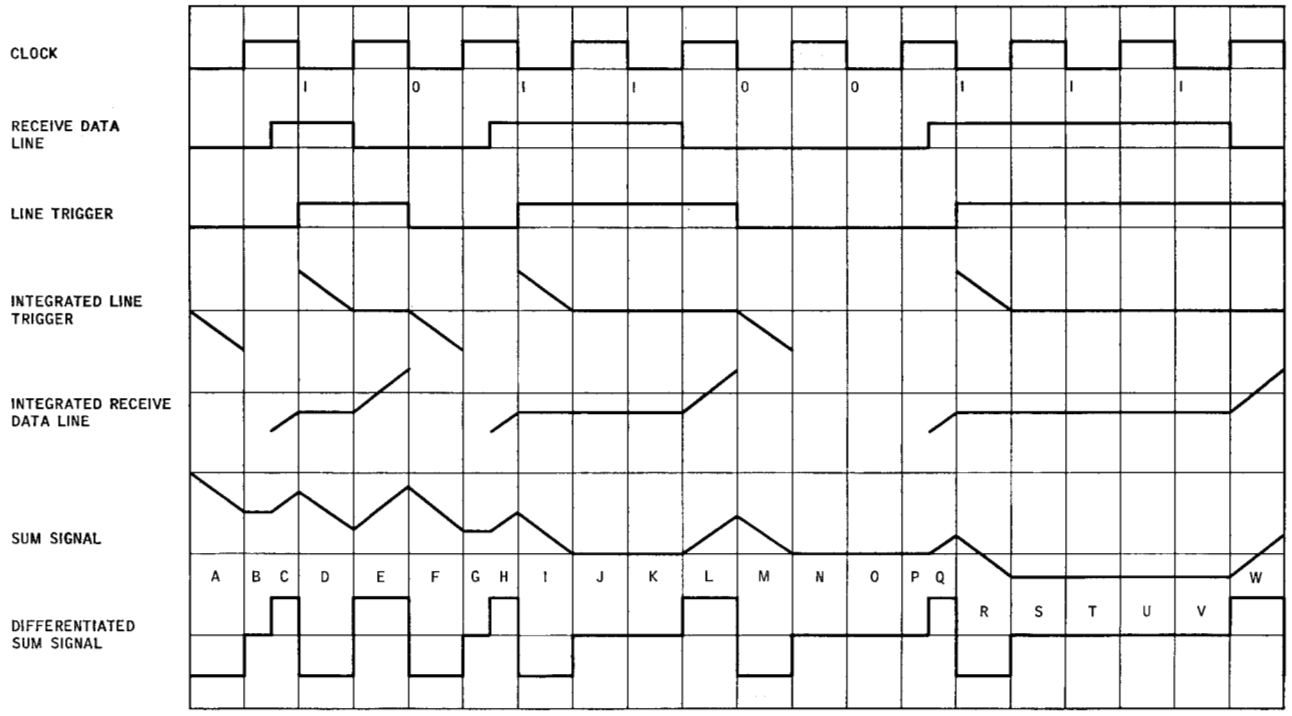
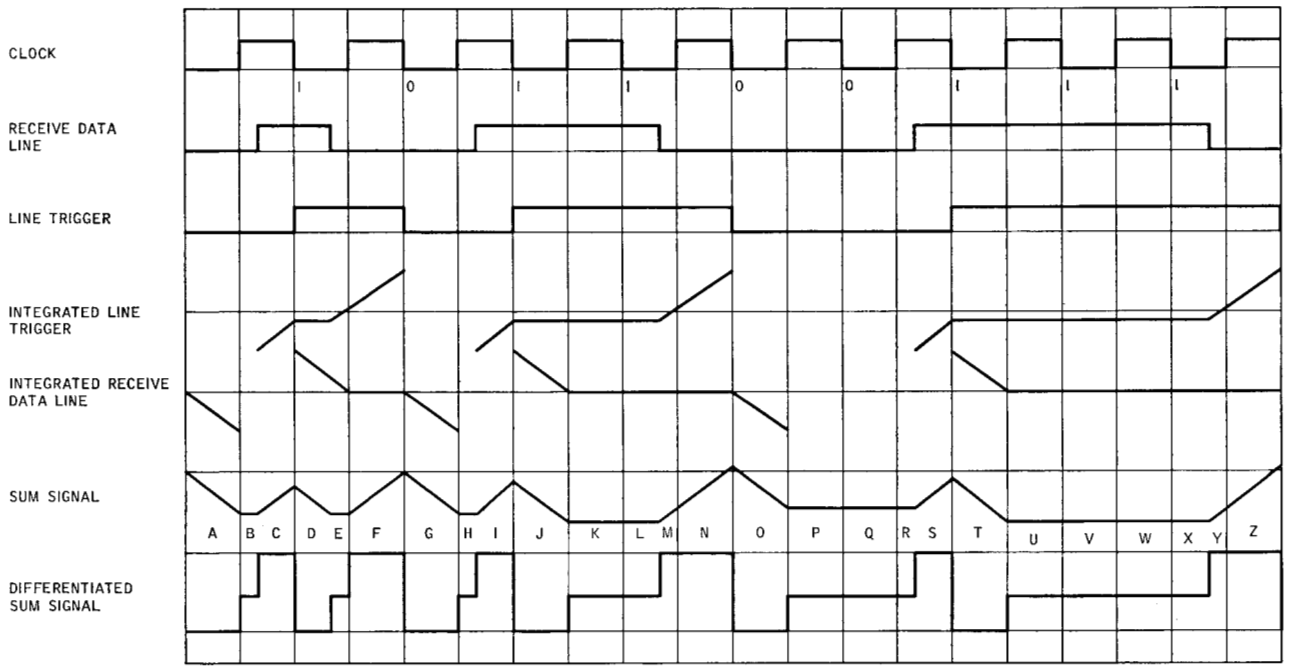


Figure 8 **Possible data condition: Clock to left, one < zero in time.**

Figure 9 **Possible data condition: Clock centered, one < zero in time.**



The three possible receive strobe positions with respect to the optimum sample time (strobe position leading, coincident with, or lagging, the optimum sample time) combined with the three possible conditions of dc bias distortion (the ONE bit time greater than, equal to, or less than the ZERO bit time) give the nine possible conditions shown in Figs. 1 through 9. For a given clocking system to operate properly the system must give a consistent correction signal for every possible condition. When Figs. 1 through 9 are examined it becomes evident that the differentiated sum signal (correction signal) is consistent and will give useful correction information for all conditions.

Theoretical system

If the frequency of the receive oscillator and the frequency of the received data are not identical, the average value of the correction signal will be a serrasoid which has a frequency equal to the difference between the frequency of the received data and that of the receive oscillator. The slope of this serrasoid is determined by the sign of the frequency difference. When the correction signal is used to correct the frequency of the receive oscillator, the slope of the correction signal will tend toward zero (dc). Figure 10 is a block diagram of the analog device.

This system can theoretically produce a signal capable of correcting the receive strobe. A closer look at the analog signals of Figs. 2, 3, 4, 5, 7 and 8 shows that they may increase in amplitude continuously towards infinity. Generating the correction signal in the analog manner indicated in Fig. 10 would be physically impossible.

Practical system

By examining the status of the received data line, the line trigger, the received clock and the desired correction signal, it is possible to generate sequential truth tables and state diagrams for each of the sequences *A*, *B*, *C*, etc., of Figs. 1 through 9. State diagrams for all possible line conditions which have been shown in Figs. 1 through 9 were individually constructed, and were then combined and simplified to that shown in Fig. 11.

Thus it is possible to generate the desired differentiated signal and hence, the correction signal, through combinatorial logic rather than analog circuitry. An example of this logic is shown in Fig. 12. Note that only one state memory element is required.

The outputs of the detector logic are + VOLTAGE ON PLUS and — VOLTAGE ON MINUS. These outputs of opposite polarity are of equal absolute magnitude. The presence of the + VOLTAGE ON PLUS signal indicates the positive portion of the correction signal. The presence of the — VOLTAGE ON MINUS indicates the negative portion of the correction signal. The absence of both signals indicates the zero portion of the correction signal. These two signals contain all the information required to generate the correction signal for each case, as shown in Figs. 1 through 9.

Once the correction signal has been developed it can be used to correct the frequency and phase of the receive strobe.

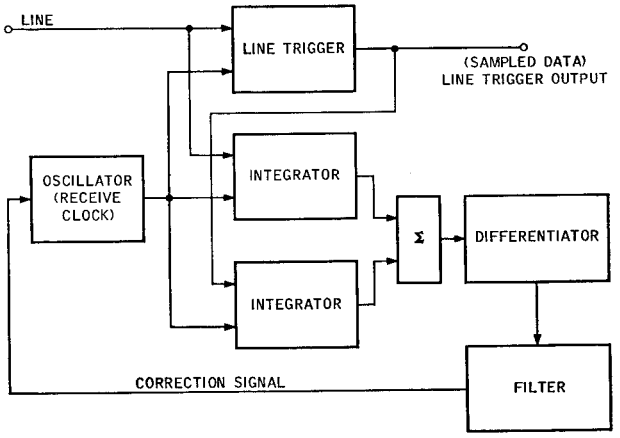
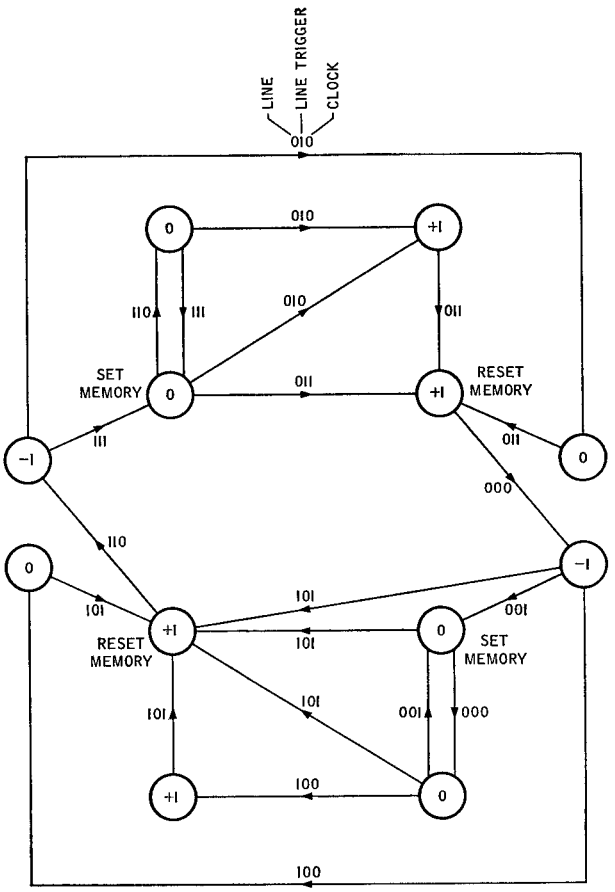


Figure 10 **Theoretical system.**

Figure 11 **Simplified composite state diagram.**



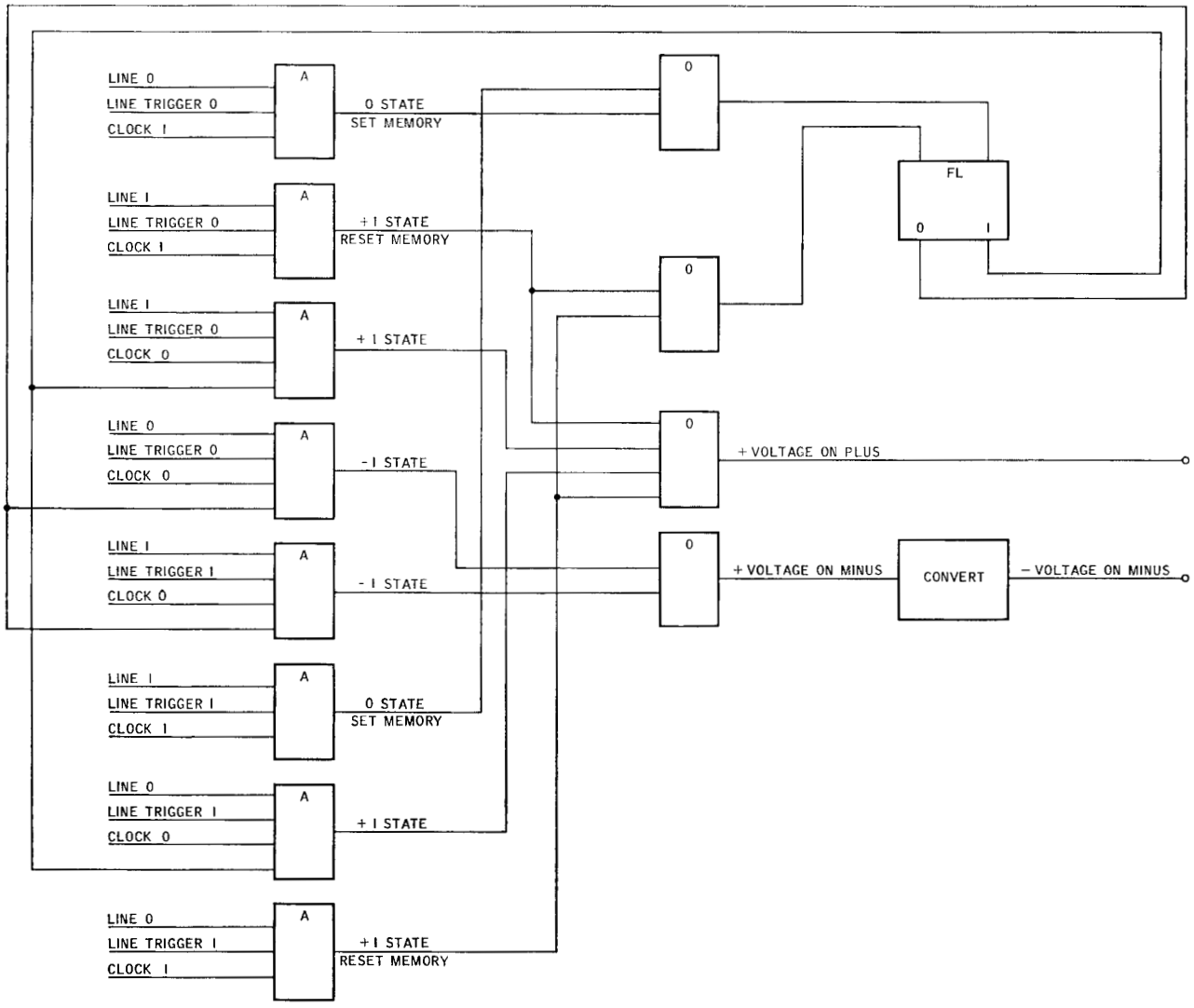


Figure 12 **Detector logic to obtain component parts of differentiated sum signal.**

The phase error as shown in Figs. 2, 3, 4, 5, 7, and 8 may be corrected by introducing a change in phase. This is accomplished by causing a momentary frequency change to the receive oscillator. A detected frequency error may be corrected by adjusting the frequency of the receive oscillator.

Frequency corrections fall into two general classes: with memory and without memory. With memory, the receive strobe frequency remains at the corrected value after the average value of the correction signal has returned to zero. An example of this would be a motor turning the tuning capacitor of an oscillator. Without memory, the receive strobe frequency returns to its original value when the average value of the correction signal returns to zero. An example of this would be a voltage-controlled oscillator in which the output frequency is controlled by an input voltage.

To achieve a frequency lock in a system without memory, the receive strobe will have to have a constant phase error. This phase error will produce the necessary correction signal to maintain a zero frequency difference.

A system without memory has been assembled as shown in Fig. 13 and has proven the validity of this theory. The system contains the following:

(1) A logical detector with two outputs.
(2) A noninverting precision mixer.
(3) Two low-gain amplifiers.
(4) A voltage controlled oscillator.

The feedback loop of the Analog Derived Clock is designed so that the correction signal amplifiers are opaque to impulse noise, which is defined for this application to be any noise spike whose duration is considerably less than one bit time. In addition, a noise burst affecting up

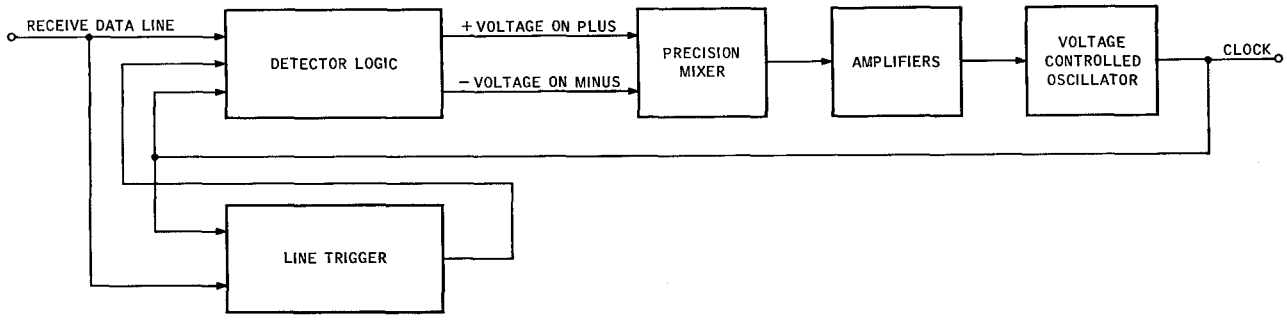


Figure 13 **Block diagram of system tested.**

to 20 bits will not cause the system to lose bit synchronization.

System use of the Analog Derived Clock

Although the Analog Derived Clock was originally intended for full-duplex operation, it was found that with modification to the using system, the same Analog Derived Clock could also be made to operate in half-duplex. A brief description of a typical systems application for these two modes of operation is given below. Thus any system using the Analog Derived Clock can be designed to be completely compatible with present low-speed, half- and full-duplex systems as well as future high-speed, full-duplex systems.

- *Full-duplex operation of the Analog Derived Clock*

Figure 14 is an example of full-duplex operation in which Terminal *A* is sending data to Terminal *B*, and Terminal *B* is sending idle and control characters to Terminal *A*, or vice versa.

To transmit data between the two terminals, the receiver of each terminal must establish bit synchronization and character framing with the transmitter of the opposite terminal. It is the function of the bit phase clock to establish and maintain this synchronization and framing. This is readily accomplished by using a crystal controlled oscillator in the transmit section of each terminal and an Analog Derived Clock (ADC) in the receiver section of each terminal.

In most cases there is no predetermined relationship between the phases of the transmit and receive strobes within the same terminal. Similarly, there is no requirement for any character phase relationship between the transmit section and the receive section of the same terminal. In fact, there is no necessity for the transmit and receive sections of a terminal to be operating at the same frequency.

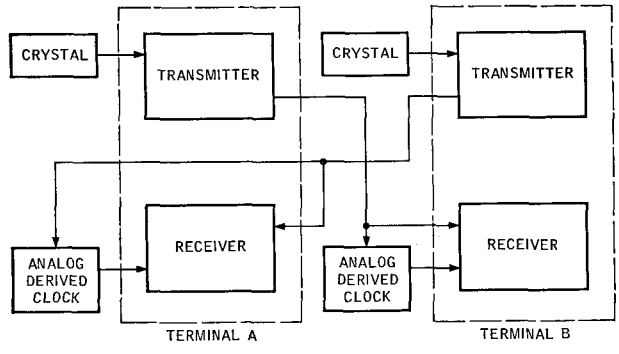
- *Half-duplex operation of the Analog Derived Clock*

The transmit clock is generated from a stable crystal oscillator of N times the actual transmit data frequency (f). The receive clock is generated from an ADC operating at N times the actual receive data frequency. For this discussion it is assumed that the speed of operation for the transmit and receive terminals is identical. Each oscillator frequency is counted down in separate counters by a factor of N. When phase and frequency synchronization are being established, the terminal that is receiving will correct its receiver's ADC until proper phase and frequency lock have been achieved. During this time its transmitter will run free. When the terminal that has been receiving becomes a transmitter, a dummy line signal and a dummy line trigger signal are generated from its own transmit crystal. These two signals in conjunction with a dummy clock signal obtained from the Analog Derived Clock will allow the receiver to maintain the phase information already obtained from the line and will change only with changes in the frequency of the transmit crystal.

While a terminal is receiving data records, its transmit clock could lose the proper phase relationship as a result of crystal drift. To prevent this, the transmit count-down in the receive terminal will be driven from its own ADC (Fig. 15).

While a terminal is sending data records, the receive count-down of the ADC at that sending terminal is under

Figure 14 **Full-duplex operation.**



the control of its own transmit crystal (Fig. 15). The crystal in the transmit terminal is controlling everything with respect to frequency and phase except the natural frequency of the receiving terminal's transmit crystal.

Line turn-around and line interruptions are recognized so that all frequency and phase information control in each terminal is switched to its own transmit crystal (see Fig. 16).

Test results

Once the feasibility of the Analog Derived Clock was established, more extensive testing was begun to determine the limits of performance. The results of this testing can be summarized as follows:

- *Clock testing*

An initial frequency deviation of 10% from the nominal operating frequency was synchronized by the ADC.

Frequency synchronization was established and maintained with only two transitions per eight-bit character. This was the minimum number of transitions attainable in the laboratory test.

Analog Derived Clocks were operated in the laboratory at many speeds up to and including 2 Mc/sec. It is interesting to note that this entire speed range was achieved by a simple substitution of four passive components.

- *System test*

For this testing a Data Communication Unit was modified to include an Analog Derived Clock capable of half- and full-duplex operation.

1) *Operation of the Analog Derived Clock in the presence of dc bias distortion.*

By introducing definite amounts of bias distortion* it was found that the clock would operate with the following percent distortion for each speed range. Distortion test was limited to these values by the machine on which the clock was installed.

Speed range	*Bias distortion*
Up to 200 kilobauds	40%
200 kilobauds to 1.5 megabauds	30
1.5 megabauds to 2 megabauds	20

2) *Communications line testing*

The Analog Derived Clock was tested over presently available communication facilities, both half- and full-duplex.

Successful reception and transmission of data were achieved with several IBM TELEPROCESSING® Data Communication Units.

Summary

It has been shown that the Analog Derived Clocking method is capable of deriving and maintaining accurate clocking information from serial data that has been subjected to distortion in excess of that encountered on present common-carrier facilities.

The Analog Derived Clock is capable of operating at speeds one to two orders of magnitude greater than present digital techniques.

* Bias Distortion: Defined in *Principles of Electricity Applied to Telephone and Telegraph Work*, American Telephone and Telegraph Co., 1961 Ed., p. 97.

Figure 15 **Half-duplex operation.**

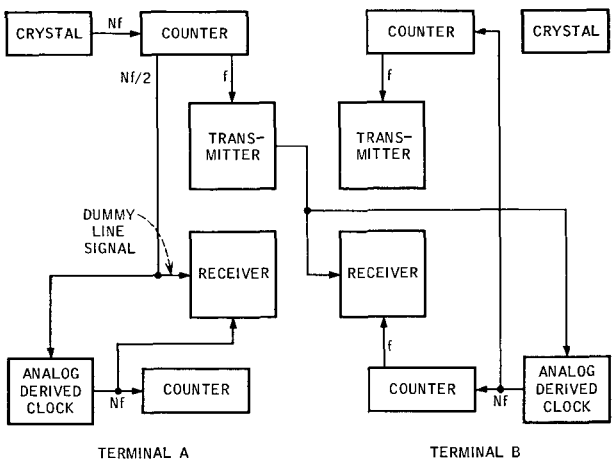
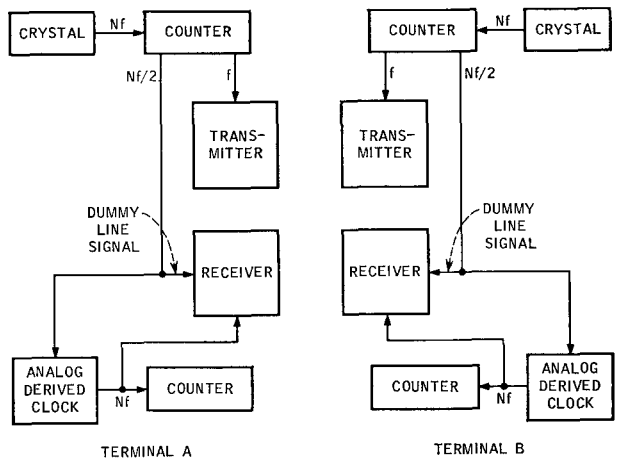


Figure 16 **Half-duplex operation during line turn-around or line interruption.**



These results were accompanied by a reduction in circuitry.

Throughout this paper applications to data communication have been assumed. It should be noted, however, that this particular clocking system can easily be adapted to synchronize any serial data source.

ADC-equipped communication systems are compatible with digitally clocked communication systems.

Acknowledgments

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