# Directional Coupling and its Use for Memory Noise Reduction

The coupling between a bit line and its adjacent sense line in a word-organized memory array is a phenomenon of considerable concern to the memory designer. In many cases, the bit noise induced in the sense line during a WRITE cycle is sufficiently large to saturate and block the sensitive sense amplifier if steps are not taken to minimize the effects of the bit-sense coupling. This Communication presents a method for directing this noise away from the input terminals of the sense amplifier by utilizing the inherently directional properties of the coupling between two parallel transmission lines.

The crosstalk between a bit or digit line and its adjacent sense line in a word-organized (two-dimensional) magnetic core or flat film memory array can be of sufficient magnitude to affect seriously the operational characteristics of a particular memory. In order for the sense line and bit line to couple efficiently to the memory cells, it is generally necessary to place them in close proximity to the cells and, as a consequence, the lines lie closely parallel to each other for a considerable distance. During a WRITE cycle, a large current is introduced into the bit line. As a result, a large signal is induced in the sense line which may be several times greater in magnitude than the READ signal from the memory cell. This induced signal can be suffi-

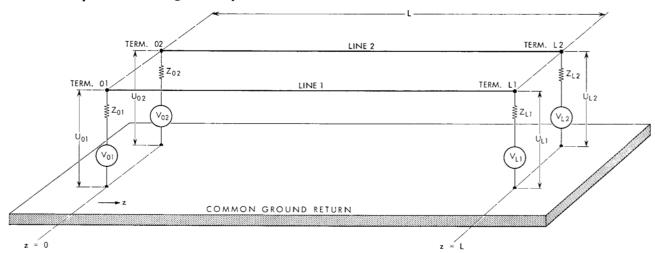
ciently large to saturate the high-gain sense amplifier and cause it to block for a relatively long period of time. It may be necessary, therefore, to provide a sufficient time delay between a write cycle and a read cycle to permit the sense amplifier to recover. As a result a significant reduction in the access time of the memory system may be necessary. Many techniques have been devised to minimize the effects of the bit-sense coupling.<sup>1,2</sup> The method described here utilizes the basic properties of the electromagnetic coupling between any two parallel TEM mode transmission lines.

## Interaction between parallel transmission lines

Consider the symbolic diagram given in Fig. 1, where two transmission lines of arbitrary cross-section are placed parallel to each other for a distance L, and are terminated to a common ground return with arbitrary impedances and generators at each of the four terminal points. If it is assumed that:

- 1) there are no conductor or dielectric losses,
- 2) the dielectric is homogeneous and isotropic,
- 3) the only mode of propagation is the TEM mode, i.e.,

Figure 1 Symbolic drawing of two parallel transmission lines.



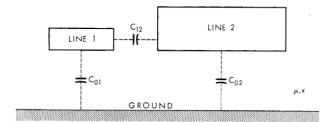


Figure 2 A typical cross-section of two parallel transmission lines showing three capacitances which can be used to fully characterize the structure.

the frequencies of interest are below the cutoff frequencies of the next higher modes, and

4) there are no variations in the cross-sectional geometry in the coupling region,

then Eqs. (1a-1d), page 255, will fully characterize the interaction<sup>3</sup> between the two lines of Fig. 1. It is important to note that no restrictions have been placed on the actual shape of the cross-section and hence these expressions are valid for any three-wire structure which meets the preceding assumptions. (The ground return is considered to be the third wire). The velocity of propagation, v, is determined by the physical constants of the dielectric material and is equal to  $1/\sqrt{\mu_{\rm E}}$ . The three parameters  $C_{01}$ ,  $C_{02}$ , and  $C_{12}$  are three capacitances per unit length whose physical significance can best be seen by referring to Fig. 2. The parameters  $C_{01}$ ,  $C_{02}$ , and  $C_{12}$  can be measured with a capacitance bridge or in certain special cases can be determined by direct analysis of the structure.

### Properties of the interaction

It is now worthwhile to examine some of the properties which can be determined from Eqs. (1a) through (1d). It will be assumed that only a single generator is present, that is,  $V_{01} = V(t)$  and  $V_{L1} = V_{02} = V_{L2} = 0$ . It is well known that, in general, the coupling between two transmission lines is directional, that is, the energy coupled from one transmission line to the other does not equally divide between the two terminals of the coupled line.4 Of particular interest is the situation where the coupling is unidirectional. In the case of TEM structures unidirectional coupling occurs in the backward direction, that is for  $V_{01} = V(t)$ ,  $U_{L2} = 0$  and  $U_{02} \neq 0$ . This case is commonly called backward coupling. The term infinite directivity is often used to refer to the case when  $U_{L2} = 0$ , where directivity is defined as 20 log  $U_{L2}/U_{02}$ . If Eqs. (1a) through (1d) are solved for  $U_{L2}$  then it is found that  $U_{L2} = 0$  and  $U_{02} \neq 0$  if Eq. (2) is satisfied. Note that this relationship is frequency independent and that only the physical parameters of the transmission line crosssection  $C_{01}$ ,  $C_{02}$ ,  $C_{12}$ , and v appear in it. This is a most

important result, since it states that none of the energy coupled from Line 1 (with the voltage source at Terminal 01) to Line 2 will be observed at Terminal L2 if Eq. (2) is satisfied. Since the conditions for  $U_{L2}=0$  are frequency independent, this effect will occur for any  $V_{01}=V(t)$ , whether a steady-state sine wave or a pulse excitatation is used. Note also that no assumptions were made with respect to the length of the coupling region as compared to the wavelengths of the frequencies of interest. Therefore, Eq. (2) is valid over any frequency range in which Assumptions 1 to 4 are reasonable.

It is often desirable to know the input impedance of a transmission line structure so that the generator impedance can be matched to the line for maximum power transfer or minimum reflections. In the case of pulses, it is desirable to have this impedance real and independent of frequency. If Eqs. (1a) through (1d) are solved for  $U_{01}$  and  $U_{01}$  set equal to  $V_{01}/2 = V(t)/2$  (which is the case of a perfect match) then one set of conditions which will give a frequency independent solution is given in Eqs. (2) and (3a) through (3c). Note that for a frequency-independent input impedance, infinite directivity is also obtained. One can infer from these equations that the values of  $R_1$ and  $R_2$  are equal to the characteristic impedances of Lines 1 and 2 respectively in the presence of each other when only one excitation is present, i.e.,  $V_{01} \neq 0$  and  $V_{L1} =$  $V_{02} = V_{L2} = 0$  or  $V_{02} \neq 0$  and  $V_{01} = V_{L1} = V_{L2} = 0$ , et cetera. Utilizing this definition of the characteristic impedance of the lines,  $Z_1 = R_1$  and  $Z_2 = R_2$ , then reflection coefficients  $\Gamma_{02}$  and  $\Gamma_{L1}$  at terminals 02 and L1 for arbitrary terminal impedances  $Z_{02}$  and  $Z_{L1}$  can be found (Eqs. (4a) and (4b)). Solving these latter equations for  $Z_{02}$  and  $Z_{L1}$  give Eqs. (5a) and (5b). If infinite directivity is desired then Eq. (2) must be satisfied and as a result a relationship (Eq. (6)) between the two reflection coefficients can be obtained. Equation (6) shows that for infinite directivity the reflection coefficient at terminal 02 must equal the negative of the reflection coefficient at terminal L1. Therefore, two of the many sets of values of  $Z_{02}$ and  $Z_{L1}$  that will result in infinite directivity are the special cases where  $Z_{L1}$  is a short circuit and  $Z_{02}$  is an open circuit and vice versa.

One other special case is also of interest. This is the situation where the cross-sections of Lines 1 and 2 and their relationship to the ground return are identical, that is,  $C_{01} = C_{02} = C_0$ . Under these conditions another set of parameters may be used to characterize the structure. Referring to Fig. 3, if voltages  $V_1 = V_2 = V$  are applied to their respective lines simultaneously a new impedance can be defined. This impedance will be the common or even mode impedance,  $Z_{oe}$ , whose value is given in Eq. (7a). Similarly, if  $V_1 = -V_2 = V$ , a balanced or odd mode impedance,  $Z_{oo}$ , can be defined, whose value is given in Eq. (7b). The product of  $Z_{oe}$  and  $Z_{oo}$  is given in Eq. (7c)

and can be easily shown to be equivalent to Eq. (2), that is, the condition that will result in infinite directivity. It can also be shown that  $\sqrt{Z_{oo}Z_{oo}}$  is equal to the characteristic impedance of either line in the presence of the other.<sup>5</sup>

## Method of reducing crosstalk

It is now appropriate to consider a method by which the properties of electromagnetic coupling between parallel TEM transmission lines can be used to reduce crosstalk between the bit and sense lines in a word-organized memory. If the memory array is organized as shown in Fig. 4, where the bit drivers and sense amplifiers are placed at opposite sides of the array and the terminal impedances chosen so that infinite directivity is obtained on the sense line, then the noise coupled from the bit lines to their adjacent sense lines will be coupled only to the backward terminal 02 and no noise will appear at the sense amplifier input terminals, L2. Since a wide range of values of  $Z_{02}$  and  $Z_{L1}$  are possible for infinite directivity, there is considerable latitude available in choosing the specific values of  $Z_{01}$ ,  $Z_{L1}$ ,  $Z_{02}$ , and  $Z_{L2}$  to satisfy other operational re-

quirements of the memory array.

For example, in very fast memories it is often desirable to match the bit driver input impedance to the bit line impedance so that reflections will be minimized. In the case of equal cross-section bit and sense lines (i.e.,  $C_{01} = C_{02} = C_0$ ) then from Eqs. (3a) to (3c) the input impedance of

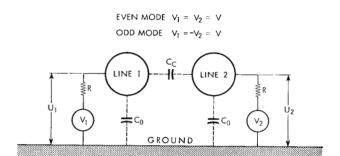
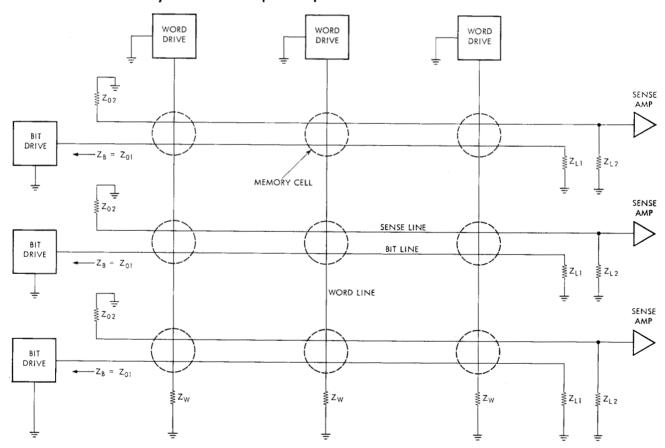


Figure 3 A typical cross-section of two parallel transmission lines with identical cross-sections and identical placement with respect to the ground return.

Figure 4 Arrangement of word-organized memory array so that noise coupled from bit line to sense line is directed away from sense amplifier input.



the driver,  $Z_B$ , and  $Z_{L1}$  and  $Z_{02}$  must all be made equal to  $\sqrt{Z_{oo}Z_{oe}}$ . The magnitude of  $Z_{L2}$  can be arbitrary, since no energy is coupled to it from the bit driver. With these values of  $Z_B$ ,  $Z_{L1}$ , and  $Z_{02}$  another problem arises. During the reading of the memory cell equal voltages,  $V_R$ , will be coupled to both the bit line and the sense line. These signals will see the even mode impedance,  $Z_{os}$ , since  $V_1 = V_2 = V_R$ . Voltages of amplitude  $U_R$  will propagate towards all four terminals of the bit-sense line combination and will experience a mismatch, since  $Z_B = Z_{L1} =$  $Z_{02} \neq Z_{oe} \neq Z_{L2}$ . The mismatch due to  $Z_{L2}$  can be easily eliminated simply by making  $Z_{L2} = Z_{os}$ . The effect of the mismatches at Terminals 01 and L1 will be reduced by the coupling factor K < 1 between the bit and sense lines. Therefore, the most significant effect will be that due to the mismatch at Terminal 02. The reflection coefficient  $\Gamma_R$  at Terminal 02 due to the cell output signal  $V_R$  is given by Eq. (8). It can be shown that for a pulse the maximum coupling factor  $K_{max}$  between the bit and sense line is given<sup>6</sup> by Eq. (9).  $K_{\text{max}}$  occurs when  $V_{01}$ has a rise time  $\leq 2L/v$ . The magnitude of  $\Gamma_R$  then is equal to the maximum coupling coefficient. Therefore, the size of the mismatch at Terminal 02 will only be significant when the bit and sense lines are strongly coupled.

For slower memories, where large multiple reflections can be tolerated but a low average input impedance to the bit lines is desired, then  $Z_{L1}$  can be set equal to 0 and  $Z_{02}$  can be made an open circuit. Infinite directivity will again be maintained and the input impedance of the bit lines, although time (or frequency) dependent, will rapidly approach zero within a time of the order of 2L/v.

Although in practice it is not possible to obtain the ideal result of  $U_{L2}=0$  because of losses, dielectric inhomogeneities, periodic loading by the memory cells and the word lines, et cetera, considerable reduction in the coupling between the bit line and the sense amplifier input in a word-organized memory array can be achieved. This technique has been tried in the laboratory with many types of memory array configurations, using both magnetic cores and thin films. In general, it has been possible to reduce the magnitude of the coupled signal by 20 db or more from what is usually experienced when the bit driver and sense amplifier are located at the same side of the array. In the case of the short-circuit, open-circuit combination, reductions as high as 60 db have been achieved.

### **Acknowledgment**

The author wishes to acknowledge the contributions of A. G. Franco (formerly of IBM Research) and A. Wasserman (of the IBM Data Processing Division) to the analytic material presented in this Communication.

# **Appendix**

$$V_{01} = \begin{bmatrix} 1 - jvZ_{01}(C_{01} + C_{12}) \cot \theta \end{bmatrix} U_{01}$$

$$+ [jvZ_{01}C_{12} \cot \theta] U_{02}$$

$$+ [jvZ_{01}(C_{01} + C_{12}) \csc \theta] U_{L1}$$

$$- [jvZ_{01}C_{12} \csc \theta] U_{L2}$$
(1a)

$$V_{02} = [jvZ_{02}C_{12} \cot \theta] U_{01}$$

$$+ [1 - jvZ_{02}(C_{02} + C_{12}) \cot \theta] U_{02}$$

$$- [jvZ_{02}C_{12} \csc \theta] U_{L1}$$

$$+ [jvZ_{02}(C_{02} + C_{12}) \csc \theta] U_{L2}$$
 (1b)

$$V_{L1} = [jvZ_{L1}(C_{01} + C_{12}) \csc \theta] U_{01}$$

$$- [jvZ_{L1}C_{12} \csc \theta] U_{02}$$

$$+ [1 - jvZ_{L1}(C_{01} + C_{12}) \cot \theta] U_{L1}$$

$$+ [jvZ_{L1}C_{12} \cot \theta] U_{L2}$$
(1c)

$$V_{L2} = -[jvZ_{L2}C_{12} \csc \theta] U_{01}$$

$$+ [jvZ_{L2}(C_{02} + C_{12}) \csc \theta] U_{02}$$

$$+ [jvZ_{L2}C_{12} \cot \theta] U_{L1}$$

$$+ [1 - jvZ_{L2}(C_{02} + C_{12}) \cot \theta] U_{L2}$$
 (1d)

where  $\theta = 2\pi f L/v$ , f = frequency, and  $v = 1/\sqrt{\mu\epsilon}$ .

$$(Z_{L1})(Z_{02}) = \frac{1}{v^2[C_{01}C_{02} + C_{12}(C_{01} + C_{02})]}$$
(2)

$$Z_{01} = Z_{L1} = R_{1}$$

$$= \frac{1}{v} \sqrt{\frac{C_{02} + C_{12}}{(C_{01} + C_{12})[C_{01}C_{02} + C_{12}(C_{01} + C_{02})]}}$$
(3a)

$$Z_{02} = Z_{L2} = R_{2}$$

$$= \frac{1}{v} \sqrt{\frac{C_{01} + C_{12}}{(C_{02} + C_{12})[C_{01}C_{02} + C_{12}(C_{01} + C_{02})]}}$$
(3b)

$$R_1(C_{01} + C_{12}) = R_2(C_{02} + C_{12})$$
 (3c)

$$\Gamma_{02} = (Z_{02} - Z_2)/(Z_{02} + Z_2)$$
 (4a)

$$\Gamma_{L1} = (Z_{L1} - Z_1)/(Z_{L1} + Z_1)$$
 (4b)

$$Z_{02} = \left[ (1 + \Gamma_{02})/(1 - \Gamma_{02}) \right] Z_2 \tag{5a}$$

$$Z_{L1} = [(1 + \Gamma_{L1})/(1 - \Gamma_{L1})]Z_1$$
 (5b)

$$\Gamma_{L1} = -\Gamma_{02} \tag{6}$$

$$Z_{oe} = 1/vC_o (7a)$$

$$Z_{oo} = 1/v(C_o + 2C_c) \tag{7b}$$

$$Z_{aa}Z_{aa} = 1/v^2 C_a (C_a + 2C_c) (7c)$$

$$\Gamma_R = -\frac{Z_{oe} - \sqrt{Z_{oo}Z_{oe}}}{Z_{oe} + \sqrt{Z_{oo}Z_{oe}}}$$
 (8)

$$K_{\max} = \frac{Z_{\circ s} - \sqrt{Z_{\circ o} Z_{\circ s}}}{Z_{\circ s} + \sqrt{Z_{\circ o} Z_{\circ s}}}.$$
 (9)

## References and footnotes

- 1. G. H. Goldstick and E. J. Klein, "Design of Memory Sense Amplifiers," IRE Trans. on Electronic Computers EC 11, 236 (1962).
- 2. C. Chong and G. Fedde, "Magnetic Films-Revolution in

Computer Memories," 1962 Proceedings of the Fall Joint Computer Conference, p. 220.

- 3. Equations (1a) (1d) are a rephrasing and extension of the analysis in: H. J. von Baeyer und R. C. Knechtli, "Ueber die Behandlung von Mehrleitersystemen mit TEM Wallen bei Hohen Frequenzen," Zeit. f. angew. Math. und Phys., 3, 271 (1952).
- 4. B. M. Oliver, "Directional Electromagnetic Coupling",
- Proc. IRE 42, 1686 (1954).
  S. B. Cohn et al., "Strip Transmission Lines and Components", Stanford Research Institute, Menlo Park, Calif., SRI Project 1114, Final Report, February 1957, pp. 45-50.
- 6. Unpublished report.

Received April 11, 1962