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Transient Analysis and Device Characterization of ACP Circuits

Abstract: Characterization of devices for high speed ACP (Advanced Circuit Program) circuits demands an accurate study of transients and switching delays. This paper describes (a) the large-signal transistor model evolved for the purpose of carrying out such an analysis; (b) methods of measuring device parameters with relevant theory; (c) computational techniques most adaptable; and (d) correlation between predicted and observed transients.

Many new ideas in the development of the device model, measurements, and computational procedure are reported and could be used for any general circuit analysis.

Introduction

Development of high-speed circuits requires detailed analysis of devices and of those properties that influence the transients, delays, and logic functions related to circuit switching operations. The main purpose of this analysis is to provide a thorough knowledge of factors responsible for limiting the speeds of practical circuits. Understanding well-defined parameters and their physical relationships to controllable factors in device design and fabrication provides potential optimization of circuits and devices. To attain this goal, the major steps required coordination of effort involving the device model, device parameters, measurements, and relationships of device parameters to actual circuit operations. This analysis is specifically related to ACP (Advanced Circuit Program) circuits where circuit and device efforts are combined and efficient coordination between circuit design and device fabrication is achieved.

The logical sequence of steps involved in the analysis is presented in Fig. 1. The major problems associated with the procedure were:

a) Availability of a sufficiently accurate model of the transistor for circuit analysis.

b) Consistent and reasonably accurate measurement techniques of device parameters which define or affect the transients and delays in ACP circuits.

c) Measurements and correct theoretical interpretations of nonlinearities in transistor parameters within applicable operational range of currents and voltages in ACP circuits.

d) Computational difficulties, especially the time required to solve a large number of nonlinear differential equations.

The large-signal model as suggested by Ebers and Moll[1,2] was not adequate for the planar type of extremely nonsymmetrical devices. The measurements of inverted parameters were difficult and inconsistent. The charge-control concept,[3] which is quite simple and useful for current drive operations to predict certain over-all delays, was not directly applicable to the ACP circuits. The large-signal approach which is based on the combination of the Ebers and Moll model, the charge-control model, and a simple equivalent circuit with nonlinear small-signal parameters was evolved for this analysis.

The measurements of definable device parameters presented the most difficult problem. The success or failure of such an analysis depends heavily on a satisfactory solution of the measurement problems. The more commonly used high-frequency parameter f_T was replaced by a relatively fundamental parameter "transit time." Special modified bridges were constructed to measure

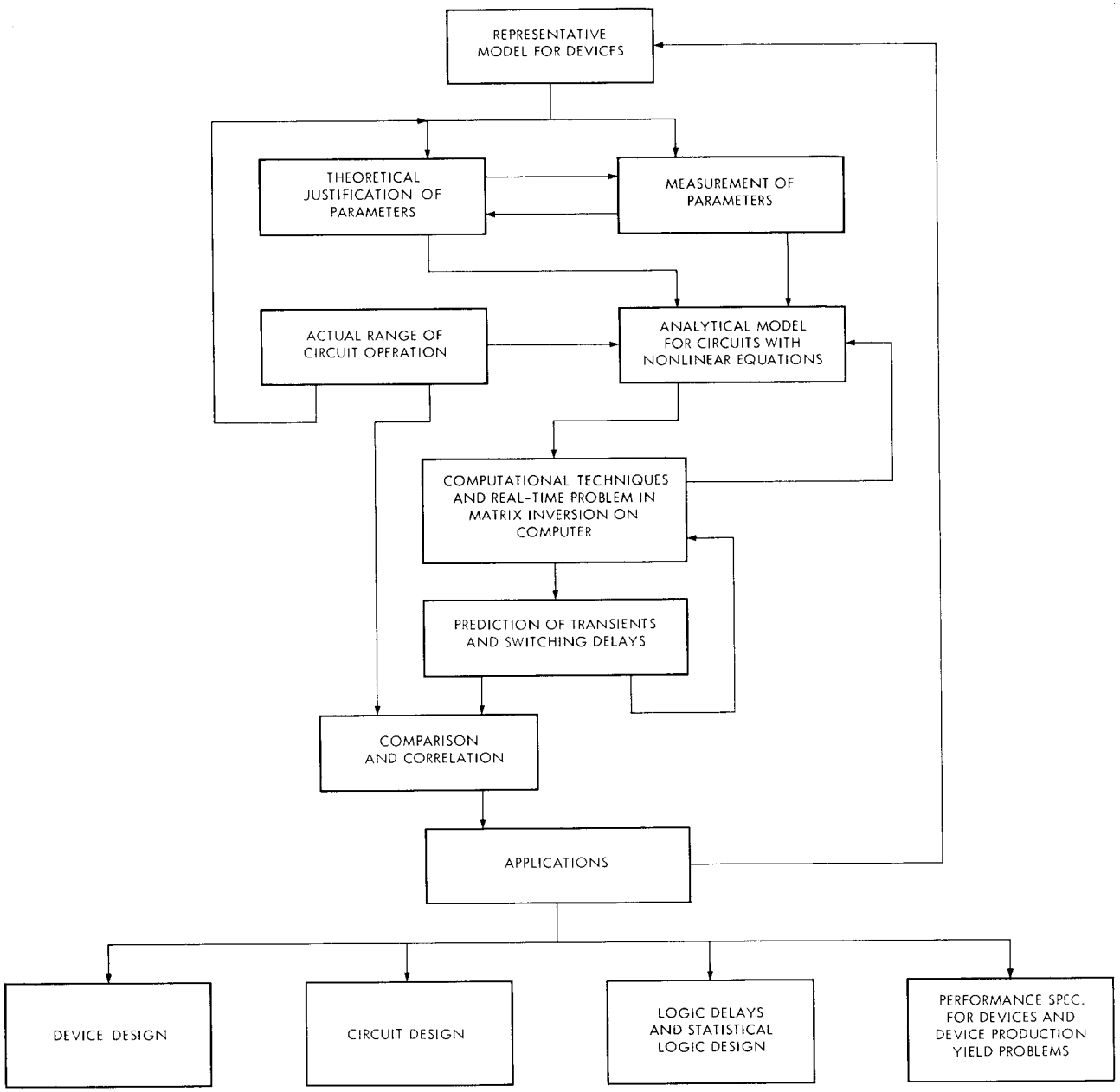


Figure 1 **Flow chart of the procedure used in analysis.**

"transit time" and "base resistance." A discussion of theory, use, and limitations of these measurements is given in the section entitled "Measurement of parameters." Alternative methods of measuring most parameters were investigated; the most suitable and accurate methods were used in the analysis.

Several nonlinearities in the device parameters were measured within the applicable ranges of ACP circuit operations and their physical justifications were analyzed. The effects of emitter crowding, high-level injection, and collector transition layer neutralization were observed within the range of circuit operations and were noted in the analysis.

Nonlinear differential equations were represented in convenient matrices for computations on the IBM 7090. Methods to reduce the computer time for transient analysis were studied. A method found acceptable for this analysis is presented in the section on computational details. Machine computations considered any driving (input voltage or current) condition. Complete output current and voltage waveforms were obtained, replacing the calculation of over-all times and delays. The computer

results were correlated with the observed waveforms and delays, and sensitivity factors of the delays to device parameters were evaluated.

Transistor model

Ebers and Moll's model[1] and charge-control concepts[3] have been used extensively in estimating delays in switching circuits. Most of these applications are limited to current drive inputs and homogeneous base transistors. In principle both of these large-signal representations are equivalent. The differences arise in interpretations of parameters and measurements. In this analysis basic elements of charge-control concepts are applied to transistors with built-in field and to multi-device ACP circuits that are primarily voltage driven. Some comments regarding the validity of the model used in the analysis and interpretation of important parameters in these applications are pertinent.

The representation of a transistor for active region operation by charge-control concept is shown in Fig. 2. Current-drive equations are:

$$I_b = \frac{Q_a}{T_b} + \frac{dQ_a}{dt} + C_{te}\frac{dV_{te}}{dt} + C_{b'c}\frac{dV_{b'c}}{dt} \tag{1}$$

$$I_e = \frac{Q_a}{T_e} + \frac{dQ_a}{dt} + C_{te}\frac{dV_{te}}{dt} \tag{2}$$

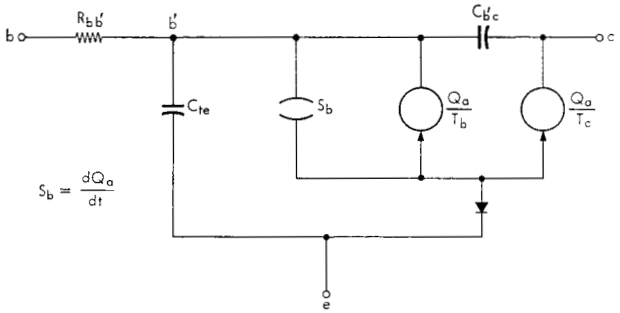
$$I_c = \frac{Q_a}{T_c} - C_{b'c}\frac{dV_{b'c}}{dt}, \tag{3}$$

where Q_a is the base charge in the active region of operation of the transistor, and T_b, T_e, T_c are time constants. Terminal currents I_b, I_e, I_c have the polarities shown in Fig. 2. $C_{b'c}$ and C_{te} are transition layer capacitances. Because $I_e = I_b + I_c$, then from Eqs. (1), (2), and (3),

$$\frac{1}{T_e} = \frac{1}{T_b} + \frac{1}{T_c}. \tag{4}$$

Equation (1) can be directly derived[4] from the continuity equation. The basic requirements for Eq. (1) are the condition of charge neutrality in the base region of the transistor and use of a simple recombination model which is generally applied for transistor analysis. It is reasonably accurate even with any of the other details of the region such as built-in fields, geometry of the device, conductivity modulation, et cetera. The validity of Eqs. (2) and (3) depends on the correct choice and measurement of T_c or T_e. It is shown below that the measurement of T_e at a relatively low frequency includes the effect of built-in field if present.

Figure 2 **The charge control model of transistor for operation in the forward active region.**



We use Eq. (1) but exclude transition layer capacitance effects to obtain the following expression for transit time:

$$I_b(s) = I_e(s) - I_c(s) = Q_a(s)[s + (1/T_b)].$$

Let $T_e(s)$ define the ratio $Q_a(s)/I_e(s)$ in general. Thus

$$T_e(s) = \frac{Q_a(s)}{I_e(s)} = \frac{T_b}{1 + sT_b}[1 - \alpha(s)],$$

where s is the Laplace transform variable and $\alpha(s) = I_c(s)/I_e(s)$.

For a low frequency,

$$T_e(0) = T_b[1 - \alpha(0)]. \tag{5}$$

For a transistor with built-in field, $\alpha(0)$ is a function of built-in field.

In case of a constant built-in field, for example,[5]

$$\alpha(0) = \frac{\exp(mw/L)}{m/n^2 \sinh(nw/L) + \cosh(nw/L)},$$

where

$m = \mu E T_b/2L$,
μ = mobility of carriers in the base,
T_b = recombination time constant in the base,
L = diffusion length or $\sqrt{DT_b}$,
D = diffusion constant of the carriers,
E = constant built-in fields,
$n = (m^2 + 1)^{1/2}$
w = base width.

Substituting the value of $\alpha(0)$ in Eq. (5), we get:

$$T_e = T_b\left[1 - \frac{\exp(mw/L)}{m/n^2 \sinh(nw/L) + \cosh(nw/L)}\right].$$

For most practical considerations, T_b is large (i.e., $T_b \to \infty$), in which case, after a few algebraic manipulations, the last expression simplifies to

$$T_e = \frac{D}{\mu^2 E^2}\left[\frac{\mu E w}{D} - 1 + \exp\left(-\frac{\mu E w}{D}\right)\right]. \tag{6}$$

For the case of an homogeneous base transistor, let $E \rightarrow 0$, and make use of L'Hospital's rule to get

$$T_e = w^2/2D. \tag{7}$$

The transit time is thus related to the details of the base region and the influence of the built-in field will be reflected in the measurement of this parameter.

The transit time $T_e(s)$ is defined earlier as a complex quantity representing ratio of base charge to emitter current. If it is assumed that there is no transient delay between application of emitter current and formation of base charge during switching application, T_e becomes a real variable. This is a basic assumption implied in charge control equations. When charge control equations are used for small-signal application with this assumption the model of Fig. 2 is similar to the equivalent circuit of Fig. 3. The assumption of noncomplex transit time defining a ratio Q_a/I_e is equivalent to an assumption of a minimum-phase-shift generator in a small-signal equivalent circuit. In this case small-signal parameters of the equivalent circuit are related to transit time by

$$T_e = C_d r_e, \tag{8}$$

where C_d is diffusion capacitance and r_e is small signal diode resistance.

By the same relation

$$T_e = 1/\omega_{\alpha_i}, \tag{9}$$

where ω_{α_i} is radian α cutoff frequency.

The excess phase shift in an α generator and an extra delay during the beginning of a switching transient both are related to the time difference between formation of base charge and application of emitter current.

We now show that this additional delay in a switching device is approximately included in this analysis. Consider an α generator with an excess phase shift represented as[6]

$$\alpha(s) = \frac{\alpha_0 \exp(-msT_e)}{1 + sT_e}. \tag{10}$$

For most applications

$$\alpha(s) \simeq \frac{\alpha_0}{(1 + sT_e)(1 + msT_e)} \tag{11}$$

$$\simeq \frac{\alpha_0}{1 + sT_e(1 + m)}. \tag{12}$$

From charge equations,

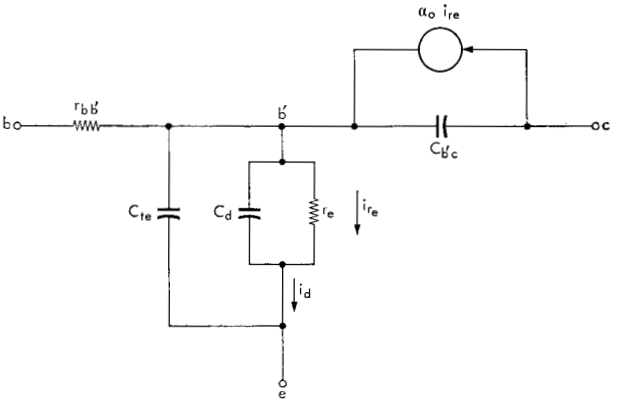
$$\alpha(s) = \frac{T_e/T_c}{1 + sT_e}. \tag{13}$$

Comparison of Eqs. (11) and (13) indicates that modification of T_e to $T_e(1 + sT_d)$ where $T_d = mT_e$, would make the charge equations more accurate. Baker and May[7] have shown that for a homogeneous base transistor, $T_d = 1/6\ T_e$ resulted in more accurate calculations. Equation (12) suggests that modification of T_e to $T_e(1 + m)$ should result in greater accuracy. It is shown in the section on measurements that the quantity $T_e(1 + m)$ is directly measured and no separate determination of m is required.

The high-speed devices under study in this paper are double-diffused, *npn* silicon epitaxial units with planar geometry. In these units, the collector junction area covers the entire base region. It is possible that some portion of the distributed base resistance may be shunted by the distributed collector capacitances under base and emitter contacts. In case of large geometry devices with relatively shallow emitter junction, this phenomenon has previously been approximated by a single lumped capacitance connected to a tap on the base resistance. Many other qualitative configurations are suggested for relatively low frequency devices but experimental verifications are generally lacking. For the present high-speed devices with extremely thin base and very small emitter area, further complications are introduced because of emitter crowding and conductivity modulation, resulting in considerable variations in base resistance under normal switching currents. To take account of all geometrical and distributed characteristics of base resistance and collector capacitance is a formidable task from the point of view of measurements and analysis. In this model, base resistance ($R_{bb'}$) and collector capacitance ($C_{b'c}$) are represented by single lumped elements. Nonlinearity of large-signal base resistance with currents and capacitance with voltage has been accounted for from measurements made under the assumed equivalency. The linear part of the collector capacitance due to land, lead and header of the device is represented by C_{bc}.

A complete large-signal transistor model used in the

Figure 3 **Small-signal equivalent circuit model.**



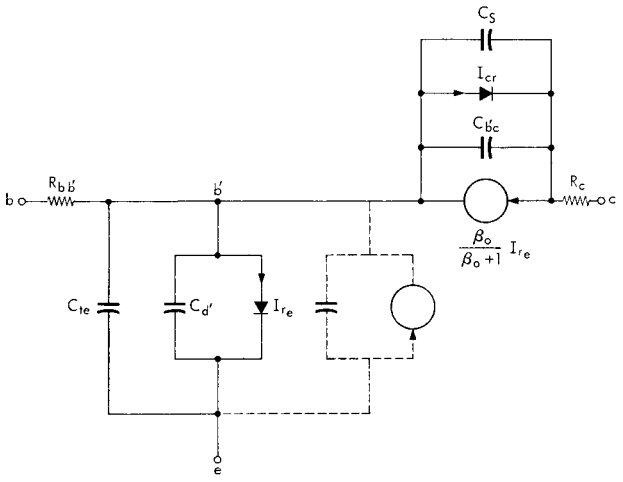


Figure 4 **The large-signal model used in this analysis.**

analysis is shown in Fig. 4. The internal parameters of this equivalent circuit are obtained from a set of ac small signal and dc measurements at the terminals of the device. The small-signal parameters are transformed wherever necessary so that they can be used in the large-signal model. The parameters of the device are nonlinear functions of these voltages and currents. Hence, it is necessary that the parameters of the model be measured at different voltage and current levels. The relationships of the internal parameters and the terminal measurements are derived on the basis of the assumed model and are given in the next section.

The diode and capacitance between nodes b' and c represent the saturation effect. Ideally, an additional current generator and a capacitance should be added between nodes b' and e (shown dotted), but very low values of inverted α for planar types of asymmetrical devices make these components negligibly small and hence they are excluded in the analysis. This model differs from the charge-control model in the following respects:

(a) Placement of the current generator between base (b') and collector (c) instead of between e' and c. This is not a basic difference because transformation is justified by Eq. (4).
(b) Placement of the emitter base diode. The diode position of Fig. 4 is more accurate and convenient for voltage drive conditions of ACP circuits.
(c) Nonlinear base resistance for a linear resistance. Base resistance has been considered to be a function of base charge. Hence, it has different values in the active and saturated regions.
(d) The value of C_d' was obtained from T_e' for a given diode current during calculations instead of using charge equation term $\partial Q_a/\partial t$.
(e) Components corresponding to saturation effect are included between nodes b' and c instead of between b' and e as proposed in the charge-control model.[3]
(f) The current generator between b' and c is made more accurate by including large signal nonlinear α instead of a linear generator implied in charge-control model.

Parameters of the model used in the analysis

Transistor model parameters are defined in Fig. 4, their measurement and transformation for circuit analysis being indicated in Table 1. Relationship between large-signal and small-signal base resistance: Small signal base resistance $r_{bb'}$ can be defined as $r_{bb'} = dV_{bb'}/dI_{bb'}$.

We specify $V_{bb'}$ vs. $I_{bb'}$ (or I_{re}) analytically as follows:

$$V_{bb'} = I_{bb'}R_{bb'},$$

where

$R_{bb'}$ = Instantaneous base resistance.

Since $I_{bb'} = \dfrac{I_E}{\beta_0 + 1}, \qquad \beta_0 = f(I_E)$

and $\dfrac{dV_{bb'}}{dI_{bb'}} = r_{bb'},$

we get

$$dV_{bb'} = r_{bb'}\left\{\frac{1}{\beta_0 + 1} - \left(\frac{I_E}{(\beta_0 + 1)^2}\cdot\frac{d\beta_0}{dI_E}\right)\right\}dI_E. \quad (14)$$

From the measurement, $r_{bb'}$ vs I_E (or I_{re}) and β_0 vs I_E are plotted, (Fig. 5) assuming finite base resistance when $I_E = 0$, $V_{bb'} = 0$.
From Eq. (14),

$$V_{bb'}(I_E) = \int_0^{I_E} r_{bb'}\left\{\frac{1}{\beta_0 + 1} - \left(\frac{I_E}{(\beta_0 + 1)^2}\cdot\frac{d\beta_0}{dI_E}\right)\right\}dI_E. \quad (15)$$

Thus, $R_{bb'} = V_{bb'}/I_{bb'}$ will be a more accurate representation of large-signal base resistance than $r_{bb'}$ and it can be plotted as a function of I_{re} or $I_{bb'}$.

Measurement of parameters

As indicated in the previous section, some of the parameters are based on small-signal measurements.

Equivalent circuit of Fig. 3 is assumed for these measurements.

- *Transit time, T_e*:

The Appendix shows that transit time is related to the intrinsic 'α' cut-off frequency and extrinsic "f_T". T_e is measured on a special bridge[8] built in the laboratory and

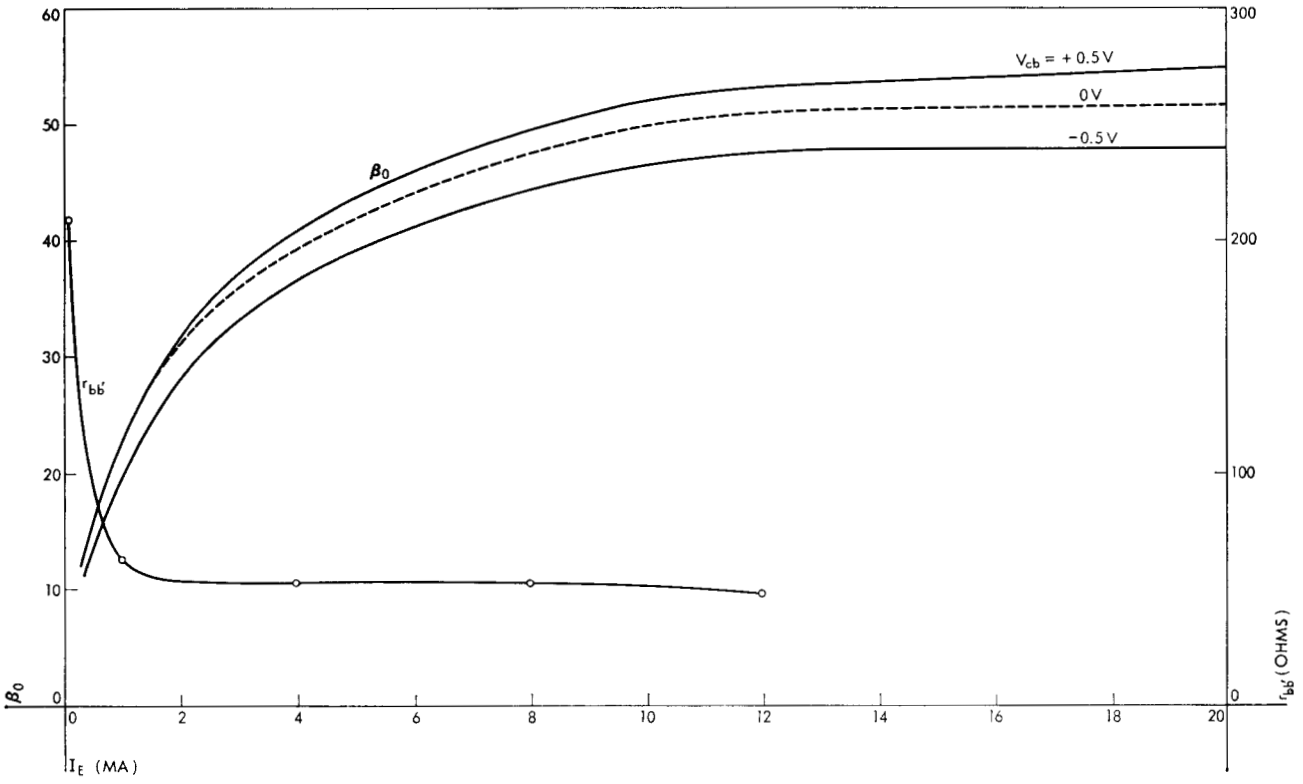
Table 1 **Description of Parameters for the Transistor Model**

Model Parameter	*Method of Measurement*	*Transformation of the parameter for circuit analysis*
1. Emitter-base diode, $D_{b'e}$: I_{re} for given $V_{b'c}$	Dc diode voltage-current curve is measured between base and emitter terminals V_{be} = Emitter-base terminal voltage.	Subtraction of the voltage drop $V_{bb'}$ in the large signal base resistance from the measured diode characteristic results in $V_{b'c}$ vs I_{re} curve. $V_{bb'}$ is obtained from Eq. (15), where $r_{bb'}$ and β_0 as a function of I_{re} or dc I_E are known from separate measurements. Hence, $V_{b'e} = V_{be} - V_{bb'}$.
2. Collector-base diode, $D_{b'c}$	Dc diode voltage-current curve is measured between base and collector terminals. V_{bc} = Collector-base terminal voltage.	Subtraction of voltage drop V_{bs} in the large signal base resistance R_{bs} and collector bulk resistance R_c from terminal diode characteristic gives $V_{b'c}$ vs I_{cr} curve. R_{bs} is the base resistance with collector-base diode forward biased. R_{bc} is obtained from small signal base resistance r_{bs} as shown later. $V_{b'c} = V_{bc} - I_{cr}(R_c + R_{bs})$
3. Dc common emitter current gain, β_0	β_0 is measured for different values of I_E.	I_E correspond to I_{re} in the model at quiescent condition. So β_0 will be altered according to the value of I_{re} during the analysis.
4. $C_{d'}$, diffusion capacitance	From $T_{e'} = T_e(1 + m)$ measurement corresponding to a range of collector-base biases applicable on circuits.	From (1) in this table and using the slope of the curve in (1), $C_{d'} = \dfrac{T_e(1 + m)}{\dfrac{\partial V_{b'e}}{\partial I_{re}}}$
5. C_{te}, emitter base transition capacitance.	This is a small-signal measurement of incremental capacitance $C(v) = dq/dv$ at different biases on the diode.	Since current through a capacitor is given by $i_c = C(v)\, dv/dt$, a curve of measured $C(v)$ vs voltage is used directly in large signal analysis.
6. $C_{b'c}$, base collector transition capacitance	Same as in (5), with the bias voltage on the collector-base terminals.	Same as in (5).
7. Large-signal (instantaneous) base resistance $R_{bb'}$ (active region)	From small-signal measurement of base resistance $r_{bb'}$ for different levels of I_E (or I_{re})	$R_{bb'} = \dfrac{V_{bb'}}{I_{bb'}}$ From Eq. (15), $V_{bb'}$, is obtained as a function of I_E. Since $I_E = (\beta_0 + 1)I_{bb'}$, $R_{bb'}$ is obtained as a function of $I_{bb'}$.
8. Large-signal base resistance R_{bs}, under saturated condition of the device.	From small-signal measurement of r_{bs} for $I_E = 0$ and collector-base diode forward-biased. For this condition, $I_{cr} = I_{bs}$.	$rbs = \dfrac{dV_{bs}}{dI_{bs}}$ $\therefore V_{bs} = \displaystyle\int_0^{I_{bs}} r_{bs}\, dI_{bs}$ Then $R_{bs} = V_{bs}/I_{bs}$ is plotted against I_{bs}. This treatment of base resistance is justified by the fact that base current can be divided into two components corresponding to active and saturated region, $I_b = I_{bb'} + I_{bs}$ $= \dfrac{I_E}{\beta_0 + 1} + I_{cr}$ In the saturated region, $I_{cr} \gg I_E/(\beta_0 + 1)$

Table 1 (Continued)

9. Collector bulk resistance R_c:	Measured by dc method.	This parameter can change with collector current I_c but for the devices under consideration and within applicable current range no appreciable change has been observed. A typical value of R_c for these devices is 5 Ω.
10. Storage capacitance C_s.	From pulse measurement of saturation time constant, T_s. Since T_s changes with collector current at the threshold of saturation, it is measured at the most representative level for the specific circuit operation.	From (2) of this Table and using the slope of the curve in (2) $C_s = \frac{T_s}{(\partial V_{b'c}/\partial I_{cr})}$

Figure 5 **Variation of dc current gain and base resistance with emitter current.**



operating on a 5 Mc signal, as shown in Fig. 6.

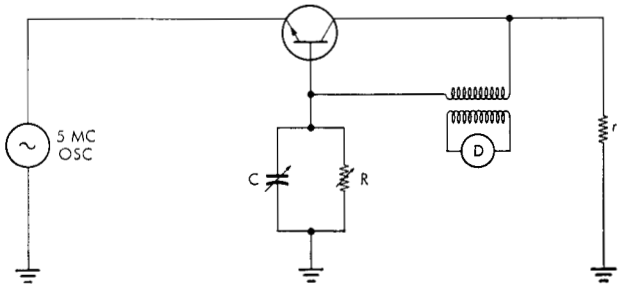
For the balance condition of the bridge, as shown in the Appendix,

$$\frac{R}{r} = \frac{\alpha_0}{1 - \alpha_0} = \beta_0 \tag{16}$$

$$T_M = \frac{CRr}{R + r}$$

$$= T_e(1 + m) + r_e C_{te}$$

Figure 6 **Transit time bridge.**



$$T_M = T_e(1 + m) + \frac{KT}{qI_E} C_{te}, \tag{17}$$

where

C_{te} = Emitter-base transition layer capacitance.
m = Excess phase shift factor in the collector generator.

A plot of T_M vs $1/I_E$ gives the $T_e(1 + m)$ intercept on the T_M axis and C_{te} may be obtained from the slope of the plot as shown in Fig. 7.

• *Comparison of f_T vs T_e*

T_e is a fundamental parameter of the device. Comparison of T_e of different devices will give a comparative idea about their base widths. It is measured independently and can be used directly in the analysis. At the null condition of the transit time bridge, the ac voltage across the collector-base terminal is zero. Hence the external collector base capacitance due to the lands and header do not affect measurements.

The measurement of "f_T" includes the effect of collector junction capacitance and external collector-base capacitance, finite load resistance and also the excess phase factor. Hence the f_T measurement does not give any parameters which can be directly used in the analysis. Other parameters have to be measured individually for the characterization of the model. On the other hand, f_T has to be measured at higher frequencies, and the effect of stray inductance and capacitance must be taken into account. Such effects are small in the transit-time bridge since the test frequency is 5 Mc.

Results from the transit-time bridge are shown in Fig. 7. Extrapolations of lines on the y axis give transit times of approximately 0.1 nsec for ACP devices. At relatively high currents, depending on the collector-to-base "diode," transit time shows a considerable increase. This is due to neutralization of the base layer near the collector base junction by high current densities[9]. This reasoning is substantiated by the strong dependence of the current at which this effect is observed on collector to base junction bias. Nonlinearity in transit time due to this effect is included in the analysis.

• *Junction capacitances $C_{b'c}$ and C_{te}*

These capacitances can be measured for various dc biases by connecting the third terminal of the device to the neutral terminal of the capacitance meter. The measured values will include the respective external capacitance due to device lands and header. This constant part of the total capacitance can be determined by measuring it with a large reverse bias for which the junction capacitances (voltage dependent part) will be negligible.

A set of C_{te} vs V_{BE} and $C_{b'c}$ vs V_{CB} were taken. An IBM 1620 computer program was written to calculate the constants in the following expressions with the least-mean-square-error:

$$C_{te} = A_1/(V_{d_1} - V_{BE})^{n_1} \tag{18}$$

$$C_{b'c} = A_2/(V_{d_2} + V_{CB})^{n_2}. \tag{19}$$

• *Base resistance, $r_{bb'}$*

The following methods were used to determine $r_{bb'}$. Only the bridge method is discussed in detail since it is found to be the most convenient and gives consistent results.

1) *Black-box approach*: Measurement of four hybrid parameters was used to synthesize the base impedance Z_B from a 'T' circuit model of the transistor.

2) *The polar plot of h_{11e}* gave the common emitter short circuit input impedance.

3) *The measurement of h_{12b}* gave the reverse voltage gain of the common-base transistor with input open circuited.

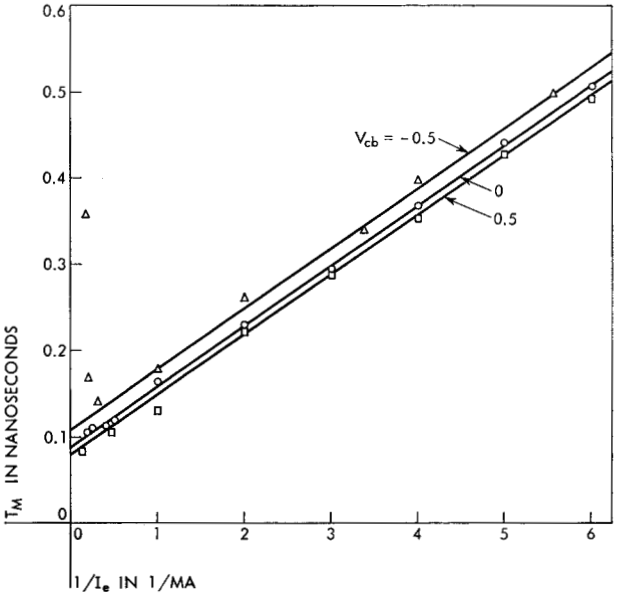
4) *Dc method of measurement of $R_{bb'}$*: $R_{bb'}$ is directly proportional to the resistivity of the base region and therefore it is also dependent on the total base charge, I_B, and indirectly on I_E. Let I_{ex} be the emitter current for which $R_{bb'}$ is to be measured.

In Figure 8 the different voltages under respective measurement condition are given by

$$V_1 = \frac{kT}{q} \ln\left[\frac{I_{E_2} + I_s}{I_s}\right] + \frac{I_{E_2}}{\beta_{0_2} + 1} R_{B_1}$$

$$V_2 = \frac{kT}{q} \ln\left[\frac{I_{E_2} + I_s}{I_s}\right] + I_{E_2} R_{B_2}$$

Figure 7 **Plot of TM vs $1/I_E$ to obtain T'$_e$.**



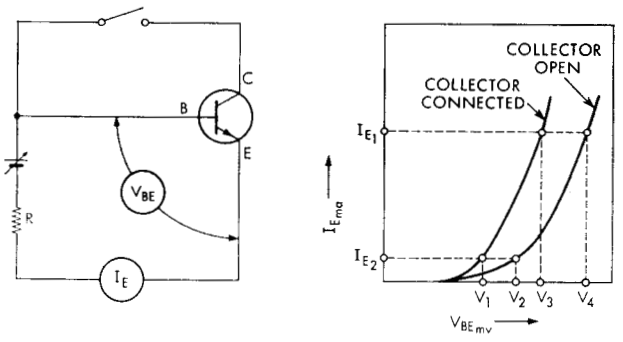


Figure 8 **Experimental setup for base resistance measurement.**

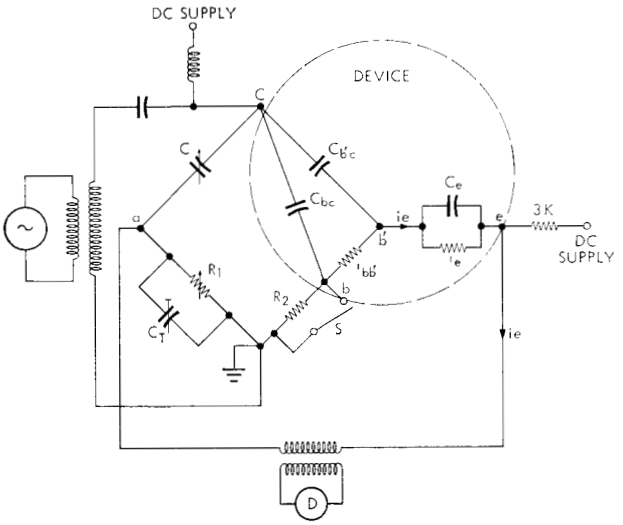


Figure 9 **Experimental setup of $r_{bb'} - C_e$ bridge.**

$$V_3 = \frac{kT}{q} \ln\left[\frac{I_{E_1} + I_s}{I_s}\right] + \frac{I_{E_1}}{\beta_{0_2} + 1} R_{B_2}$$

$$= \frac{kT}{q} \ln\left[\frac{I_{E_1} + I_s}{I_s}\right] + I_{E_2} R_{B_2}$$

$$V_4 = \frac{kT}{q} \ln\left[\frac{I_{E_1} + I_s}{I_s}\right] + I_{E_1} R_{BM},$$

where

R_{BM} = base resistance to be measured at dc base current level equal to I_{E_1} or emitter current level of $I_{ex} = (\beta_{01} + 1)\, I_{E_1}$ under normal operation;

$\beta_{01}, \beta_{02}, \beta_{03}$ = values of β_0 for the values of I_E equal to I_{ex}, I_{E_1}, I_{E_2} respectively.

$$I_{E_2} = \frac{I_{E_1}}{\beta_{0_2} + 1}$$

R_{B1}, R_{B2} = base resistances under the respective measurement conditions.

Assuming $(\beta_{02} + 1)(\beta_{03} + 1) \gg 1$, it can be easily seen that

$$R_{BM} \simeq \frac{V_4 - V_3 + V_2 - V_1}{I_{E_1}}$$

5) *A bridge method*[10] *to measure $r_{bb'}$ and $C_{b'c}$.*

In Fig. 9, the detector current is i_e and is zero at the balanced condition of the bridge. Therefore αi_e generator is not considered in the collector. In high-frequency devices, C_{bc} is often comparable to the junction capacitance $C_{b'c}$ and must be considered. $C_{b'c}$ can be directly obtained by micro-probing and $C_{b'e} + C_{bc}$ can be separately obtained by capacitance meter.

With switch S closed, and balance is obtained for $C = C_1$, then

$$C_1 R_1 = r_{bb'} C_{bc'}. \tag{20}$$

If junction capacity C_{bc} is known, then $r_{bb'}$ is obtained. If switch S opened, let $C = C_2$ under the null condition of the bridge; then

$$R_1 C_2 = (r_{bb'} + R_2) C_{b'c} + R_2 C_{bc}$$

$$\therefore R_1 C_2 = (C_{b'c} + C_{bc}) R_2 + r_{bb'} C_{b'c}. \tag{21}$$

If $R_1 C_2 V_s R_2$ is plotted and extrapolated for $R_1 C_2 = 0$ we get $r_{bb'}\ (C_{b'c}/(C_{b'c} + C_{bc}))$, as shown in Fig. 10.

The bridge can be used to measure $C_{b'c}$ by repeating the above measurement for another value of V_{cb} as shown in Ref. 10. If C_{bc} is small compared to $C_{b'c}$, then extrapolation on Fig. 10 gives $r_{bb'}$ directly and $C_{b'c}$ is obtained from the intercept on the $R_1 C_2$ axis hence $C_{b'c} = R_1 C_2 / r_{bb'}$ for $R_2 = 0$.

Measurement of $r_{bb'}$ for a transistor in saturation

Base resistance of the transistor is expected to differ in the saturation region compared to the active region because of the large charge concentration in the base region during saturation. For a saturated transistor, the collector-base diode is forward biased. Therefore the collector diode resistance and diffusion capacitance can no longer be represented by a simple capacitance as shown in Fig. 9. A saturated transistor model is shown in Fig. 4.

If the emitter and collector terminals are interchanged, the base-emitter dc diode voltage is kept at zero, and the collector base diode is forward biased, the collector current will be I_{cr}. The product of $R_1 C_1$ in Eq. 20 will equal $r_{bs} C_{te}$ where C_{te} is the base-emitter depletion layer capacitance for $V_{BE} = 0$.

Thus a new set of r_{bs} vs I_{cr} plots can be obtained. For a transistor in deep saturation r_{bs} was found to be as small as 10 ohms.

• *Measurement of* R_c

The value R_c is measured with the collector-base junction forward biased. Referring to Figs. 11(a) and 11(b),
V_j = the actual junction voltage

$$= V_{BC} + I_C R_c - I_B R_{bs}$$

$$= V_{BC} + (I_{cf} - I_{cr})R_c - R_{bs}(I_{bs} + I_{cr})$$

$$= V_{BC} + I_{cf}\left(R_c - \frac{R_{bs}}{\beta_0}\right) - I_{cr}(R_c + R_{bs}), \quad (22)$$

where $I_{B_0} = I_{cf}/\beta_0$

For $I_E = 0$, $I_{cf} = 0$, $I_c = -I_{cr}$.
From Eq. (22) and Fig. 11,

$$V_2 = V_j + I_{cr}(R_c + R_{bs}) \quad (23)$$

$$V_1 = V_j + I_{cr}(R_c + R_{bs}) - I_{cf}\left(R_c - \frac{R_{bs}}{\beta_0}\right). \quad (24)$$

From Eqs. (23) and (24),

$$\therefore V_2 - V_1 = I_{cf}\left(R_c - \frac{R_{bs}}{\beta_0}\right)$$

$$\therefore R_c = \frac{V_2 - V_1}{I_{cf}} + \frac{R_{bs}}{\beta_0}, \quad (25)$$

where

R_{bs} = base resistance of the transistor in the saturation region measured separately. Since this is very small, R_{bs}/β_0 is only a fraction of an ohm at I_{cr} = 10 ma and can be neglected.

I_{cf} = collector current as shown in Fig. 11 (a) corresponding to $I_E = K =$ 12 ma as used in Fig. 11 (c).

The preceding Eq. (25) states that for a transistor in saturation, $V_2 - V_1$ are due to a drop in the collector bulk resistance R_c.

• *Measurement of saturation time constant,* T_s

The expression of T_s can be obtained on the basis of charge-control equations[3] as

$$T_s = \frac{t_s}{\ln (I_{B_2} - I_{B_1})/(I_{B_2} - I_{BS})},$$

where

$I_{BS} \simeq I_{cm}/\beta_0$

I_{cm} = collector current when the transistor is on the threshold of saturation.

T_s can be obtained from

1. Slope of the curve

t_s vs $\ln\left[\frac{I_{B2} - I_{B1}}{I_{B2} - I_{BS}}\right]$.

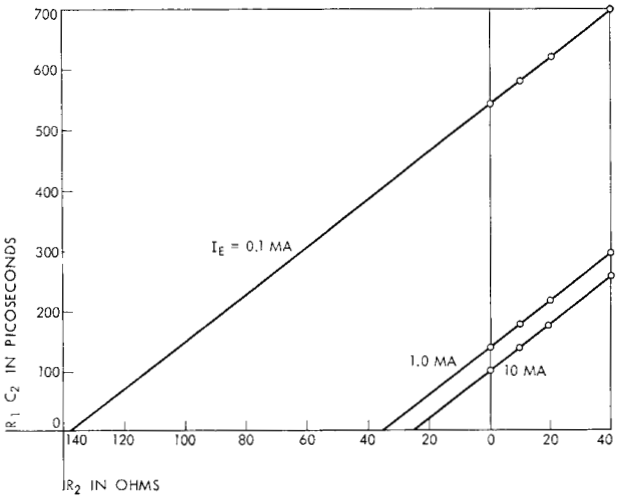


Figure 10 **Plots to obtain $r_{bb'}$ for different I_E.**

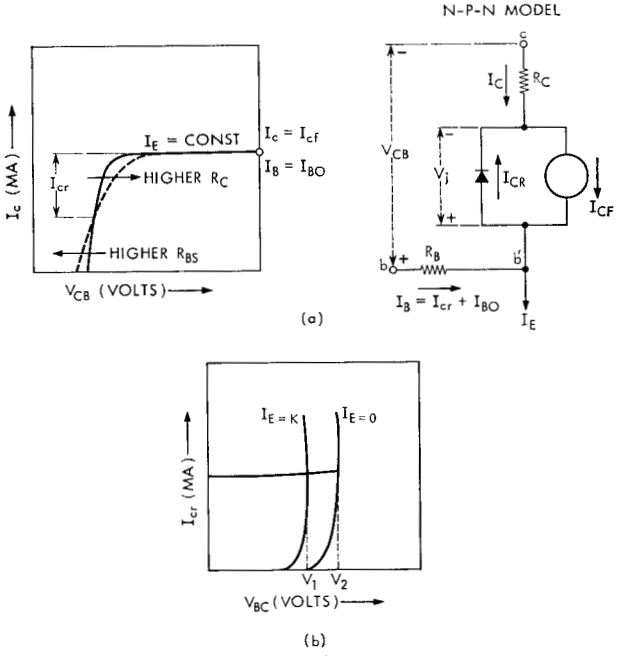


Figure 11 **Model and characteristics of collector-base diode.**

2. Setting

$$\ln\left[\frac{I_{B2} - I_{B1}}{I_{B2} - I_{BS}}\right] = 1.$$

So that $T_s = t_s$, consider magnitudes to arrive only at:

$$\frac{|I_{B2}| + |I_{B1}|}{|I_{B2}| + |I_{BS}|} = 2.72$$

or $$|I_{B1}| = 2.72\,|I_{BS}| + 1.72\,|I_{B2}|. \quad (26)$$

I_{BS} varies for different transistors and as a rule of thumb:

$$0.1I_{cm} \leq I_{B_2} \leq 0.5I_{cm}. \tag{27}$$

The circuit used for the measurement is given in Fig. 12.

For a chosen I_{B_2}, I_{B_1} can be obtained from Eq. (26). The resultant t_s can then be taken as T_s. Several precautions should be observed when making this measurement.

1. The turn-on pulse of I_B should be wide enough to assume that the transistor has reached its steady-state before being turned off.

2. The turn-off pulse should be flat for a period larger than T_s and have a sharp edge so that constant I_{B_2} can be assumed.

Computations of switching circuit transient response

In previous sections, the transistor model (Fig. 4) was characterized for use in large-signal analysis. The model for nanosecond switching pulses was verified by the correlation obtained between the observed circuit responses and the responses predicted by simulating the multitransistor circuits on the IBM 7090 computer. Figure 13 describes a complete setup for the current switch with resistive loads. As far as possible, the stray parameters of the jig used in the bench test were included in the circuits.

Although several general transient analysis programs have been written, the restrictions placed on the network configurations and the relatively excessive analysis time made them unsuitable for ACP circuit analysis. Hence, separate programs were written to analyze each circuit. The philosophy behind each program was to accomplish the analysis in the shortest possible time and still retain a desired degree of accuracy.

An important consideration in reducing the analysis

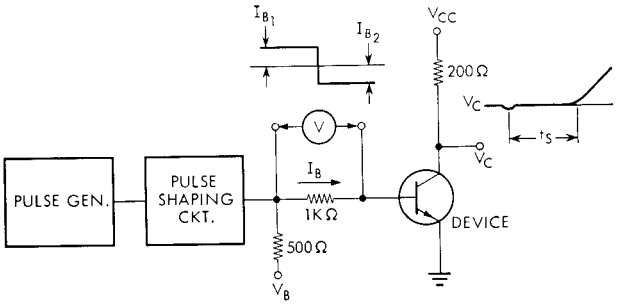
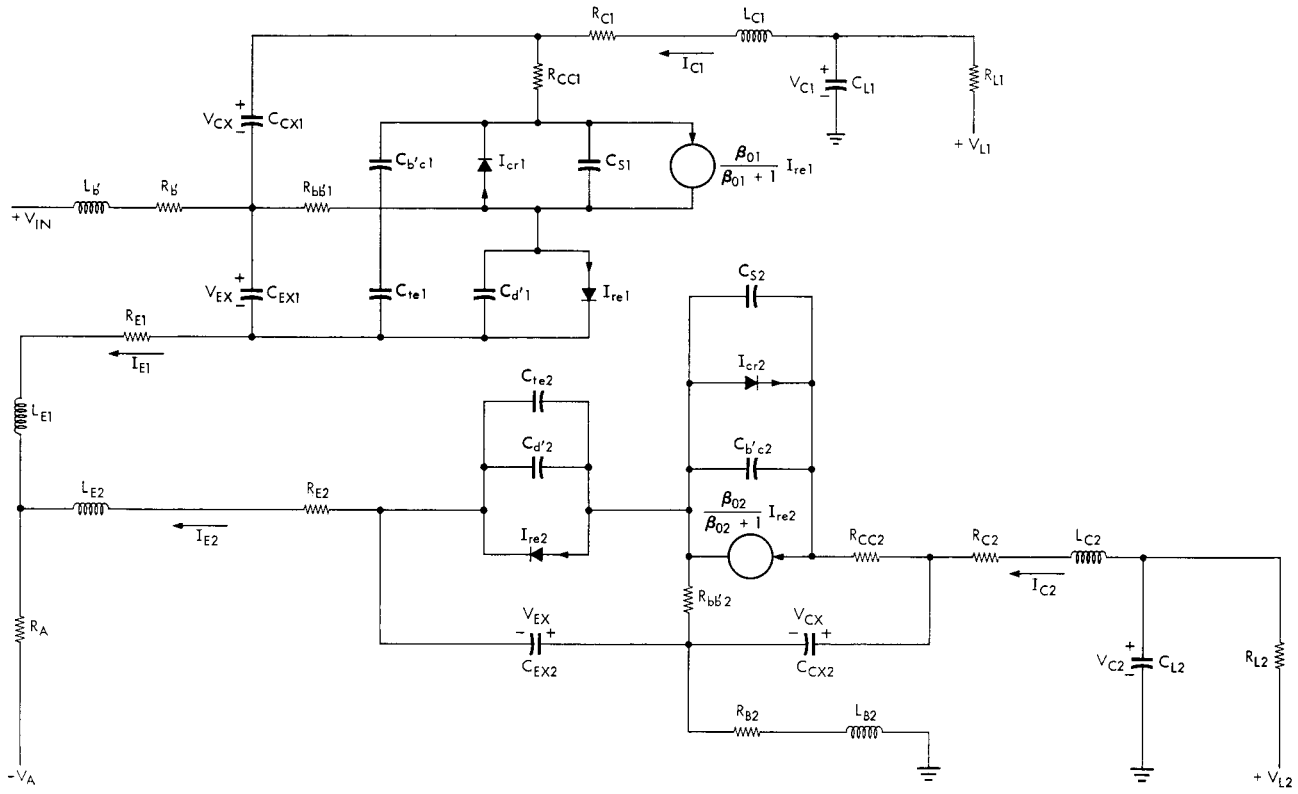


Figure 12 **Experimental set-up for T_s measurement.**

Figure 13 **Current switch network.**



time and in program flexibility was the choice of circuit equations. Using a combination of voltage and current equations, sets of first-order differential equations were derived to simulate each circuit. Since each transistor was isolated from the rest of the circuit by stray capacitance, each set of equations could be divided into linear equations which define the bias circuit and nonlinear equations which define each transistor. In matrix notation these equations were as follows:

For the bias circuit:

$$[L]\left[\frac{di}{dt}\right] = [E \pm iR \pm v]$$

$$[C]\left[\frac{dv}{dt}\right] = [I \pm vG \pm i]$$

For each transistor:

$$[C(v)]\left[\frac{dv}{dt}\right] = [I(v) \pm vG(v) \pm i]$$

Solving for $\left[\frac{di}{dt}\right]$ and $\left[\frac{dv}{dt}\right]$, we have

For the bias circuit:

$$\left[\frac{di}{dt}\right] = [L]^{-1}[E \pm iR \pm v]$$

$$\left[\frac{dv}{dt}\right] = [C]^{-1}[I \pm vG \pm i]$$

For each transistor:

$$\left[\frac{dv}{dt}\right] = [C(v)]^{-1}[I(v) \pm vG(v) \pm i].$$

Matrix inversion is a relatively lengthy process and is to be avoided whenever possible. Since the bias circuit was completely linear L and C need to be inverted only once. The transistor model, however, was almost completely nonlinear, which necessitated inverting $C(v)$ at least every time increment. After the equations were chosen in the manner shown, $C(v)$ was a diagonal matrix, which could be inverted by a series of divisions.

Since several different circuits were being analyzed it was important to be able to switch from one circuit to another with as little programming as possible. Using the aforementioned equations, analysis of a different circuit merely necessitates changing the bias circuit equations.

Measured transistor parameters were defined by graphs. Straight-line approximations were assumed between measured points. If a nonlinear parameter was a function of more than one variable, it was represented by a family of curves. Again a straight-line approximation was used between the points on a given curve and the family of curves. The accuracy of this type of representation may be increased by measuring more points. Diffusion capacitance was expressed in closed analytic form.

The philosophy of the numerical integration routine was the same as that of the overall program—rapid calculation and retention of a desired degree of accuracy. The first condition was met by using equations of third degree or less. The second condition was satisfied by allowing the integration step size, or interval, to be variable. Since the size of the integration interval to a large extent controls the computation time, the ability to vary the interval size is very important in the analysis of high-speed circuits. If the interval is kept constant its value would be determined by the smallest circuit time constant. Once this time constant approaches its limit, the integration interval may be increased without any appreciable loss in accuracy. The optimum numerical integration routine would operate with the largest interval possible. At present, a clear-cut method to determine the maximum integration interval for nonlinear differential equations is not available. The routine used tries to approximate this idea as close as possible.

The following predictor and corrector equations are used to obtain three starting values:

$$Y_{N+1}{}^{P} = Y_N{}^{C} + \Delta t \frac{dY_N{}^{P}}{dt} \qquad \text{(Predictor)}$$

$$Y_{N+1}{}^{C} = Y_N{}^{C} + \frac{\Delta T}{2}\left[\frac{dY_{N+1}{}^{P}}{dt} + \frac{dY_N{}^{P}}{dt}\right]. \qquad \text{(Corrector)}$$

Once the starting values have been computed, a new corrector is used:

$$Y_{N+1}{}^{C} = Y_N{}^{C} + \frac{1}{3}\left[Y_N{}^{C} - Y_{N-1}{}^{C} + 2\,\Delta T \frac{dY_{N+1}{}^{P}}{dt}\right].$$

The maximum interval, ΔT, is specified by the user. The minimum is set equal to 2^{-16} of the maximum interval. The interval is then allowed to vary between these two limits based on the following error criteria:

$$R = \left|\frac{Y_{N+1}{}^{C} - Y_{N+1}{}^{P}}{Y_{N+1}{}^{C}}\right|$$

1. If $R < 0.003$, the interval is doubled until it reaches its maximum value.

2. If $0.003 < R < 0.045$ the interval is kept constant at its previous value.

3. If $R > 0.045$ the interval is halved.

If it is necessary to halve the interval, the following corrector formula is used:

$$Y_{N+1/2}{}^{C} = Y_N{}^{C} + \frac{1}{8}\left[Y_N{}^{C} - Y_{N-1}{}^{C} + 6\Delta t \frac{dY_N{}^{P}}{dt}\right].$$

The interval is not allowed to be halved more than twice

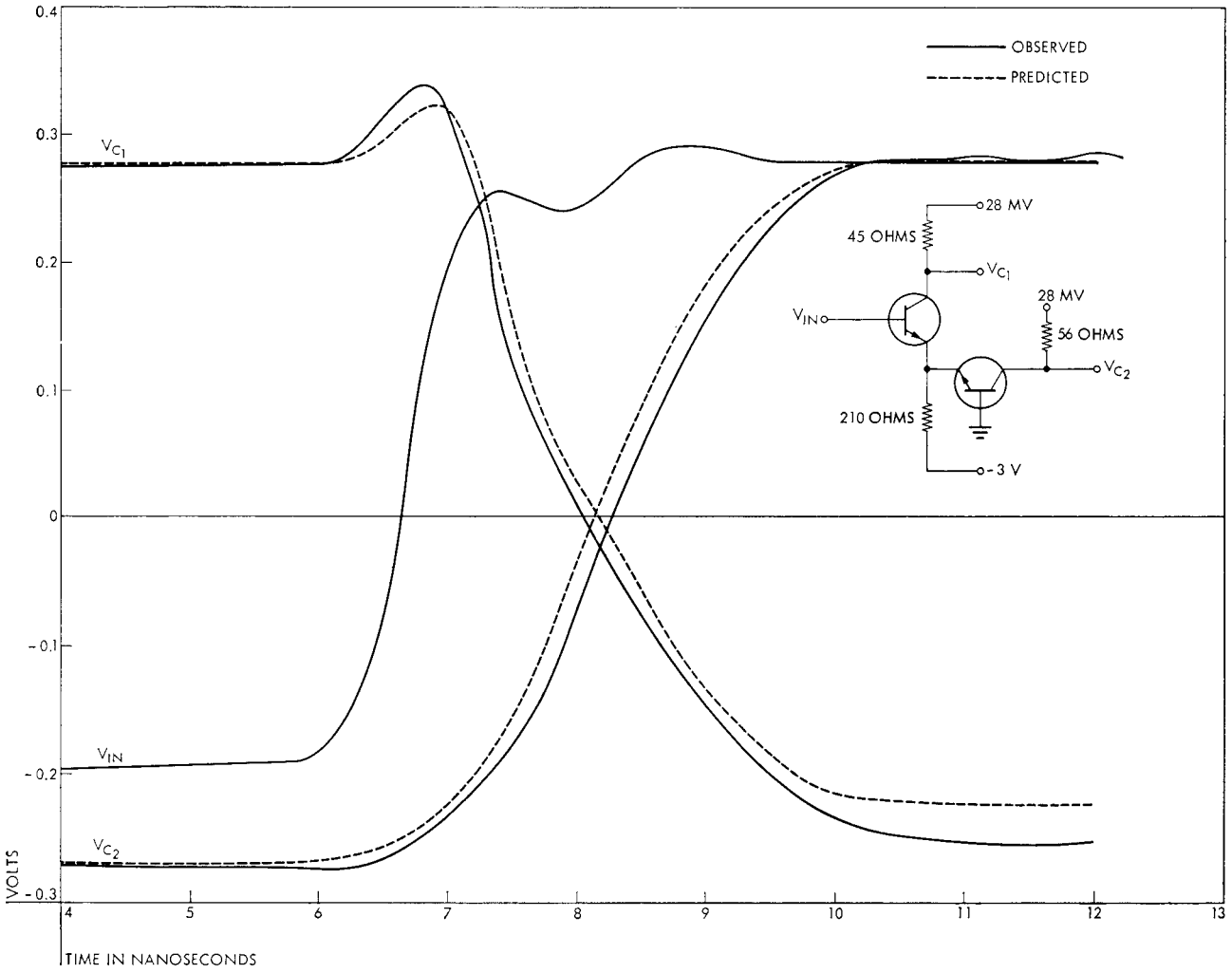


Figure 14 **Current switch.**

in succession. Should this be found necessary, the interval is automatically set equal to its minimum value.

With these techniques, computation of turn-on and turn-off responses for a two-transistor circuit took approximately five minutes and a three-transistor circuit took approximately seven minutes.

Discussion of the results of computer analysis

Figure 14 shows general correlation between the observed and predicted response for the current switch block. The difference in the steady-state values was found mainly to be due to the change in the diode characteristics. For the typical input voltage swing the collector-base diode in current switch does not go into deep saturation and the effect of the saturation time constant does not have a significant effect on the circuit delay. The initial overshoot in the out of phase output V_{C_1} was found to be due mainly to the feed-through capacitor C_{bc} between collector and base. Circuit delay was also found to be affected only slightly by variation of β_0 with emitter current and variation of transit time with collector-base diode voltage.

Figure 15 shows the correlation between computed and observed waveforms for a cascode circuit. In addition to all the factors of the current switch, two more parameters, base resistance in saturation and the storage time constant T_s, are required.

For evaluating the effect of device parameters on delays, parameters were varied one at a time, keeping other parameters unchanged. Increase or decrease in delays was correspondingly predicted. Sensitivity factors for all important device parameters with current switch and cascode circuits were thus evaluated. A sensitivity factor with respect to a parameter is defined as a percentage change in average delay due to a one percent change in the parameter. These are summarized in Table 2. Importance of base resistance for these primarily voltage driven circuits is evident. Surprisingly, the transit time, which is given a primary importance in device design and material study,

ranked third for both the practical circuits.

The following comments are based on a number of computer predictions made with these two basic circuits.

Since the large-signal base resistance depends on the integration of small-signal base resistance, the value of base resistance at lower currents influences the delays considerably. Also, the current at which emitter crowding substantially reduces base resistance is important in characterization. Delays and transient responses are very sensitive to dc voltage-current characteristics which in turn depend on base resistance. As a result, an error in the measurement of base resistances in the active region or in saturation doubly influences the transients.

As indicated in the section on measurements, the transit time was found to increase at higher currents, especially at slightly forward-biased collector-to-base "diode" junction. These variations are included in the correlation study. However, for most presently available devices and current levels up to 12 ma, this increase does not produce substantial change in delays. Any changes in the method of forming the collector base junction or reduction in collector area could make this effect a predominant limitation on high-speed circuits. The influence of the storage time constant on cascode circuit delays as indicated by the sensitivity factor is small, but overshoots that result from a large T_s in the circuit produce undesirable effects in logic. This would be appreciated in the study of the IMPLICATION circuit discussed next.

The IMPLICATION circuit in Fig. 16 is a combination of the current switch and the cascode circuit with a logic function described by $C = A + \bar{B}$. Different transient responses occur due to differences in input signal sequences. Figure 16 shows the correlation between computed and observed waveforms for output voltage for one particular sequence. This sequence pertains to a single-shot logic circuit when the same input is applied at A and B but the input at A is delayed by a prescribed time.

Applications

The capability of simulating devices and circuits on computers yields a number of possibilities. Some of the direct and indirect uses to which this analysis is adapted will be qualitatively discussed.

Table 2 **Sensitivity factors for current switch and cascode delays**

Parameter	*Current Switch*	*Cascode Inverter*
$R_{bb'}$	0.8	0.4
$C_{b'c}$	0.6	0.3
T_e	0.4	0.2
T_s	—	0.15
β_0	0.1	0.1
C_{te}	0.1	0.1

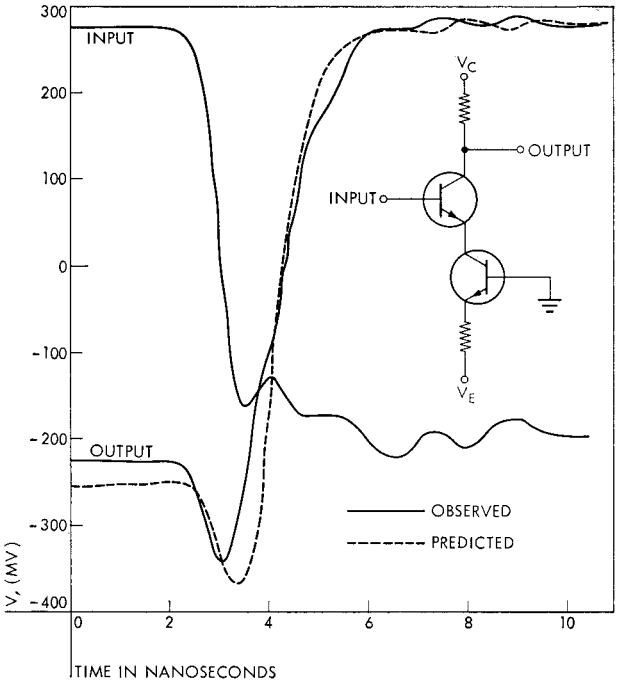


Figure 15 **Cascode circuit response.**

The importance of base resistance and collector capacitance is evident from the sensitivity study of basic circuits. In device design, these factors are basically governed by the number of stripes, doping profiles, junction areas, and other fabrication considerations. Decrease of one parameter increases the other and, for a specific application, a compromise must be made. Since base resistance is predominantly a function of current, and since collector capacitance is a function of collector-base junction voltage, circuit operational conditions have a predominant influence in arriving at this compromise. Similarily low storage time and high β are based on accepted circuit design tolerances and the status of device technology.

Variations of delays in circuits with different devices are functions of parameters, supply voltages, resistances and stray impedances. By proper control of device parameters, chances of circuit delays that are larger or smaller than prescribed values are made tolerably small. For a relatively small range of delays, variations in parameters may be assumed as linearly related to the conveniently defined delay. With this assumption and from the computations of (a) nominal value of delay (D) for mean values of all the relevant parameters and (b) sensitivity factors for delay with respect to all variables, the distribution of delay is obtained by using

$$\Delta D = \sum_{i=1}^{n} (Si)\, \Delta x_i,$$

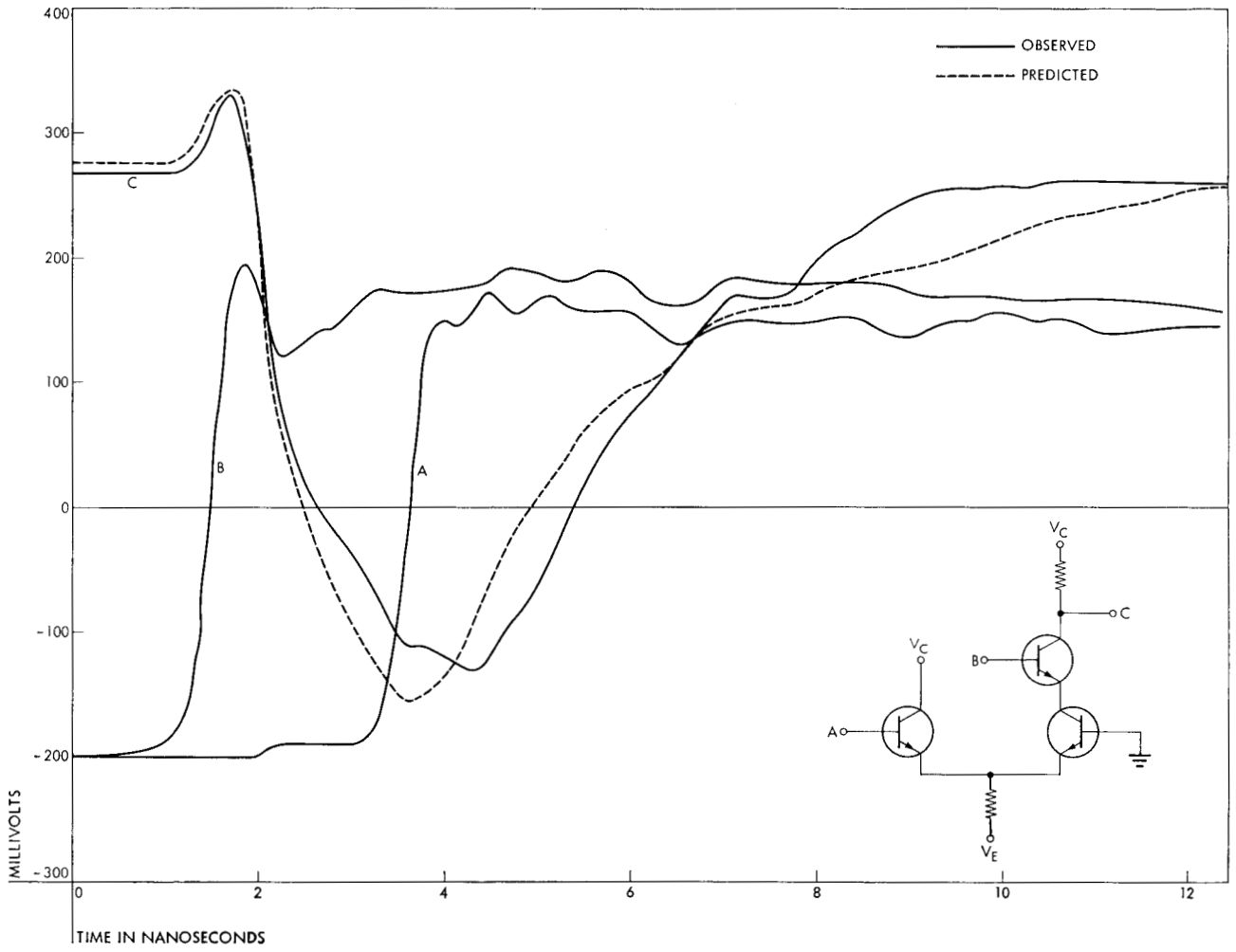


Figure 16 **Implication circuit correlation, single-shot logic operation.**

where Δx_i refers to variation in parameter x_i, and S_i refers to sensitivity factor of D with respect to variable x_i at mean value.

With interest at one end of the distribution, more accurate results are obtained if sensitivity factors are computed for that end.

It is a normal practice to accept devices or circuit modules on the basis of worst-case circuit performance tests. With knowledge of the transient study as reported here, these tests can be made more precise and effective, and often eliminated.

Conclusion

The study of ACP circuits with presently available devices has resulted in:

a) A satisfactory device model for ranges of currents and voltages applicable to ACP circuits.

b) Evaluation of many measurement techniques and determination of most efficient and consistent ones for characterizing the device. Some measurement methods are new while others are modified for suitability to the available high-speed planar transistors.

c) Relatively fast yet accurate computational techniques usable on a large computer.

d) A capability to simulate ACP circuits on a computer for any devices reasonably conceivable with present technology. This provides a method for optimizing device and circuit designs, statistical delay analysis in circuits and solution of problems concerned with performance tests.

Appendix

The small-signal model of the transistor as shown in Fig. 3 can be divided into its intrinsic and extrinsic parts. The high-frequency parameter widely known as "f_T" corresponds to this over-all model and its expression should include all extrinsic parameters. Transit time T_e as measured in this paper is a parameter of the intrinsic model.

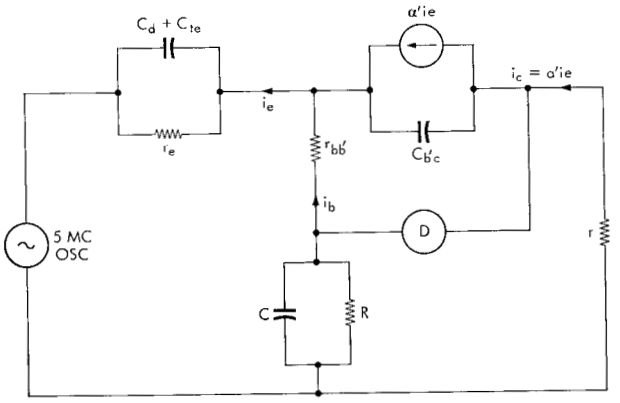


Figure A-1 **Transit time bridge.**

In this Appendix, an expression for f_T as related to the transit time will be derived.

In general, the intrinsic "generator" can be related to diode current i_d (Fig. 3) as a complex function of frequency including excess phase factor m:

$$\alpha_i i_d = \frac{\alpha_0 \exp(-jm\omega/\omega_{\alpha i})}{1 + j\omega/\omega_{\alpha i}} i_d$$

where

$$\omega_{\alpha i} = \frac{1}{C_d r_e} = \frac{1}{T_e},$$

$$= \alpha_0 i_{re} \exp(-jm\omega T_e)$$

$$= (\alpha_0 i_e)/(1 + j\omega T') \exp(-jm\omega T_e), \qquad (28)$$

where

$$T' = (C_d + C_{te})r_e = T_e + C_{te}r_e$$

In the range of frequencies where this model is valid, if we now assume that $m^2\omega^2 T_e^2 \ll 1$. Then

$$\exp(-jm\omega T) \exp \approx 1/1 + jm\omega T_e.$$

Assuming further that $m\omega^2 T_e T' \ll 1$, then from Eq. 28,

$$\alpha_i id \approx \frac{\alpha_0 ie}{1 + j\omega(T' + mT_e)} = \alpha' i_e. \qquad (29)$$

Terminal current gain A_i under common emitter condition will be defined as $A_i = i_c/i_b$. Assuming a nonzero collector bulk-resistance R_c of the transistor and a small load resistance R_L under test condition during measurement of "f_T" (ideally the frequency at which $|A_i| = 1$ with $R_L = 0$), we get a general expression of A_i in the Laplace transform domain

$$A_i = \frac{(p + a_1)(p + a_2)}{(p + b_1)(p + b_2)(p + b_3)}$$

where

$$R_l = R_L + R_c$$

$$C_e = C_d(1 + m) + C_{te}.$$

$$= C_{d'} + C_{te}$$

If the pole and zeros are calculated for typical parameters the frequency response of A_i will be controlled by a single pole and other factors will start to affect A_i at much higher frequency ($\gg$ 100 Mc).

The value A_i will have an initial drop at nearly 6 db/octave as has been experimentally verified by ac measurement of current gain from 30 to 1000 Mc. A_i will be approximately given by

$$A_i = \alpha_0/[(1 - \alpha_0) + p\{r_e(C_{d'} + C_{te} + C_{b'c} + C_{bc}) + R_l(C_{b'c} + C_{bc})\}] \qquad (31)$$

Let C_c = collector capacitance as measured on the capacitance meter = $C_{b'c} + C_{bc}$.

$C_{d'}r_e = C_d r_e (1 + m) = T_e(1 + m) = T_e'$ as measured on the transit time (proved later).

Now define measured "f_{T_M}" as the frequency at which $|A_i| = 1$, then from Eq. (37),

$$f_{T_M} \approx \frac{1}{2\pi\{T_e' + r_e(C_c + C_{te}) + C_c(R_L + R_c)\}}. \qquad (32)$$

Equation (32) reduces to the approximate relation for $m = R_L = R_C = C_C = 0$,

$$f_{T_M} \approx \frac{1}{2\pi\{T_e' + r_e C_{te}\}}.$$

This approximate relation differs from actual value of f_{T_M} as given in Eq. 32 by significant amount for fast devices with low T_e.

Equation for balance in transit time bridge

The bridge can be redrawn as shown in Fig. A1. At balance, current through detector is zero,

$$(i_c - \alpha' i_e)\frac{1}{(j\omega C_{b'c})} = i_b r_{bb'} = (i_e - i_c)r_{bb'}$$

or, as given by Eq. (33),

$$A_i = \left[\frac{\alpha_0 + p\{\alpha_0 r_{bb'}C_{bc} - r_e(C_{bc} + C_{b'c})\} - p^2(r_e r_{bb'}C_{bc}C_{b'c})}{(1 + pr_{bb'}C_{bc})\{p^2 C_{b'c}R_l C_e r_e + p(C_{b'c}R_l + R_e C_{b'c} + r_e C_e) + (1 - \alpha_0)\} + \{(r_e + R_l) + pR_l C_e r_e\}pC_{bc}}\right] \qquad (30)$$

$$i_e\left\{r_{bb'} + \frac{1}{j\omega C_{b'c}}\right\} = i_e\left\{r_{bb'} + \frac{\alpha'}{j\omega C_{b'c}}\right\} \quad (33)$$

From Eq. (33),

$$\frac{i_c}{i_e} = a' = \frac{j\omega r_{bb'} C_{b'c} + \alpha'}{j\omega r_{bb'} C_{b'c} + 1}. \quad (34)$$

Also,

$$i_c r = i_b\left(\frac{R}{1 + j\omega CR}\right)$$

$$= (i_e - i_c)\left(\frac{R}{1 + j\omega CR}\right). \quad (35)$$

From Eq. (35)

$$\frac{i_c}{i_e} = a' = \frac{R}{(r + R) + j\omega CrR}. \quad (36)$$

Equating the right-hand side of Eqs. (34) and (36) and under the assumption that at the test frequency of 5 Mc,

$\omega r_{bb'} C_{b'c} \ll \alpha_0 (< 1)$

and

$\omega^2 r_{bb'} C_{b'c} (T' + mTe) \ll 1,$

we have

$$\alpha_0[(r + R) + j\omega CrR] = R[1 + j\omega(T' + mT_e)] \quad (37)$$

Equating real and imaginary parts,

$$\alpha_0 = R/r + R$$

$$\text{or} \quad \beta_0 = \alpha_0/1 - \alpha_0 = R/r. \quad (16)$$

and, in addition,

$$CrR/r + R = T' + mT_e = T_e(1 + m) + kt/qi_E C_{te} = T_M. \quad (17)$$

Hence a plot of T_M vs $1/I_E$ will give T_e $(1 + m)$ and slope of the straight line in Fig. 7 gives C_{te}.

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