D. J. Crawford
W. D. Pricer
J. J. Zasio

An Improved Tunnel Diode Memory System

Abstract: Beginning with a brief history of tunnel diode memories, this paper describes the factors leading to the present design approach. Array design criteria are discussed at length. Examples of engineering applications are given, including a cross-sectional model of a "scratch pad" memory for use with Advanced Circuit Program logic circuitry.

Introduction

This paper describes a tunnel diode memory system that is basically different from those previously reported. The storage array characteristics of the new system considerably simplify the design of the associated driving and sensing circuits. In addition, the simple circuit comprising the basic storage cell contains only one semiconductor device, the tunnel diode.

In order to show clearly the new features of this tunnel diode memory system, we will first give a brief historical review of the art. The possibilities of the tunnel diode as a storage element in memory applications were recognized very shortly after its discovery. The foremost property is its high switching speed. Because of the nonlinear, negative-resistance characteristics, very simple bistable circuits could be designed using the tunnel diode. The peak-current characteristic of the tunnel diode indicated a stable threshold which would simplify the design of selection circuitry.

Most of the early cells are one- and two-resistor combinations[1,2] (Fig. 1a). The basic cells were easy to understand and design, and in addition were fairly simple to fabricate. Designing a multicell array, however, presented several problems. The amount of current a cell draws from the driving source is a function of the information state of the cell. Furthermore, the sum of all the currents drawn by many cells in parallel across a drive line produces a substantial requirement of total current. The combination of these two properties of the early arrays requires that the driving lines and the driving circuits attached to the lines have a very low impedance. Such low-impedance arrangements are difficult to achieve, particularly at very high frequencies. In addition to the driving problem, the inherent low impedance of the array makes it difficult to extract an output signal with a sufficient signal-to-noise ratio and signal amplitude to make detection possible.

Because of these difficulties, modifications of the simple array of Fig. 1 began to appear.[3-5] Kaufman[3] described modifications to the basic system, adding additional circuitry, as shown in Fig. 1b. He described a resonant transformer system as a means to couple the outputs of the cells and to achieve a larger signal and higher signal-to-noise ratio than could be obtained with the basic system.

A different modification[4] was investigated at IBM (Fig. 1c). The third resistor in each cell permitted the introduction of a direct-current bias, with several beneficial effects. The net result was a decrease in the loading of the drive lines, and an increase in operational tolerances. In addition to the bias resistor, a separate line was used to connect the sense outputs of the cells together. This line permitted a larger signal to be received at the array output and also allowed cancellation of driving noise from the bit-line axis. Although a working model employing this type of array was built, this memory model did not possess sufficiently good operating characteristics to make it attractive as a good engineering approach. Concurrently, other workers in the technology began to consider the addition of a second nonlinear element to the cell.[6-9] Typical of this new approach are the cells reported by Chaplin and Thompson (Fig. 1d), and the cell reported by Kaufman (Fig. 1e). Although the addition of a second nonlinear element increased the cost of the cell, it provided sufficiently increased isolation to make the operational characteristics of the array more attractive.

In retrospect, certain facts were becoming evident.

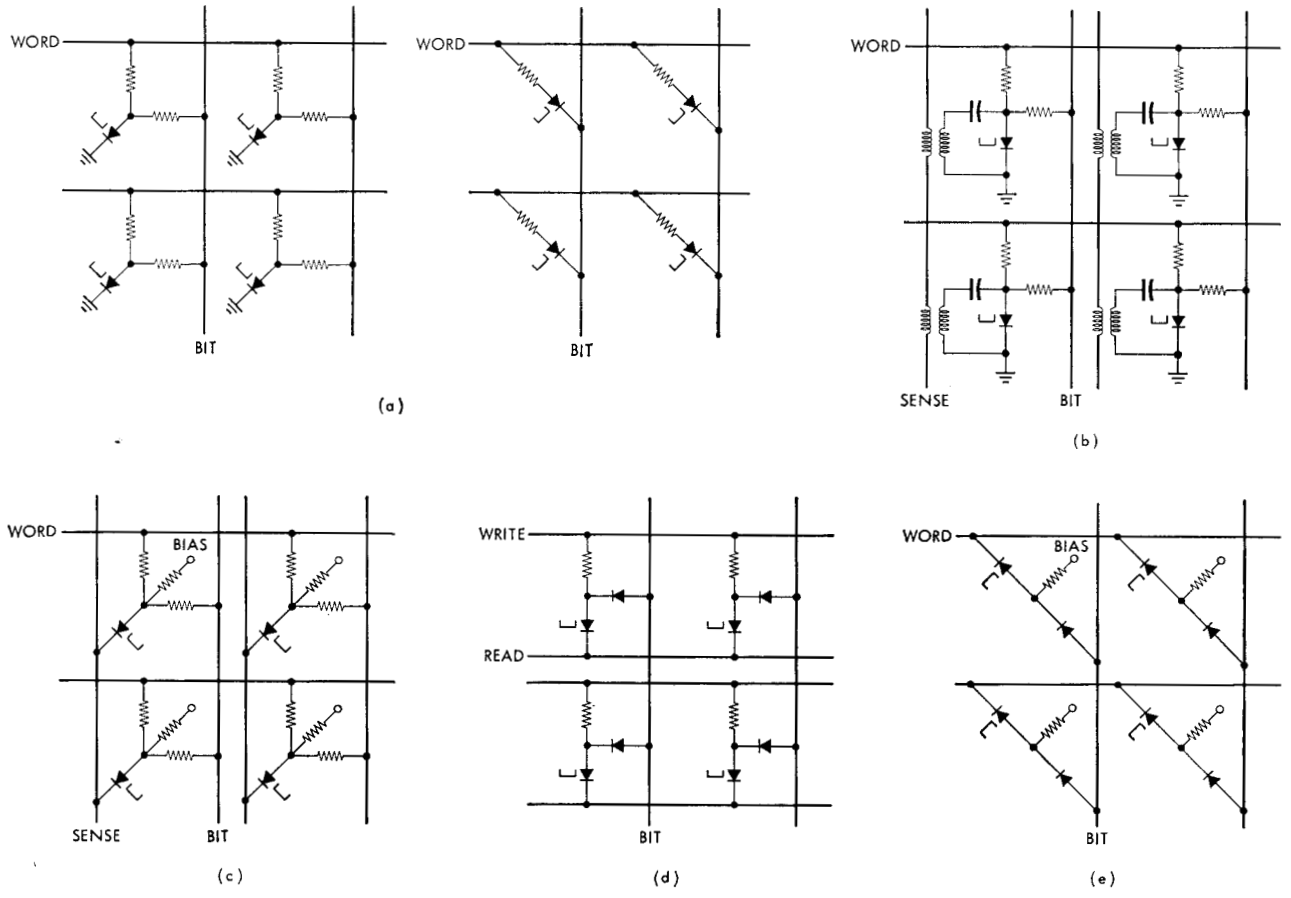


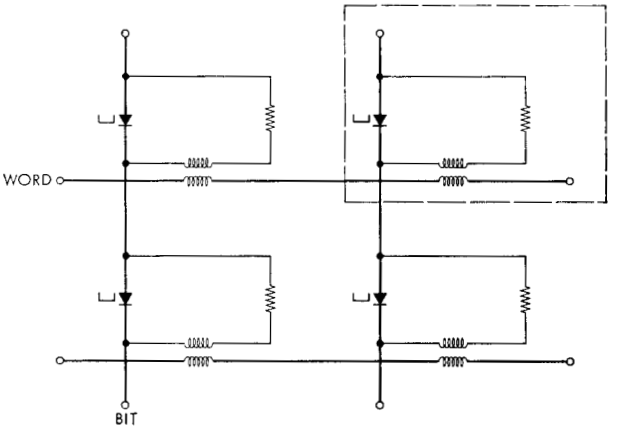
Figure 1 **Evolution of cell design.** *(a) Typical early cell. (b) Typical modification. (c) IBM modification of basic cell. (d) Cell with second nonlinear element. (e) Cell with back diode. (See text.)*

First of all, the switching speed of the tunnel diode itself had little or nothing to do with the limitations of the speed of the memory system. Even from the very beginning, the switching speed of the tunnel diode outstripped the capabilities of the memory arrays and associated circuits. Another fact which began to be appreciated was that the time delay of signal propagation in tunnel diode memory arrays of a workable size was small compared to the delays through the associated circuitry outside of the array. Instead of designing driving and sensing circuits to match an array, the array should be designed to match the engineering design limitations of the external circuitry. In particular, the impedance levels, currents, and signal amplitudes of the array should be matched to those most readily available from high-speed circuits made up of transistors and tunnel diodes. A new memory system was conceived by W. D. Pricer and H. P. Wolff which reflected such a philosophy.

Storage array description

In contrast with the parallel-connected array systems previously employed, the new memory system to be described here has cells which are serially connected in both the word and the bit axes. The basic storage cell is as shown in the dashed-line box in Fig. 2. It consists of a tunnel diode shunted by a series-connected load resistor and transformer secondary. A biasing current is introduced to the tunnel-diode storage cell along the bit axis. During

Figure 2 **Array configuration.**



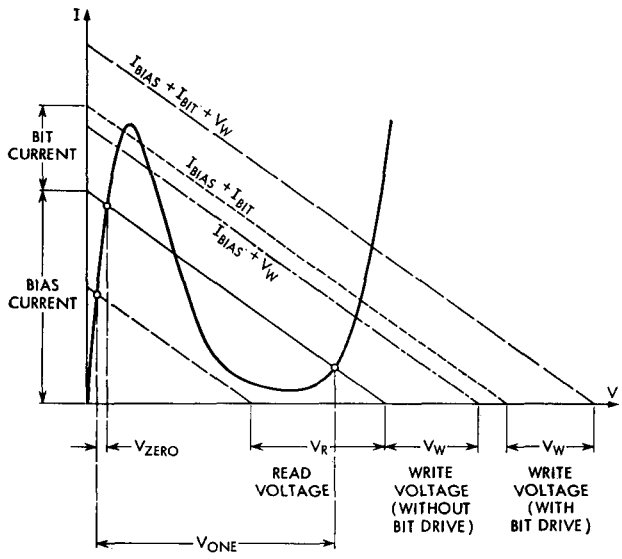


Figure 3 **Tunnel diode load line diagram.**

the writing portion of a memory cycle, this biasing current can be increased by the addition of a bit current. The word driver introduces voltage excursions within the storage-cell loop by means of the transformer. The normal bias current through the tunnel-diode cell is such that the tunnel diode can be either in a high-voltage region or a low-voltage region.

The cells are series-connected along two axes (Fig. 2) in order to form the basic memory array configuration. Figure 3 shows the load-line diagram for the basic storage cell. The current bias and the load resistor are such that the cell normally has two stable states. During the READ operation, the voltage induced into the secondary of the cell transformer shifts the load line and clears the cell from the high-voltage state to the low-voltage state, if the cell has been storing a ONE. The net voltage drop when the cell changes its operating point from the high-voltage to the low-voltage state is transmitted through the series connection of the diodes on the bit line to the end of the bit line, where it can be detected.

On the other hand, if the cell was storing a ZERO, it initially would be in the low-voltage state. The shifting of the load line, in this case by the READ voltage, V_r, produces only a very small voltage as the ZERO response. At the conclusion of the READ cycle, all the cells associated with the particular word have had their information read out and are left in the low-voltage state.

During the WRITE portion of the cycle, the writing voltage, V_w, appears across the cell transformer secondary and shifts the load line towards the peak current region. The amplitude of V_w is insufficient by itself to drive the load line past the peak. To write a ONE, the current through the bit line is increased by the addition of the bit current. The sum of the bias current, the bit current, and V_w is sufficient to carry the load line beyond the peak current point of the diode, and the diode switches to the high-voltage state. The bit current plus the bias current are insufficient to carry the load line beyond the peak. Because of this, cells on the same bit line which were not a part of the selected word are unaffected.

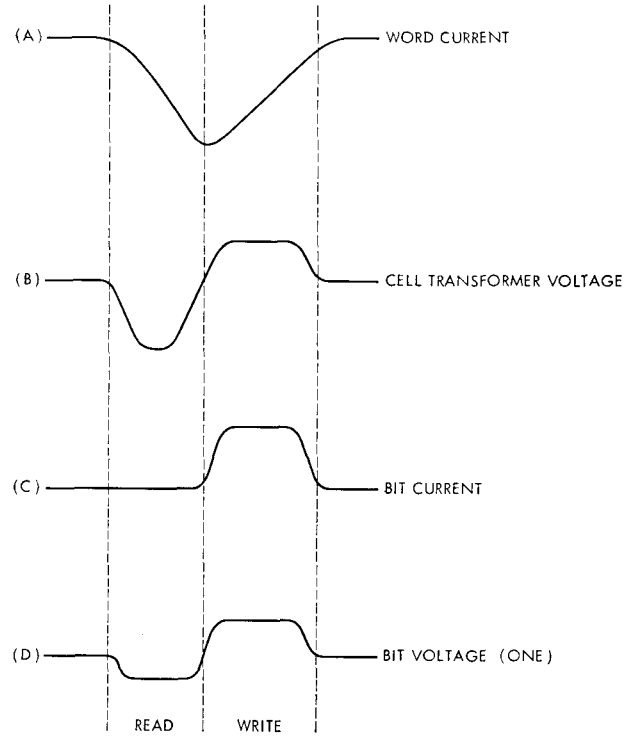
- *Word axis*

The word-driver circuit provides a triangular-shaped current waveform into the word line, as shown in Fig. 4. The word line itself consists of a pair of parallel wires on a printed wiring board which are short-circuited at the far end. The word line is driven through a transformer so that the voltages appearing at the driving ends are balanced with respect to ground. By this means, capacitive coupling into the individual storage cell secondaries tends to cancel out. The cell transformer is designed to differentiate the word-current waveform. The voltage that appears at the two terminals of the cell transformer is shown in Fig. 4b.

- *Bit axis*

The bit axis represents a lossy transmission line with phase distortion. An analysis of the bit axis propagation characteristics was made by Barbetta.[10] The basic shape of the response when typical circuit constants are present is shown in Fig. 5. Note that the waveform is characterized

Figure 4 **Idealized waveforms.**



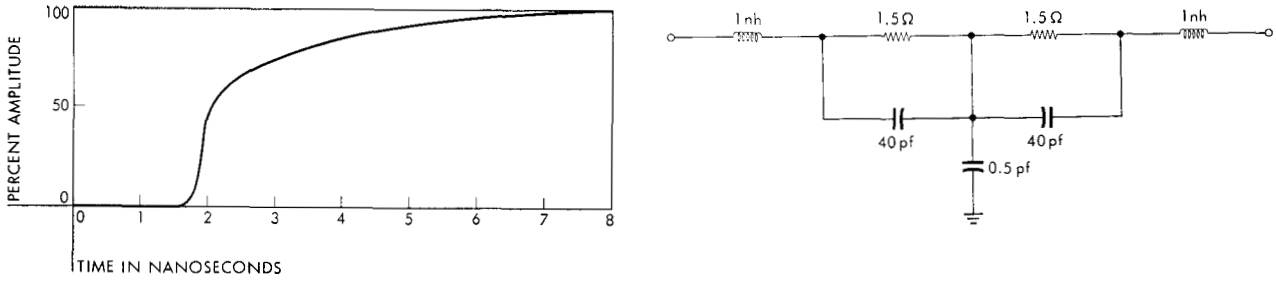


Figure 5 **Calculated response of lossy transmission line made up of 64 sections.** *The diagram on the right is the equivalent circuit for a single section.*

by a sharply rising leading edge followed by a slower rise to the final value. In a small memory of about 16 words, the bit-line delay is short enough so that the regeneration circuit can be connected to one end of the line, and the other end can be grounded. With a larger memory of about 64 words, two things can be done to minimize the regeneration delay. In the first technique, the array can be constructed of two halves, which can be folded to give the bit line a hairpin configuration. This permits sensing and driving the two ends of the line at one point on the array. The other technique is to set the detection threshold of the sense amplifier at a lower point on the signal (e.g., 50%) so that recognition occurs earlier. This is possible because of the excellent ONE-to-ZERO ratio of the signal.

- *Cell transformer*

Calculations have been made to find an optimum design of transformers suitable for this type of high-frequency application. One means of checking the calculations has been the construction and measurement of cell models which were twenty times actual physical size. These scaled models presented electrical parameters large enough to be accurately measured.

The transformer must be designed to have a high ratio of mutual inductance to mutual capacitance and a very high resonant frequency. This is done by carefully controlling the winding spacing. A printed circuit transformer so designed is shown in Fig. 6. A mechanically wound transformer based on the same criteria is shown in Fig. 7. Each transformer has a symmetrical primary. By using a word drive that is balanced to ground, the effects of primary-to-secondary capacitance are minimized. To preserve inherently good ONE-to-ZERO ratio of the cell, and the good operating tolerances, shielding between bit lines has been found to be necessary.

Driving circuits

Experimental circuits have been designed and tested to determine the speed capabilities of such a memory system. Although such information on the ultimate speed could be derived only from a fully populated operational model, some critical experiments have been performed.

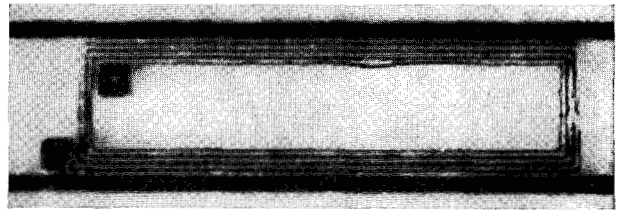


Figure 6 **Printed circuit transformer.**

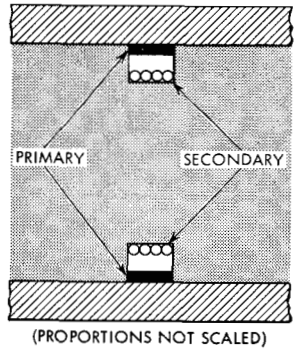


Figure 7 **Mechanically wound transformer.**

A word driver capable of driving 72 bits at 10-nsec READ-WRITE cycle time is shown in Fig. 8. This circuit has been operated at a repetition rate of 100 Mc into a dummy line simulating 72 bits. Sensing and bit drive circuitry capable of reading and regenerating stored information has been tested and is shown in Fig. 9. The photographs show the physical arrangement of the circuit elements in Figs. 8 and 9.

Over-all considerations

The new memory configuration provides substantial operating improvements. A large output signal (typically

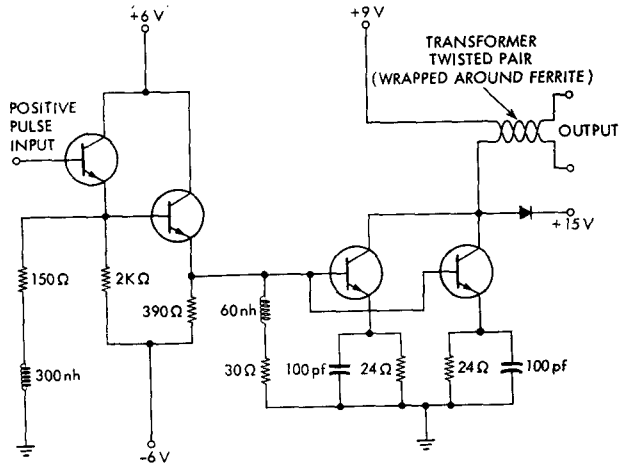
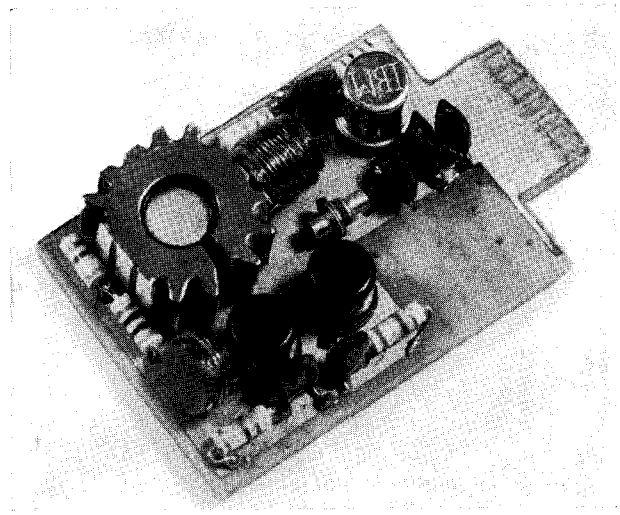


Figure 8 **100-Mc Word driver.**



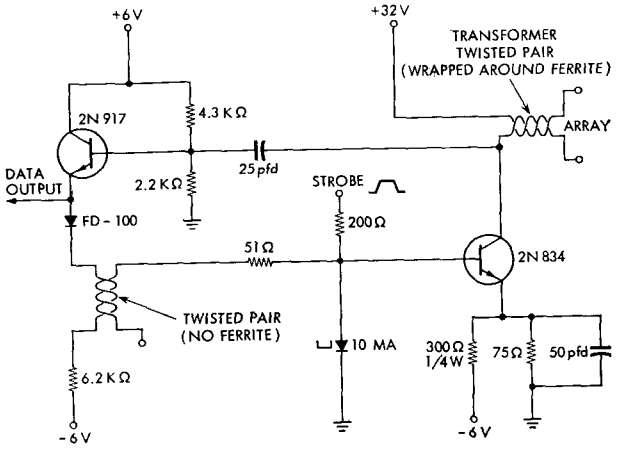
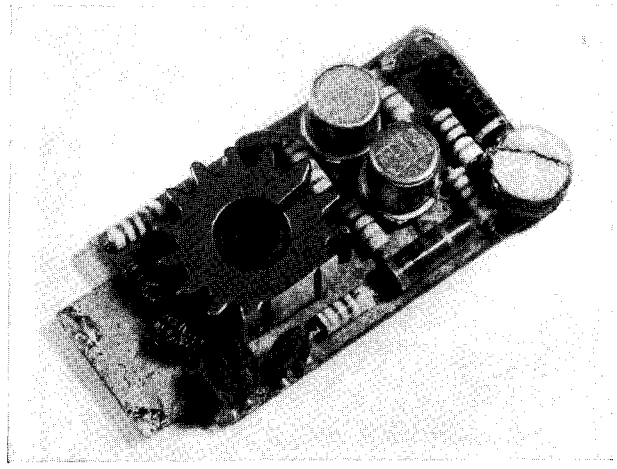


Figure 9 **Combined bit driver and sense amplifier.**



400 mv) is obtained from the array, with a signal-to-noise ratio of about 20 to 1 (Fig. 11). In addition, the bit-drive axis requirement is very small (typically less than 10 ma). This favorable combination vastly simplifies and thereby hastens the process of regenerating stored information after it has been destructively read. As previously described, the differentiating transformer requires only a monopolar input current drive to the primary. This simplification also results in increased circuit speed. The driving impedance of the word line can be adjusted by changing the word-drive output transformer turns ratio to provide high-efficiency matching to the drive transistors. As an added benefit, diodes with higher peak-current characteristics (typically 20 ma or more) may be used in the array. Such diodes are less fragile and easier to make than the lower-current variety used in most earlier memories. These improvements are made at the expense of array propagation characteristics and the inclusion of a high-frequency transformer in each cell.

Applications of the new system

The new memory system described herein offers a considerable flexibility of design, with the cell transformer as the key item that can drastically change the characteristics of the memory array. In a recent production model of an IBM 7030 system, a tunnel-diode memory was included as an index register.* It contains 17 words of 73 bits each. In this particular memory, it was desired to utilize circuit speeds that would be compatible with the rest of the data processing system. As a result, the cell transformer was designed with a ferrite core to increase the mutual coupling between the primary and secondary. The increased mutual

* *Note added in proof:* See *Electronic Equipment Engineering* **11**, No. 6, 16, (June 1963).

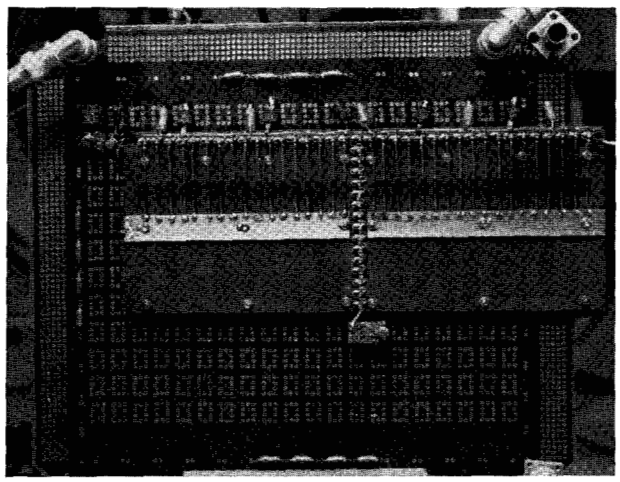


Figure 10 **Cross section of scratch-pad 16-word, 36-bit tunnel diode memory with simulated loading on all bits.**

coupling permitted the use of slower waveforms and simplified the problem of making the memory circuits compatible with the circuits contained in the data processing system.

An example of construction and design for higher speed is illustrated by a scratch-pad memory system for a high-speed arithmetic unit utilizing ACP circuits. The circuits and array of this system are designed for operation in a 20-nsec READ-WRITE cycle. Construction of the fully populated model has not yet been completed. This memory was designed to contain 16 words with 36 bits per word. The pictures and waveforms shown in Fig. 10 and 11 are from a cross-sectional engineering model.

To simplify the construction of this model, an air-core transformer was designed that utilized a secondary winding made of small-diameter wire. A controlled air gap was used between the primary and secondary to decrease the capacitive coupling. Figure 7 shows a cross-sectional view

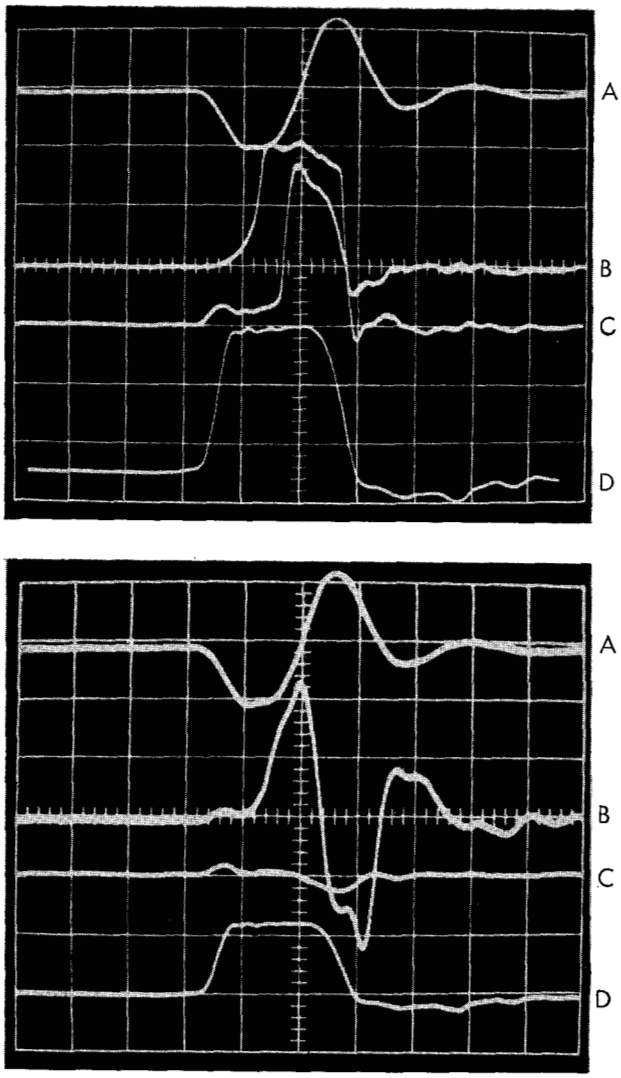


Figure 11 **Scratch-pad tunnel diode memory waveforms.** *Above: (A) Word driver, 10 v/cm. (B) Memory bit tunnel diode, 200 mv/cm; (C) sense tunnel diode, 200 mv/cm; (D) strobe, 1 v/cm. Below: (A) word driver, 10 v/cm; (B)* ONE *input to sense; (C)* ZERO *amplifier 200 mv/cm; (D) Strobe = 2 v/cm. Horizontal: 5ns/cm. (In the photographs, one large division corresponds to one cm.)*

Figure 12 **Secondary winding of word axis transformer. Magnification 17×.**

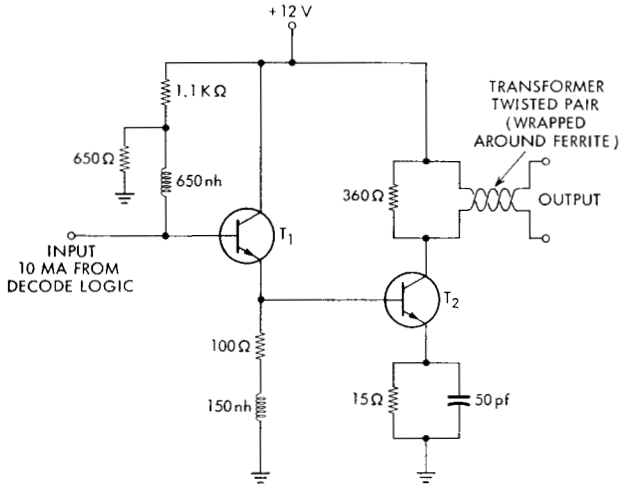


Figure 13 **Word driver for scratch-pad memory.**

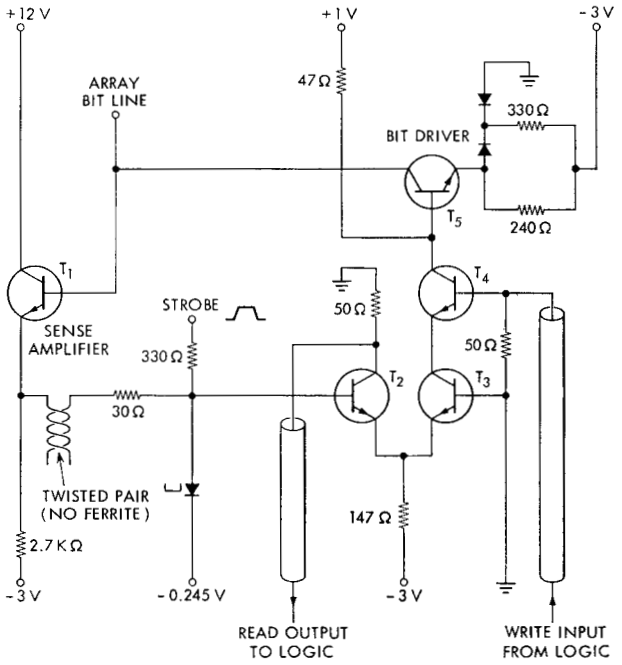


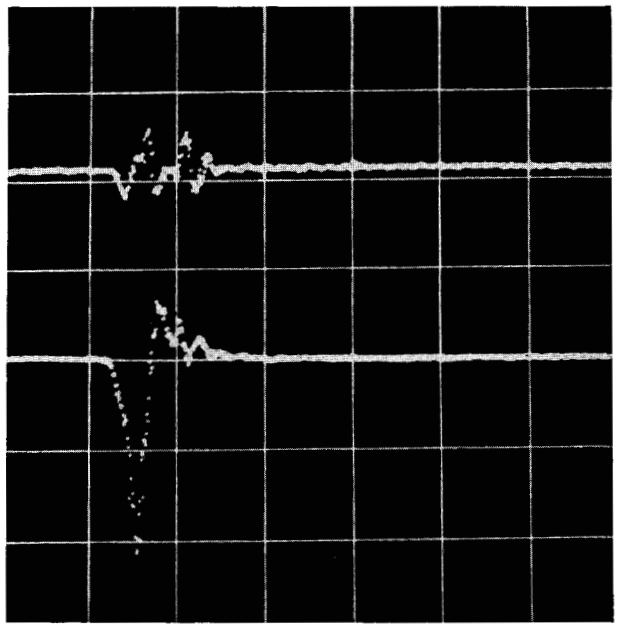
Figure 14 **Bit driver control logic and sense amplifier.**

of the transformer. Figure 12 shows a photographic view of a transformer secondary prior to the assembly of the secondary winding between the circuit boards containing the strip-type transmission lines used for the primaries. After the transformer assembly is completed, the tunnel diodes and resistors are mounted on the pins protruding from the top of the assembly. The over-all matrix assembly is mounted on a multilayer laminated wiring board that is used for the associated circuitry. The fully populated memory with all decoding and driving circuitry will be constructed on a 6″ × 10″ portion of a multilayer wiring board. Figures 13 and 14 show word and information control circuits used in the scratch-pad memory system of Fig. 10.

Nondestructive read-out experiments

Although only the destructive read-out form of operation of the new memory system has been described, a non-destructive-read-out operation is also possible. In applications where this mode of operation can be utilized to advantage, increased speed can be obtained with only a small additional amount of added circuitry. By restricting the word drive current to a fraction (typically one-fourth) of its normal value, the cells can be interrogated without changing their state of storage. A typical output signal for this mode of operation is about 100 mv. Figure 15 shows the ONE and ZERO signals from a cell that has been interrogated in this manner.

Figure 15 **NDRO signal from tunnel diode cell.** *Upper trace,* ZERO*; lower trace,* ONE. *Vertical coordinate, 10 nsec/div; horizontal, 50 mv/div.*



Conclusions

The series-coupled approach to the design of a tunnel-diode memory system represents a fresh and promising attack on the problems associated with high-speed memory design. It has been shown in this paper that this design

approach substantially simplifies the driving and sensing circuits, which have been major limitations of previous systems.

For example, the unipolar current waveform plus the modest current requirements of the word driver result in a fast and simple word driver circuit. The scratch-pad memory driver of Fig. 13 uses only two transistors and the 100-Mc word driver of Fig. 8 uses four transistors. The most attractive arrangement for a high-speed system is to have one driver per word. Because the word driver circuits are simple, this is a practical method.

When the sensing and bit driving functions are combined in one circuit, maximum advantage can be taken of the large signal and small bit-drive requirement. Such a combined regeneration circuit is illustrated in Fig. 9, which contains only two transistors and a tunnel diode. In the case of the scratch-pad memory system described, the particular applications required additional control circuitry in the regeneration loop as is illustrated in Fig. 14.

Configuration of the ACP circuits suitable for word-address decoding have been studied.* Because of the powerful logic capabilities of these circuits, a 64-word decoding network can be accomplished through only two circuit levels using less than 200 semiconductor devices. This logic capability permits very short decoding times.

The maximum size and speed limitations of this type of memory system have been considered. Memories of up to 64 words (72 bits/word) appear to be practicable for high-speed operation when properly designed and packaged. From experimental and theoretical considerations of the driving and regeneration circuits, address-decoding network, and array delays, the authors conclude that complete READ-WRITE cycle times of 10 to 20 nsec for such a 64-word system can be achieved.

* To be published in the *IBM Journal*.

Acknowledgments

In a long-range project such as this, many people have made contributions to the over-all results but unfortunately only a few can be specifically mentioned. In particular, F. L. Post and R. J. Barbetta analyzed the bit-line characteristics, and C. H. Stapper investigated transformer characteristics. H. A. Fonatsch displayed unlimited patience in constructing miniature assemblies, and L. E. LaFave skillfully assisted by the construction and testing of circuits. K. Roche was responsible for the mechanical design of the array. J. K. Shortle and his group designed and built the tunnel-diode memory for the IBM 7030 system.

References

1. J. A. Rajchman, "Computer Memories: A Survey of the State-of-the-Art," *Proc. IRE*, **49**, 104 (1961).
2. R. C. Sims, E. R. Beck, Jr., V. C. Kamm, "A Survey of Tunnel-Diode Techniques," *Proc. IRE*, **49**, 136 (1961).
3. M. M. Kaufman, "Tunnel Diode Tenth Microsecond Memory," *IRE International Convention Record*, 114 (1960).
4. W. D. Pricer, P. A. Henderson, A. S. Myers, unpublished work.
5. J. C. Miller, K. Li, A. W. Lo, "Tunnel Diode as a Storage Element," *Digest of Technical Papers*, International Solid State Computer Conference, p. 52 (February, 1960).
6. G. B. B. Chaplin, P. M. Thompson, "A Fast Word Organized Tunnel-Diode Memory Using Voltage-Mode Selection," *Digest of Technical Papers*, 1961 International Solid State Circuits Conference, p. 40.
7. S. Takahashi, O. Ishii, "High Speed Memory Uses Tunnel Diode Circuit," *Electronics*, **34**, 66 (October 20, 1961).
8. D. L. Berry, E. A. Fisch, "High Speed Tunnel-Diode Memory," *Digest of Technical Papers*, 1961 International Solid State Circuits Conference, p. 112.
9. M. M. Kaufman, "Tunnel-Diode, Tunnel-Rectifier 15 Nanosecond Memory," *Solid State Design* **3**, No. 2, 23 (1962).
10. R. J. Barbetta, "Analysis of a Tunnel Diode Transmission Line," IBM Data Systems Division Technical Report TR00.969.

Received March 14, 1963