J. R. Kiseda
H. E. Petersen
W. C. Seelbach
M. Teig

A Magnetic Associative Memory

Abstract: This paper describes a computer storage system in which data flows in and out of the memory on the basis of content rather than location (address). In addition, a small experimental model of this system is described, using ferrite cores as novel associative memory storage elements.

Introduction

In some computer applications there is a need for the retrieval of stored information on the basis of content rather than location.[1,2] Storage systems with such retrieval capabilities have been termed *associative memories*.[3] These systems reduce, to a considerable extent, the housekeeping tasks inherent in conventional memories. Although the same type of retrieval could be accomplished in conventional memories by various program stratagems, those methods are somewhat inefficient.

The basic idea of associative memories is not new and has been implied or directly mentioned in the references listed.[4-8] Some of these systems have attempted to implement associative memories by using cryotrons. This paper will present a novel approach to the design of practical associative memories, first, by examining the logical requirements of a basic associative memory register; second, by implementing this basic register with presently available devices that are economically feasible; and last, by indicating some critical design parameters.

In addition, a small model of a basic associative memory system using ferrite toroids will be described. This model demonstrates the technical feasibility of operation of the individual components in an integrated system.

Finally, in order to give the reader some idea of the potential utility of associative memories, a large, fully associative memory system will be described, along with a brief discussion of its capabilities from the programmer's point of view.

General concepts

The presence and location of a word stored in an associative memory can be determined by specifying any known portion of this word. This known portion of the word will be referred to as the *associative criterion*. Thus, a single word in memory may have a multiplicity of associative criteria. Also, several words may have a common associative criterion. Hereafter, by definition, a unique associative criterion is one which results in the location and/or retrieval of a single stored word and will be referred to as the *unique case*. A non-unique associative criterion can result in the location and/or retrieval of more than one word in storage and will be called the *non-unique case*.

The associative criterion consists of two parts—the data portion and the mask portion. The data portion consists of the known segment of the word being sought. The mask portion represents those bit positions in the word which should be ignored during the search.

In order to locate a word stored anywhere in an associative memory, the following capabilities must be realized: there must be a means for performing a nondestructive comparison of the associative criterion with every word in memory; this must be coupled with a means for identifying a matching word; and finally there must be a means of access to the matching word location to provide a subsequent readout.

Let us first consider the comparison (associative search). Assuming that the stored data is to be interrogated nondestructively and that both the data and mask portion of the associative criterion are in binary form, then the element which makes a bit comparison must have the following truth table:

Criterion		*Storage*	
Mask	*Data*	*0*	*1*
0	0	**0**	**0**
0	1	**0**	**0**
1	0	**0**	**1**
1	1	**1**	**0**
		Output of a comparator	

In the truth table a "0" in the mask column signifies a "masked" bit.

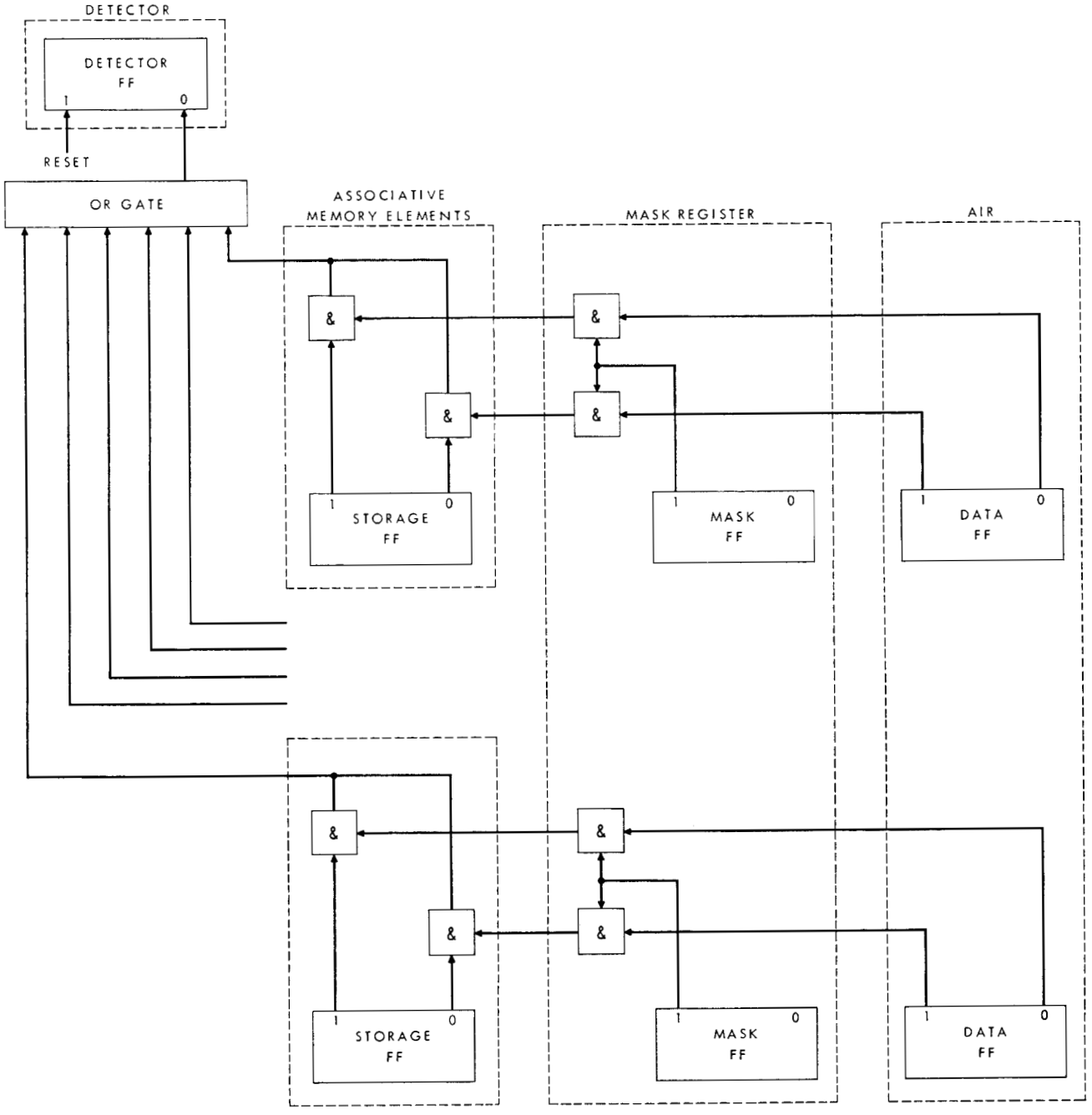
Next, let us consider the capability of recognizing a match (detection). The detector should be able to distinguish between a "match" condition ("0" in the truth table) and a "mismatch" condition ("1" in the truth table) at the output of a comparator element. The presence of one or more mismatches in a memory word must change the detector state from its original match condition.

Finally, consideration of a means of access to the matching word will not be mentioned now, since the problem is a simple one employing known techniques and in no way approaches the complexity of the capabilities discussed in the previous two paragraphs.

Logical implementation of general concepts

A simple logical representation of an associative memory register in combination with a detector and its criterion inputs are shown in Fig. 1. The register containing

Figure 1 **A logical representation of an associative memory register.**



the data portion of the associative criterion will be referred to as the *associative interrogation register*, or AIR. The register containing the "mask" portion of the associative criterion will be called the *mask register*.

The logical blocks, connected as shown, can perform the basic function of an associative memory. In short, it can be seen that the AIR presents search data to the memory element to be nondestructively compared with the stored data. For any bit position not to be searched, the mask will block the output from the AIR. Any "mismatch" outputs from the memory elements will trigger the detector into a mismatch state.

Hardware implementation of Fig. 1

In order to efficiently implement the word register in Fig. 1, the nondestructive storage element and the comparator should be combined into an element which performs according to the previously stated truth table. This element will be called an *associative memory element*. Figure 2 shows two logical equivalents of such an element. In Fig. 2(a) the single logical block shown could perform as an associative memory element.

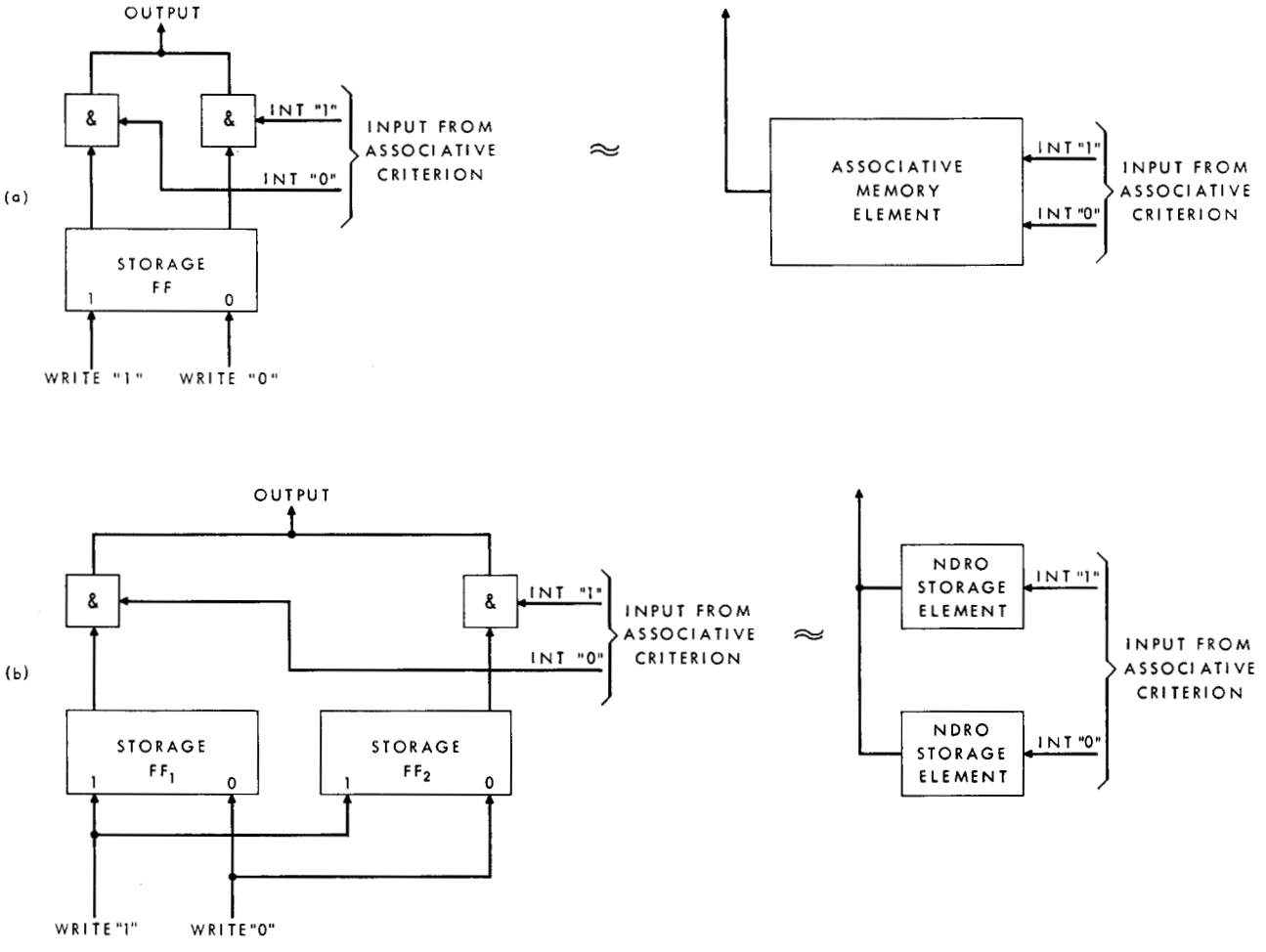
Figure 2(b) shows how an associative memory element can be represented by a combination of two nondestructive readout (NDRO) memory elements. Now a variety of devices (multipath cores, tunnel diodes, card read-only devices, et cetera) could be used since the system design requires the memory elements to possess only good NDRO capabilities.

Since we would like to build an associative memory system using NDRO magnetic memory elements, we can consider multi-aperture devices, Newhouse-type operation[9] and some type of partial-switching technique. Although all of these devices and techniques can be used, most of the presently available devices and operating schemes exhibit low signal/noise ratios, low signal levels and complexity in writing and/or wiring. For this reason a new NDRO memory technique, discovered in the course of this effort, has been utilized.

Two ferrite cores, operating in this new NDRO mode, when suitably interconnected, yield an associative memory element which operates according to the stated truth table. The detailed operation will be described later.

The OR operation in Fig. 1 can be accomplished by

Figure 2 **Logical equivalents of an associative memory element.**



linking all the associative memory elements contained in one register with a single word-sense loop which can include the detector element. This then permits the familiar word-organized array configuration.

Although, in theory, a parallel-by-bit, parallel-by-word associative search is possible, finite signal/noise ratios of the memory elements require a serial-by-bit, parallel-by-word search. Since the search is serial by bit, the detector, which at the start of the search cycle is in the match state, should change state the first time a mismatch appears from any bit on its word line. It should remain in a mismatch state until reset by some external signal. This operation suggests that the detector be a binary storage device, such as a magnetic core.

The toroidal associative memory device and array

The addition of a dc restoration field significantly improves the NDRO characteristics of toroidal ferrite storage cores. This new technique is based on the fact that "minor" static hysteresis loops have lower thresholds than the "major" loop. This property permits the biasing of a ferrite core with a magnetic field in excess of some minor loop threshold but below the threshold of the major loop.

The two states of this element (ZERO and ONE) are defined in a manner similar to a conventional memory core, namely, the positive and negative remanent flux states, except for a shift in the operating points due to the presence of the bias field.

The nondestructive interrogation of the ONE state of the core is performed by applying a current pulse to the core in a direction opposite to the direction of the bias current and of such an amplitude and duration as to cause partial irreversible switching. In addition there appears to be some reversible flux change because of the viscosity effect.[11] The bias will now restore that portion of the irreversibly switched flux which has a threshold lower than the restoring bias. After a few interrogations, the core will be in a "disturbed ONE" state which is on a minor loop but close to its initial state on the major loop. Once the core is in its disturbed state, any further interrogation will not cause any additional "creeping" of the core. It should be noted that for successive interrogations there is a 20% increase from the first to the n^{th} voltage output. This may be explained by the "re-entrant loop" phenomenon.[10,16]

The interrogation of the ZERO state of the core results in a small flux change due to the shuttling on the major loop. Hence, the core operates as a nondestructive readout binary memory element.[9]

A typical voltage response, of this element, to a 100 nsec, 1.4 AT current pulse can be seen in Fig. 3.

This technique was utilized in a two-core-per-bit associative memory element as shown in Fig. 4. Two pairs of orthogonal wires per core are required. The operation of the cores can be described with the aid of the ϕ-NI relationships of the two cores also shown in Fig. 4. At the beginning of a CLEAR-WRITE cycle, both cores are brought to nearly identical ϕ-NI points on their corresponding loops by the application of the B bias pulse. The function of the B bias pulse, as applied to the M' cores, is to overcome the dc A bias and exceed it by an amount equal to the magnitude of A bias. Hence, both cores of the two-core-per-bit arrangement will switch in unison during the application of the CLEAR-WRITE pulses. The switching time of the CLEAR operation can be arbitrarily fast because of the linear selection organization. The WRITE time on the other hand is limited by the 2:1 selection writing arrangement used. By setting the magnitude of the A bias to the vicinity of the core dc threshold, write speeds approaching $\frac{S_w}{2H_0}$ can be achieved, i.e., one-half the normal 2:1 selection write times are obtainable in contrast to unbiased or conventional modes.

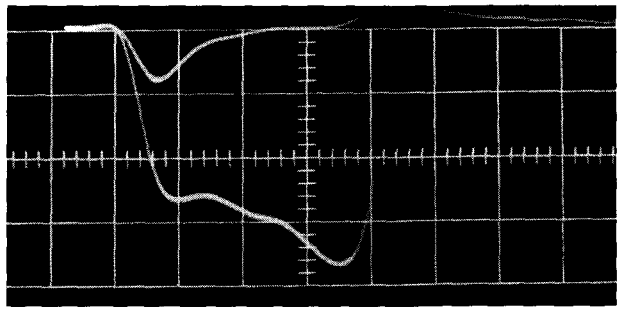


Figure 3 **Typical match and mismatch ("zero" and "one") voltage outputs from a 50×80×25 mil ferrite core.**
Vertical scale: 100 mv/turn/div. Horizontal scale: 20 nsec/div.

The word-sense loop as shown in Fig. 4 is wound series opposing and hence effectively cancels the induced signals that would normally appear in the detector sense loop during a CLEAR-WRITE cycle. This decoupling between the CLEAR-WRITE drive lines and the word sense loop is essential for the realization of low-impedance magnetic-semiconductor detectors of low cost. It is clear that in the absence of decoupling, the loading action of the sense loop could be appreciable, especially when a majority of the cores in any register of reasonable word length are switching.

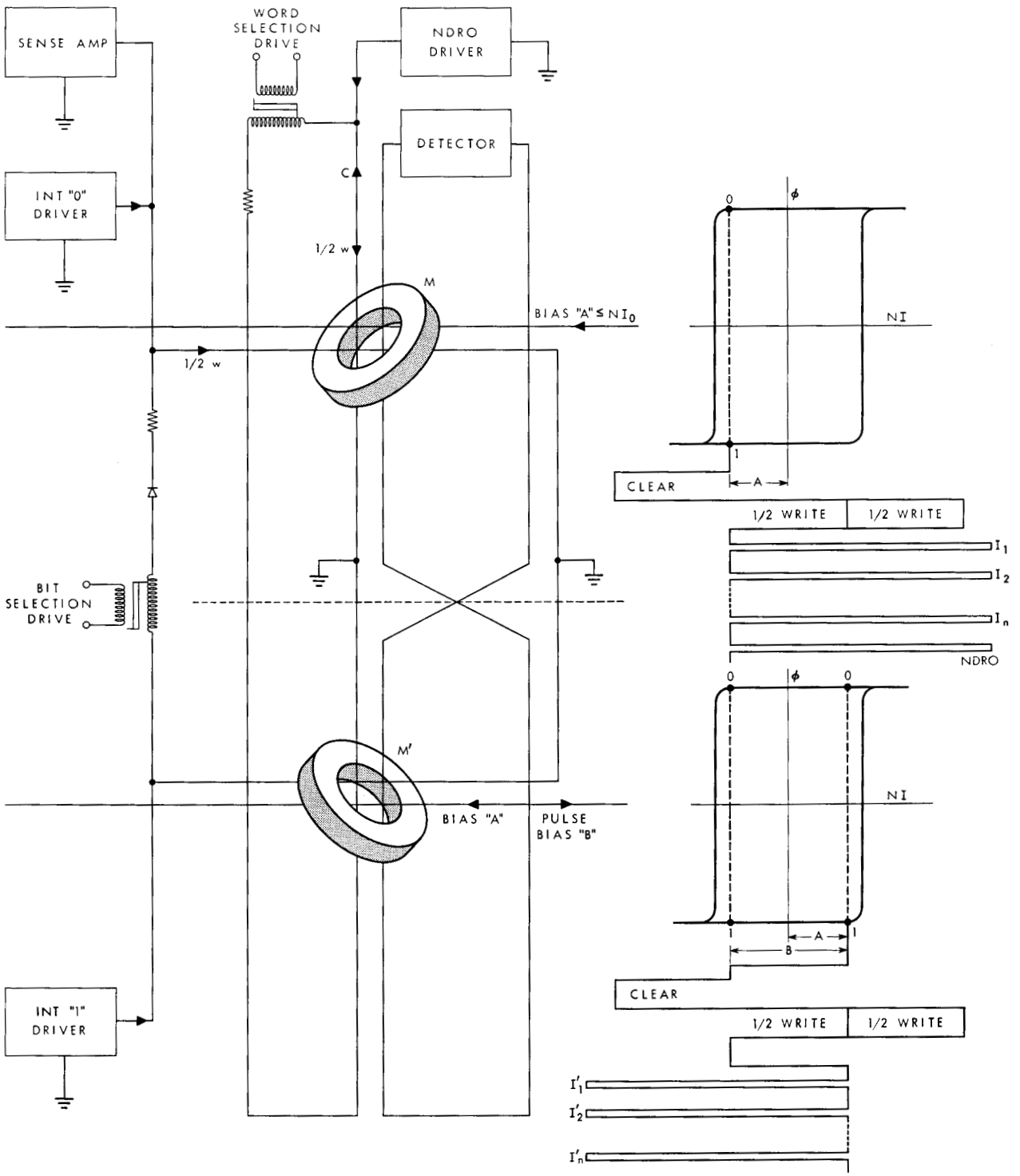
The interrogation, as previously stated, is parallel-by-word and sequential-by-bit. Depending on whether the search is to be for a ONE or ZERO, one core or the other of a pair is always interrogated with a unipolar nondestructive current pulse. On the other hand, if a bit portion is to be masked, neither core is interrogated.

By judicious grounding of a bit drive line, sharing of this line with the interrogation and digit sense can be accomplished as shown in Fig. 4. Since only one or the other shared digit line can be energized by an interrogation current at a given time, the information state of a core in a pair can be effectively sensed by the detector.

Experimentation has shown that a unipolar interrogation sequence, as is the case of the two-core-per-bit or-

ganization under discussion, has proven the most desirable since a stable residual minor loop condition is acquired in one core of the pair after a measurable number of unipolar interrogations following a WRITE cycle. Once the stable minor loop point is reached, the mismatch signals induced in the detector sense loop tend to stabilize. The match signals, on the other hand, do not change significantly between the first and n^{th} interrogation. This stabilization of minor loop conditions cannot be achieved with presently available magnetic materials operating in

Figure 4 **Core array wiring Φ—*NI* relationships** *(see text, p. 109).*



a bipolar mode typified by the one-core-per-bit arrangement.[3]

The flux transfer and detection problem

The general problem of the flux transfer between an interrogated storage core and the detector is common to both one- and two-core-per-bit organizations. See the one-core-per-bit organization shown in Fig. 5. The bits of this register are labeled B_1 through B_m and, as indicated, are coupled to a detector (D) through a loop of wire. A nondestructive search is accomplished by sequentially interrogating the a_i windings of Fig. 5 in this and all other memory registers. Therefore only one core in a given register will be energized at any given time. The energized or transmitter core will induce a signal in the loop which is to cause the detector or receiver core to change its state. The presence of the unselected cores, together with the distributed impedances of the coupling or sense loop, cause attenuation of the transmitted signal. The analysis of the relationships between the transmitter, load and receiver is complicated because of the magnetic nonlinearities. The unselected cores and distributed impedances comprise an attenuation network. The equivalent lumped series inductance and resistance of the loop itself can be determined by standard means. Since register sense lines can be made electrically short in a word-organized system, transmission line effects can usually be neglected. An equivalent parallel LR circuit representing a core driven in a memory array by half-select current pulses has been reported in the literature.[12] A parallel and independent investigation by the authors has substantiated the validity of such a model in conductively coupled transfer circuits, as shown in the Appendix.

The following analysis considers the case in a two-core-per-bit arrangement where a mismatch or ONE signal is to be transmitted to a detector via the word-sense loop. Although no analysis of the transmission of a match is presented, a similar approach can be used.

Flux transfer analysis of an *m* bit register

An equivalent circuit representation of an interrogated storage core developing a mismatch signal across its output coupled to a magnetic detector through $2m-1$ cores is shown in Fig. 6. The assumed models for the interrogated memory core and detector core shown in this figure are represented for simplicity by single-shell analogs developed in the Appendix. Circuit equations can be written relating the circuit response to the drive current in terms of equivalent circuit parameters. From these equations, the task of achieving an optimum design can be realized with a minimum of experimentation.

Two conditional requirements are placed on the analysis:

1. The loop current $[(i)t]$ must be constrained such that its instantaneous peak does not overcome the threshold and disturb the information state of unselected cores in the register. In theory the bias restoration field strength can approach H_0 only when the loop current $[(i)t]$ is zero, since the direction of this loop current is in the same direction as the dc restoration bias. In practice a bias field strength 90% of H_0 and loop currents exceeding H_0 by 10% at pulse widths of 0.1 μsec do not disturb the state of unselected cores.

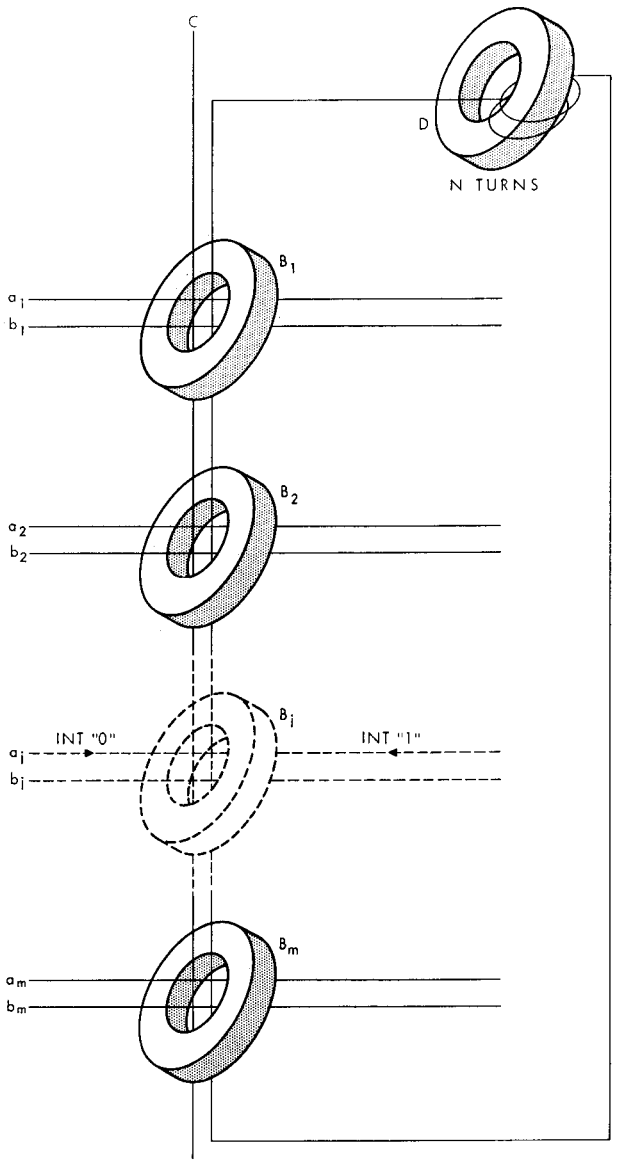


Figure 5 **An associative memory word register.**

2. The volt-time integral of $e_d(t)$ must be at least equal to the flux linkage input $(N\phi_d)^*$ of a purely magnetic detector. Only the initial unipolar area of $e_d(t)$ is considered, since it is assumed a detector can be constructed that will switch irreversibly on a given input polarity and become decoupled on the ensuing fly-back or opposite polarity portion of the transmitted signal (see Fig. 8). Thus, irreversible switching of the detector must be ac-

*Subscript d refers to the detector core parameters.

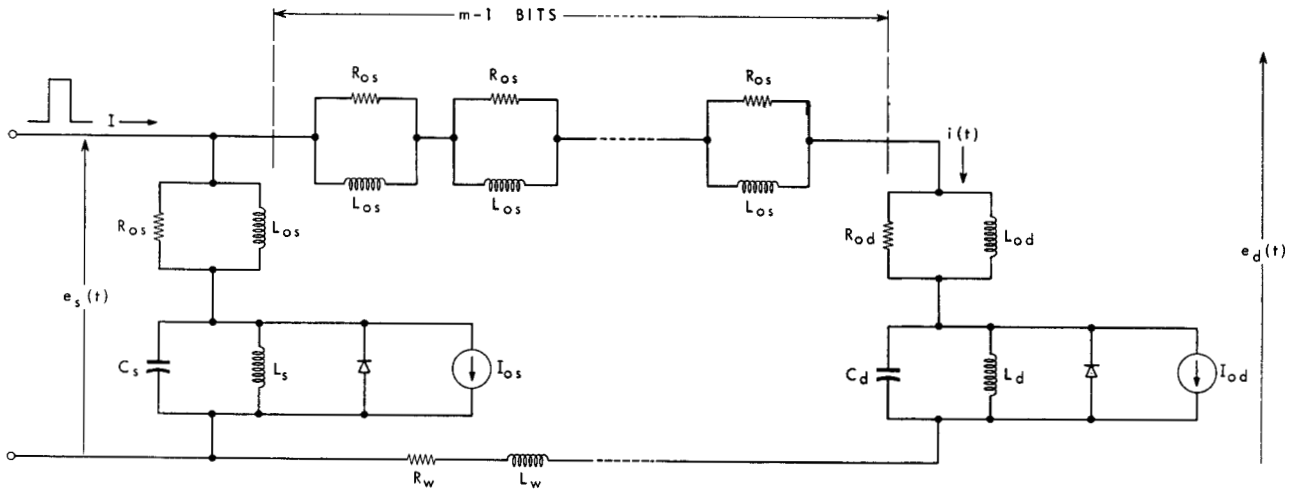


Figure 6 **The sense loop equivalent circuit.**

complished during a ONE condition even though the volt-time integral of the ONE and the ZERO signals are by nature zero over a complete cycle, differing only in peak magnitudes during the cycle.

While all the essentials are included in the equivalent circuit representation of Fig. 6 the form of the resulting equations do not lend themselves to simple calculations. The difficulty arises when the reactive elements, the series wire inductance L_w and the parallel equivalent unselected core inductances L_{0s}* are included in a general analysis. The problem can be greatly simplified by considering the special case where the intrinsic time constant, L_{0s}/R_{0s}, is long relative to the interrogation duration and the time constant, $L_w/\sqrt{L_d/C_d}+(m-1)R_{0s}$, is short relative to the interrogation duration time τ and by neglecting R_w, R_{0d}, and L_{0d}. When practical situations are examined, these assumptions seem justified.

In this manner the problem reduces to the solution of a simple resistance divider network where the interrogated and detector cores are treated as resistors of magnitude $\sqrt{L/C}$ with appropriate threshold circuitry. This represents a maximum attenuation condition in terms of flux transfer, and hence a "worst case."

For this special case where the search current pulse width is such that L_{0s}, R_w, L_{0d}, R_{0d}, and L_w can be neglected, it can be shown that the flux linkage relation of the loop is

$$\alpha\phi_s=\frac{l_d(2m-1)K\phi_s[S_{wd}+H_{cd}\tau]}{l_sS_{ws}N}+N\phi_d, \tag{1}$$

where

$$\frac{K\phi_s}{S_{ws}l_s}=R_{0s}.$$

The other parameters are discussed in the Appendix.

It can also be shown that the reversible flux ($\alpha\phi_s$) generated at an interrogated storage core can be most efficiently transferred, in terms of search drive power, to the detector when the two terms of Eq. (1) are set equal. It follows that the number of bits in a register is as shown

$$m=\frac{N_\alpha l_sS_{ws}}{4Kl_d[S_{wd}+H_{cd}\tau]}+\frac{2}{1}. \tag{2}$$

For practical register lengths the induced nondestructive voltage of an interrogated storage core would be essentially the open circuited or unloaded voltage response. It follows from this consideration that the interrogation drive current, I, applied to a storage core is then

$$I\cong l_s\left[\frac{S_{wrBs}}{\tau}+H_{0Bs}\right], \tag{3}$$

where the subscript B refers to the biased core.

The peak power during an interrogation pulse supplied to the storage core is

$$P_s\cong\left[\frac{S_{wrBs}}{\tau}+H_{0Bs}\right]\frac{2N\phi_dl_s}{\tau}. \tag{4}$$

Dividing Eq. (4) by (1) yields a useful expression specifying the amount of peak interrogation power required as a function of bit storage capacity. For example the total peak power that a search driver must be capable of supplying is the power per bit of storage multiplied by the total bit volume of the array. The result of the division of Eq. (4) by (1), neglecting the one-half in Eq. (1), is

$$\frac{P_s}{\text{bit}}=\frac{P_s}{m}\cong 4K\left[\frac{1}{\tau}+\frac{H_{0Bs}}{S_{wrBs}}\right]\cdot V_d\left[2B_{rd}\right]\left[\frac{S_{wd}}{\tau}+H_{cd}\right], \tag{5}$$

where V_d is the volume of the detector element. Eq. (5) indicates the general design trend a magnetic detector should take, since the peak power, or the product of back voltage and applied current requirements during

*Subscript s refers to the storage core parameters.

interrogation, represents one of the more difficult problems encountered in the design of high-speed magnetic memories.

For a given interrogation pulse width, τ, it is apparent that the choice of detector material and geometry should be made on an energy basis which implies the use of materials having low magnetic moments, fast-switching coefficients and low thresholds. The geometry of the device should be such that the total magnetic volume is as small as practical. In this way the peak interrogation power requirements per bit storage can be minimized.

It should be noted that since P_s is inversely proportional to τ^2 (see Eq. (5)) a moderate increase in interrogation pulse width significantly reduces interrogation power.

Detector

The function of the detector is to switch irreversibly upon the first mismatch condition appearing in an interrogation or search cycle and to remain in that state regardless of the pattern of inputs for the remaining portion of the interrogation cycle. On the other hand, the detector must not switch on *m* ZERO signals throughout the interrogation cycle. It is clear that a single core detector embodiment as shown in Fig. 5 will have difficulty in remaining in a "set" state after a mismatch has been detected because of the presence of the fly-back or overshoot portion of the nondestructive ONE signal. A three-core detector and an equivalent multipath variation, circumventing this inability to decouple and remain in a set state, is shown in Fig. 7. The operation of the three-core embodiment is as follows:

1. Initially all detector cores *A*, *B*, *C* are reset.

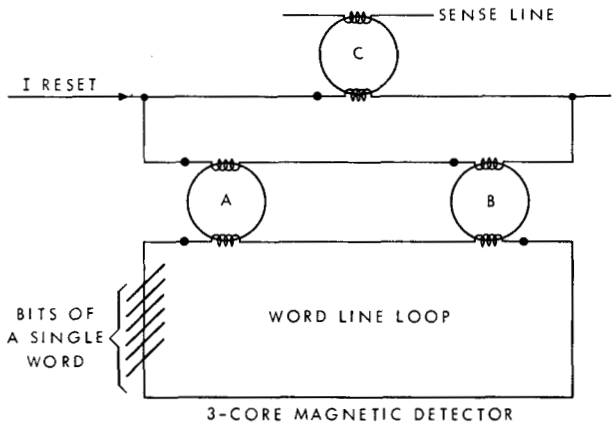
2. Zero signals are below the threshold of the circuit and thus effect no change.

3. With the initial portion of a ONE signal causing a clockwise current flow in the word loop, *B* will switch and in turn switch Core *C*.

4. With the overshoot of the ONE causing a counterclockwise current flow in the word loop both Cores *A* and *B* will switch in unison, unaffecting Core *C*.

5. After Steps 3 and 4 have occurred, the circuit is insensitive to further signals produced in the word line loop.

Therefore, the circuit performs the necessary function of recording the presence of a mismatch corresponding to a ONE signal between the stored information and AIR. For purposes of analysis the three-core arrangement can be approximated by a single core having twice the mean magnetic path length of a single core. The fly-back or overshoot portion of the ONE signal in the analysis can now be disregarded since the analysis need only be concerned with the initial or unipolar portion of the ONE signal. The operating efficiency in terms of peak interrogation power per bit of storage is greatly increased by adding an inexpensive transistor to the core circuits



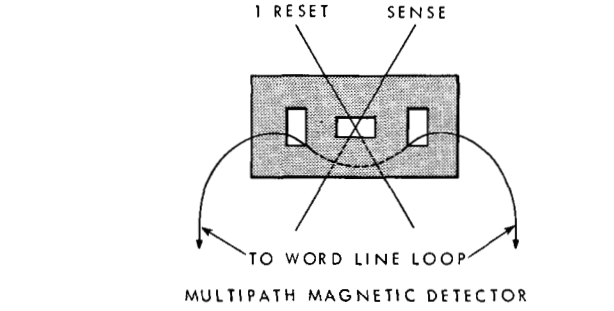


Figure 7 **Two variations of magnetic detectors.**

of Fig. 7 to form a blocking-oscillator mode detector, Fig. 8. This improvement in operating efficiency is due to the fact that the interrogated storage core need only supply the trigger energy necessary to initiate the blocking oscillator action upon which the detector element switches to the "set" state. Experimental blocking-oscillator detectors have been built and operated. These blocking oscillators require an order of magnitude less input switching energy from the word loop line than the all-magnetic counterpart. For purposes of analysis the blocking-oscillator arrangement can be handled in a manner similar to the case where purely magnetic devices are used. The input to the blocking-oscillator detector can be represented by the equivalent circuit corresponding to the magnetic portion of the detector. Experimentation will yield the trigger flux linkage relationships necessary to initiate blocking-oscillator action. Once the trigger input flux linkage requirements have been established, the analysis is conducted considering the blocking oscillator detector as a single core requiring a partial flux linkage change in excess of the experimentally determined trigger linkage requirement.

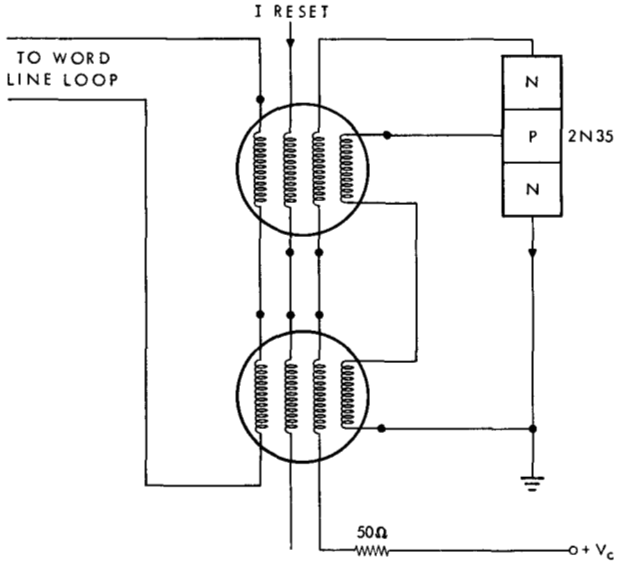
Ideally the detector design would be influenced solely by conditions and requirements specified during a search operation. This of course is not the case with the sense organization and the low-impedance detection device shown in Fig. 5. Depending on the number of bits/word, much higher voltages can be induced in the sense loop

during the CLEAR and/or WRITE operation than would be induced normally during a nondestructive search. Tests have shown that selective writing can be achieved, usually at great expense in time. For example, a 16-bit word of standard 50×80 cores coupled to a magnetic detector through a 29-inch loop of No. 28 wire could be written into in anywhere from 1.5μsec to 30μsec, depending upon how many cores in the register were switching. The variability and magnitude of the CLEAR-WRITE times involved, render the sense organization of Fig. 5 impractical when high-speed memory operation is required. However, the desirability of low-cost detection is justified when one considers the economics involved in the construction of large-capacity associative memories. The problem indicative of the sense organization of Fig. 5 is one of detector impedance levels. A solution in the form of a two-core-per-bit scheme, shown in Fig. 4, decouples the sense loop from the word and digit excitation windings during CLEAR and WRITE by virtue of the series-opposing wiring of the sense loop, as shown.

A detector of the form shown in Fig. 8 was designed to accommodate $80 \times 115 \times 55$ mil ferrite storage cores. The choice of this size core for the storage element represents an intentional overdesign to compensate for any unknown and unanticipated difficulties in implementing the model. A detector was built using a 21-mil high, 3-hole core of low-coercive-force material, electrically equivalent to the individual 2-core detector input structure shown in Fig. 8. This particular detector required a minimum flux trigger in excess of one maxwell. Other detectors using a 15-mil high, 3-hole core made of another low-coercive-force material require flux triggers in excess of 0.5 maxwell, but at an appreciably higher input impedance level. A high level of detector input impedance can accommodate more attenuation in the form of increased word lengths.

A long word line was constructed, consisting of one hundred $50 \times 80 \times 25$ mil standard IBM ferrite cores, operating in a biased NDRO mode and coupled to a detector of the type shown in Fig. 8. Interrogation of any core

Figure 8 **Blocking-oscillator detector.**
Upper trace: collector voltage, vertical scale 5 v/cm. Lower trace: mismatch word line output, vertical scale 0.2 v/cm. Time scale is 0.2 μsec/cm.



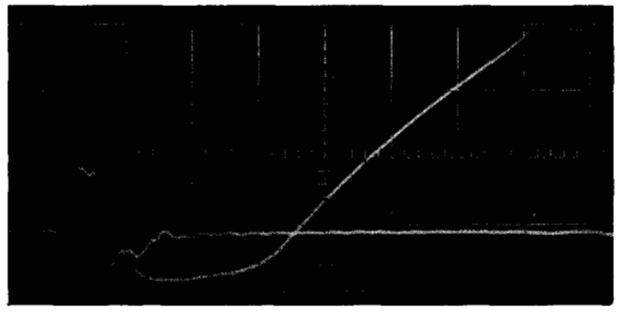
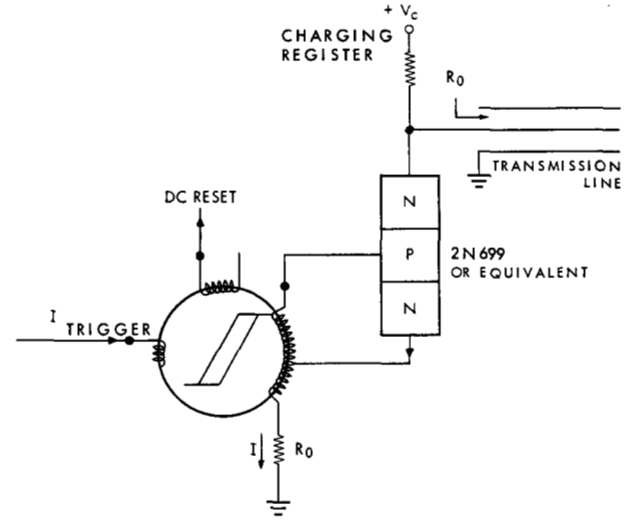
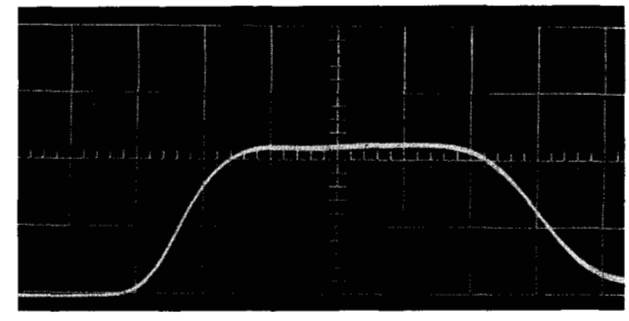


Figure 9 **Interrogation driver using delay line discharge.**
Scale for trace: vertical 0.5 amp/cm, horizontal 20 nsec/cm.





in this word line resulted in the successful transfer of a mismatch signal to the detector (see photograph in Fig. 8). The detector was constructed using a low cost alloy-junction transistor (SYL 2N35).

Search and NDRO driver

In Fig. 9 a simplified schematic of the interrogation driver is shown. The maximum search-rate was set at 5 mc. A 0.1 μsec interrogation pulse width was specified with a 0.1 μsec dwell time allowed between bit positions for "bringing up" the circuits comprising the AIR.

The duty cycle requirements for the individual interrogation drivers is at worst equal to the ratio of the basic search rate (5 mc) to the number of associative bits. For practical associative field lengths ($\sim$32 bits), the maximum individual interrogation rate is in the 100 kc range. Energy discharge drivers are known for their ability to produce highly stable, short-duration current pulses at relatively low repetition rates. Highly stable interrogation current pulses are desirable, since the maximum resolution between a match and mismatch occurs near the region of turnover, that is, the point where further increase in drive causes destruction or loss of the mismatch information state. The energy-discharge technique employed in the model was to discharge a transmission line into its characteristic impedance. A typical interrogation current pulse is shown in the photograph of Fig. 9. The driver designed on this basis operated successfully at 100 kc repetition rate. Experimental evidence shows that the drive capabilities of the driver-type described, using a 50 Ω lumped-parameter charging line with two IBM 089 transistors,* is limited to the region of 100 cores per driver. This evidence was compiled on a line of $50\times80\times25$ ferrite storage cores. The actual interrogation drive count for a practical size memory could be reduced significantly by means of the following:

1. Use of smaller storage cores
2. Improvements in storage core materials
3. Better constant-current sources capable of driving larger magnetic loads
4. Current steering circuits in which one interrogation driver can be used to drive two core planes.

A current-steering technique[13] which has been demonstrated feasible for this application can cut the driver count by a factor of two. Exploitation of this area offers the greatest potential driver count reduction.

The number of words that can be interrogated by a single driver is limited by its output impedance and its voltage rating. Hence, a larger number of words can be handled by drivers having higher output impedance and a higher voltage rating.

A reduction in interrogation drive current can be achieved by use of physically smaller cores and/or by improvements in the storage core materials, e.g., a $50\times80\times25$ ferrite requires a 1.5-1.6 AT drive at 0.1 μsec pulse width to operate in the vicinity of the turnover point in a bias restoration mode.

*Equivalent to Fairchild 2N699.

The engineering feasibility model

The prime objective of this feasibility model was to show the integrated operation of some specialized devices and techniques in a limited system operation. The most important function to be demonstrated is the associative search resulting in the retrieval of uniquely matching words. The remaining functions, such as the handling of non-unique cases, are reasonably straightforward applications of conventional logic blocks. (Model specifications are listed in the table below.)

The model consists of two memory arrays M and M', suitably interconnected to yield a two-core-per-bit organization, as shown in Fig. 10. Each word in the memory is coupled to its respective detector via a word sense line. For associative search purposes, the associative criterion is inserted into the AIR and mask register, which in the case of this model consist of hand-operated switches. For the unmasked bits, depending whether an AIR switch was in the ONE or ZERO position, a corresponding interrogation driver is triggered. For example, if the AIR contains a ONE in a given bit position the interrogation driver in that bit position will pulse the interrogation line of the M' array. For the case of a ZERO in the AIR, the M array would be interrogated. The interrogation drivers are triggered in succession to provide a serial-by-bit, parallel-by-word search.

At the end of the associative search, if a unique match exists, only one detector will remain in the match state. To determine the location of this matching word, the detector plane is reset. During the reset operation, two signals are induced in two orthogonal wires threading the output cores of the detector to provide the X and Y address of the matching word. This address is stored in the X and Y address registers which, with the aid of

Model specifications

array	2-core-per-bit, word organized (Fig. 4)
ferrite cores	Size ($0.080\times0.115\times0.055$ inch) (NI_0=0.6 AT)
capacity	2 words at 2 bits per word
detector	A special blocking oscillator (Fig. 8)
search drivers	Delay line type (Fig. 9)
WRITE *drivers*	Laboratory type
READ *drivers*	Same as search drivers
search pulse	0.1 μsec, 2.2 AT
half-select WRITE *pulse*	0.75 μsec, 1.1 AT
CLEAR *pulse*	0.75 μsec, 1.1 AT
NDRO pulse	0.1 μsec, 2.2 AT
DC bias	0.55 AT
peripheral logic	100 kc

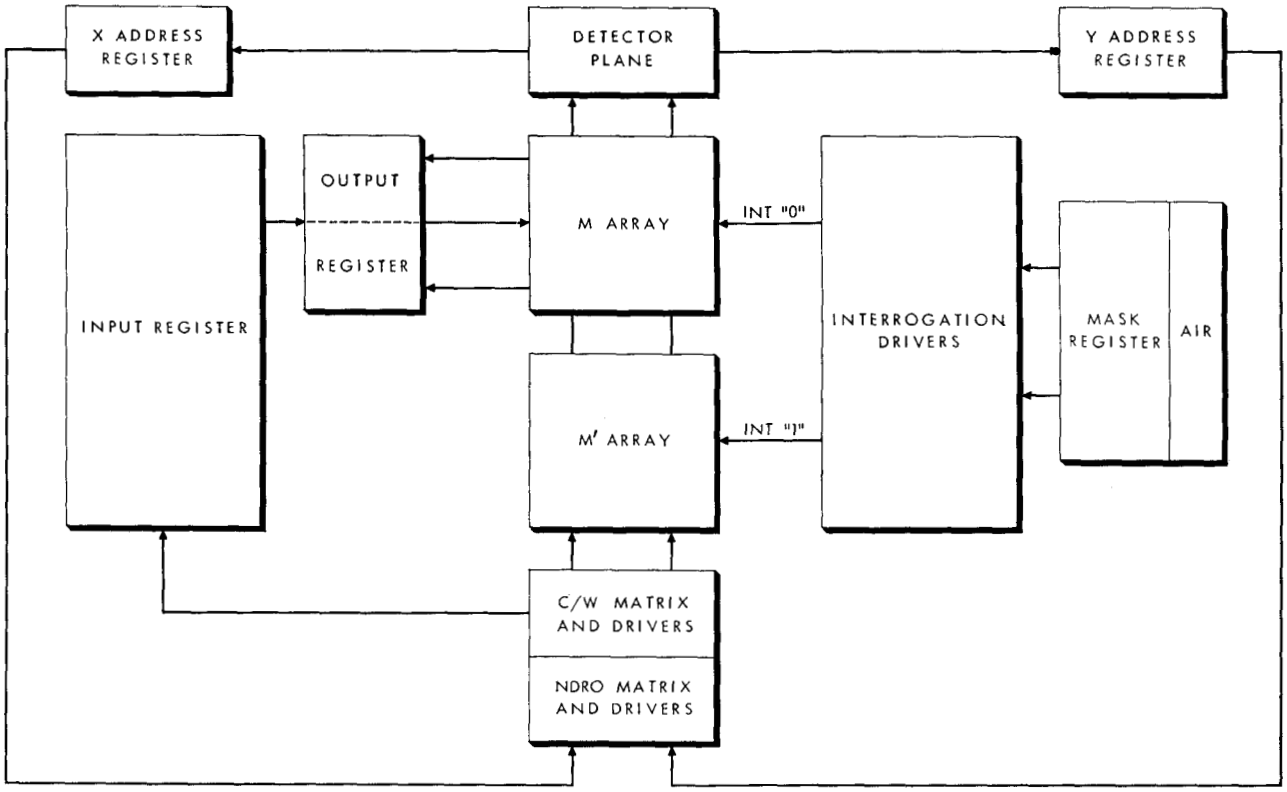


Figure 10 **Block diagram of experimental associative memory model.**

suitable logic, enables the nondestructive reading and/or clearing and rewriting of the matching word. The input register for the WRITE operation was again implemented by manually operated switches.

In order to write a word into an empty memory location, the detector at that location was disabled to produce a match condition artificially and was followed by a writing cycle.

A proposed full-scale associative memory system

A generalized system diagram of the proposed associative memory system is shown in Fig. 11. This system may be programmed to perform the following general operations:

1. An associative search.
2. Nondestructive or destructive readout of the associatively or addressably located words.
3. Writing of externally supplied data into an associatively or addressably located word line.
4. Control of search, readout and writing.

- *The associative search*

In order to perform an associative search of the memory, the two portions of the associative criterion are loaded into the associative interrogation register (AIR) and into the mask register. This combined information will select the proper combination of interrogation drivers to perform a comparison of the information contained in the AIR with the masked information stored in the memory. This comparison is performed in a sequential mode by interrogating one bit plane at a time for the reasons mentioned previously.

Upon completion of the interrogation cycle (i.e., interrogation of the last unmasked bit plane) the only detectors which retained their original reset or "match" state will be the ones corresponding to words matching the associative criterion. Hence the detector plane matrix is a location map of all the words in memory which contain the information identical to the associative criterion.

- *Retrieval of associatively located data*

Upon completion of the associative search cycle, the X and Y detector plane control units nondestructively examine the detector matrix plane. The result of this examination is interpreted by the match-type indicator and is relayed to a central memory control unit. If none of the stored words matches a given associative criterion, a no-match signal is received by the central memory control which is under program control. This program will now determine the next operation to be performed. It can either continue to change the associative criterion until at least one match is found in the memory or it may instruct the system to disregard this particular search cycle and proceed to the next instruction.

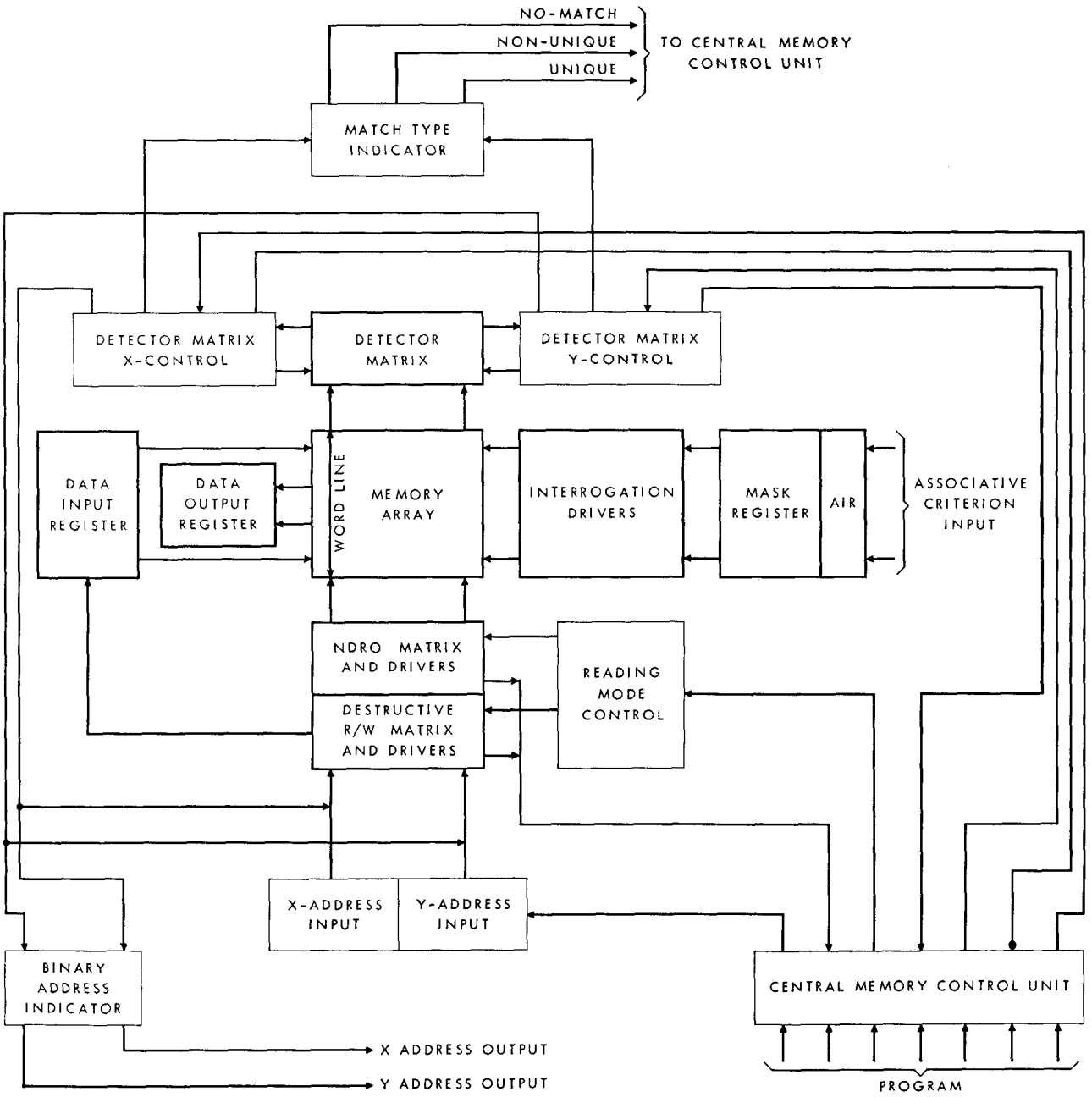


Figure 11 **Generalized system diagram for proposed associative memory.**

If, on the other hand, at least one match existed in the memory, the X and Y detector plane control units will activate the X and Y READ drivers corresponding to the location of the first matching word. Upon completion of the readout, the central memory control receives a pulse from the readout arrangement, signalling the completion of the readout. If more than one match exists (a non-unique case), the central memory control unit causes the X and Y detector controls to activate the X and Y READ drivers corresponding to the location of the next matching word. This procedure is repeated until either all words in the memory, matching a given associative criterion, have been read out or until the readout is interrupted by external programming.

The readout of an associatively located word may be performed either nondestructively or destructively. In the case of the destructive readout it is followed by a WRITE. The type of readout to be performed is chosen by external programming, which conditions the reading mode control unit.

As a by-product of retrieval, an address is generated which may be decoded into a machine code. This address may be used at a later date to retrieve that particular word (providing that word is still in the memory) in a

conventional addressable mode, either destructively or nondestructively.

• *Writing*

In order to write information into a memory register, the location of that register must be known. The location of the register may be provided either by specifying an externally supplied address or by specifying some associative criterion.

If the address of a register is known, such as in the case of a totally empty memory, a conventional addressable READ-WRITE cycle follows. If, on the other hand, associative writing is to be used, an associative search must precede the conventional READ-WRITE cycle.

In order to replace a given Record *A* in storage by some other externally provided Record *B*, a criterion for retrieval of Record *A* must be specified and, after Record *A* is read out, Record *B* is written into the location by internal addressing. If, on the other hand, a non-unique criterion was specified, Record *B* will be written into the first word location determined by the *X* and *Y* detector matrix plane control which matched that criterion. If more than one record is to be successively written into the memory on an associative basis, a non-unique criterion is specified to locate all the words matching this criterion and the externally provided records will be written into these locations in succession, controlled by the *X* and *Y* detector control units. For example, if externally supplied records, *A*, *B*, *C*, et cetera, are to be written into empty registers (all ZERO words), the associative criterion would consist of all ZERO bits. The result of this associative search would be the mapping in the detector matrix plane of all empty cells in the memory. The *X* and *Y* detector matrix plane control units would activate the destructive READ-WRITE drivers corresponding to the first empty cell and Record *A* would be written into that location. Next, the *X* and *Y* detector plane control units would be notified via the central memory control unit of the completion of this WRITE operation and would proceed to write in the next record, namely, Record *B*. This process is repeated until either all records are written into the empty registers or until the memory is filled to capacity. In either case, the central memory control unit would be signalled.

Another technique of loading an associative memory, suggested by L. Haibt,[14] can be accomplished by keeping track of the number of empty cells in the memory and by identifying each such cell by a number. These numbers are used as associative criteria for location of empty cells. In order not to confuse the empty cell number with actual data in storage, an additional bit position for each register is required. A ZERO in that bit position can represent an empty cell, while a ONE can represent a data word. This additional information must be included in the criteria.

A counter, which keeps track of the empty cells in the memory, provides the number of the last empty cell. Furthermore, it is updated for each WRITE and destructive READ operation.

• *Controls*

From the preceding discussion, it is obvious that the central memory control unit, via external program, controls all the operations of the memory. In addition it may keep track of empty cells (all ZERO words) available in the memory by updating an empty cell counter during the destructive READ and WRITE operations. This gives the programmer additional information.

The functions of the lower order control units such as the *X* and *Y* detector plane controls and reading mode control have been described previously, and are under the control of the central memory control unit.

Applications

The applications of associative memories, as seen by the authors, fall into three main classes. First in line, and perhaps the most obvious, might be the use of an associative memory in types of problems involving a serial search. In this application, the time necessary to perform this task is considerably less than that of conventional memories. Into this category fall applications such as variable or fixed look-up tables of all sorts.

Next, a class of less obvious applications would be the use of an associative memory subsystem for housekeeping tasks in large data handling systems. In one such use, a large file may be streamed past a small associative memory which could contain, for example, requisition data. This permits rapid up-dating of large, unordered files.

Last, the least obvious and probably one of the more useful applications from a programming standpoint would be that an associative memory would permit the use of more sophisticated mathematical tools in the solution of group theory and matrix problems, e.g., the use of a non-unique associative criterion for finding a common set in a group of sets.

Other applications which may fall into one or more of the preceding classes are: character recognition, error correction, exchange memories, self-sorting, et cetera.

Conclusions

In this paper three major steps have been taken towards data retrieval by association: a clear definition of the problem in terms of basic logic requirements; a practical implementation of these requirements; and last, a qualitative analysis which can be used as a design tool. The analysis of the problem substantiated by tests performed on the model and separate experiments performed on long word lines, together with search drive experiments, indicate that the significant problems in implementing a reasonable size associative memory are, in many respects, similar to those encountered in the implementation of conventional, high-speed, word-organized memories.

The word capacity of associative memories is restricted primarily by the interrogation drive problems. In order to increase the word capacity, hard tube or distributed drive techniques would be used. It is reason-

able to conclude that with optimization of components and distributed drive techniques, larger associative memories (for example, 4000 words × 72 bits), operating at a 10 mc search rate, can be developed.

It is obvious that the initial cost of associative memories would be higher than that of conventional storage. However, it is the total system cost, including programming, initial cost of hardware, et cetera, relative to the capability of the resultant system that will determine their economy and utility.

Appendix: The derivation of an electrical analog of a simple nonlinear magnetic structure

Quantitatively, the values of R_0 and L_0 (Fig. 12a) can be determined by measuring the essentially constant, quasi-dc slope of the ϕ_{max} vs NI S-curve in the region below threshold and the slope of the initial peak volts/turn vs NI curve. The S-curve data will yield the equivalent inductance/turn^2 while the initial peak volts/turn data will give the equilavent resistance/turn^2. It is reasonable to say that the below-threshold inductance and resistance per turn squared are related to the dimensions of a toroid by the following:

$$\frac{L_0}{N^2} \cong \frac{\mu_r A}{l_m} \tag{6}$$

and

$$\frac{R_0}{N^2} \cong \frac{K_1 A}{l_m}, \tag{7}$$

where μ_r is the average permeability in the region of remanence, A is the core cross-sectional area, l_m is the mean magnetic path length and K_1 is a constant of the material.

Experimental evidence shows that when fast rise pulses (10 nsec) are used in the measurement of the volt/turn curve, the first observed peak appearing in the voltage response varies linearly with NI. The addition of a bias current in opposition to the drive current translates the curve by the amount of the bias. These responses do not have the characteristic threshold one observes when measuring the second or broadest peak of the voltage response. This lack of initial peak threshold has been observed in a number of ferrite materials and also in molybdenum-permalloy tapes. In Fig. 12(a) an equivalent circuit representing a core driven below its inelastic threshold is shown. The L/R time constant as stated by Eq. (8), to the degree of approximation, is dependent on intrinsic material properties and not on physical size or on the number of turns:

$$\frac{L_0}{R_0} = \frac{\mu_r}{K_1}. \tag{8}$$

The storage core

Elastic switching or the ability to read nondestructively the magnetic state of a core with drive fields greater than the dc threshold is reported in the literature.[11] The

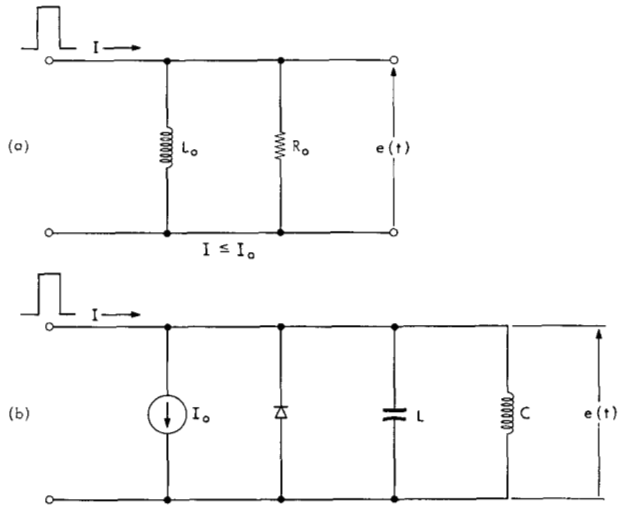


Figure 12 **(a) The below-threshold equivalent circuit for a magnetic toroid core. (b) Electrical analog for irreversible switching.**

elastic switching curve[15] affords a means for determining the maximum nondestructive repetitive unipolar field strength that may be applied for a given pulse width. This pulse threshold, or turnover point, usually represents a point of maximum resolution between a stored ONE and ZERO state when the binary information states are defined as being in the regions of positive and negative remanence, respectively. Eq. (9) relates the "turnover" drive to the material properties of a core for a given pulse width τ of drive

$$H_{T0} = \frac{S_{wr}}{\tau} + H_0. \tag{9}$$

The addition of a dc bias restoration field in opposition to the direction of nondestructive READ, enhances the NDRO properties of ferrite material in terms of greater resolution between the stored ONE and ZERO states and increased α or percentage of the total flux that can be extracted nondestructively.[9] The effect of bias on the inelastic and elastic switching curves as shown in Fig. 13 are primarily translation of the former, and translation and rotation of the latter. The elastic switching curve for the bias mode can be represented by the following equation:

$$H_{T0} = \frac{S_{wrB}}{\tau} + H_{0B}. \tag{10}$$

In the development of an equivalent circuit for a core operating in a NDRO mode, Eqs. (9) or (10) are used in relating the maximum field that may be applied for a particular pulse width.

Recent work[16] has shown that irreversible switching of a toroid can be represented on a shell basis by the following equation:

$$e(t) = k \sin \omega t. \tag{11}$$

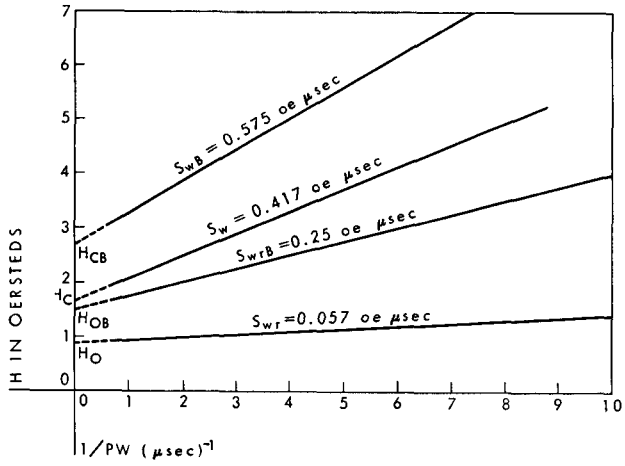


Figure 13 **Switching curves, ferrite core 80×115×55 mil; ϕ_1=22.4 maxwells; bias=0.54 AT.**

Since the switching time t_s can be related to the ratio of S_w and excess field $(H-H_c)$ by

$$t_s=\frac{S_w}{H-H_c}, \tag{12}$$

the determination of k can be made by integration of Eq. (11) between zero and t_s. The left-hand side of Eq. (11) for reasonably square-loop materials can be approximated by the ONE flux linkage $N\phi_1$. The constant k is now determinable and it can be seen that

$$e(t)=\frac{NB_rA(H-H_c)\pi}{S_w}\sin\frac{(H-H_c)\pi t}{S_w}, \tag{13}$$

where $0\leqslant t\leqslant t_s$ and $\omega=\dfrac{(H-H_c)\pi}{S_w}$.

In Fig. 12(b) a synthesized parallel LC network is shown. The network is shunted by an ideal diode and current source to simulate the threshold condition indicated in Eq. (12).

The voltage response of this network to a step of current (I) is represented by the equation

$$e(t)=(I-I_0)\sqrt{\frac{L}{C}}\sin\frac{t}{\sqrt{LC}}, \tag{14}$$

where $0\leqslant t\leqslant\pi\sqrt{LC}$.

When like terms in Eqs. (12) and (14) are equated, L, C and I_0 are

$$L=\frac{B_rAN^2}{l_m(H-H_c)} \tag{15}$$

$$C=\frac{S_w^2l_m^2}{\pi^2(H-H_c)l_mB_rAN^2} \tag{16}$$

$$I_0=\frac{H_cl_m}{N}. \tag{17}$$

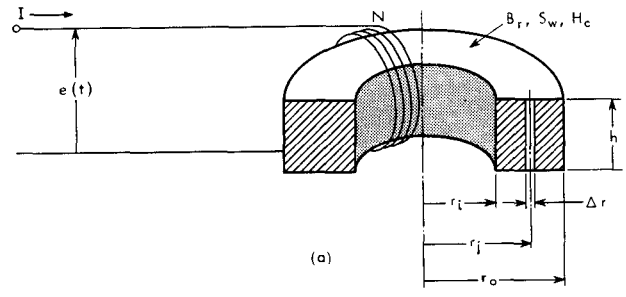
In Fig. 12(b) is shown an equivalent circuit for a core shell switching state. Eqs. (15) through (17) are used to calculate the parameter values of the equivalent circuit. The electrical analog for a shell of a switching core can be extended to represent a physical toroid having a diametral ratio less than unity. This can be done by considering the core as a series of independent concentric shells with cross-sectional area equal to $h\times\Delta r$, as shown in Fig. 14(a). In this manner the analog would yield a series of parallel LC circuits shown in Fig. 14(b) and the voltage response would be the voltage summation of all voltages appearing across each parallel LC combination.

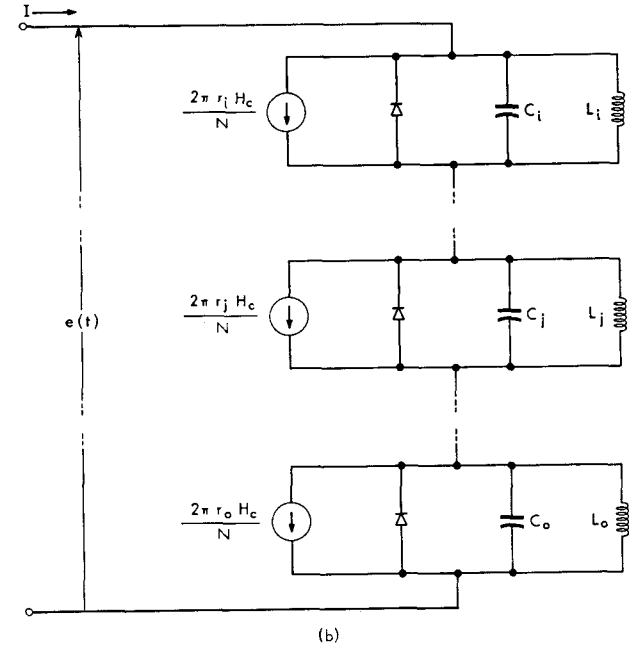
A ferrite core with a diametral ratio of 0.7 was tested for its magnetic parameters. From these parameters a single-shell equivalent circuit was constructed and its voltage response was compared to the actual response of the core under conditions of identical step current excita-

Figure 14 **(a) Core circuit. (b) Electrical analog for a core having a diametral ratio other than unity.**

$$Cj=\frac{4S_w^2r_j^2}{[NI-2\pi r_jH_c]B_rN^2h\Delta r}$$

$$Lj=\frac{N^2B_rh\Delta r}{NI-2\pi r_jH_c} \quad \text{where } r_i\leqslant r_j\leqslant r_o$$





tion. The experimental results of this comparison are shown in Fig. 15. The equivalent *LR* circuit for below-threshold drive was added in series with the irreversible equivalent circuit. While the curves are not a perfect fit, the general characteristics of the switching waveform are preserved. It is of interest to note that the curves fit better at higher drive, which is to be expected, since the effects of diametral ratio are less pronounced at the higher drive condition. It should be pointed out that the analysis of Tancrell and McMahon[16] also predicted better results at higher drives. The combination of reversible and irreversible models can indeed be used as a reasonable analytical representation of a core that is switching from a remanent to opposite saturation state. In partial and nondestructive switching modes where the reversal of magnetization is incomplete, care must be taken in the application of the model since the predominantly inelastic volt-time area predicted by the model can be significantly reversible in the actual case.

Acknowledgments

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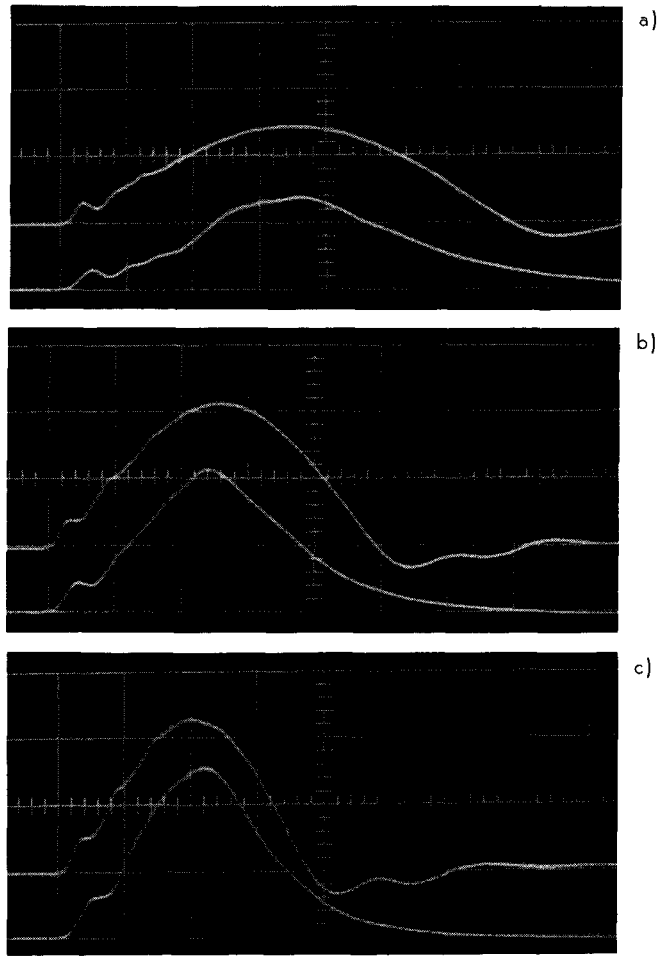
Figure 15 **Comparison between actual core output voltages (lower traces) and their respective equivalent circuit outputs (upper traces). Vertical scale 400 mv/turn/div., horizontal scale 100 nsec/div. Ferrite core: MgMn, 80×115×55 mil, $S_w I_m = 0.272 \times 10^{-6}$ AT-sec, $H_c l_m = 1.04$ AT, $B_r A = 11 \times 10^{-8}$ webers, N=5 turns.**

	Drive (AT)	*L* (μh)	*C* (mfd)	I_0 (A)
a) Low drive	1.5	5.5	0.0054	0.2
b) Medium drive	1.75	3.68	0.0036	0.2
c) High drive	2.0	2.74	0.0027	0.2



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