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Electrical Properties of Vapor-Grown Ge Junctions

Abstract: A method of fabricating *p-n* junctions and *p-n* junction devices by a closed-cycle iodide vapor-growth process is described. The electrical characteristics of junctions made by alternately depositing *p*-type and *n*-type germanium onto a germanium substrate compare favorably with those fabricated by other means. Device arrays, such as diode matrices, and multijunction structures have been made by this process. If sufficient control can be achieved, devices having a wide range of impurity distributions and geometric configurations will be possible.

Introduction

The "closed-cycle" disproportionation reaction of Ge and I_2 not only has produced Ge of high purity and crystalline perfection, but also has produced Ge doped with donors or acceptors.¹ Although the doping mechanism is not fully understood and precise control of the impurity distribution in the deposited Ge has not yet been achieved, various kinds of experimental *p-n* junctions have been grown.

Such junctions are of special interest because the fabrication process is considerably different from conventional methods. This new method offers several advantages, one of which is the possibility of achieving a wide range of impurity distributions. Moreover, since this deposition can be performed at a temperature of 400°C or even lower, diffusion is minimized, and glass and other low-melting-point masks can be used to achieve special configurations and arrays.

This article describes the process itself and presents current-voltage characteristics of several different kinds of junctions fabricated by this process. Device applications are also discussed.

Variable-capacitance diodes and tunnel diodes produced by vapor growth are described in two accompanying papers.^{2,3}

Procedure

The apparatus and materials used in this investigation are essentially similar to those described elsewhere in this issue.¹ The furnace arrangement and its temperature profiles are shown in Fig. 1. This arrangement permits

successive depositions of *p*-type and *n*-type material, utilizing widely separated *p*-type and *n*-type source Ge regions. The material is deposited from the source region held at ~550°C, while the other "idle" source is held at a temperature at which it takes no significant part in the reaction. Other arrangements included a third source region containing intrinsic Ge which was used to dilute the doping from the other sources. In order to switch doping from one conductivity type to the opposite type, the temperature profile is reversed.

Doping of the depositing layers has been effected by three different methods: the doping agent dissolved in the source Ge, the doping agent used in elemental form and placed in the tube next to intrinsic source Ge or in a separate temperature zone, and the iodide of the doping impurity loaded into the tube with the other materials. The first method proved to be most versatile of the three; that is, a wider variety of impurities could be used. As an example, an atom of As dissolved in the source Ge cannot be transported until the Ge surrounding it is removed, whereas in the second method the As would be vaporized rapidly. This advantage is especially important when it is desired to change from donor doping with As or P to acceptor doping. The temperature of the "idle" source region must be kept approximately equal to the temperature of the seed region, otherwise GeI_2 and GeI_4 vapor will condense there. If elemental As or P is exposed, as in the second method, even at this idling temperature, it tends to vaporize either because its vapor pressure is sufficiently large or because it reacts chemically with I_2 .

The actual mechanisms by which impurities are transferred from the source to the depositing Ge are not well understood and have only recently been investigated carefully.⁴ However, it was previously observed that donors are transferred more readily than are acceptors. When either As, P or Sb was dissolved in the source Ge, concentration in the deposit has been as high as that necessary for degeneracy.

For the acceptors, Ga and B have been found to be transferred to the depositing Ge more readily than are other acceptors. However, the maximum concentration achieved with either of these acceptors was about $10^{18}/\text{cm}^3$. When doping in the deposits was compared with that of the sources, it was found that the fraction transferred was roughly 0.01. For indium, the fraction was still smaller, and for aluminum it was negligible. It is likely that the fraction of any impurity transferred depends considerably upon the temperatures of the source and of the growing crystals, but the detailed nature of this dependence has not been investigated. The doping phenomena reported in this paper relate to the conditions shown in Fig. 1.

When the temperature profile of the furnace is reversed to change the type of doping, as indicated earlier, the doping does not change instantaneously. Some time is required for the impurity iodide concentration in the vapor, and therefore the impurity concentration in the depositing Ge, to reach a steady-state condition. There are a number of ways in which this delay can be controlled or even put to use. For example, the nature and concentration of the impurity dissolved in the source Ge used to fabricate the graded base of a drift transistor are chosen such that the impurity iodide decomposes more slowly at the site of the growing crystal than the impurity combines with iodine at the source. Then the concentration of the impurity iodide in the vapor and the impurity concentration in the deposit would gradually increase. To produce an abrupt junction between uniformly-doped regions, impurities are chosen whose iodides decompose at the site of the growing crystal more rapidly than does GeI_2 . There is then a relatively small number of these impurity atoms in the vapor, and deposition of these impurities stops soon after the temperature profile is adjusted to deposit from the opposite type source. If, however, a long time is required for impurities to build up in the vapor or to be depleted from the vapor, a "dump-zone" can be used, instead of the seed zone, to receive the depositing Ge (and impurities) during the time that the transition is being made from one doping type to the other. This dump-zone can be either a previously used source zone or an extra zone provided in the tube. One dump-zone configuration is described by Marinace.³

Diode current-voltage characteristics depend on minority carrier lifetimes and on carrier mobilities in addition to impurity concentrations and concentration gradients used. Lifetimes measured on bulk samples by observing photoconductive decay have run from 1 to 60

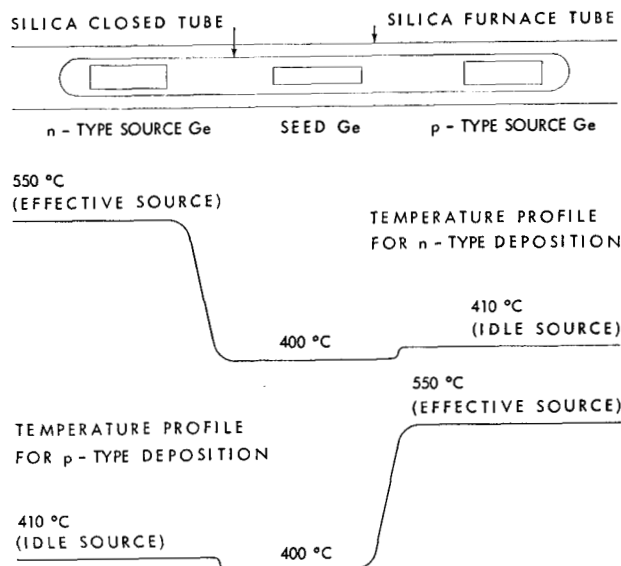


Figure 1 Diagram of closed tube and furnace for vapor growing n-type and p-type layers successively.

microseconds. These values are consistent with the observed dislocation density and are quite adequate for device applications. The measured Hall mobilities are fully comparable to those found in melt-grown Ge.¹

Nonplanarity of junctions could conceivably reduce the breakdown voltage of deposited junctions if sharp points or ridges were present in the junction contour. Microscopic examinations of junctions and deposited surfaces indicated that there were varying degrees of departure from perfect planarity. For example, depositions on {110} and {211} planes appeared to be macroscopically more planar, but microscopically less planar, than those on {111} planes. However, no effect definitely attributable to nonplanarity in the junction characteristics have been observed.

Three types of junctions were studied. The first was the type formed by depositing Ge of one conductivity type upon a seed of opposite conductivity type, with the electrical junction coinciding with the interface between seed and deposit. This kind of a junction is accompanied by a layer of high dislocation density near the interface.^{1,5} The thicknesses of these high-dislocation density layers varied in an as yet unaccountable way in different experimental depositions; some work now in progress⁶ indicates that it is possible to eliminate the disturbed layers and greatly reduce the dislocation density in vapor-grown crystals.

The second type of junction studied was that formed by first depositing Ge of one conductivity type and then, without interruption, depositing Ge of the opposite conductivity type. This was done by inverting the temperature profile of the furnace apparatus shown in Fig. 1.

The third type of junction studied was that formed by the well-known alloy process using vapor-grown doped Ge instead of melt-grown doped Ge. This type of

junction was made primarily to determine whether any peculiarities which might exist were due to the deposited material itself or due to the method of junction fabrication.

In addition, measurements were made on commercial diodes and on experimental transistor structures to provide a further comparison for these experimental diodes.

Experimental results

• Junction Properties

In order to evaluate vapor-grown junctions, static current-voltage characteristics were obtained by standard methods. The data were then plotted appropriately to attempt to determine the mechanism of conduction in the diodes.

In a p - n junction in which the current flow is limited by the rate of diffusion of minority carriers away from the junction⁷ (diffusion model), the ideal rectifier equation is applicable:

$$I/I_s = \exp(qV/kT) - 1, \quad (1)$$

where I represents current, V is applied voltage, q is the electronic charge, k is Boltzmann's constant, T is absolute temperature, and I_s is independent of voltage and is equal to the current which flows over the barrier at large reverse bias.

In general, p - n junctions do not follow the ideal rectification formula. Deviations are taken into account by rewriting this equation as:

$$I/I_0 = \exp(qV/\eta kT) - 1. \quad (2)$$

Both I_0 and η are, in general, functions of voltage and temperature. The term I_0 replaces I_s in Eq. (1) and describes the deviation from ideal characteristics for reverse bias, while η is a measure of this deviation in the forward-bias condition.

An excess current due to the generation and recombination of carriers in the space-charge region has been postulated to help explain the deviation from the ideal characteristics.⁸ The current due to this effect alone is expected to follow Eq. (2) with a value of $\eta=2$ and I_0 proportional to the width of the space-charge region. (The number of generation-recombination centers in the region is proportional to the width of the region.) The value I_0 , therefore, varies as $(V_D - V)^{1/2}$ for abrupt junctions and as $(V_D - V)^{1/3}$ for linearly graded junctions, where V_D is the barrier height at equilibrium. The total current is the sum of that expected by diffusion and recombination, and the observed value of η would be expected to lie somewhere between 1 and 2. The value of η then is a measure of the relative current flow by the two processes.

Deviations from the Eqs. (1) and (2) occur for high forward and reverse applied voltages. Because of the voltage drop in the series bulk resistance (R) of the diode, the value of V in these equations should be replaced by $(V - IR)$. This is generally not easily done because R is a function of current (due to the con-

ductivity modulation). For high reverse voltages, the current increases more rapidly than expected with voltage because of carrier multiplication effects and/or tunneling.

Forward and reverse current-voltage characteristics representative of a large number of junctions of the three types discussed earlier are plotted in Figs. 2 and 3, respectively. Diode 262 is an alloy diode fabricated by fusing pure In into a wafer of Sb-doped vapor-grown Ge of approximately 0.5 ohm-cm. The junction area is 10^{-3} cm². Diode I-B is a vapor-grown diode fabricated by depositing from a Ge source heavily doped with P and then idling this source as the deposition from another source heavily doped with B is initiated. Capacitance measurements indicated a retrograde distribution of impurity at the junction, that is, in the more lightly doped side the net impurity concentration decreases with an increase in distance from the junction. The junction area is 1.5×10^{-2} cm². Diode 224-B is made in the same way with the exception that the sources are not doped as heavily. Capacitance measurements indicated a linearly graded junction. The junction area is 1.8×10^{-4} cm². Diode 253 is a junction formed by depositing Ga-doped Ge of 0.2 ohm-cm resistivity on Sb-doped Ge (melt-grown) of 2 ohm-cm resistivity. Its area is 1.2×10^{-2} cm².

Fig. 2 shows a normalized plot of current against forward voltage for these experimental diodes at room temperature. For comparison, characteristics of a General Electric alloy diode (IN92) and ideal characteristics (Eq. 1) are also plotted. Fig. 3 depicts I/I_s against reverse voltage for these same units. The value of I_s was determined for each unit by extrapolating the reverse characteristic (I_0 vs V plotted linearly) in the range between 0.1 and 1.0 v to the $V=0$ axis. This agreed with the values obtained by extrapolating the straight-line portions of the $\ln I$ vs V curve (forward bias) to the $V=0$ axis, except for the cases of interface diodes (see Diode 253, Fig. 2) where no straight-line portions exist. The actual current values can be obtained from a knowledge of I_s . The values of I_s for the various units are listed below:

Unit	I_s
224B	0.07 μ a
I-B	0.3
253	6.0
262	0.9
IN92	23.0

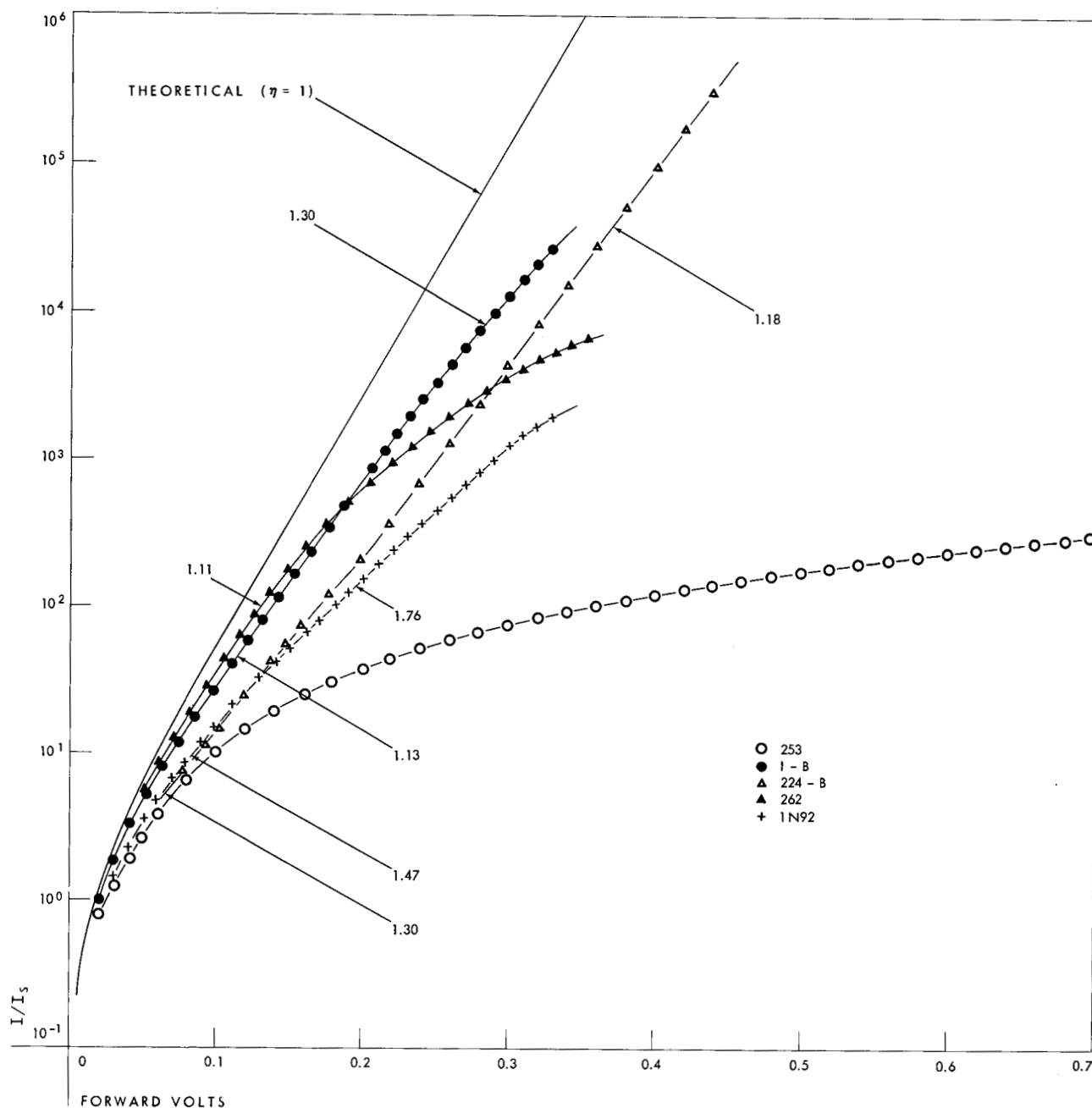
Diode 262 is an alloy diode on vapor-grown Ge. This diode comes close to following the ideal characteristics. The value of η is equal to 1.11 and I_0 is nearly a constant over an appreciable voltage range. The deviation from a straight line in the higher current region of Fig. 2 can be explained by a bulk resistance of 15 ohms. In the reverse characteristic there is an increase in current starting at about 4 v reverse bias which tends to

level off at about 8 v. The reason for this "hump" is not known. Capacitance measurements indicate that this junction is abrupt and that the net donor concentration in the germanium is 4.1×10^{15} atoms/cm³. The avalanche breakdown voltage expected for this case is 48 v.¹¹ The experimental value of 42 v is in satisfactory agreement.

Diodes I-B and 224B are representative of the all-deposited (vapor grown) type. Both of these units have two voltage ranges where η is constant. The change of η with respect to voltage is opposite for the two cases. For

I-B, $\eta=1.13$ for voltages less than about 0.23 v and $\eta=1.30$ above this. This junction is a retrograde junction and, because of the high doping near the junction, the space-charge region is narrow so that little generation-recombination current is expected. The decrease in η for high currents is presumably because the concentration of minority and majority carriers are comparable.⁹ For diode 224B, η has a value of 1.30 in the low-voltage range and 1.18 at higher voltages. Capacitance measurements on 224B indicated a linearly graded junction in which the net donor or acceptor concentration can be

Figure 2 Forward current-voltage characteristics of several types of diodes. (See text.)



expressed by the form

$$(N_D - N_A) = 6 \times 10^{19} X,$$

where X represents distance from the junction in cm and $(N_D - N_A)$ is in atoms/cm³. The transition region width at zero bias is about 8 microns. This is reasonably wide and the high initial value of η may be due to generation-recombination current. The decrease in η with an increase in voltage would then be due to the increased fraction of diffusion current. Storage time measurements¹³ indicate the carrier lifetime in the region of the junction to be about 0.3×10^{-6} sec. The avalanche breakdown voltage expected¹² for a diode with this impurity grading is 56 v. The experimental breakdown voltage is 43 v. Since Diode I-B is a retro-grade junction, no breakdown voltage could be predicted. For Diode 224B an unexpected hump in the reverse $V-I$ curve similar to that in Diode 262 is observed.

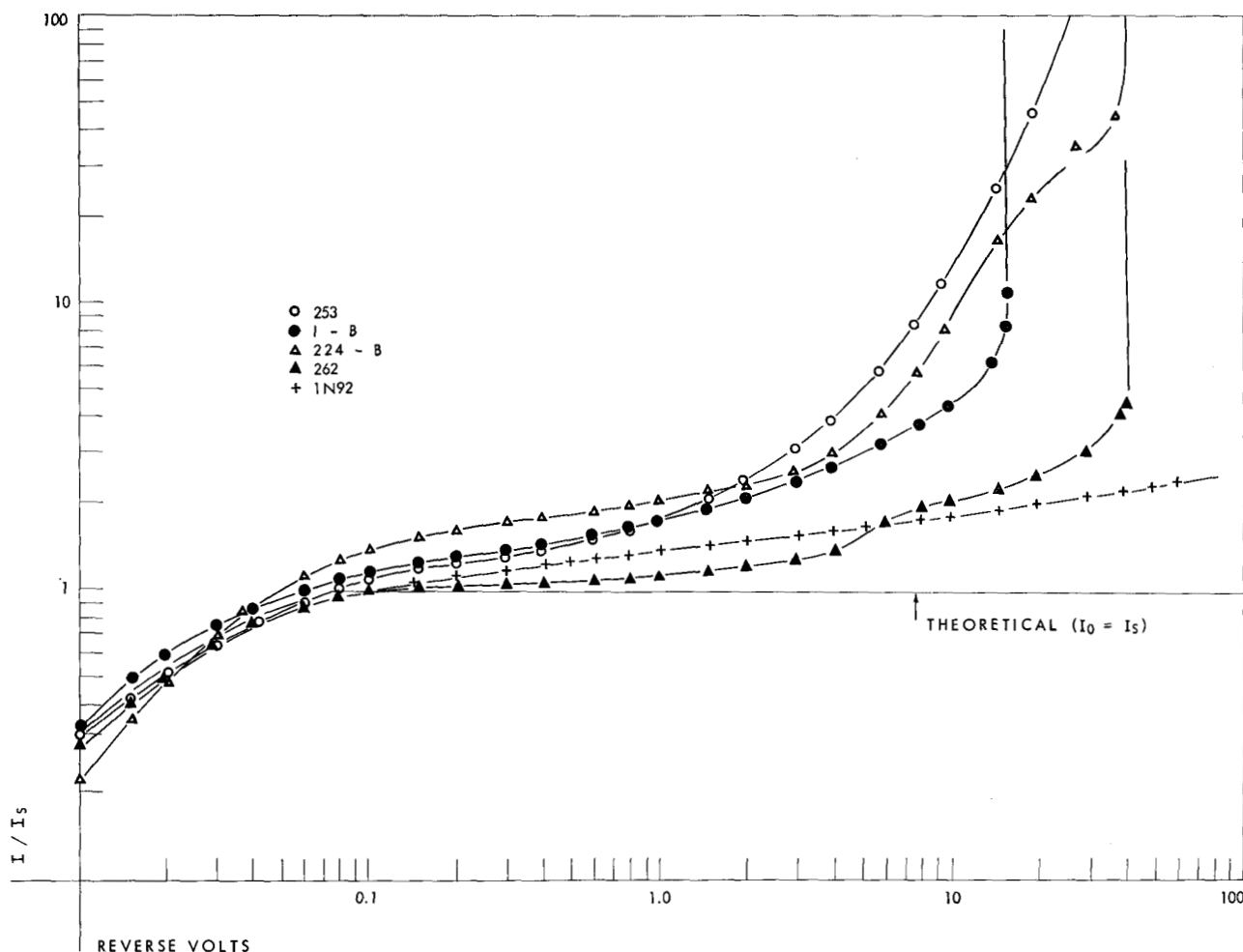
Diode 253 is a typical interface diode. The $V-I$ characteristics varied considerably from that of the ideal case. From the forward characteristic we can see that η

is rapidly changing with voltage. The effect of a large series resistance has been ruled out as a cause of the apparent increase of η with an increase in voltage. This was done by taking the $V-I$ characteristic at 78°K. At this temperature η behaved reasonably well and the series resistance was measured to be 4.5 ohms. The series resistance would not be expected to be much larger than this at room temperature and so the variation in the characteristic can be considered to be a result of a variation of η . The breakdown in this diode is "soft." This also is characteristic of diodes of this type. Some diodes, however, in addition to a considerable amount of softness, do avalanche at high voltages. Storage time measurements indicate that either no injection occurs or that lifetime is less than 0.03×10^{-6} sec (the minimum value that can be measured on our equipment).

Current-voltage characteristics were taken on these units at 78°K. Values of η between 3 and 5 were observed for low voltages and values between 1.2 and 1.8 at high voltages. The characteristics of diodes of these three types seem to be quite similar at this temperature.

A commercial alloy diode (General Electric 1N92) is

Figure 3 Reverse current-voltage characteristics of several types of diodes.



plotted for comparison with the experimental units. The value of η was found to be 1.47 at low voltages and 1.76 at higher voltages. The reverse current follows the ideal characteristics very closely up to about 0.1 v and then slowly increases with voltage.

Since even the lowest value of η for these diodes is about 10% greater than that expected by the ideal formula, it was thought that deviation from unity η may be caused by noninjected current (generation-recombination current, for example), and this would cause a low injection efficiency if such a junction were used as a transistor emitter. To test this hypothesis the forward $V-I$ characteristics of the emitter of a $p-n-p$ alloy transistor having a grounded-emitter current gain (α_{cb}) of 150 were measured. The values of η were found to be 1.09 and 1.26 respectively at low and at high voltages. We can see from this that the deviation from a unity value of η for the all-deposited junctions does not necessarily preclude high injection efficiency.

• Transistors

The alloy-junction process proved valuable, too, when used with vapor-grown Ge to fabricate simple alloy transistors, as shown in Fig. 4a. With base widths of 0.002 to 0.005", current gains (α_{cb}) were in the neighborhood of 50, establishing, as expected, that minority-carrier transport efficiency in vapor-grown Ge was comparable to that in melt-grown Ge. Collector breakdown voltage values agreed with those expected from measured resistivity values. Hybrid alloy-deposited transistors were fabricated with a deposited junction or a deposit-substrate junction as a collector and an alloy junction as an emitter as depicted in Figs. 4b and 4c. With base widths of 0.002" to 0.005", the observed current gains were comparable to those obtained from the alloy transistors described above. This established that these types of junctions could function as collectors. Collector characteristics were typical of the deposited and deposit-substrate junction characteristics presented in the last section.

Transistors with deposited emitters as well as collectors, as shown in Figs. 5a and 5b, have not had current gains as high as those of the alloy and hybrid alloy-deposited transistors. With base thicknesses of about 0.001", the highest current gain achieved was 12. Measurements indicated that injection efficiencies of the deposited emitters were low and that this was due to insufficient doping in the emitter regions. Moreover, the characteristics of deposited junctions presented earlier suggest that some vapor-grown junctions may contain an appreciable number of recombination centers and may not have a high injection efficiency. The combination of emitter junctions of high injection efficiency with thin base widths has not yet been achieved. There does not, however, appear to be any inherent reason why fully deposited transistors are not feasible with the improvements in the perfection of vapor-grown materials, as well as in doping control, which are being developed.

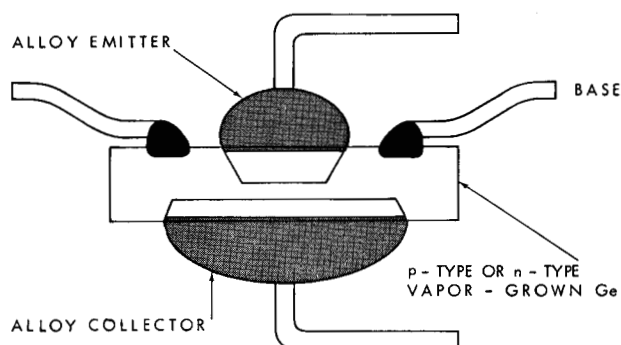


Figure 4a Alloy transistor using vapor-grown Ge.

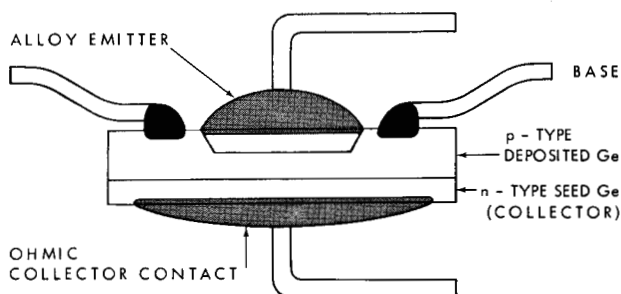


Figure 4b Hybrid transistor with alloy emitter and vapor growth/seed collector junction.

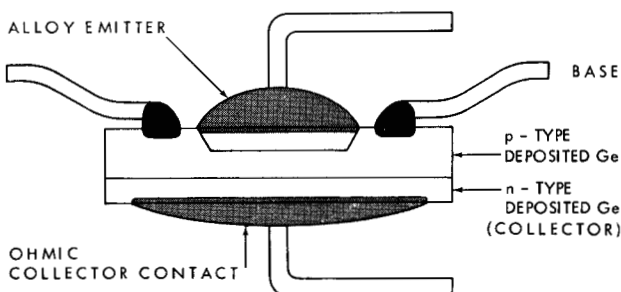


Figure 4c Hybrid transistor with alloy emitter and vapor-grown collector junction.

• Device arrays

One of the main advantages promised by the vapor-growth process is its compatibility with many masking techniques. Several of these masking techniques were tried. One involved cutting holes or slots in the seed wafers in a desired pattern and then depositing Ge in these apertures. Of course, Ge deposited on the faces of the seed wafer as well, but it was a relatively easy matter to lap and etch off this extraneous growth. Fig. 6a is a photomicrograph of a seed wafer (slot size 0.075" $\times$ 0.015") plus deposit after the faces of the wafer had been lapped and etched. The faint lines, which were

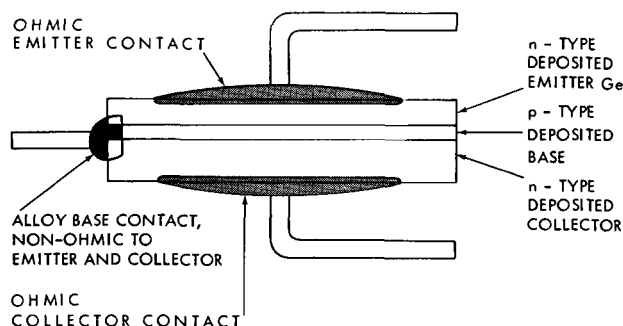


Figure 5a Vapor-grown transistor with emitter same size as collector.

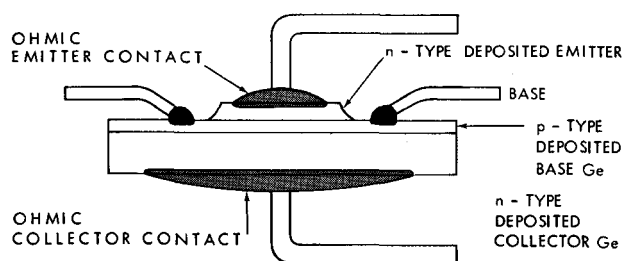


Figure 5b Vapor-grown transistor with emitter area reduced by etching.

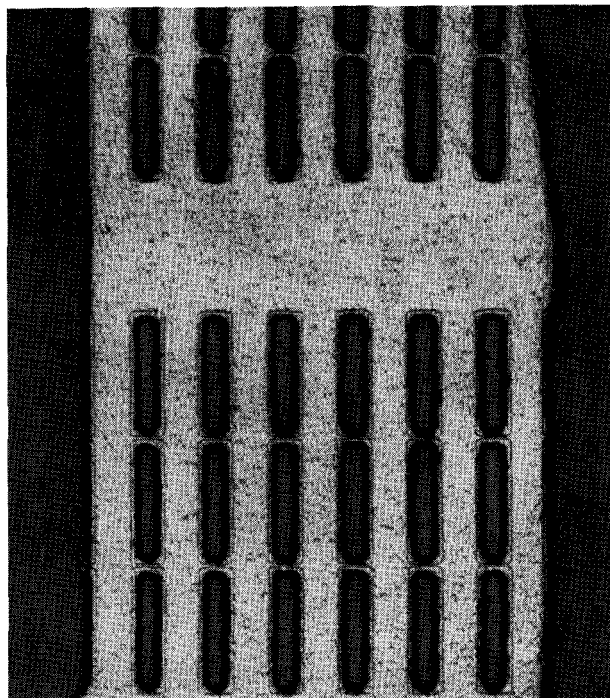


Figure 6a "Self-masked" deposit and substrate after lapping and etching. Slot size 0.75'' $\times$ 0.015''. (10 $\times$).

brought out by etching, delineate the interface between deposit and substrate. In this particular specimen, the substrate is 5 ohm-cm *p*-type and the deposit is 0.03 ohm-cm *n*-type. Fig. 6b shows a strip sawed from a wafer similar to that shown in Fig. 6a. A strip like the one shown was fitted with appropriate ohmic contacts and used as an array of unipolar transistors. The channel was cut to be 4 mils thick. Etching reduced this width somewhat, but not sufficiently to permit pinch-off before breakdown. Networks of junctions similar to those of Fig. 6a can be formed by the deposition process into appropriate topological forms to perform logic.

Masking was done also in a straightforward manner. A glass plate with holes in it was positioned atop a seed, the material vapor-deposited, and the glass plate removed. The substrates then had an array of mounds of single-crystal Ge on them. These mounds, with appropriate doping, have been made with *p-n* junctions in them. An interesting variation of this was tried. A plate of glassy material was chosen which had a temperature coefficient of expansion nearly equal to or slightly greater than that of Ge. The walls of the apertures in the plate were rough. After depositing *p-n* junctions in all of the apertures, the seed was lapped away, leaving a glass matrix with an array of Ge disks all of the same orientation embedded in the matrix. This is shown in Fig. 7. The spacing between centers of the disks is, in this case, 0.022''. The characteristics of these junctions have been inferior to the characteristics of the deposited junctions reported earlier in this article.

For device arrays of this kind, two serious problems must be considered. First, there is the problem of determining the conditions under which junctions that do not need etching to make them operational can be produced within the apertures. Second, there is the more general problem of making interconnections between units of arrays.

Discussion

The data presented on the junction properties show that simple diodes can be produced by the vapor-growth process. The fully-deposited diodes are of the most interest, and it is seen that they compare favorably with Ge diodes produced by other means. Diodes which have η close to unity appear to have a large ratio of diffusion

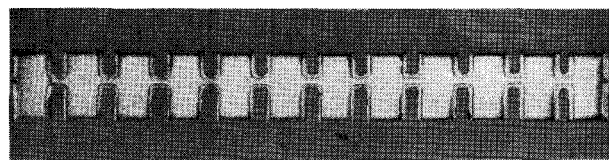


Figure 6b Strip of unipolar transistors sawed from a wafer similar to that shown in Fig. 6a. (7 $\times$).

current to generation-recombination current. Such junctions should be useful, therefore, as emitters in transistors. Those with higher values of η , however, might be expected to be poorer in this respect.

Difficulty has been encountered in producing high-gain transistors by successively depositing alternately doped layers. This has been ascribed to inadequate control of doping and growth rate. If sufficient control can be achieved, devices having a wide range of doping distributions and geometric configurations will be possible.

Acknowledgments

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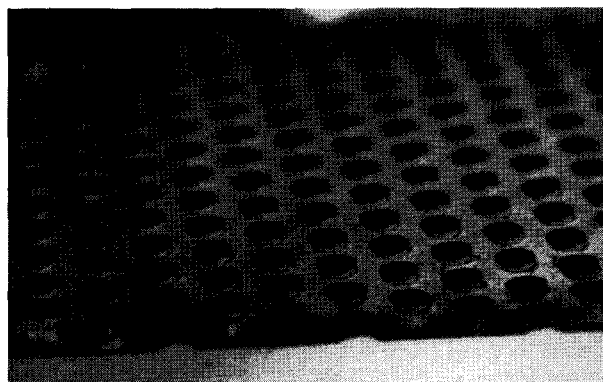


Figure 7 Ge p-n junction disks deposited in glass matrix. Distance between centers of disks is 0.022".

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