

A Full Binary Adder Employing Two Negative-Resistance Diodes

Abstract: Full binary pulse addition may be performed using only two negative-resistance diodes. Amplified Sum and Carry outputs can be provided which are virtually in coincidence with the input signals. A full adder is described, employing Reeves-Cooke positive-gap diodes which operate with pulses of 20-millimicrosecond duration.

Introduction

A basic calculation performed by electronic computers is the addition of two multi-digit binary numbers. Whether the two numbers are added simultaneously, that is in parallel, or in serial time sequence, the two lowest-order digits are added to produce a Sum, and a Carry which is then presented for addition to the next lowest-order pair of digits. Addition thus requires three binary input channels and two binary output channels in a circuit which is commonly called a full binary adder.¹ A common way of constructing an adder with crystal rectifying diodes employs 16 rectifying diodes and requires that four levels of diode logical circuits be driven in series to produce the Sum and Carry outputs. For very-high-speed operation,² the logical circuitry may so attenuate the input pulses that amplification is needed. Time delays through the amplifiers may then be intolerably long for the operation of the circuit. This article is concerned with a type of full binary adder which uses two negative-resistance diodes and no other diodes, and produces a pulse output which is amplified and virtually in coincidence with the input pulses. Because of the short rise and fall times inherent in diode as contrasted with triode structures,³ a logical circuit employing only diodes possesses additional interest.

Importance of the full binary adder as a logical circuit has been recently emphasized by Dunham,⁴ who has shown that by biasing one of the three input terminals a useful variety of logical functions may be performed.

Principle of operation

The full binary adder to be discussed here is shown schematically in Fig. 1. The three binary inputs, I_A , I_B , I_C , are

added in the summing resistor, R_1 , to produce three voltage levels at point P . Components D_1 and D_2 are diode devices which conduct heavily, or "fire," when the voltage across them exceeds a critical value. Suppose that D_1 has the lower critical voltage. When one pulse is present at any input, one unit of voltage appears at P , D_1 fires and produces a Sum output. When any two inputs are present, two units of voltage appear at P and both D_1 and D_2 fire. However, the firing of D_2 eventually shuts off D_1 ; so only a Carry is produced. When all three inputs are present, D_1 and D_2 fire again, but now the three units of voltage at P are sufficient to keep D_1 on in spite of D_2 ; consequently, a Sum and Carry are produced. This action is that required of a full binary adder. To show how this operation can occur, we may consider that the diode devices D_1 and D_2 have the ideal voltage-current characteristics shown in Figs. 2a and 2b. It will be shown subsequently why these characteristics are in fact ideal and how such characteristics may be realized in practice. The circuit behavior of Fig. 1 may be most readily understood by replacing that part to the left of point Q by its Thévenin equivalent and that to the right by a composite diode D (see Fig. 2c) which consists of D_1 and D_2 in parallel connection. The resistors R_s and R_c have been shown outside of the devices D_1 and D_2 so that the Sum and Carry may be clearly shown. In what follows, R_s and R_c will be assumed negligibly small. The I - V curve of D is shown as the heavy solid line in Fig. 2c. It is constructed by adding the currents of Figs. 2a and 2b at corresponding values of voltage and by applying the law of parallel-resistance addition to the slope resistances. We shall say

that a diode is "off" when it is in the a portion of its characteristic, and "on" when it is in the c portion. Points T and R will be called "turnover" and "return" points, respectively. Small letters a , b , and c denote portions of the characteristic as well as the slope resistances of these portions; capital letters denote points on the I - V characteristic. To verify the characteristic of Fig. 2c, we suppose that D_1 and D_2 are driven in parallel by a current generator. As the generator current I and the voltage V increase from zero along the lower part of the composite characteristic a, b, c , D_2 remains off until its turnover voltage is reached. D_1 is thus in parallel with the large resistance a_2 , and the curve abc is just the characteristic of D_1 , namely the curve of $a_1b_1c_1$. At the turnover point of D_2 , however, D_2 starts to turn on and the composite curve follows DF . This curve has slope b_2 because, approaching DF as we have, b_2 is in parallel with the infinite resistance c_1 . At point F the voltage across the parallel combination has fallen to the return voltage of D_1 and something will happen to the characteristic at this point. What happens may be determined by considering the upper portion of the composite characteristic a', b', c' . At point G , both diodes are on, and D_2 stays on until V falls to its return voltage at H . Consequently, this portion of the composite characteristic is equivalent to c_2 acting in parallel with a_1, b_1, c_1 . At H , however, D_2 begins to turn off and the composite curve goes along HJ' , with slope b_2 (corresponding to b_2 in parallel with the high resistance a_1). At point J' the voltage has risen to T_1 , at which value D_1 turns on. We may now complete the characteristics from F and J' by drawing the dashed lines $J'J$ and FK to represent the rapid change of voltage which would be observed if, as we are supposing here, the composite characteristic were to be traced out by a current generator.

With the aid of the composite characteristic we may

now describe the circuit operation of Fig. 1. As a further simplification we may replace the circuit to the left of point Q by a Thévenin generator of electromotive force E and internal resistance R_L . This generator is shown in Fig. 2c. The series current, I , that flows through R_L is determined in the usual way by drawing a line on the composite characteristic of slope $-1/R_L$ with intercept of E on the voltage axis. The operation is as follows. As E is raised from 0 to a level below E_1 , no output occurs. When E is raised to E_1 , the load line intersects c at L and indicates that D_1 is turned on. As E is increased to E_2 , the load line intersects a' at M and indicates that D_2 is turned on, but that D_1 is off. This follows because $V(M)$ lies to the left of $V(R_1)$. This last condition is critical in the operation of this circuit. As E is raised to E_3 the load line intersects c' at N and indicates that both diodes are fully on. It is seen that this behavior is just that previously asserted of the circuit in Fig. 1. It may now be noted that because the diodes D_1 and D_2 are assumed to pass no current when they are "off", the consequences are that spurious input pulses cannot feed through to the outputs and there is no signal at the Sum output when the Carry alone is on. The flatness of the a and c portions of the diode characteristics have the desirable practical consequence that variations of input pulse heights about the four values, 0, E_1 , E_2 and E_3 produce no changes in the Sum or Carry outputs. For these reasons the characteristics of Figs. 2a and 2b are ideal. A further point to be observed is that the final state of the circuit is attained only by passing through all previous states of the circuit. In practice, this has the consequence that when the two inputs are present, a small spurious Sum pulse exists before the Carry diode can turn off the Sum diodes. This spurious pulse can be avoided in one of several standard ways. An occurrence of this pulse is shown in Fig. 5.

Figure 1 Block diagram of a full binary adder.

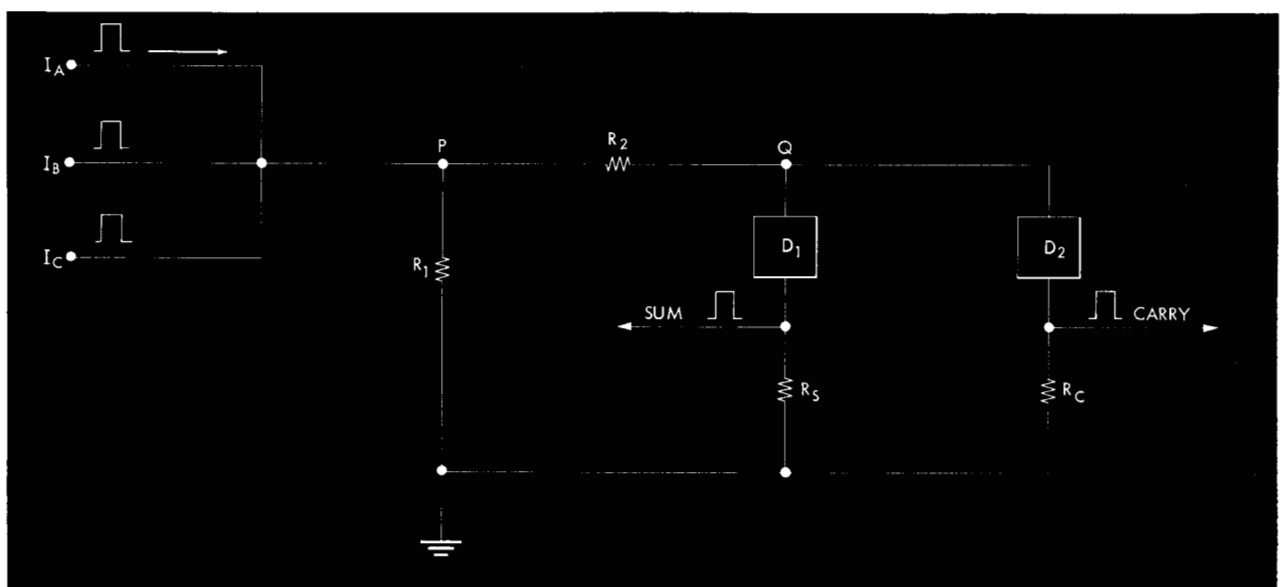


Figure 2a Diode D_1 ideal voltage-current characteristic.

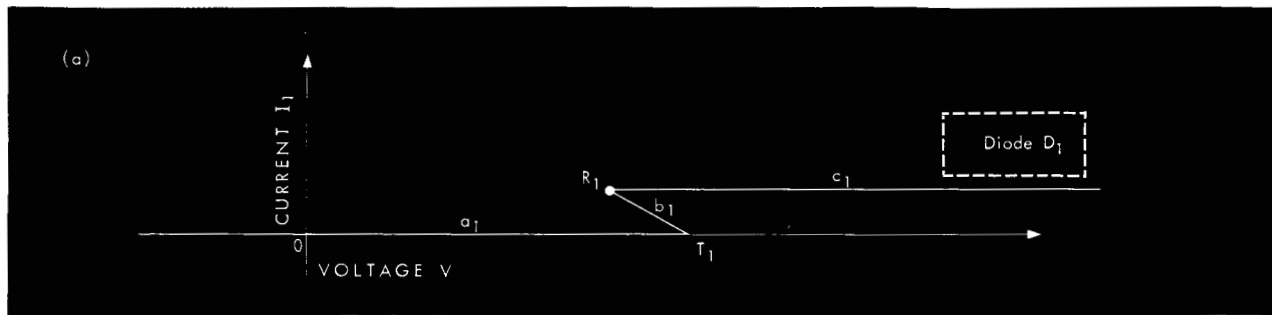


Figure 2b Diode D_2 ideal voltage-current characteristic.

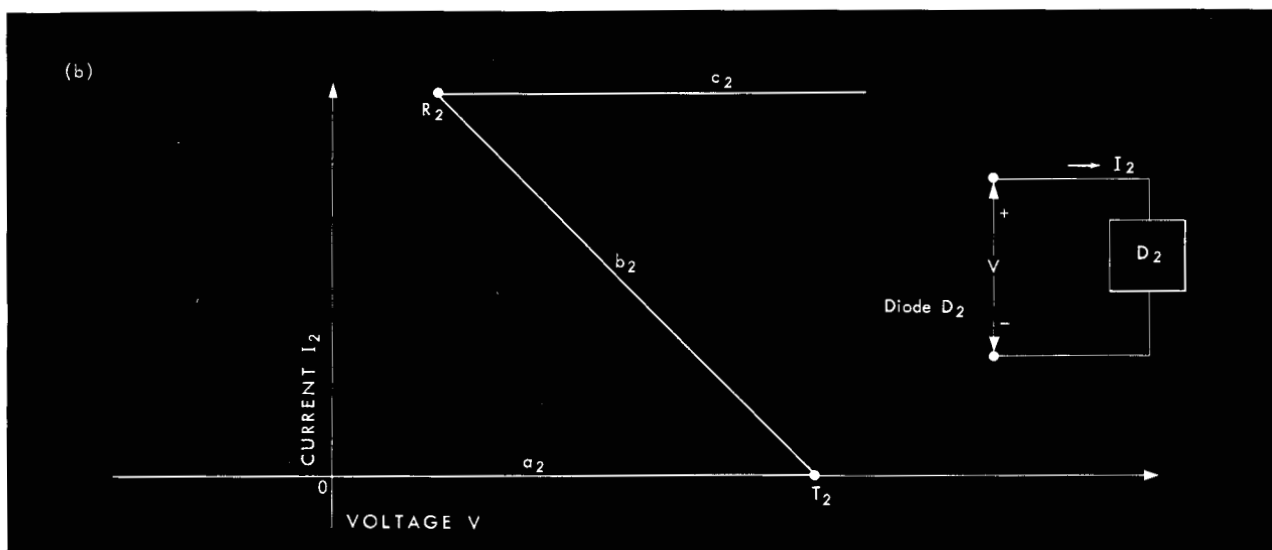
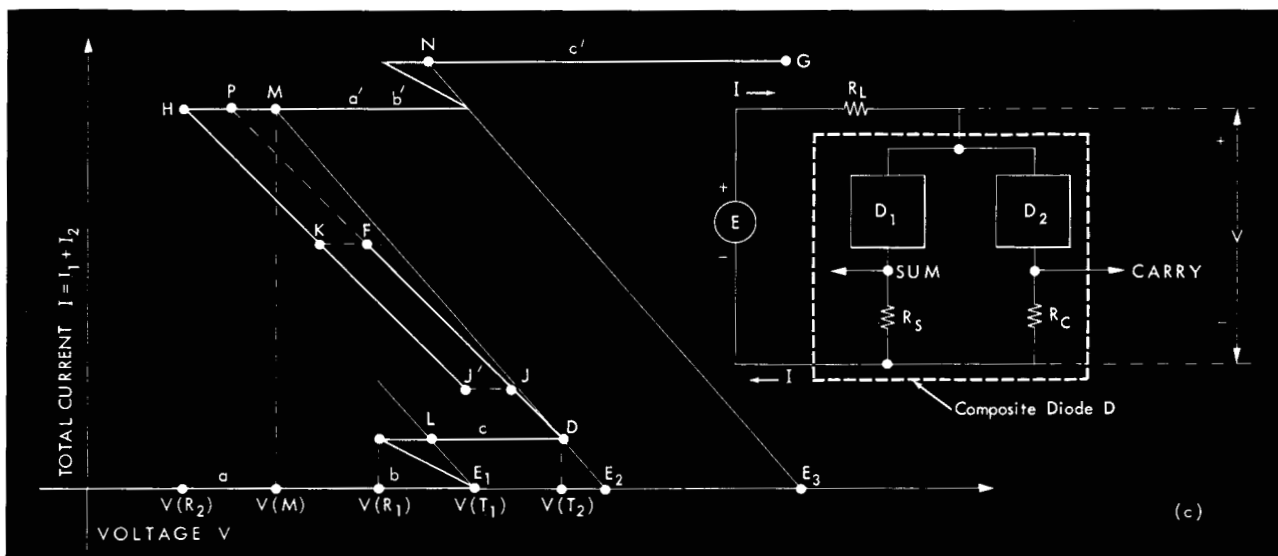


Figure 2c Composite characteristic of diodes D_1 and D_2 in parallel connection.



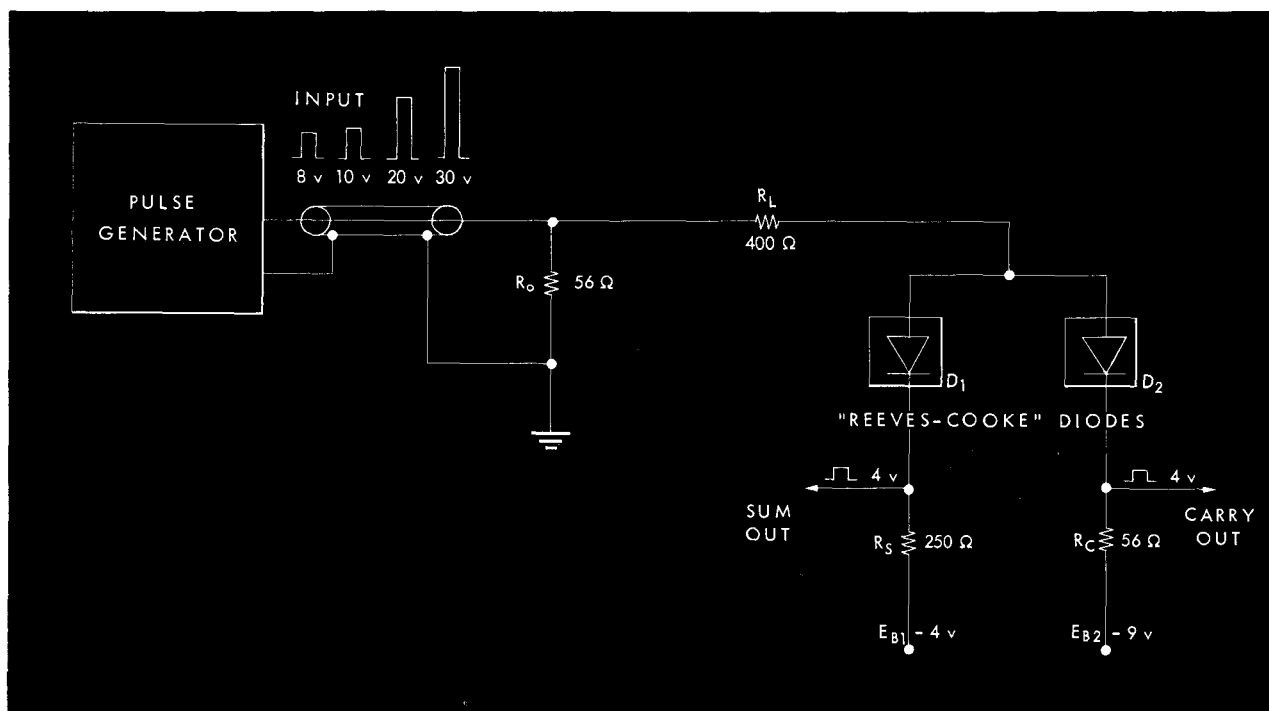


Figure 3 Schematic diagram of full binary adder employing two negative-resistance diodes.

Because the binary inputs in Fig. 1 are summed, it is necessary that the intervals $0-E_1$, E_1-E_2 and E_2-E_3 be approximately equal. In Appendix I the conditions for achieving this in general, and for obtaining voltage gain in the Sum and Carry outputs, are derived by graphical analysis.

Full binary adder employing "positive-gap" diodes of Reeves and Cooke

A binary adder was built and tested according to the principles discussed in regard to the circuit of Fig. 2c. Out of several existing possibilities, two negative-resistance diodes of the type described by Reeves and Cooke⁵ were used. These diodes were chosen because of their high speed of operation and because they are representative of an important class of negative-resistance semiconducting diodes. The circuit (Fig. 3) is the same as that of Fig. 2c except that R_s and R_c have been increased to values large enough to provide sizeable output signals and to affect the operation of the circuit. Furthermore, biasing batteries have been added which alter the size of the input pulses required for operation. Both of these differences are studied in detail in Appendices I and II. The dc characteristics of the diodes D_1 and D_2 are shown in Fig. 4. For short pulses ($<20 \text{ m}\mu\text{sec}$), the turnover voltages may be as much as a few volts greater than the static value.

The summed input to the adder was simulated (Fig. 3) by the 100-cps pulse output of a Spencer-Kennedy Lab. pulse generator. The pulse duration was $20 \text{ m}\mu\text{sec}$; the rise and fall times of the pulse across R_o in Fig. 3 were between 1 and $3 \text{ m}\mu\text{sec}$. The pulse voltage output of the

generator was set successively to the values 8, 10, 20 and 30 volts. As shown in the top two traces of Fig. 5, the 8-volt pulse produces a negligible feed-through to the outputs owing to the high off-resistances of both diodes. At 10 volts the Sum turns on, and the Carry feed-through is still negligible. In the next two traces with the input at 20 volts the Sum turns on momentarily giving a small spurious pulse. Eventually the Carry turns on and completely shuts off the Sum output. In the bottom two traces, the Sum and Carry are both full on. The output amplitudes here are seen to be equal and they are about 4 volts, indicating that a voltage loss of about a factor of 2.5 was experienced. With suitable diodes and correct circuit parameters, however, voltage gain can be realized in this circuit at both Sum and Carry outputs. The matter of output gain is taken up in Appendix I.

Further applications

The basic action ascribed to the adder of Fig. 1 can be achieved if the devices D_1 and D_2 are regenerative, voltage-level-sensitive devices (of the Schmitt-trigger type, for instance). If D_1 has a high input impedance and is capable of providing gain at the Sum output (for example, if D_1 were a triode tube) then only D_2 need be regenerative for the circuit to provide binary addition with Sum and Carry gain. In this case D_1 provides an amplified Sum output with one unit of input signal. At two units, D_2 fires and shuts off D_1 ; at three units D_1 turns on again and D_2 is also on.

A second type of $I-V$ characteristic having negative resistance can be obtained by interchanging the voltage

and current axes of Fig. 2a. Such characteristics are found in practice — for example, in the plate characteristics of a tetrode⁶ (Dynatron). Dynatron-type characteristics are sometimes called short-circuit stable, whereas those of Fig. 2a are called open-circuit stable. Interchanging I and V in the characteristics of the devices D_1 and D_2 in Figs. 2a and 2b means that the ordinate of Fig. 2c is to be read $V = V_1 + V_2$. Consequently, an adder may be constructed from characteristics of the Dynatron or short-circuit-stable type by connecting the two devices in series. A transformation of the generator of Fig. 2c must be made; the final adder is shown in Fig. 6.

Appendix I — Details of adder operation

In this Appendix we shall show that an adder like that of Fig. 2c may be constructed which has voltage gain at the Sum and Carry terminals and operates with equal increments of input voltage. As a preliminary step we shall show how a given characteristic such as that of Fig. 2a may be modified to suit our purposes. In Fig. 7 a battery and a resistor R_s have been placed in series with a negative-resistance diode ND_1 whose I - V characteristic is shown as the dashed line with turnover point at T_1 . The solid curve is now the I - V characteristic seen looking into the composite device D . There are three features of the modified (solid) characteristic which will be used presently, viz., the shift in turnover voltage by amount E_B , the increase of slope resistance from b_1 to $b = b_1 + R_s$, and the fact that when the diode is on, the voltage across R_s can be seen to be just the dashed line segment indicated in Fig. 7 as V_s . The fact that the characteristic of D_1 may be shifted horizontally in the manner of Fig. 7 permits us to dispense with labelling the zero of voltage on the voltage axis. In Fig. 8 then, let us draw the voltage axis and assume that along it $I = 0$. On this axis, mark off three equal unit intervals AC , CE , and EF . The four points, A , C , E and F represent respectively the four states of E , the input voltage to the adder, which have to be $E = 0$, E_1 , $2E_1$ and $3E_1$. The turnover point of the composite

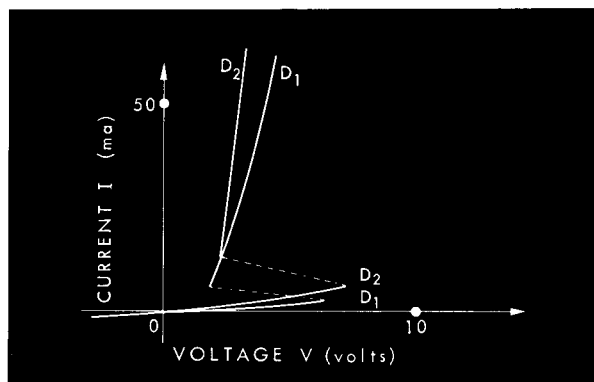


Figure 4 DC characteristics of Reeves-Cooke diodes used in full binary adder employing two negative-resistance diodes.

Figure 5 Sum and Carry outputs of full binary adder (Fig. 3). Pulse duration is 20 mμsec.

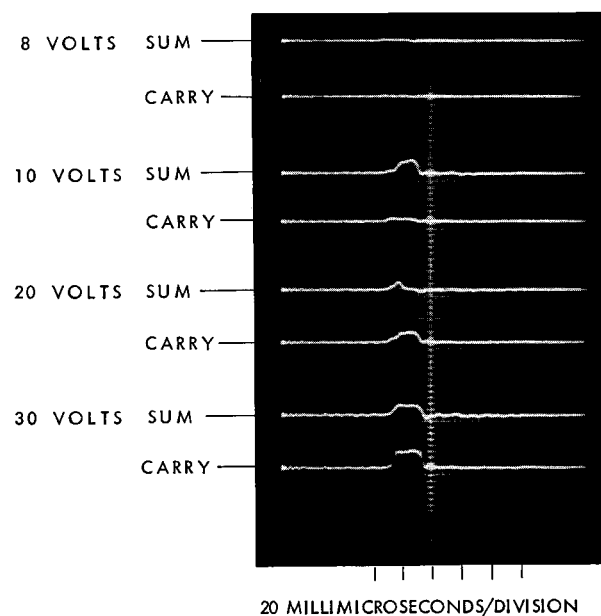
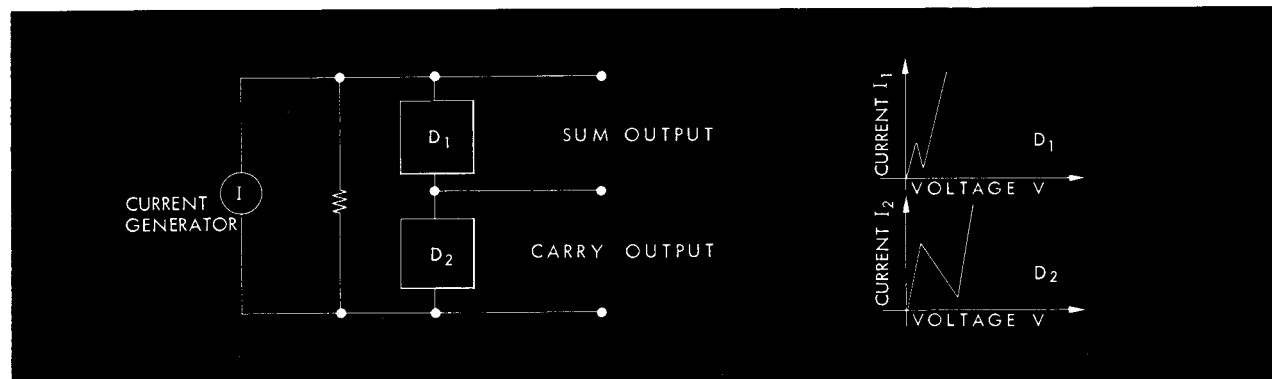


Figure 6 Schematic diagram of full binary adder employing two negative-resistance diodes in series connection.



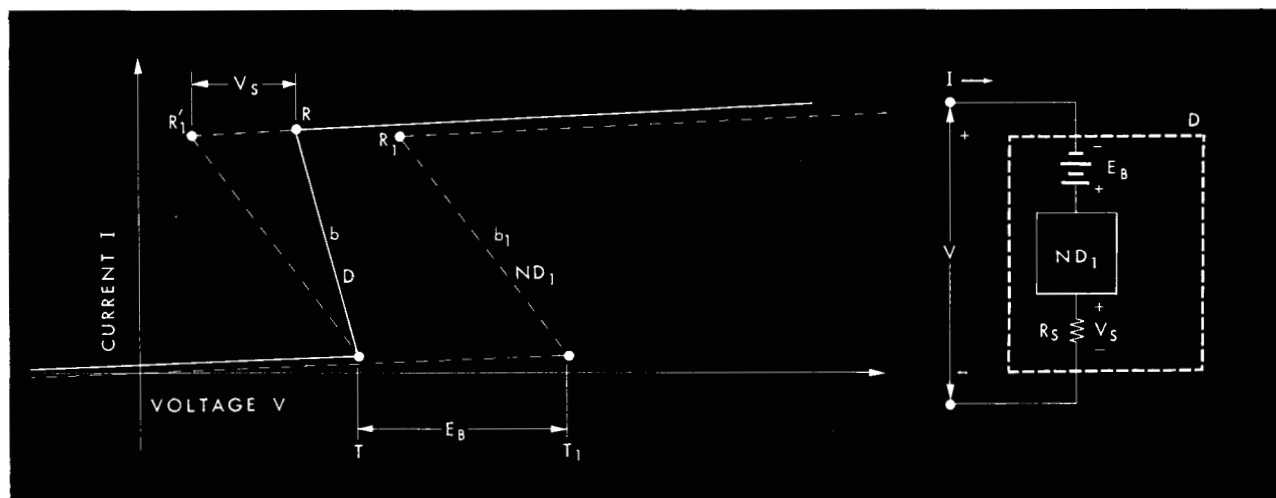
diode D_1 should lie midway between A and C for maximum firing tolerance; mark this point as B . Similarly, the turnover point for the composite diode D_2 should lie above C so that there is no possibility of this diode firing on one unit of input voltage (i.e., $E=E_1$); furthermore, it should also lie midway between C and E for maximum tolerance. Mark this point D .

The rest of the construction is as follows: Draw the verticals BG and DH . The turnover points of the diodes in the upper part of the composite characteristic must lie on these verticals, as is clear from Fig. 2c. Next, draw the horizontal line $J'J$ at distance AC from the voltage axis. This line can represent the c portion of the D_1 diode in general, because the current scale has not yet been specified. Arbitrarily choose as the b portion of the D_1 diode the vertical line BK . That this can be done has been made clear from Fig. 7. By making R_s sufficiently large, the b portion of the composite characteristic can be made vertical. Although this choice seems arbitrary, K can not lie too much further to the right along $J'J$ and some advantages can be lost by having it lie much further to the left. Next draw the load line CK , to show that at C the lower diode is turned fully on. Draw the other two load lines through E and F , parallel to CK . Note that the composite curve must turn over at L because the turnover of D_2 lies along DH . It now so happens because of the choice of the load line CK (B and D are fixed by the tolerance requirement) that EM will pass through L as it should. From intersection O of BG and FN , draw the horizontal OP . At point O both diodes must be on, so OP is the upper portion, c' , of the composite characteristic. The remainder of the upper portion of the composite characteristic may now be completed since the turnover point of D_1 must fall on BG , and OP is determined. This construction gives the upper part of the characteristic then as $POQR$. Now denote the intersection of the load line EM with the upper part of the characteristic as S . At S

the D_1 must be shut off which means that S must lie to the left of K , and it is seen in this case that this is so. Next, lay off T to the left of S by the tolerance amount arbitrarily equal to AB . We may consider that point T corresponds to point P in Fig. 2c, and consequently that the slope of TL is also the slope of b_2 . Draw DU parallel to TL ; point U now represents H of Fig. 2c and also the composite return point R of D in Fig. 7. To the left of U , lay off an interval equal to $2(AC)$; mark this point W' . From what was said about V_s in Fig. 7, then $W'U$ becomes the voltage across R_o , the carry output. Similarly, the point X may be laid off two units to the left of K for a voltage gain of 2 in the Sum output. The characteristics of the negative-resistance diodes ND_1 and ND_2 themselves are finally obtained by drawing $W'D$ and XB according to the construction in Fig. 7. These curves are shown separately in Fig. 9. If the origins of the available negative-resistance diodes were actually at O_1 and O_2 , then the battery voltages E_{B1} and E_{B2} would be required, as shown in Fig. 9, for point A to represent the zero-input condition ($E=0$).

Several qualitative and quantitative conclusions of interest can be drawn immediately from Fig. 8. In the first place, the tolerance in point B is that it could be as low as A but no higher than shown. This means that the turnover voltage of diode D_1 could drift down, and the circuit would still function. Similarly, D could drift down as far as C . If the fall in B and D could be kept to, say, 2 volts, then AC could be 4 volts. Turnover minus recovery voltage of the two diodes can be read off Fig. 8 as the abscissas WD and YB . In the present case, with a voltage gain of 2 in both outputs and taking AC as 4 volts, we have $WD=18$ volts and $YB=8$ volts. These values are readily achieved in practice. The current scale of Fig. 8 would be set by the speed of operation required. High speed frequently necessitates large turn-on currents to charge distributed capacitance rapidly. For pulses which rise in

Figure 7 Modification of the characteristic of negative-resistance diode ND_1 by series addition of biasing battery and resistor.



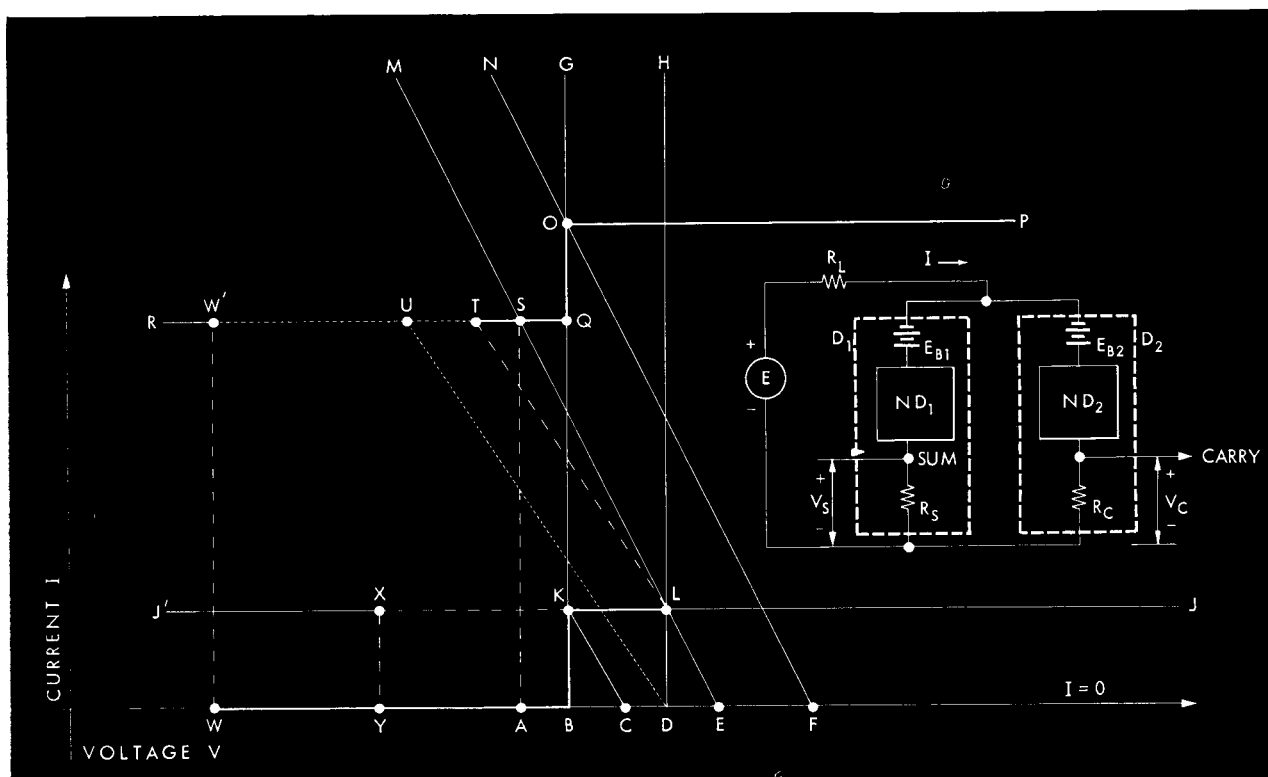
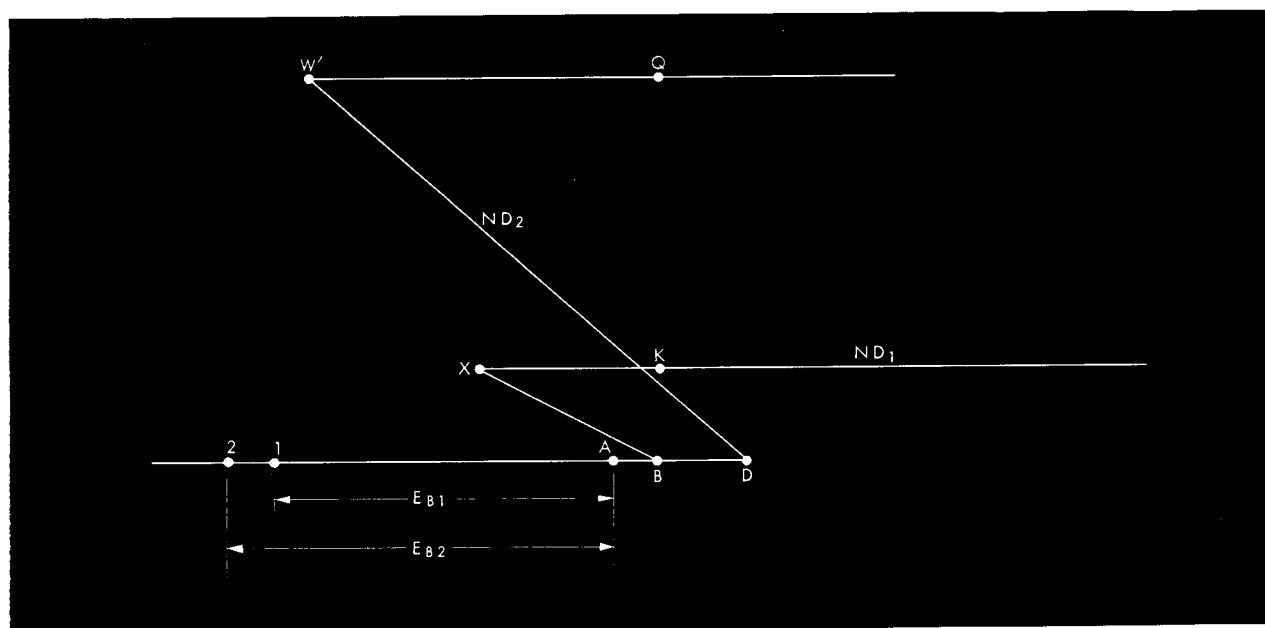
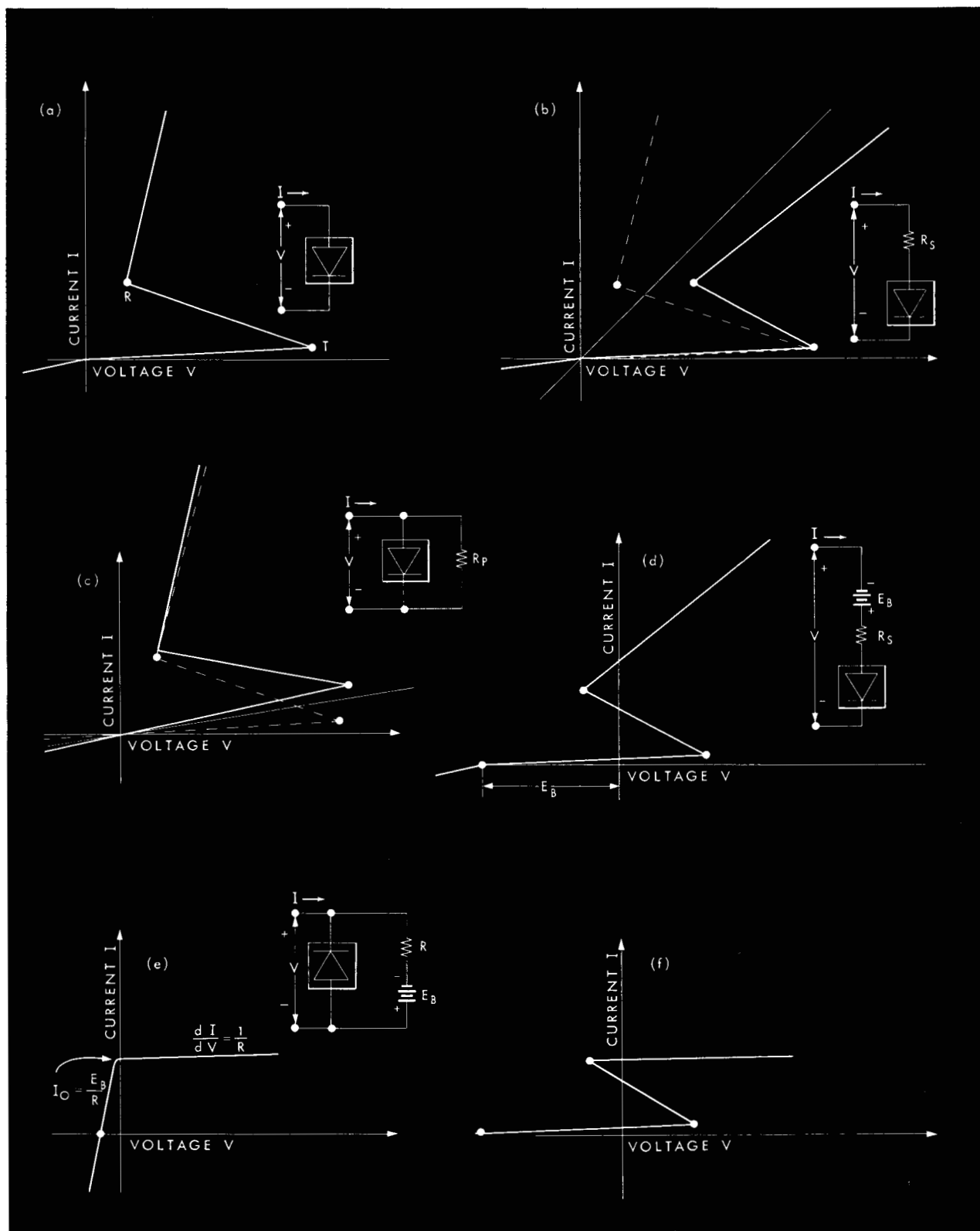


Figure 8 Graphic analysis of full binary adder employing two negative-resistance diodes in parallel connection.

Figure 9 Characteristics of negative-resistance diodes ND_1 and ND_2 derived from the graphical analysis of Fig. 8.





230 Figure 10 Modifying the observed characteristic of a negative-resistance diode.

several millimicroseconds, a current level for I_f of 10 milliamperes would be adequate. It is seen at once from Fig. 8 that the D_2 diode would have to pass 40 milliamperes in its "on" condition. Again, these are reasonable values. Once the current scale is established, and the tolerances are given so that the voltage scale is established, the load resistor R_L may be determined from the ratio of BC to BK . In the typical example being discussed here, BK is 10 milliamperes, and BC is 2 volts; hence R_L would be 200 ohms. This value is compatible with high speed operation.

In Appendix II, we shall show how the characteristics of a typical negative-resistance diode can be modified to yield an ideal one of the sort assumed in the preceding discussion.

Appendix II — Ideal characteristics from those of existing negative-resistance diodes

A representative type of negative-resistance diode might have the characteristics shown in Fig. 10a. The voltage gap might be 10 volts and the return current might be 10 milliamperes. In Fig. 10b, the effect of adding series resistance to the diode of Fig. 10a is shown by the heavy solid line. At each common current value, the corresponding voltages of the dashed and light lines have been added. In Fig. 10c, the effect of added parallel resistance is shown; here the current of the dashed and light-line curves have been added at each value of common voltage. In Fig. 10d, a battery is added in series with R_s and the diode. The effect is to shift the heavy solid curve of Fig.

10b horizontally to the left. In Fig. 10e a current limiter is shown. For small negative values of V a quiescent current, I_0 , flows through the rectifying diode to the battery, E_B , and the diode has a small value of slope resistance. Finally, I builds up to I_0 , and the diode opens up, whereupon the slope resistance changes abruptly to R . In Fig. 10f, the current limiter of Fig. 10e is put in series with the circuit of Fig. 10d, and the characteristic of Fig. 10f is obtained. Here again, the composite curve is obtained by adding voltages at each common value of current.

References

1. R. K. Richards, "Arithmetic Operations in Digital Computers," (Van Nostrand Company, Inc., Princeton, N. J., 1955), p. 89 ff.
2. R. M. Walker, D. E. Rosenheim, P. A. Lewis, A. G. Anderson, *IBM Journal* **1**, 257 (1957).
3. W. Shockley, *BSTJ* **33**, 799 (1954).
4. B. Dunham, *IBM Journal* **1**, 116 (1957).
5. A. H. Reeves and R. B. W. Cooke, *Electrical Communication* **32**, 112 (1955).
6. F. Terman, *Radio Engineer's Handbook*, (McGraw-Hill Book Company, Inc., New York, 1943).

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