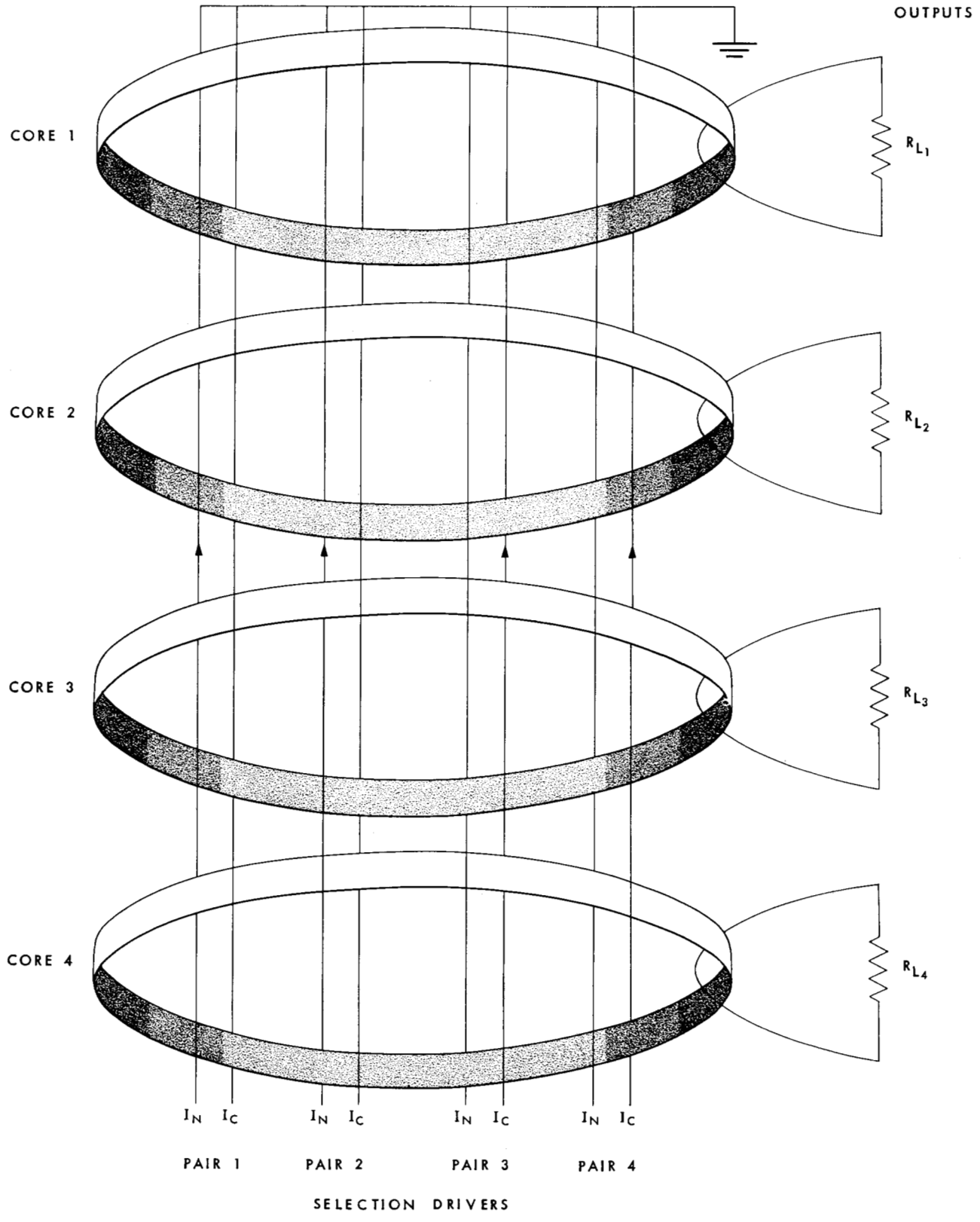

Figure 1 **Winding diagram for a 4-output, load-sharing matrix switch.**

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A Load-Sharing Matrix Switch

Abstract: A matrix-switch winding pattern has been developed which allows the power from several pulse generators to be combined into a single high-power pulse to drive a computer core memory. This pulse may be directed into one of a group of outputs. The method of operation, including the logical basis for changes in number of outputs, is described.

The device is suitable for the X-Y drivers of a transistor-driven core memory because one switch allows a group of fast, low-power transistors to deliver a large drive pulse to one drive line on one side of the memory. A 16-output load-sharing matrix switch has been used in the X-Y drive system for a 2-μsec memory.

Introduction

Load-sharing matrix switches combine the power from several sources into a single, high-powered output pulse. Each pulse generator feeding this type of matrix switch need furnish only a fraction of the power delivered to the load. A load-sharing matrix switch in this way permits use of relatively low-power, transistorized drivers to operate a core memory requiring large pulses for its drive lines.

Conventional matrix switches are commonly used to reduce the number of drivers necessary to operate a core memory. A matrix switch described by J. A. Rajchman[1] operates 200 memory drive lines with 40 drivers. R. E. Merwin[2] describes how the IBM 705 uses 33 unipolar drivers and two matrix switches instead of the 260 drivers which would be required for direct connection to memory drive lines.

It can be important, however, in a transistor-driven core memory to economize on the amount of power required from each driver. This reduction of required driver power is achieved by a load-sharing matrix switch and is especially useful in a core memory requiring more driver power than can be obtained from available transistors.

In a load-sharing matrix switch described by Rajchman,[3] several unselected cores receive excitation which tends to drive them further into saturation. This results in spurious outputs and an increased driver load. Spurious outputs from the matrix switch might start to switch unselected memory cores and destroy their stored information or produce incorrect outputs from the memory. Also, the drivers must furnish the additional power which goes into spurious outputs and is wasted.

This paper describes a load-sharing matrix switch with a minimum of spurious outputs.

Operation of the load-sharing matrix switch

The novel characteristics of this new load-sharing matrix switch result from the pattern in which the input wires are wound on the cores, and from the manner of pulsing them. The pattern of winding the inputs through the switch cores ideally results in zero net ampere-turns of excitation on all cores except the selected one if the pulse generators are operated properly. The new principle described in this paper may be called "load-sharing selective excitation." The choice of input voltage and current supplied to the selected core, the number of turns on the input and output windings, and the core dimensions and material are a matter of transformer design and are not of major concern here. Whether linear or square-loop core material is used in a particular application might affect such transformer characteristics as pulse droop, but would not affect the ability of the input windings to excite only one core. Our main interest, therefore, is in the manner in which the input windings are connected and pulsed.

The properties of the load-sharing matrix switch to be discussed here are the selection of a single output, the low noise level on the remaining outputs, and the load-sharing action.

The windings for a simple four-output load-sharing matrix switch are shown in Fig. 1. The pulse generators are shown as current sources and the memory drive lines as resistor loads for the outputs. An output pulse is delivered to a resistor load by simultaneously pulsing one wire of each input pair. The pulse pattern for Normal N or Complement C wires determines which output will be selected to receive the pulse.

Core 3, for example, may be selected by applying input currents 1_N, 2_N, 3_C, and 4_C. The total input excitation on the core is four times the ampere-turns supplied

from each winding because all the currents pass through the core in the same direction. Core 3 acts as a transformer with a certain input excitation to deliver a *read* pulse to the load R_{L3}. Similarly currents 1_C, 2_C, 3_N, and 4_N add in Core 3, but since the excitation is in the opposite direction a *write* pulse is delivered to the load R_{L3}. Table 1 lists the combination of input currents required to select each core in the four-output switch.

Figure 1 shows that each non-selected core will have two inputs exciting it in the *read* direction and two in the *write* direction. To the extent that the input currents are equal at each instant of time, each non-selected core will have zero input excitation.

Figure 1 also shows that the output power from the selected core is contributed equally by the four operating input sources. If each input winding has the same number of turns and supplies the same number of ampere-turns, then each driver must supply the same current and the same voltage. Consequently each input driver supplies the same power. In this example a driver must furnish one-fourth of the power delivered to the load plus one-fourth of the power needed to operate the switch core.

This basic description of the matrix switch may be completed by a convenient way of describing the winding connections. We already know that each input winding has the same number of turns. The only unique property of a particular winding on a particular core is the direction of core excitation. We can designate a winding which excites a core in the *read* direction by *R* and one in the *write* direction by *W*. Table 2 shows the direction of excitation caused by each winding of our four-output matrix switch.

Tables 1 and 2 are a complete, simplified description of a four-output switch showing how the windings are connected and pulsed. Since the selection pattern for a *write* pulse in Table 1 is exactly the reverse of the selection pattern for a *read* pulse, the *write* pattern will be omitted from further discussion. Similarly, in Table 2 the complement winding in a pair always excites the core in the opposite direction from the normal winding. By the same reasoning, then, the direction of the complement winding will be omitted from further discussion. It seems reasonable to use a single pattern to represent the *read* selection pattern as well as the direction of excitation caused by each normal winding on each core. Table 3 is a pattern using *plus* and *minus* to describe a four-output matrix fully. To obtain a *read* selection pattern, substitute *N* for *plus* and *C* for *minus*. To obtain a *normal* winding pattern, substitute *R* for *plus* and *W* for *minus*. A matrix switch can then be described with a more compact notation.

Expansion of matrix switch size

The load-sharing matrix switch may be expanded most conveniently by doubling its size. The number of inputs as well as the number of outputs is doubled when the matrix switch is enlarged. A matrix switch pattern is doubled in size by repeating it in the first, second and third quadrants of an enlarged pattern. The reverse of the pattern is placed in the fourth quadrant to complete the expanded matrix-switch pattern.

The method of expansion is illustrated in Table 4. Table 4a shows the general method and Table 4b shows the expansion of a 4-output pattern into an 8-output pattern.

The method of expansion is reasonable because it is related to the way the switch operates. The basic pattern in Quadrant II corresponds to a 4-output, 4-input pair switch (Table 4b). Adding Quadrant III may be thought

Table 1 **The selection pattern for a 4-output matrix switch.**

	Read output					*Write output*			
Core	*Pair* 1	*Pair* 2	*Pair* 3	*Pair* 4	*Core*	*Pair* 1	*Pair* 2	*Pair* 3	*Pair* 4
1	*N*	*N*	*N*	*N*	1	*C*	*C*	*C*	*C*
2	*N*	*C*	*N*	*C*	2	*C*	*N*	*C*	*N*
3	*N*	*N*	*C*	*C*	3	*C*	*C*	*N*	*N*
4	*N*	*C*	*C*	*N*	4	*C*	*N*	*N*	*C*

Table 2 **The directions of excitation applied by the normal and complement windings on a 4-output matrix switch.**

	Normal windings					*Complement windings*			
Core	*Pair* 1	*Pair* 2	*Pair* 3	*Pair* 4	*Core*	*Pair* 1	*Pair* 2	*Pair* 3	*Pair* 4
1	*R*	*R*	*R*	*R*	1	*W*	*W*	*W*	*W*
2	*R*	*W*	*R*	*W*	2	*W*	*R*	*W*	*R*
3	*R*	*R*	*W*	*W*	3	*W*	*W*	*R*	*R*
4	*R*	*W*	*W*	*R*	4	*W*	*R*	*R*	*W*

of as the addition of 4 outputs. Quadrants II and III of the enlarged pattern describe a switch mutation which selects a pair of outputs. One of the selected pair is always in Quadrant II and the other always in Quadrant III. The two selected outputs always have the same polarity (*read* or *write*) pulse. Similarly, Quadrants I and IV describe a switch mutation with a pair of outputs as indicated above. The difference is that the two selected outputs have opposite polarity. The actual enlarged switch makes two switch mutation outputs add (for instance, Quadrants I and II) and the other two cancel (Quadrants III and IV). The expansion method is based on the addition and cancellation of switch mutation outputs in the top and bottom halves of the expanded pattern.

Decoding

The logical decoding which selects the drivers to turn on during a *read* or *write* pulse is different from that used in conventional matrix switches. Instead of picking one driver out of a large group, the new matrix switch requires that one driver in each pair be turned on during an output pulse.

The decoding network for this load-sharing matrix can easily be worked out from the selection pattern.

Summary and evaluation

Economy of driver power is certainly obtained by using the load-sharing matrix switch. For instance, each driver for a 16-output matrix switch has to supply only one-sixteenth of the output power and the power required to operate the switch core. The relatively low power required from each driver allows the use of fast, low-powered transistors[4] to obtain fast, high-power pulses for memory driving. However, there is no economy in the number of drivers. Two drivers per matrix switch output are required.

Low spurious outputs are obtained from this load-sharing matrix switch. Ideally, there would be no spurious outputs because the input excitation exactly cancels on non-selected cores. If the inputs in a practical situation have an amplitude variation of 9%, then the "worst case" spurious output from a non-selected core is 9% of the selected output. It can be shown that the "worst case" spurious output can occur only on one core at a time. In this situation the remaining non-selected cores must have no spurious outputs. Variations in the timing of drive pulses may be considered to be variations in their instantaneous amplitude in the determination of spurious outputs.

Low spurious outputs are an important advantage because little power is being wasted in the form of stray drive-line pulses that do no useful work. The power which the drivers must deliver is reduced by minimizing the spurious outputs. Also, they mean that the memory drive currents need not be lowered as much to keep spurious outputs from switching non-selected cores.

The load-sharing property of the matrix switch improves the reliability of the memory drive system. The open-circuit failure of a driver for a 16-output switch reduces the memory drive current only 6% because the excitation on the selected core is reduced only 6%. It is entirely possible in a practical situation for the memory drive current to remain within its tolerance if one driver fails. Actually an open circuit in a switch winding will be the most common failure if fuses are used in each input winding. For continued memory operation a shorted transistor must not become a shorted turn on the matrix switch.

The load-sharing matrix switch is a more complex device than conventional matrix switches. The decoding which selects the drivers to turn on is somewhat more complicated for this switch than for older types. There are more windings on this type of matrix switch than usual, although the construction technique shown later minimizes wiring difficulty.

Table 3 **Descriptive pattern for a 4-output matrix switch. This table represents the *read* selection pattern or the direction of the normal winding excitation.**

Core	*Pair* 1	*Pair* 2	*Pair* 3	*Pair* 4
1	+	+	+	+
2	+	−	+	−
3	+	+	−	−
4	+	−	−	+

Table 4a **General 2*N*-output matrix switch pattern.**

II *N* output pattern	I *N* output pattern
III *N* output pattern	IV complement of the *N* output pattern

Table 4b **Descriptive pattern for an 8-output matrix switch.**

	Pair				*Pair*			
Core	1	2	3	4	5	6	7	8
1	+	+	+	+	+	+	+	+
2	+	−	+	−	+	−	+	−
3	+	+	−	−	+	+	−	−
4	+	−	−	+	+	−	−	+
5	+	+	+	+	−	−	−	−
6	+	−	+	−	−	+	−	+
7	+	+	−	−	−	−	+	+
8	+	−	−	+	−	+	+	−

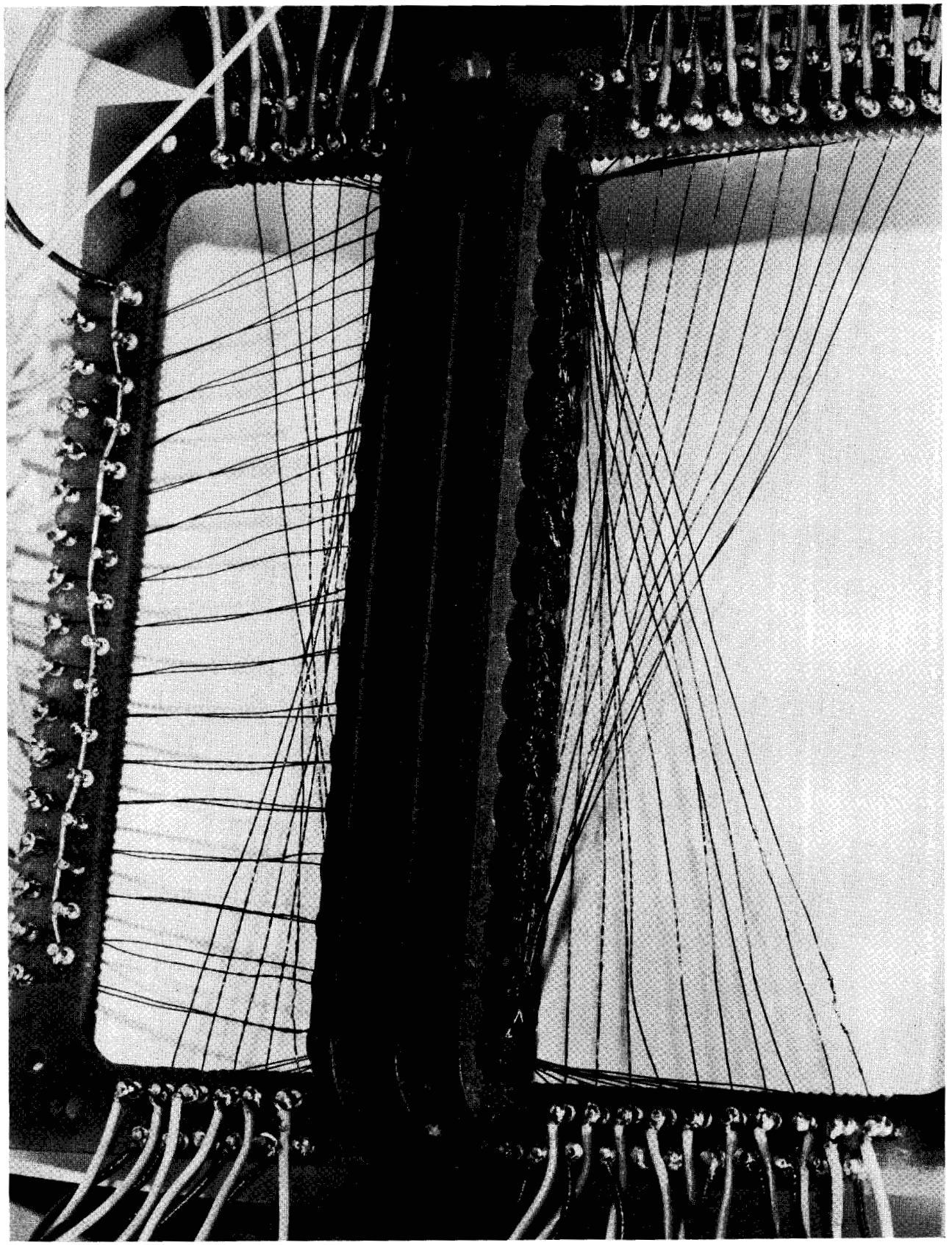


Figure 2 **A 16-output, load-sharing matrix switch constructed as a unit.**

Table 5 **Descriptive pattern for a 16-output, load-sharing matrix switch.**

	Input Pair Numbers															
Core	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
2	+	−	+	−	+	−	+	−	+	−	+	−	+	−	+	−
3	+	+	−	−	+	+	−	−	+	+	−	−	+	+	−	−
4	+	−	−	+	+	−	−	+	+	−	−	+	+	−	−	+
5	+	+	+	+	−	−	−	−	+	+	+	+	−	−	−	−
6	+	−	+	−	−	+	−	+	+	−	+	−	−	+	−	+
7	+	+	−	−	−	−	+	+	+	+	−	−	−	−	+	+
8	+	−	−	+	−	+	+	−	+	−	−	+	−	+	+	−
9	+	+	+	+	+	+	+	+	−	−	−	−	−	−	−	−
10	+	−	+	−	+	−	+	−	−	+	−	+	−	+	−	+
11	+	+	−	−	+	+	−	−	−	−	+	+	−	−	+	+
12	+	−	−	+	+	−	−	+	−	+	+	−	−	+	+	−
13	+	+	+	+	−	−	−	−	−	−	−	−	+	+	+	+
14	+	−	+	−	−	+	−	+	−	+	−	+	+	−	+	−
15	+	+	−	−	−	−	+	+	−	−	+	+	+	+	−	−
16	+	−	−	+	−	+	+	−	−	+	+	−	+	−	−	+

The following sections show that the load-sharing matrix switch can be built in a practical form and operated as a useful device.

Present application

A computer now being designed will contain a 2-μsec memory driven by transistors. A drive line for this memory requires a 585-ma, 100-v pulse. Therefore the peak power input to the drive line is 58.5 w.

The drive pulse can be obtained from a 16-output load-sharing matrix switch. The descriptive pattern is shown in Table 5. The total peak-power input to the matrix switch is about 65 w because the switch efficiency is about 90%. Each of the 16 drivers operating during a pulse furnishes about 4.1 w peak power. Fast transistors can be obtained to deliver 11-v pulses with a 0.1-μsec rise time. Each transistor furnishes a 370-ma, 0.5-μsec pulse.

The ferrite switch cores are 125 mils I. D., 250 mils O. D., and 1.8 inches long. The core is made in 12 sections to facilitate core fabrication and matrix switch winding. Each core is made of two adjacent stacks of 6 sections to reduce winding length. Figure 2 shows the present construction of the matrix switch.

Since the switch must provide fast, high-power pulses, the stray capacity and inductance are minimized by winding the matrix switch as a unit rather than as separate cores with connections.

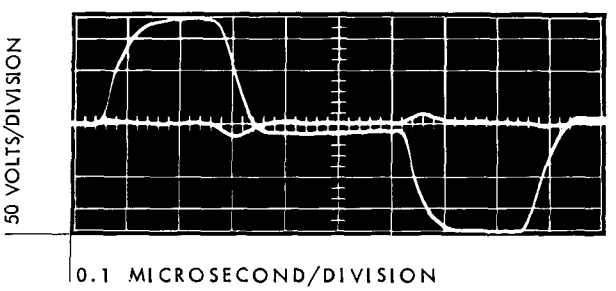
The selected output and the maximum non-selected output of the present matrix switch are shown in Fig. 3.

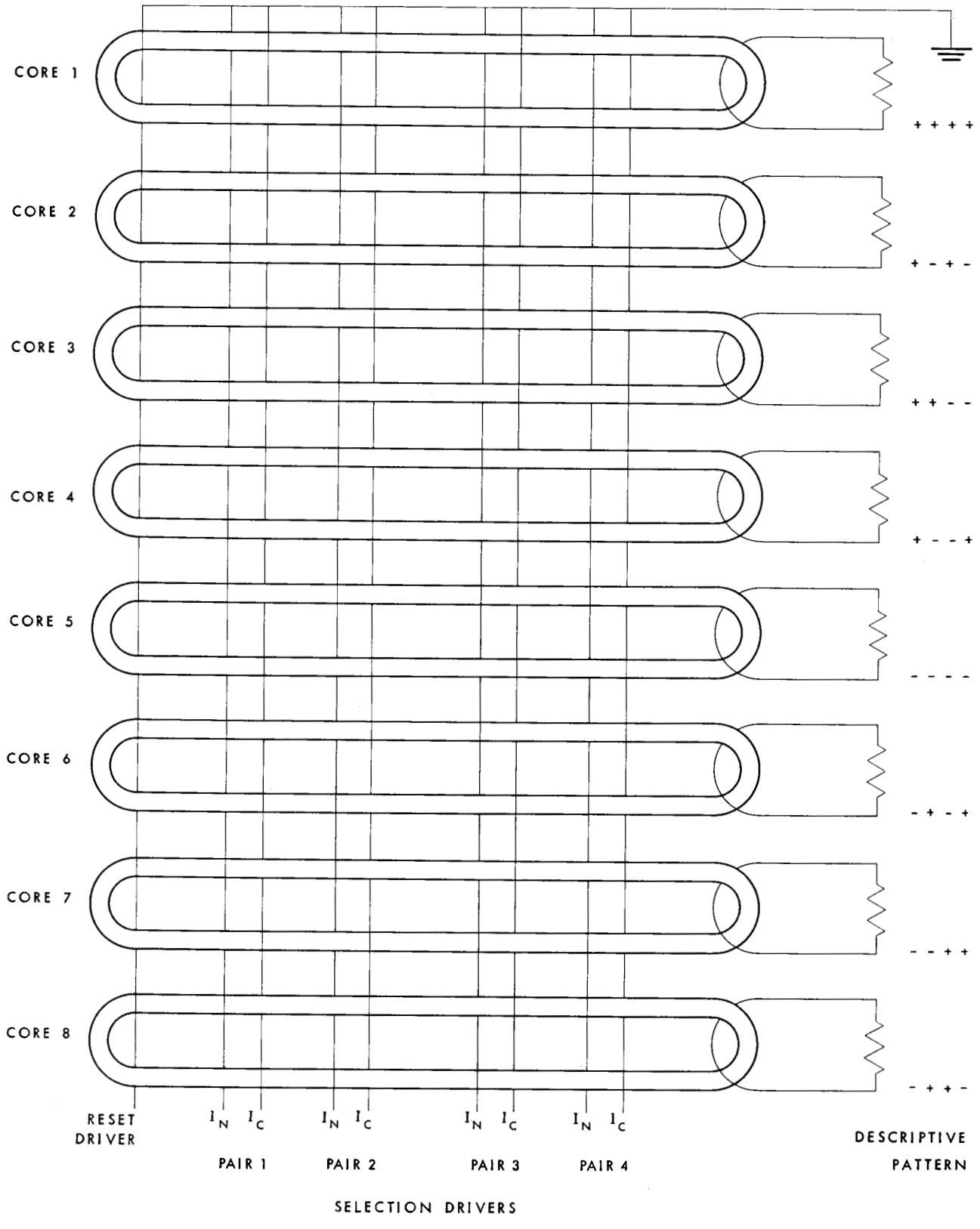
Possible applications

Although a load-sharing matrix switch has been built in a given configuration with a particular set of electrical characteristics, it has many possible applications. Generally speaking, the principle of "selective excitation" can be used wherever a high-power pulse must be delivered to one of a group of loads. Selective excitation may be combined with several conventional matrix switches which depend on the excitation of one load (a row of cores) out of a group of loads (several rows in a matrix). Such combinations would divide the power presently required from a single driver among several drivers.

The coincident current matrix switch described by Rajchman[1] is a rectangular array of biased cores. Currents equal to the bias are applied to one row and one column. The core at the intersection of the selected row and column then gives an output. Coincident current matrix switch operation depends on the excitation of one row out of several and one column out of several. A set of load-sharing windings could be wound on the cores in

Figure 3 **The selected output and the maximum spurious non-selected output of a load-sharing matrix switch. The same vertical oscilloscope scale is used for both.**





210 *Figure 4* **An 8-output, load-sharing, modified matrix switch.**

a similar matrix of biased cores so that each column of cores has identical windings, and thus one column could be excited separately. Another set of load-sharing windings could be wound on the cores to excite each row similarly. The noise outputs would be essentially those of a conventional coincident-current matrix switch. Thus two "crossed" winding sets could be used to share among several smaller drivers the load normally fed by a single driver.

The "set-a-line" type of matrix switch[5] also depends on the excitation of a single row and a single column of cores in a ferrite plate. Therefore, two sets of windings could be used to share the load normally fed by a single "set-a-line" matrix switch driver.

A somewhat more novel variation of the winding scheme has been developed. The winding diagram for a modified load-sharing matrix switch is shown in Fig. 4. It can be seen that the number of selection drivers for this 8-output matrix switch is the same as the number of drivers required for a 4-output basic matrix switch. A reset winding, which is connected to a large driver capable of supplying the entire output power, has been added. The selection drivers have the same selection pattern as a matrix switch on half of the cores and the complement pattern on the other half of the cores. The cores used must have high remanent flux. The cores are kept reset to a reference state of a remanent flux between cycles by the reset driver. In the modified load-sharing matrix switch, the selection drivers are pulsed in the same manner used for a basic matrix switch. Actually two cores receive excitation during the selection pulse—one is driven out of the reference state and one is driven toward the reference state. The latter would have a somewhat larger output than the other non-selected cores. Thus more outputs can be obtained by adding a reset winding and driver and by tolerating some slightly higher spurious outputs.

Acknowledgment

Of the many people who contributed to this work, L. B. Stallard did most of the early design and testing of the matrix switch. N. G. Vogl, Jr. worked out the present design, and R. J. Flaherty did the logical design for the decoding network. W. W. Lawrence, Jr. was Project Engineer in charge of this work. The work on which this paper is based was supported by the Department of Defense.

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