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Effects of Low Temperatures on Transistor Characteristics*

Abstract: The four-pole parameters of a group of similar *pnp* alloy junction transistors were measured in the frequency range from 0.5 to 5 mc and from room temperature down to that of liquid nitrogen. The measured parameters are translated into simple electrical networks for application in these frequency and temperature ranges.

Theoretical expressions for the transistor parameters are evaluated. This evaluation utilizes the effects of temperature on surface-recombination effects, on hole mobility, and on carrier lifetime that have been reported in the literature.

The transistors were subjected to grounded-emitter pulse tests in which the transistors were driven from beyond cutoff to the edge of saturation. These tests show that, for a given output pulse current, rise time decreases with temperature. The tests with the transistor in liquid nitrogen show further that rise time decreases as the output current pulse increases. Under these conditions it is possible for a 30 mw, 3 mc alloy-junction transistor to deliver a one-ampere output current pulse with a rise time of a few tenths of a microsecond and with a grounded-emitter gain of about 20.

Introduction

Transistors, like many other types of mechanical and electrical devices, operate less effectively as temperatures increase. For this reason new and improved transistor materials are being sought. The advent of low-temperature technology, however, suggests the possibility of operating transistors efficiently in one of the many coolants now available. It seems desirable, therefore, to study the effects of low temperatures on transistor characteristics.

In this study several similar germanium *pnp* alloy transistors having a nominal power rating of 30 mw and a nominal grounded-base cutoff frequency of 3 mc were subjected to an extensive series of tests in the frequency range from 0.5 to 5 mc, at temperatures ranging from room temperature down to that of liquid nitrogen. These data provided an excellent opportunity to study the extent to which basic transistor theory is verified in practice. In addition, the measured parameters were translated into those of simple electrical networks that are valid over the frequency and temperature ranges used.

A liquid nitrogen bath, of course, permits power dissipation considerably greater than normal without exceeding the operating temperature limits within the transistor itself.

Grounded-emitter pulse-response data are presented, showing the effects of temperature on response and showing the effects of passing heavy currents through the transistor.

Theoretical considerations

The basic theory upon which transistor operation depends is now well understood.[1] In the development of the theoretical relationships the transistor equivalent circuit is assumed usually to comprise two basic parts, one of which is due to the so-called intrinsic transistor that accounts for the diffusion of minority carriers through the base region, and the other to several additional physical properties such as surface recombination, circuit capacitances, leakage losses, bulk resistances of the transistor elements, lead reactances, et cetera.

In their simplest form, the relationships that apply to the intrinsic transistor assume a one-dimensional model and a density of the minority carriers in the base region that is small with respect to the impurity concentration in

*Presented in part at 1957 Transistor and Solid State Circuits Conference (Sponsored by IRE-AIEE-Univ. of Pa.) at Philadelphia, Feb. 14, 1957.

this same region. Using those assumptions, expressions for y_{11i}, y_{12i}, y_{21i}, and y_{22i}, the four-pole parameters for a grounded-base *pnp* intrinsic transistor, are developed.[1] These expressions are:*

$$y_{11i}=G\theta \coth \theta+y_n,$$

$$y_{12i}=-(G\theta \operatorname{csch} \theta)/A,$$

$$y_{21i}=-G\theta \operatorname{csch} \theta,$$

$$y_{22i}=(G\theta \coth \theta)/A,$$

where

$$G=\left(\frac{q}{W}\right)\mu_p p_n \exp(\Lambda V_{eb'})$$

$$\theta=\left(\frac{W}{L_p}\right)\left(1+j\omega\tau_p\right)^{\frac{1}{2}}$$

$$y_n=\frac{G\sigma_b W}{\sigma_e L_n}(1+j\omega\tau_n)^{\frac{1}{2}}$$

$$\frac{1}{A}=\frac{1}{\Lambda L_p}\frac{\partial W}{\partial V_{cb'}}\operatorname{csch}\frac{W}{L_p}+\frac{\exp(\Lambda V_{cb'})}{\exp(\Lambda V_{eb'})}$$

To represent the transistor more completely, certain elements are added to those representing the intrinsic transistor, as shown in Fig. 1. In this Figure, $y_{bb'}$ is the bulk base conductance, y_{SR} is the surface-recombination admittance, $b_{cb'}$ is the collector-base barrier susceptance, and b_c is the susceptance arising from stray capacitive effects in the high-impedance collector circuit.

In this study four *pnp* alloy junction transistors, having a 30-mw nominal power dissipation rating at room temperature and a nominal grounded-base cutoff frequency of 3 mc, were tested in ambient temperatures ranging from that of liquid nitrogen to room temperature (300°K). During the tests the applied dc collector-base voltage was held at −6 v and the dc emitter current was held at 4 ma. For several temperatures in the range used, the small-signal, four-pole admittances of the transistors were measured in the frequency range from 0.5 to 5 mc, inclusive. Of interest, then, are not only the results obtained from these tests, but also the extent to which these results corroborate the theory of transistor operation.

In the study of the theoretical relationships involved, the following assumptions are made:

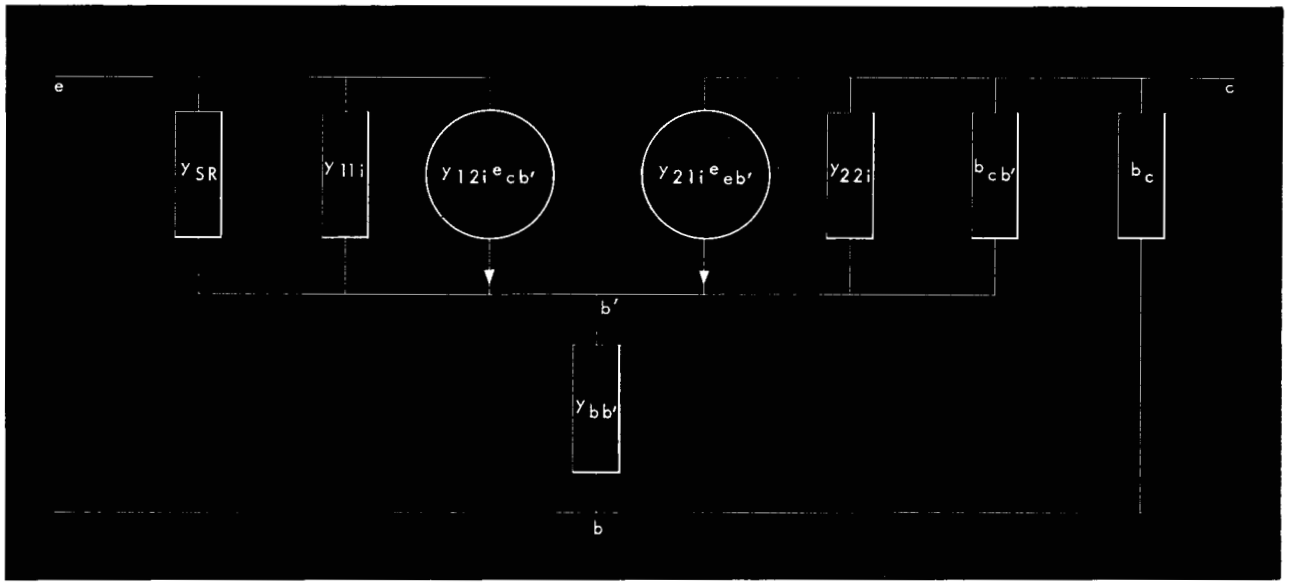
1. In the temperature range used, the physical dimensions of the transistor are not appreciably altered.
2. The transistor operates extrinsically.
3. The permittivity of germanium is independent of temperature in the range considered.
4. The electrical base width is not appreciably affected by temperature in the range considered.
5. Since the base width is small with respect to diffusion length and since the collector acts as an infinite sink for minority carriers in the base, the minority carrier density in the base is a linear function of distance into the base measured from the collector-base boundary.
6. The admittances arising from surface-recombination effects and from the flow of base majority carriers across the emitter-base boundary are small with respect to the admittances arising from the flow of base minority carriers from the emitter through the base into the collector.

Using these assumptions we find that $G=qI_e/kT$.

Extensive studies have been made on mobilities of carriers in germanium. These studies show that the relationship between mobility and temperature is characterized by a log-log plot on which the curve exhibits a

*For symbol definitions and units, refer to Appendix.

Figure 1 **Transistor equivalent circuit.**



negative slope near room temperature and a positive slope near 0°K. The temperature at which the inflection in the curve occurs is a function of the resistivity of the germanium under consideration. It has been reported[2] that in the higher temperature region the relationship between mobility and temperature is, to a good approximation, $\mu_p \propto T^{-2.3}$. Because of the extended temperature range of measurements reported in this paper, however, this relationship does not fit at the lower end of the temperature scale. A better first-order approximation might be obtained, therefore, by using an exponent somewhat less than that which applies in the upper temperature range. For the moment, then, let $\mu_p \propto T^b$, where b is a constant to be determined.

The expression for θ may be rewritten in the form

$$\theta = W\sqrt{\frac{q}{\mu_p kT}}\left(\frac{1}{\tau_p}+j\omega\right)^{\frac{1}{2}}$$

$$= AWT^d\left(\frac{1}{\tau_p}+j\omega\right)^{\frac{1}{2}}$$

where A is determined by physical constants and the constant of proportionality between μ_p and temperature; and d by the choice of b.

If, now, $\omega > 10(1/\tau_p)$, then, to a good approximation,

$$\theta = AWT^d\sqrt{\omega}\ \angle 0.5\tan^{-1}\omega\tau_p\ .$$

Further, if $\omega >> 1/\tau_p$, then

$$\theta = AWT^d\sqrt{\omega}\ \angle 45°.$$

The effects of these approximations on transistor parameters will be discussed in this paper.

With respect to the expression for $1/A$ we note that with $V_{cb'} = -6$v, the term $\exp(\Lambda V_{cb'})/\exp(\Lambda V_{eb'})$ is completely negligible. If, now, we make the assumptions that have been listed above and use the values of the physical constants listed in the Appendix, then

$$\frac{1}{A} = 1.727\times 10^{-8}\frac{T}{W\sqrt{\sigma_n}}$$

where σ_n is the conductivity of the base region at 300°K.

The admittance $y_{bb'}$ is considered to be the base bulk conductance, and thus has no susceptive component. The value of the base bulk conductance depends upon the dimensions of the base and the conductivity of the base material. This latter is $\sigma_n = qn_n\mu_n$.

Since the germanium is operating extrinsically, $y_{bb'} \propto \mu_n$. The dependence of μ_n on temperature is subject to the same considerations as is the case with μ_p. Thus, we shall say that $y_{bb'} \propto T^f$, where f has a value that may differ from -1.6, the exponent generally applied in the range of room temperatures.

The remaining components of the circuit of Fig. 1 may be dealt with quickly. The literature[3] shows that

$$y_{SR} = qp_n sA_s\Lambda(1+j\omega\tau_p)^{\frac{1}{2}}\exp(\Lambda V_{eb'})$$

where A_s is the surface area over which surface recombination is effective and s is the surface recombination velocity. When the dimensions of the transistors under test are known the value of A_s may be estimated. It has been found[4] that the value of s is affected markedly by the condition of the germanium surface. For the transistors under test, the germanium surfaces had been carefully etched. Using the value of s corresponding to etched surfaces, an estimated value of y_{SR} may be obtained. This value was found to be small with respect to the value of y_{11i}, with which it is in parallel.

The value of the collector-base barrier capacitance may be estimated from the dimensions of the transistor, the depth of penetration of the electrostatic field into the base region and the permittivity of germanium. Thus the order of magnitude of $b_{cb'}$ for the frequency range involved may be obtained. The manner in which these values are adjusted will be discussed in the section entitled "Experimental Results."

The value b_c may be considered as a stray output susceptance that accounts for output terminal susceptances not otherwise included.

Unfortunately the point b' of Fig. 1 is not accessible for the connection of measuring equipment. The experimenter must restrict himself to measurements taken at the emitter, base and collector of the transistor. These measurements may be the usual four-pole parameters, y_{11b}, y_{12b}, y_{21b}, and y_{22b} of the network. Of interest, therefore, are the relationships between these measured admittances and the elements of the circuit of Fig. 1. Analysis of this latter circuit yields the following expressions:

$$y_{11b} = \frac{(y_{11i}+y_{SR}+y_n)(y_{22i}+jb_{cb'})-y_{12i}y_{21i}+(y_{11i}+y_{SR}+y_n)y_{bb'}}{y_{11i}+y_{SR}+y_n+y_{12i}+y_{21i}+y_{22i}+jb_{cb'}+y_{bb'}},$$

$$-y_{12b} = \frac{(y_{11i}+y_{SR}+y_n)(y_{22i}+jb_{cb'})-y_{12i}y_{21i}-y_{12i}y_{bb'}}{y_{11i}+y_{SR}+y_n+y_{12i}+y_{21i}+y_{22i}+jb_{cb'}+y_{bb'}},$$

$$-y_{21b} = \frac{(y_{11i}+y_{SR}+y_n)(y_{22i}+jb_{cb'})-y_{12i}y_{21i}-y_{21i}y_{bb'}}{y_{11i}+y_{SR}+y_n+y_{12i}+y_{21i}+y_{22i}+jb_{cb'}+y_{bb'}},$$

$$y_{22b} = \frac{(y_{11i}+y_{SR}+y_n)(y_{22i}+jb_{cb'})-y_{12i}y_{21i}+(y_{22i}+jb_{cb'})y_{bb'}}{y_{11i}+y_{SR}+y_n+y_{12i}+y_{21i}+y_{22i}+jb_{cb'}+y_{bb'}}.$$

In evaluating the expressions for these four parameters, nine quantities must be known in addition to such physical constants as the charge on an electron, Boltzmann's constant, et cetera. The nine quantities are the base width

W, the temperature T, the frequency ω, the minority carrier lifetime τ_p, the base conductivity σ_n, the collector-base capacitance $C_{cb'}$, the base spreading admittance $y_{bb'}$, and the admittances arising from majority carrier flow from base to emitter and from surface-recombination effects y_n and y_{SR}.

In Figs. 2 through 9 are shown plots of the theoretical real and the theoretical imaginary parts of the four transistor admittances as functions of temperature, each plot having curves for 1, 2 and 4 mc. These curves apply to a transistor in which the base width is 0.0015 cm (0.00058 in.), the base conductivity at 300°K is 1 (ohm-cm)$^{-1}$, the collector-base capacitance is 8$\mu\mu f$, and the base spreading conductance is 0.0095 mhos. The reasons for the choice of these values will become apparent later.

It is recognized that a basic assumption in the development of the theoretical relationships that have been presented is that minority-carrier density in the base region is small with respect to impurity density. It is also recognized that for the operating current used and for the conductivity of the base material, the ratio of carrier density to impurity density is not as small as might be desired at room temperature. However, as temperature is reduced, the ratio becomes smaller and the simplified theory more applicable.

It will be noted that the curves in Figs. 2 through 9 split apart at the low temperatures in some instances, becoming two or three curves. One branch is valid when the assumption that $\tau_p \rightarrow \infty$ holds. These curves are designated by the symbol ∞. There is evidence[4] that the lifetime of minority carriers decreases markedly as temperature is lowered from room temperature to that of liquid nitrogen. The reported observations indicate that a sample having a carrier lifetime of 70 microseconds at room temperature will have a carrier lifetime of 3 microseconds at liquid nitrogen. Using these values as a guide the assumed values for τ_p were compiled in Table 1. Where the upper limit values in Column A were used in computing the four-pole parameters, the curves are designated by the letter A, and where the values of Column B were used, the curves are designated by the letter B.

Table 1 **Assumed lifetime of holes in base region**

Temperature, °K	*Upper Limit (A)* τ_p, μsec	*Lower Limit (B)* τ_p, μsec
315	120.0	42.4
300	84.8	30.0
275	60.0	21.2
250	42.4	15.0
225	30.0	10.6
200	21.2	7.5
175	15.0	5.3
150	10.6	3.25
125	7.5	2.65
100	5.3	1.63
75	3.25	1.33

Table 2 **Hypothetical admittances arising from base-emitter electron flow and from surface recombination**

Temperature, °K	$y_{SR}+y_n$, *Mhos*
315	0.00149
300	0.00150
275	0.00165
250	0.00180
225	0.00200
200	0.00233
175	0.00370
150	0.00640
125	0.0112
100	0.0186
75	0.0310

Inspection of the four expressions for the four-pole parameters of the transistor reveals that portions of the numerators and the denominators are the same in all four expressions. It so happens that the denominator is of particular interest. Since the algebraic sum of the relatively large real terms of the intrinsic parameters is very small, a slight alteration in the real part of y_{11i} or y_{21i}, the dominant terms in the denominator, will markedly affect the real part of the denominator. In particular it is found that a 1% change in the real part of y_{11i} may affect some of the transistor parameters by as much as 10% at room temperature. The effect is even more drastic at lower temperatures, where the magnitudes of the intrinsic parameters become greater.

The presence of surface recombination produces changes equivalent to a variation of y_{11i} referred to above. There is evidence[4] that surface-recombination velocity is affected by temperature, increasing by a factor of 300 as temperature is decreased from room temperature to that of liquid nitrogen. Using this information as a guide, a table (Table 2) is set up in which an assumed value of $y_{SR}+y_n$ for each temperature is set down. These values are assumed to be real and are added to the appropriate values of y_{11i} in the computation of the transistor parameters, the plots of which appear in Figs. 2 through 9.

Experimental results and equivalent circuits

Experimental tests on the *pnp* alloy transistors of this study were carried out using a Wayne-Kerr Model B601 Admittance Bridge. A General Radio Type 1001-A Signal Generator served as a signal source, and an HRO-60 Receiver as a null detector. Direct-current bias for the transistor was supplied from dry cells with the proper voltage dividers and instruments for adjusting and observing dc operating conditions. There is, of course, the problem of preventing the dc circuits from affecting the ac measurements. To insure accuracy in measurement, special jigs were constructed. These jigs minimized lead inductances in the circuits under measurement and provided inductances and capacitances of sufficient magni-

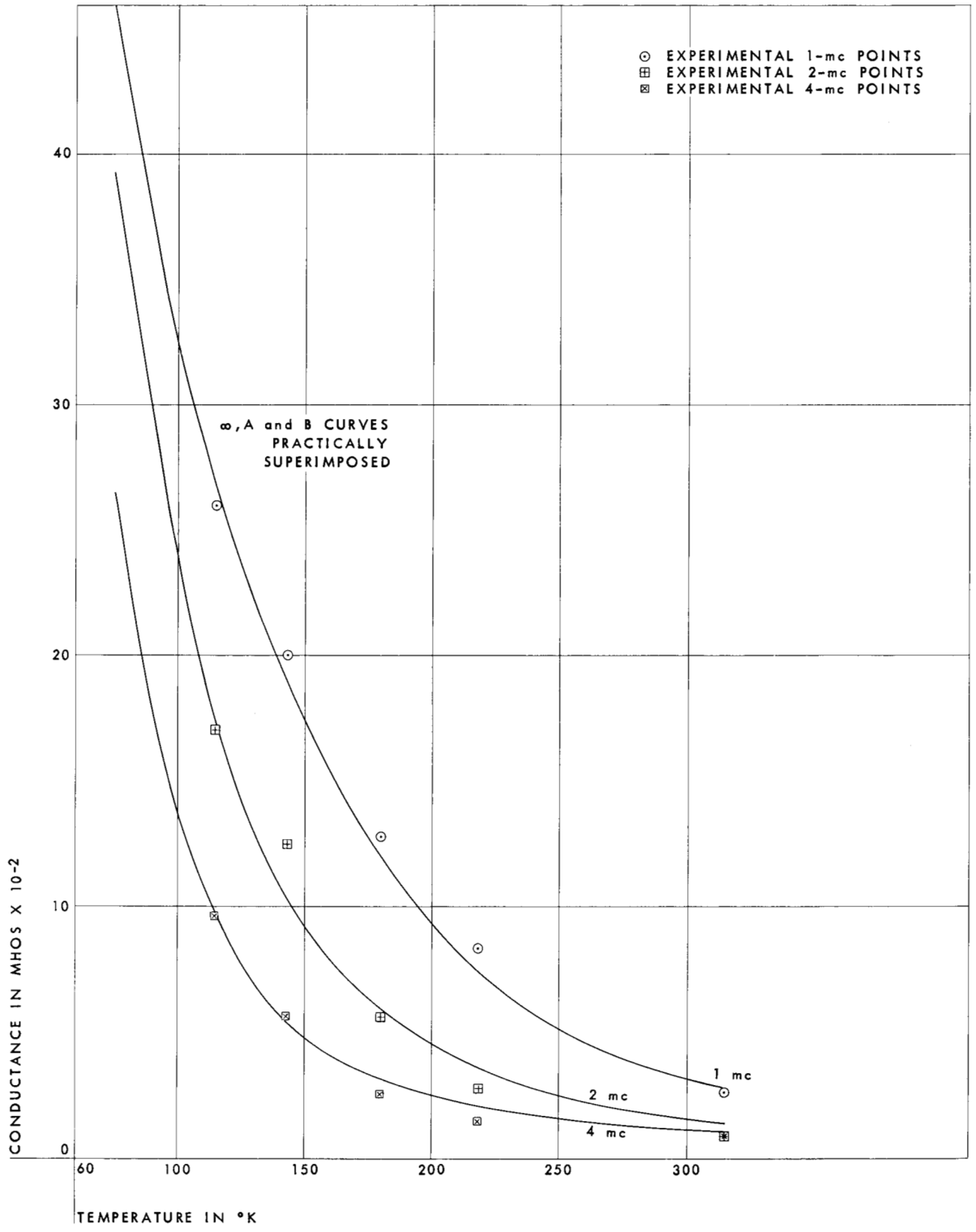


Figure 2 **Theoretical grounded-base input conductance, *pnp* alloy transistor. In this and succeeding figures, $V_{cb'} = -6v$ and $I_e = 4$ ma.**

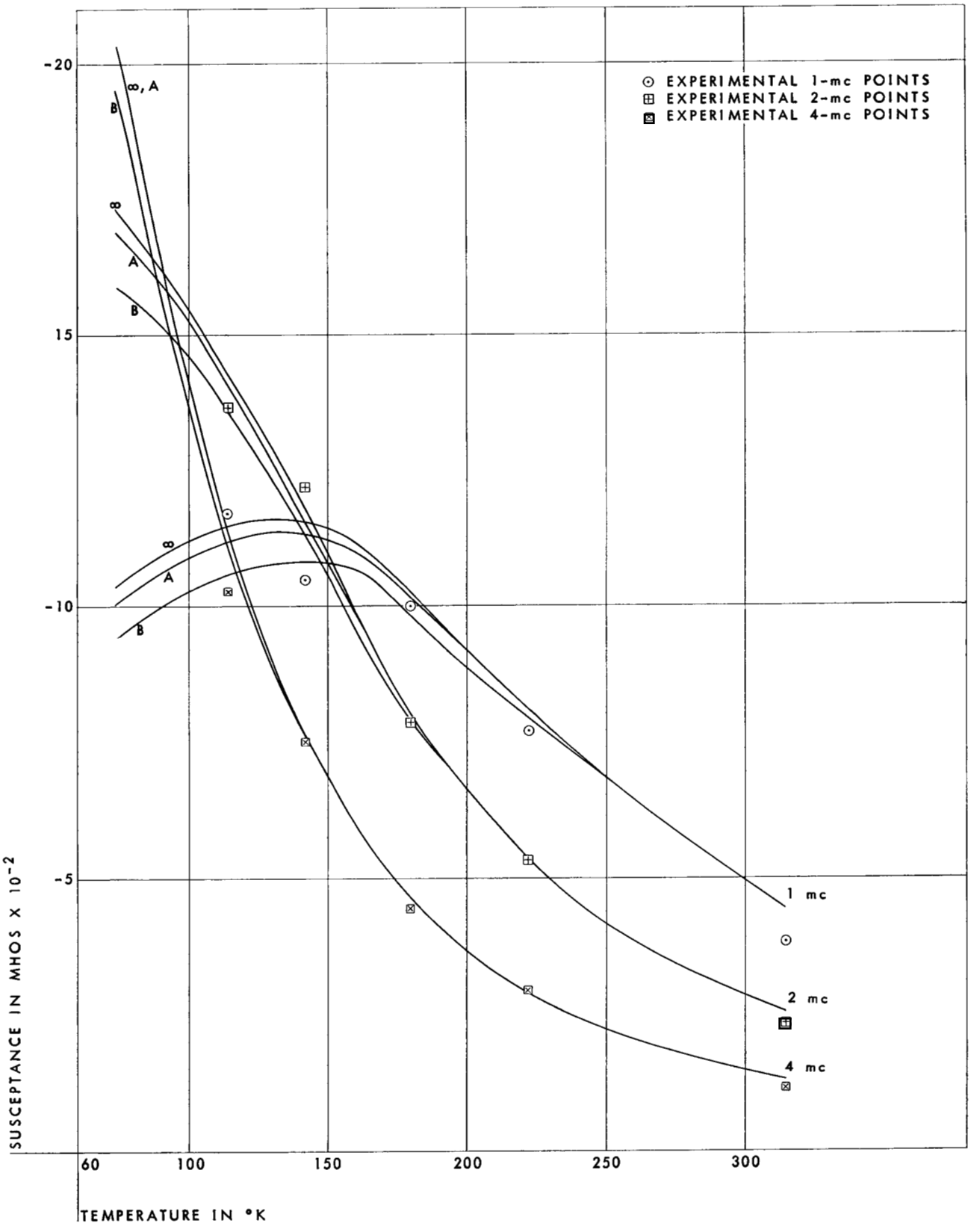


Figure 3 **Theoretical grounded-base input susceptance, *pnp* alloy transistor.**

tude to insure that measured values would be within a few percent of actual values. To insure accuracy, one set of jigs was used for the lower frequencies and a second set for the higher frequencies.

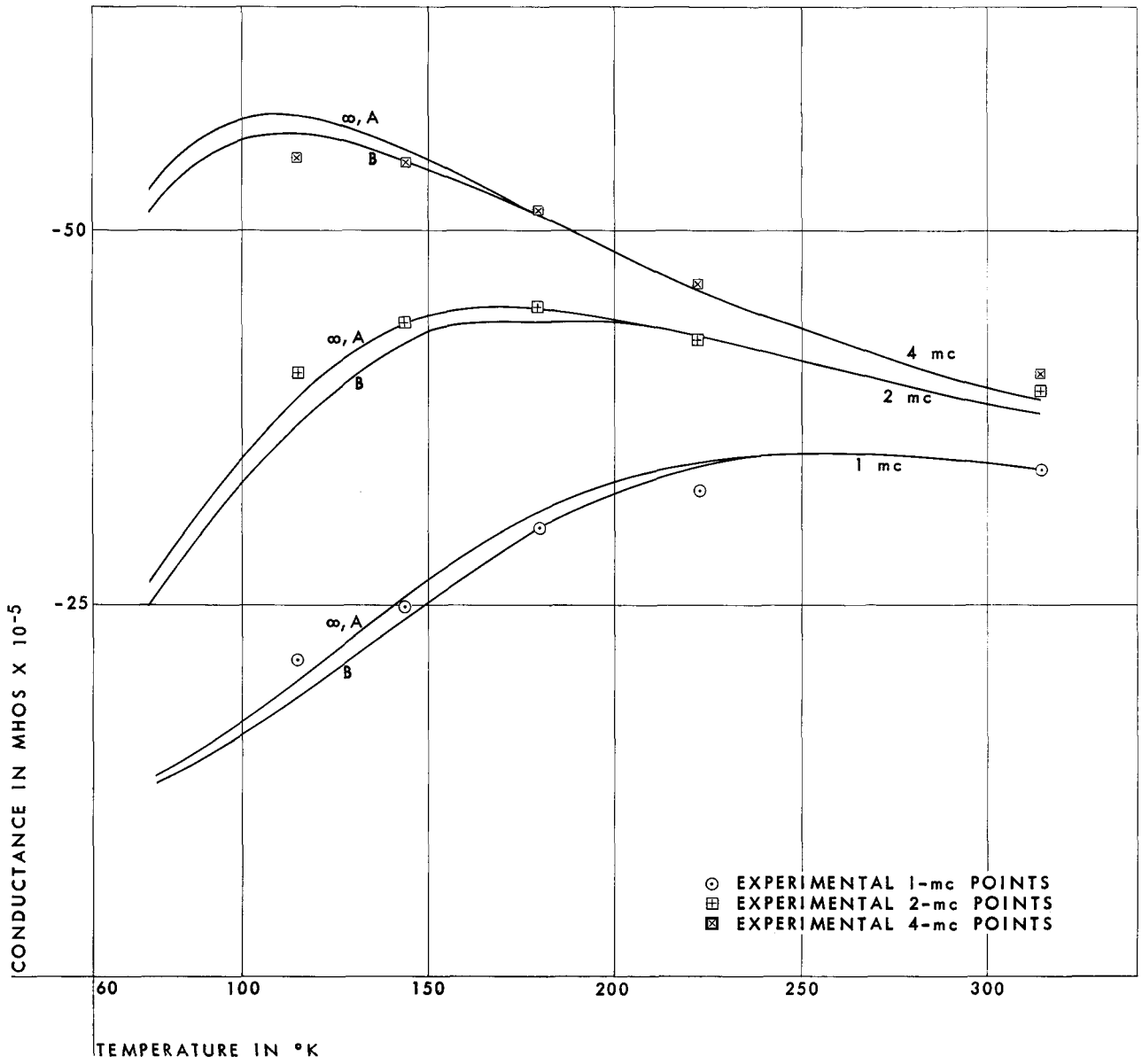
Early in the measurements it became apparent that at room temperature the algebraic sign of g_{21b} changed in the frequency range used. While it is possible to arrange the Wayne-Kerr Bridge to measure a negative conductance, the accuracy of the results is somewhat impaired and some complication is added to the calculation of the results. It seemed advisable, therefore, to avoid these inconveniences by measuring y_{11e} rather than y_{21b}. Since

$$y_{11e}=y_{11b}+y_{12b}+y_{21b}+y_{22b},$$

the measurement of the grounded-emitter parameter and three grounded-base parameters will permit the calculation of the fourth grounded-base parameter if desired. For this reason a set of grounded-emitter curves was included in the last section.

To control the ambient temperature, the transistor is snugly fitted into a milled slot in one end of a copper cylinder 1 inch in length and ½ inch in diameter. A small hole drilled radially into the cylinder allows the insertion of a thermocouple junction into the cylinder in such a way that it is in contact with the transistor case. This complete assembly is then inserted into a styrofoam jacket with outside diameter of 1¼ inches. The transistor emitter, base, and collector leads protrude from the end of the copper cylinder for insertion into the jig socket during measurements.

Figure 4 **Theoretical grounded-base reverse transconductance, *pnp* alloy transistor.**

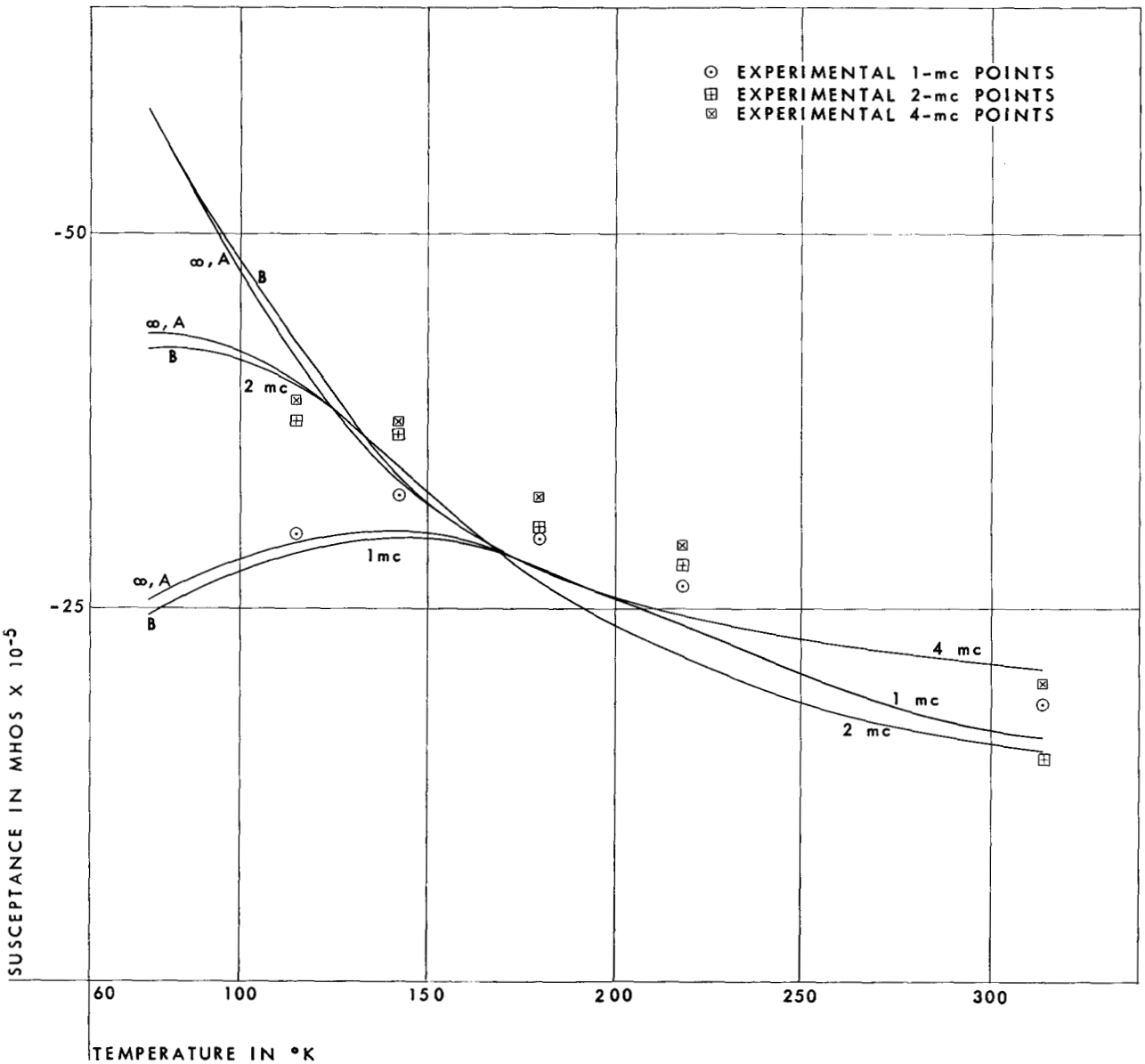


As a first step in the measurements, the copper cylinder with the transistor and the jacket were placed in liquid nitrogen and allowed to come to the temperature of the liquid. The assembly could then be removed by the operator who, using gloves, could easily and quickly insert it into the jig socket and proceed to balance the bridge, after having established the proper dc bias conditions. These initial steps could be taken several times to insure a minimum deviation of temperature from that of liquid nitrogen. The transistor was then allowed to warm up to room temperature with dc operating conditions fixed, and measurements taken at the desired temperatures as indicated by the thermocouple voltage. Usually about 25 minutes was required for this thermal transient. Temperature change was therefore slow enough so that the bridge could be maintained in balance for accurate measurements during the period.

The results of these tests were set down in graphical form coordinating each of the eight measured transistor parameters as a function of frequency and temperature. By this means any large errors in data could be quickly detected and the similarity of the four transistors could be verified. The problem to be solved at this point was the best means to bring these experimental data into agreement with the theoretical results predicted by the equations given above.

As a starting point, room-temperature conditions were considered, since quite a bit is known about the operation of the transistor under these conditions. For example it is known that with a 24-mw dissipation the tempera-

Figure 5 **Theoretical grounded-base reverse transsusceptance, *pnp* alloy transistor.**



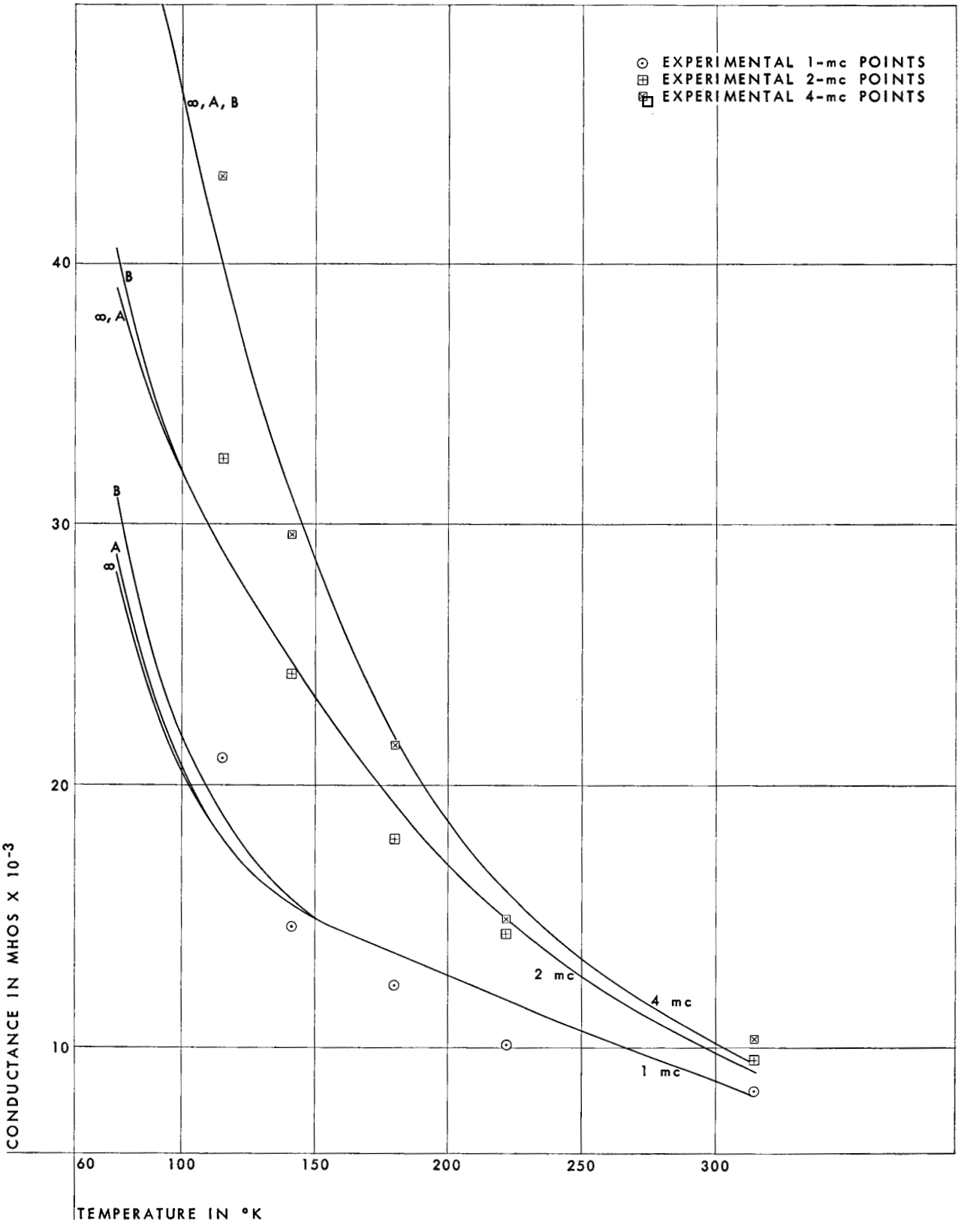


Figure 6 **Theoretical grounded-emitter input conductance, *pnp* alloy transistor.**

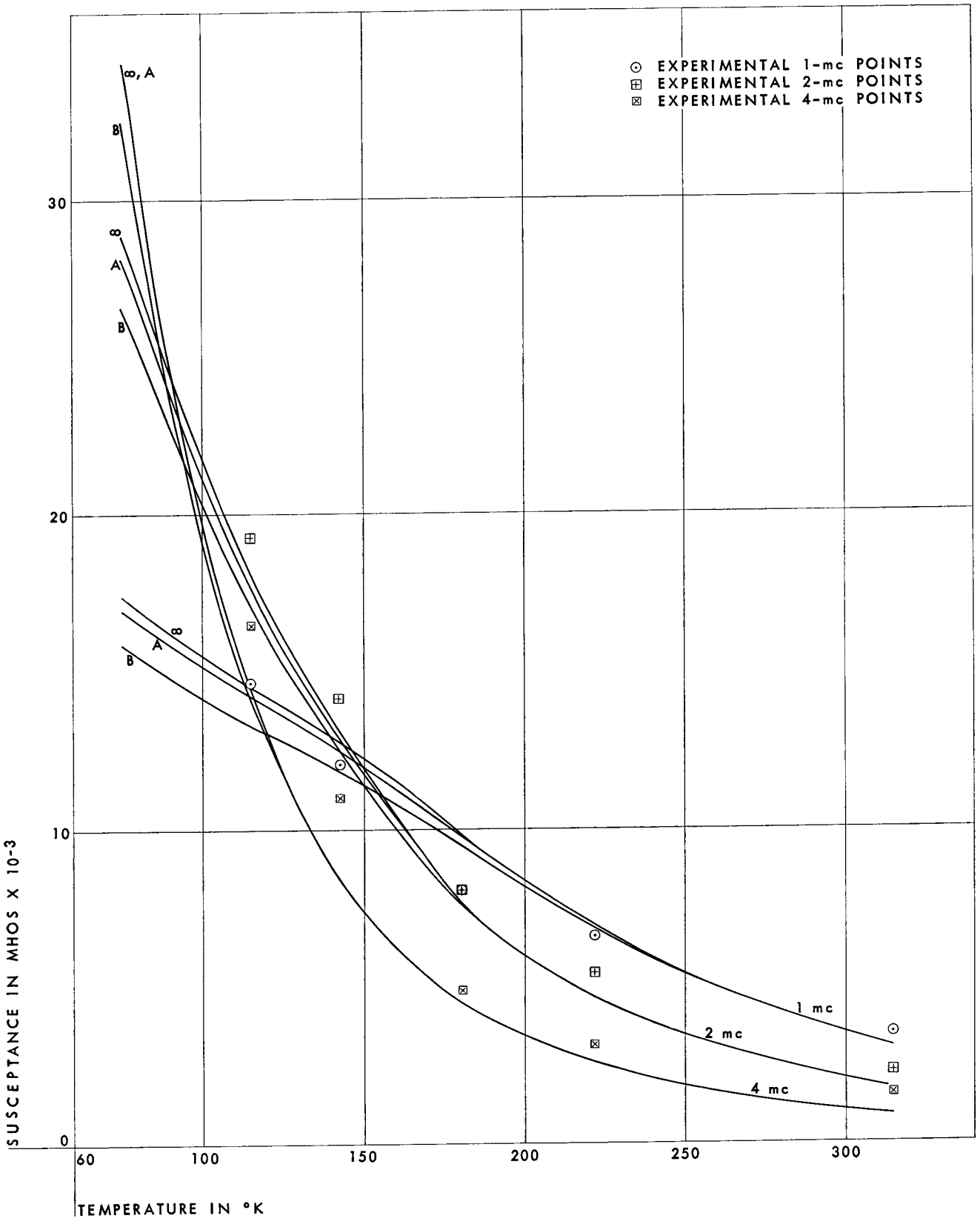


Figure 7 **Theoretical grounded-emitter input susceptance, *pnp* alloy transistor.**

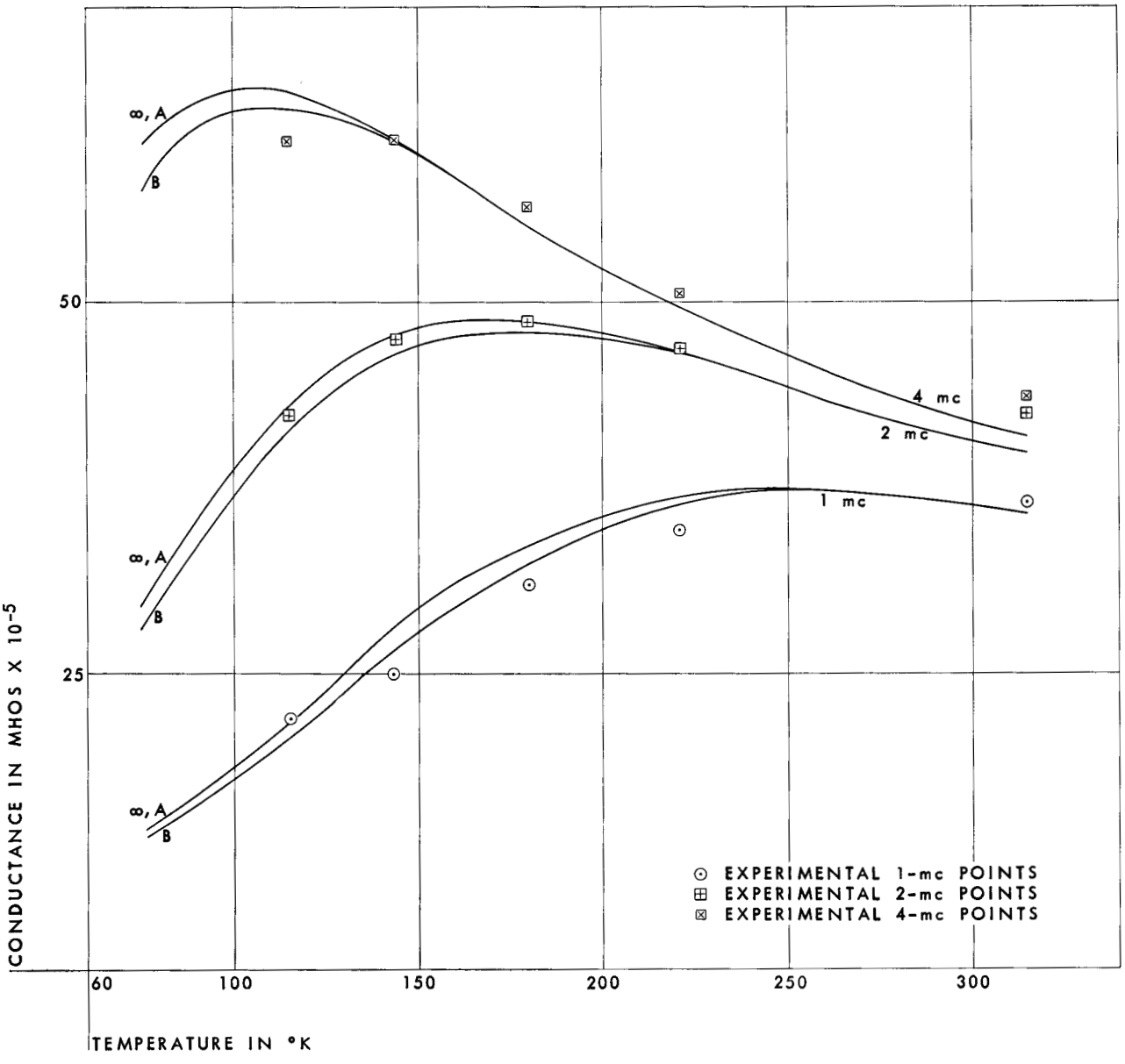
ture rise of the transistor should be about 15° above ambient. We therefore assume that the temperature is 315°K. Manufacturing specifications for base width, minority-carrier lifetime, and base conductivity were obtained. A final bit of information could be obtained from the experimental curves. The room-temperature curves for g_{11b} and g_{11e} seem to exhibit definite asymptotic tendencies. These values serve as a guide for the assumed value of $y_{bb'}$.

The theoretical equations can now be solved for y_{11b}, y_{12b}, y_{22b}, and y_{11e}.* The several variables involved were systematically varied in an effort to find the best agreement between theoretical and experimental results. For room temperature, theoretical and experimental values of g_{11b}, b_{11b}, g_{12b}, b_{12b}, g_{11e}, and b_{11e} were compared at frequencies of 1, 2, and 4 mc. The best agreement occurred for the values stated at the end of the previous section and with the value of $y_{SR}+y_n$ indicated for 315°K in Table 2. At this temperature minority-carrier lifetime in the range of values considered had no effect on predicted results.

Since the mechanical and electrical characteristics of the transistor are now specified at room temperature, it should be possible to use known and assumed temperature variations of these characteristics to obtain agreement between observed and predicted parameters over the temperature range used. Of interest, then, are the ways in which $y_{SR}+y_n$ and τ_p vary with temperature and the values of the exponents b and f, referred to previously.

*This work was done on the IBM 650 Data Processing Machine.

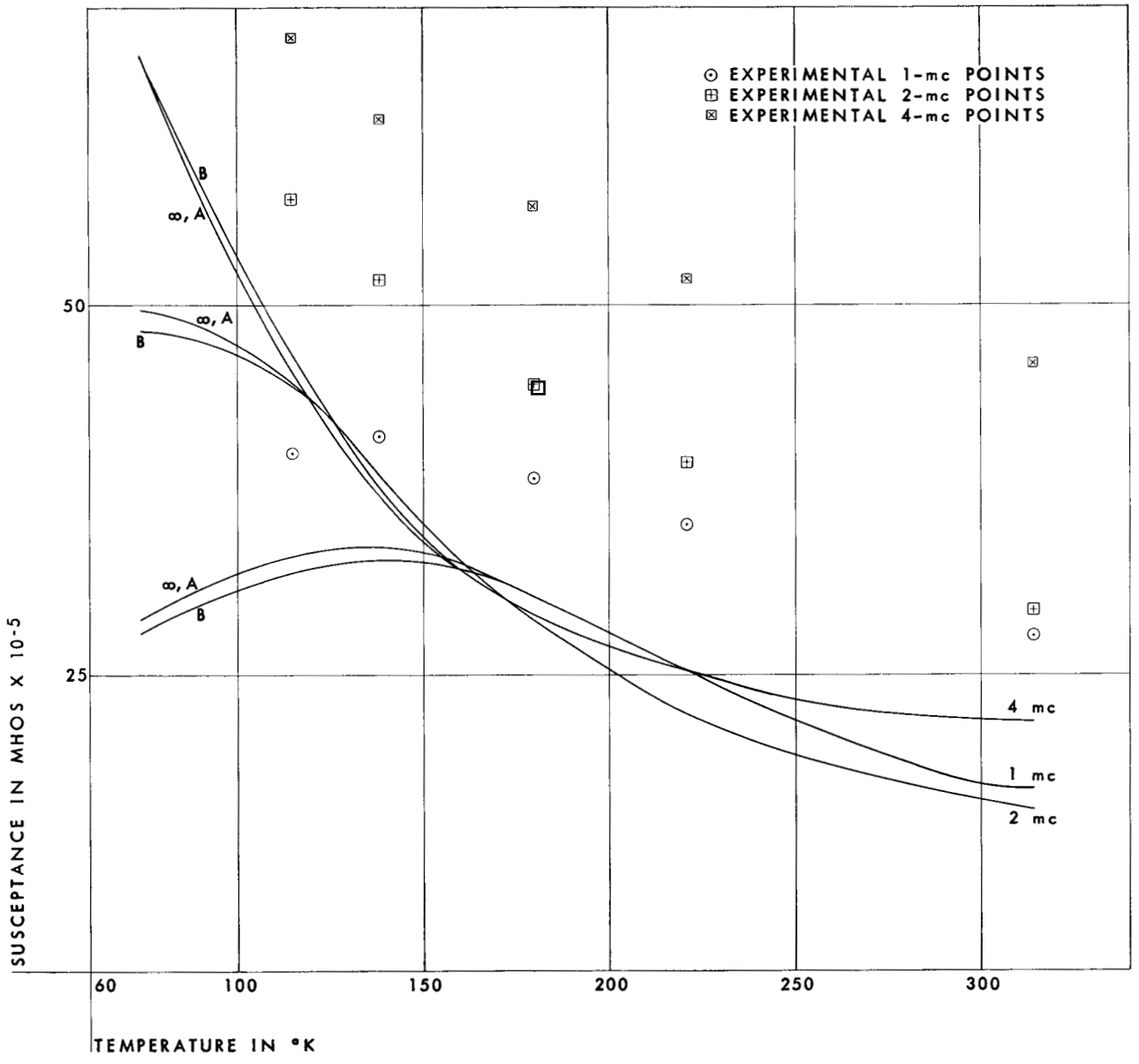
Figure 8 **Theoretical grounded-base output conductance, *pnp* alloy transistor.**



Tables of values for $y_{SR}+y_n$ and for τ_p and values for b and f were varied systematically in machine programs until the resulting theoretical curves were brought into best agreement with the experimentally observed results. The tables finally selected were those presented as Tables 1 and 2. The value chosen for b was -1.8 and that for f was -1.6.

A major problem in bringing the experimental and the theoretical curves into agreement is the determination of the temperature at which the transistor is operating. The thermocouple is in contact with the transistor case, but since there is a thermal gradient between the transistor and its case, the thermocouple indication must be corrected in some manner. We are certain that there is a one-to-one relationship between thermocouple indication and transistor temperature, since the dc operating conditions are always the same for a given thermocouple indication. Thus, with the transistor submerged in liquid nitrogen, the measured values of g_{11b}, b_{11b}, g_{12b}, b_{12b}, g_{11e}, and b_{11e}, when spotted on the theoretical curves in Figs. 2 through 7, should all lie at a temperature greater than that of liquid nitrogen. Actually, the temperatures corresponding to these experimental points on the theoretical curves will vary. The choice of tables of values for $y_{SR}+y_n$ and for τ_p and the choice of values for the exponents b and f were made to minimize the variation in these temperature indications, not only for the values measured at liquid nitrogen temperatures, but also for the values measured at other temperatures and spotted on the theoretical curves.

Figure 9 **Theoretical grounded-base output susceptance, *pnp* alloy transistor.**



The experimental data used in this matching procedure were taken from the experimental curves at 1, 2 and 4 mc for each of the five thermocouple temperatures used, namely, 80°, 125°, 175°, 215°, and 298°K. After matching had been optimized, it was found that the transistor temperatures corresponding to the respective temperatures listed above were 115°, 143°, 180°, 220°, and 315°K. The appropriate experimental points are therefore located at these latter temperatures in Figs. 2 through 7. It can be seen that there is a reasonably good agreement between theory and experiment.

It will be noted that, in the effort to correlate theory and practice, the curves for g_{22b} and b_{22b} were not used. It was thought that in the low-admittance output circuit the measurements would be very susceptible to any stray conductances or susceptances that might exist across the output terminals.

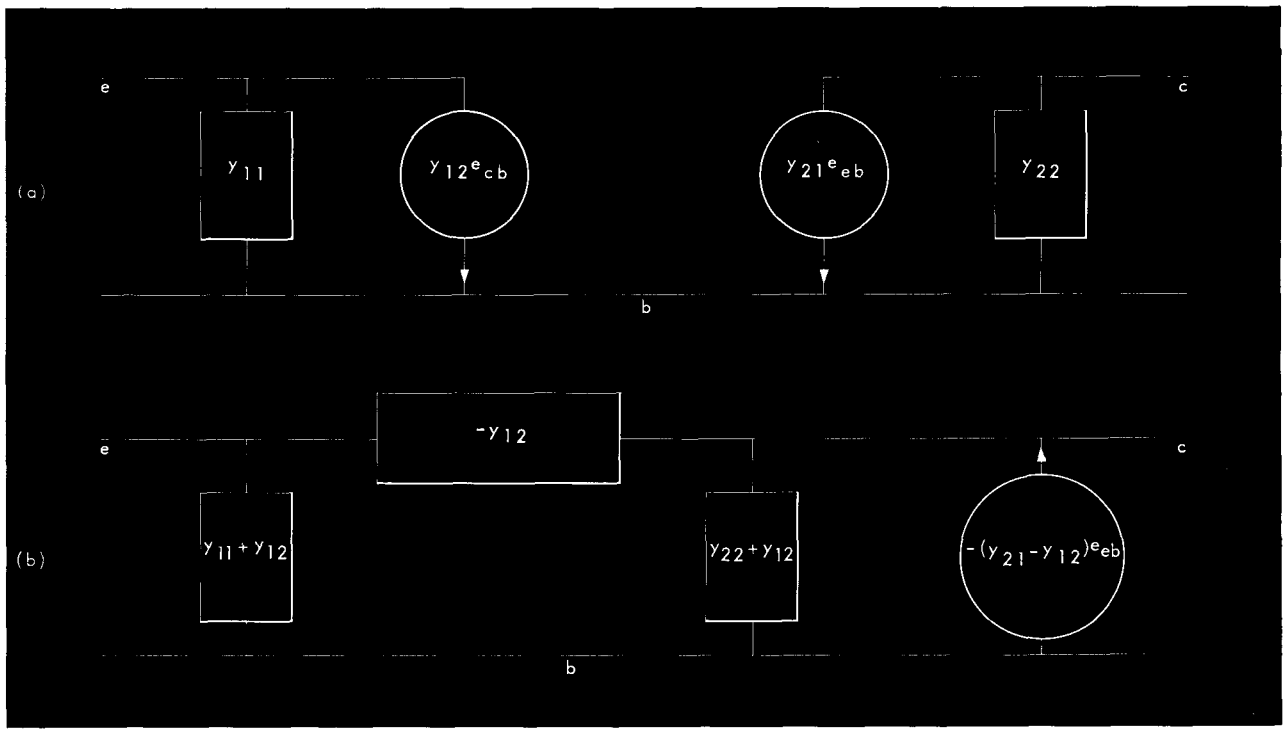
The appropriate experimental values of g_{22b} and b_{22b} corresponding to the five temperatures noted above were read from the appropriate curves and spotted on the theoretical curves in Figs. 8 and 9. It will be noted that, insofar as g_{22b} is concerned, any stray output conductance is negligibly small. In the case of b_{22b}, however, the discrepancy between the theoretical and experimental values clearly shows that a stray output capacitive susceptance exists. When the difference between theory and experiment was averaged after each was adjusted for frequency, a stray capacitance across the transistor output was found to be 11.3 $\mu\mu$f.

In summary to this point, then, four nearly identical *pnp* alloy junction transistors were subjected to an extensive series of tests during which frequency and temperature were varied. The data thus obtained were plotted and the values read from these experimental curves were used to evaluate several of the factors that appear in theoretical relationships for a simplified single-dimension theory of the transistor. The variations of these factors with temperature were adjusted until there was good agreement between curves based on these theoretical relationships and the experimental data. In fitting theory to practice, transistor operating temperatures are determined, thus giving some insight into transistor operation at low temperatures.

It may now be of interest to represent the several transistor parameters as electrical networks containing resistance, inductance, and capacitance. The equivalent circuit thus far considered is shown in Fig. 10a. Such a circuit may be transformed into a variety of equivalent circuits, such for example, as that shown in Fig. 10b. We shall investigate the components of this latter circuit.

As an example of the method used, consider Fig. 11a, on which the parameter y_{12} at a thermocouple temperature of 215°K is plotted in the complex plane. The circled data points show the parameter at the four frequencies used for the experimental study. It is noted that if a susceptance proportional to frequency is subtracted from each datum, the resulting points, shown by uncircled dots, seem to define a semicircle. After several susceptances and several semicircular plots were tried for each susceptance assumed, the plot shown on Figure

Figure 10 (a and b) **Transistor equivalent circuits.**



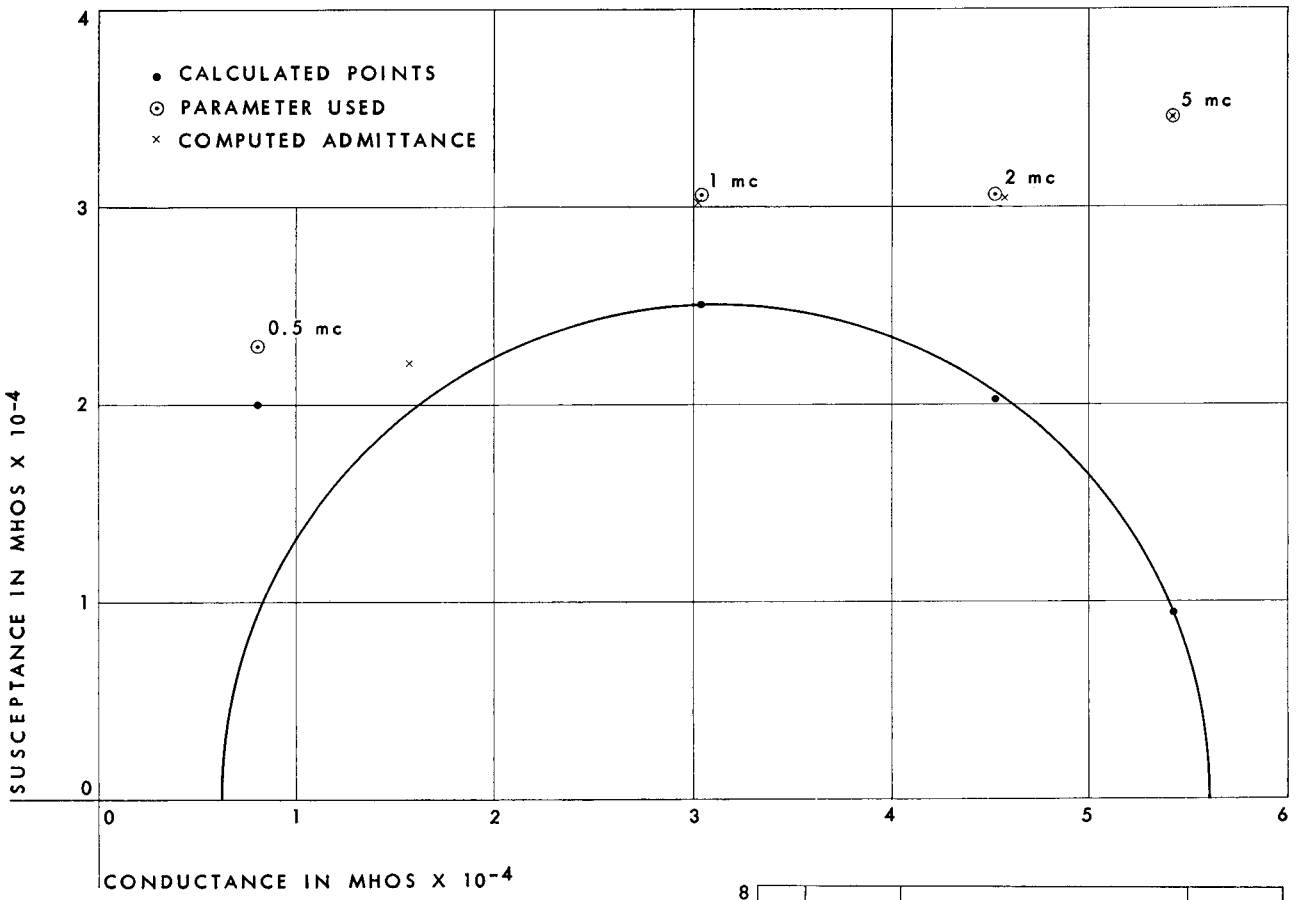


Figure 11a **Characteristics of y_{12} at 215°K.**

11a was taken as the best compromise. The network representing $-y_{12}$ therefore consists of three branches. One branch is the susceptance originally subtracted from the data points. The second branch is a series combination of conductance and capacitive susceptance defined by the radius of the semicircle. The third branch is a conductance defined by the intercept of the semicircle nearest the origin. The network is shown on Figure 11b. As a check on the selection of the semicircular plot, the admittance of this network may now be calculated at the four frequencies involved. The results of these calculations are shown by the points marked X on Figure 11a.

Figure 12a shows a plot for the second type of circuit that was analyzed. In this instance the complex plot lies in the fourth quadrant, thus indicating that the network has an inductive component. Once again it is necessary to subtract the susceptance to have the points best approximate a semicircle. The network corresponding to Fig. 12a therefore also has three branches, one a capacitive susceptance, one a series combination of conductance and inductive susceptance, and one a negative conductance. The network is shown in Fig. 12b.

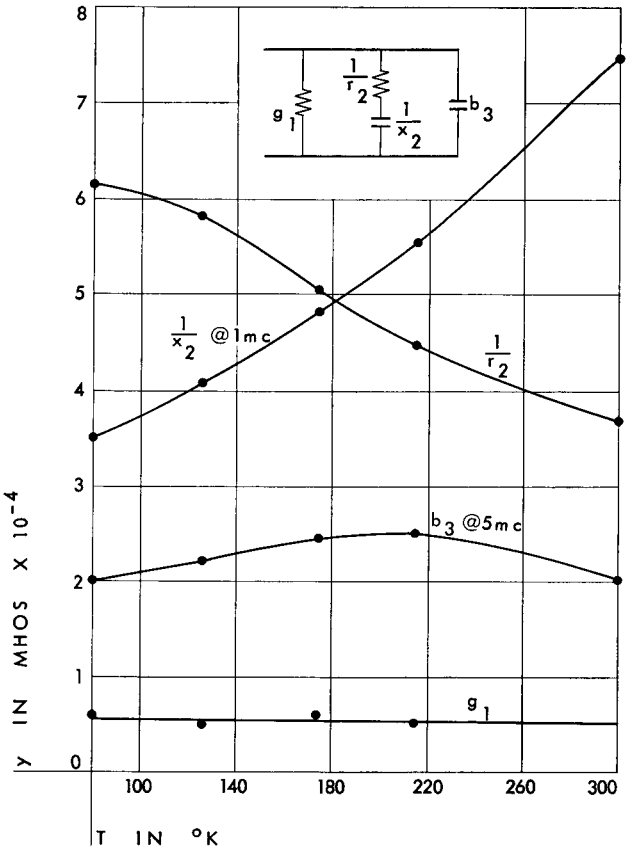


Figure 11b **Characteristics of $-y_{12}$ vs temperature.**

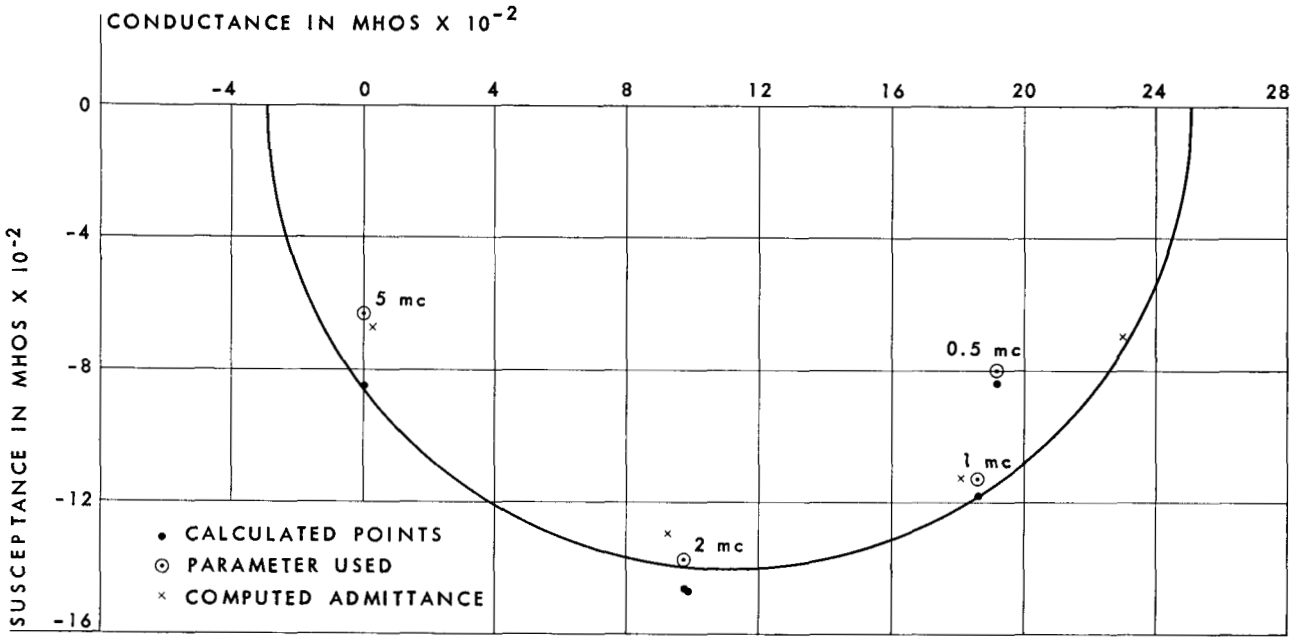
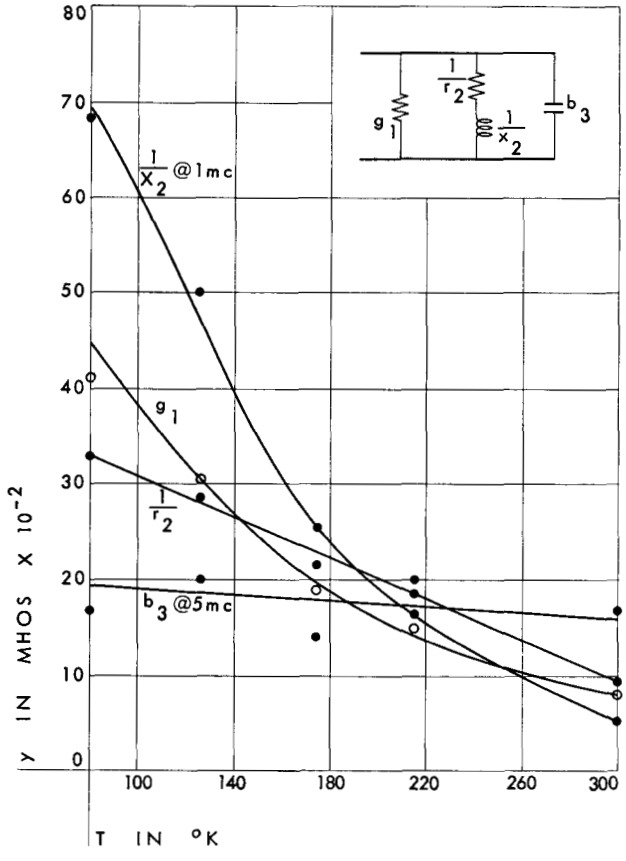


Figure 12a **Characteristics of $(-y_{21}+y_{12})$ at 125°K.**

Figure 12b **Characteristics of $(-y_{21}+y_{12})$ vs temperature.**



Analyses such as those described above were carried out for each of the parameters of Fig. 10b at each of the temperatures used in this study. The results of these additional analyses are presented in Figs. 13 and 14. It is interesting to note that similar networks now have been reported,[5] although the method of obtaining them is quite different from the one described here.

Pulse response and heavy-current tests

In computational applications of transistors the response to pulse input signals is of great interest. Where the transistor is assumed to be represented adequately by simple equivalent circuits composed of linear elements, there is a direct relationship between the steady-state response and the pulse response of the network. Assume, for example, that one of the transistors under test were to be operated at the dc conditions under which these tests have been conducted, and assume that equivalent circuits that have been obtained for this operating point are independent of small voltage and current excursions about this operating point. If these assumptions are valid, then the differential equations for the circuit can be used to predict the response of the circuit to small input pulses superimposed on the dc operating conditions. There will be a direct relationship between the pulse response of the circuit and the bandwidth.

As the analyses of the previous section were carried out it was noted that, as temperature decreased, the points defining the semicircles tended to move toward the low-frequency region of the semicircles. This means that, at a given frequency, as the temperature is lowered the transistor is in a relatively lower portion of its frequency band.

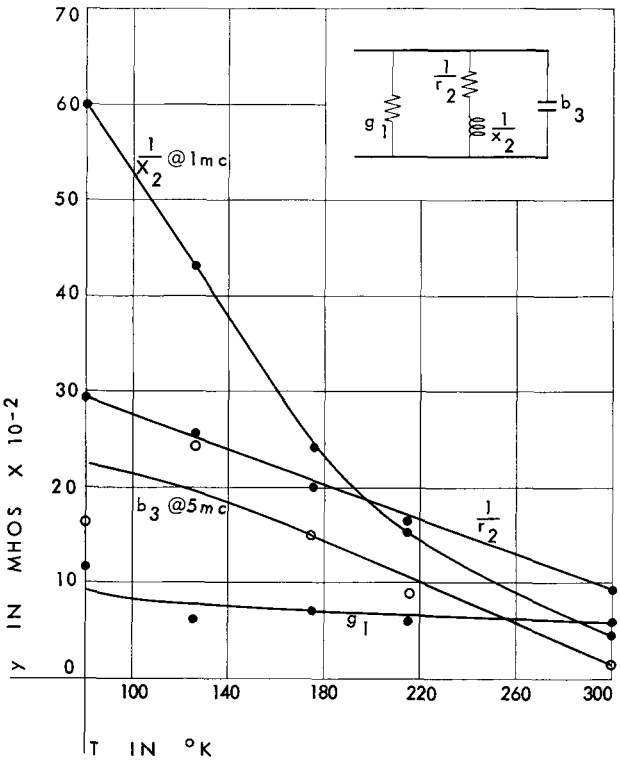


Figure 13 **Characteristics of $(y_{11}+y_{12})$ vs temperature.**

From the curves of Figs. 2 through 9 the values of complex α for several temperatures at a given frequency may be calculated. When this is done it will be found that with a decrease in temperature the magnitude of α increases and that the phase angle decreases. Once again this seems to indicate that the transistor is operating in a lower portion of its frequency band as temperature is decreased.

From both of these observations one would conclude that, if the transistor were connected as a grounded-base amplifier and were subjected to an input step function of emitter current superimposed on the steady-state emitter current of 4 ma, the rise time of the load voltage would improve as temperature is decreased. This statement assumes that the changes in emitter current and collector voltage are small on application of the input step function of current.

For pulse inputs, the excursions of voltage and current cannot generally be considered to be small. With this in mind it was decided to operate one of the test transistors as a grounded-emitter pulse amplifier, driven by the base input from beyond cutoff to the edge of saturation. As a preliminary step a dc test was run with the transistor operating at the edge of saturation, that is, with the collector-base voltage at zero. The circuit diagram and the test results are shown in Fig. 15. If it can be assumed that the transistor temperatures are roughly the same in these tests as in the tests reported in Figs. 2 through 9, then the information from these two sources may be combined and a qualitative picture of the collector characteristics may be sketched.

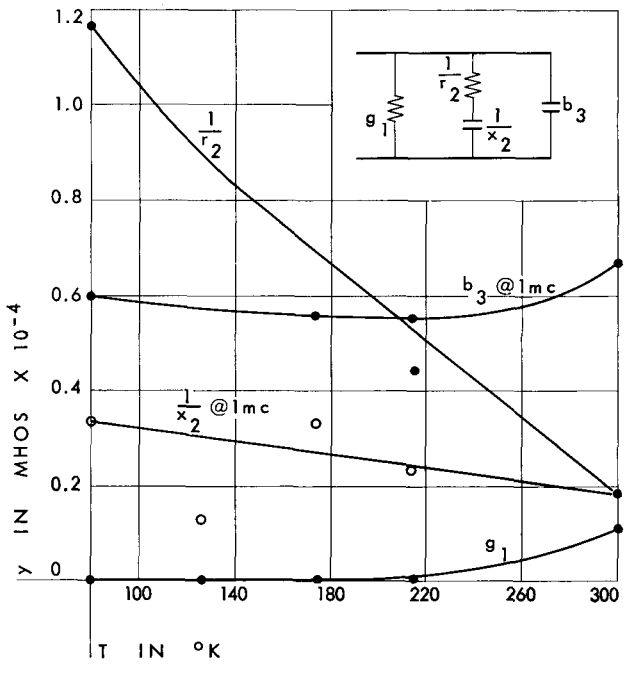
The circuit used for obtaining pulse test data is shown in Fig. 16. The oscillographic results of the tests are presented in Figs. 17a, 17b, and 17c. Figure 17a shows that for a given output-current amplitude, rise time improves as temperature decreases. It should be noted that when the input pulse is applied, the operating point moves from beyond cutoff through the unsaturated region toward the edge of saturation. It has been shown above that in the unsaturated region the bandwidth of the transistor increases as temperature is decreased. Thus when the operating point is in this region the response of the transistor becomes more rapid as temperature decreases. We might expect, then, the oscillographic results shown in Fig. 17a.

With the transistor in an environment of liquid nitrogen, there is the possibility of passing large currents without danger of producing excessive temperatures within the transistor. The oscillographic results show that output-current rise time is further improved as the magnitude of the output current pulse increases. For the larger output-current magnitudes, Fig. 15 indicates that these improved rise times are obtained with smaller input currents than would be required at room temperature.

Conclusion

As a result of these tests and studies we can say that there is quite good agreement between simple basic

Figure 14 **Characteristics of $(y_{22}+y_{12})$ vs temperature.**



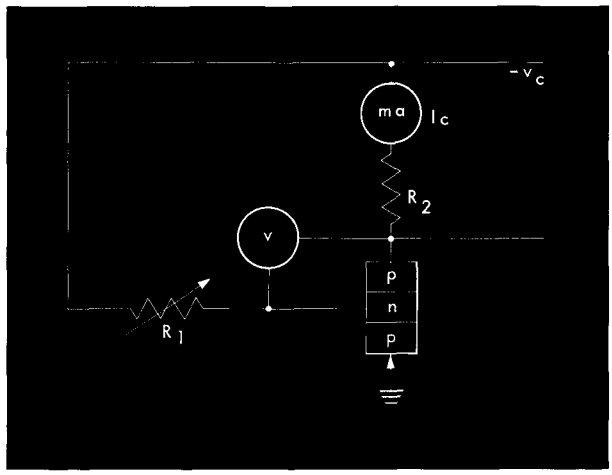


Figure 15 **Transistor low-temperature dc test data.**

a) Liquid nitrogen temperature

I_c, ma	R_1, ohms	R_2, ohms	R_1/R_2
8	20000	1000	20
25	3300	100	33
50	4200	100	42
100	5200	100	52
150	5400	100	54
200	540	10	54
250	520	10	52
500	300	10	30
1000	200	10	20

b) Room temperature

I_c, ma	R_1, ohms	R_2, ohms	R_1/R_2
8	60000	1000	60
25	6400	100	64
50	6100	100	61
100	5000	100	50
150	4200	100	42
200	360	10	36

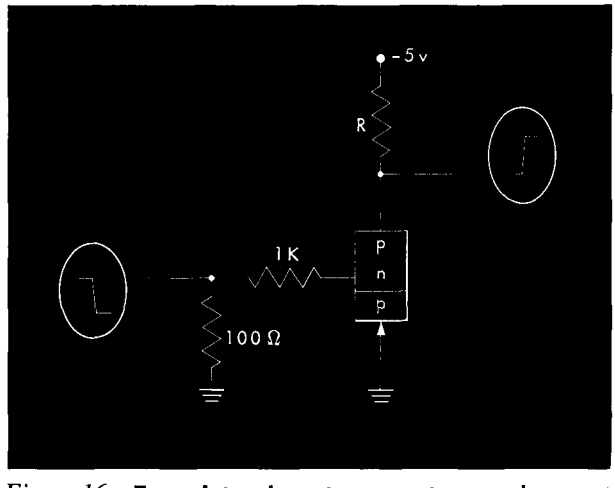


Figure 16 **Transistor low-temperature pulse test data.**

I_c, ma:	8	50	100	250	500	1000
R, ohms:	620	100	50	20	10	5

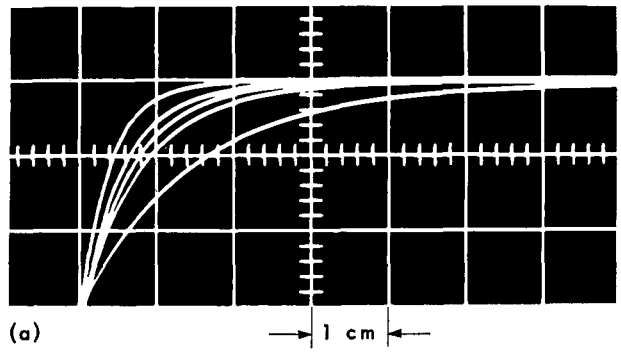


Figure 17a **Transistor inverter turn-on output pulses for peak collector current of 8 ma and thermocouple temperatures of 80°, 125°, 175°, 215°, 298°K. Lower temperatures yield more rapid rise time. Time scale 2μsec/cm. (Oscilloscope traces).**

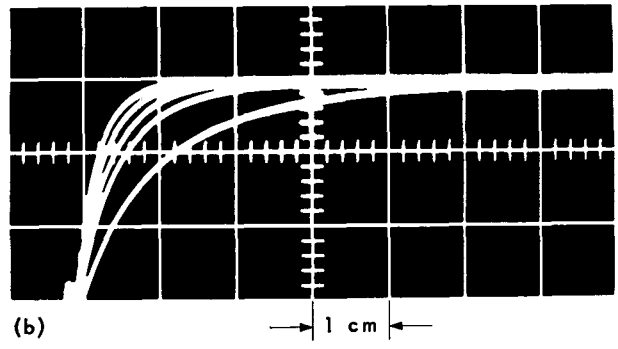


Figure 17b **Transistor inverter turn-on output pulses at liquid nitrogen temperature for peak collector currents of 500, 250, 100, 50 and 8 ma. Larger currents yield more rapid rise time. Time scale 1μsec/cm.**

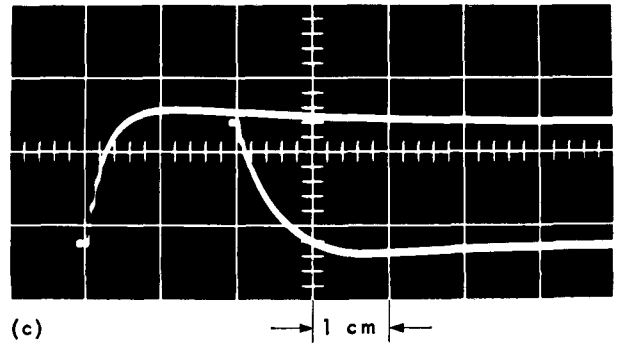


Figure 17c **Transistor inverter turn-on and turn-off output pulses at liquid nitrogen temperature for peak collector current of 1 amp. Time scale 1μsec/cm.**

transistor theory and actual experimental results. In obtaining this agreement it was necessary to include the effects of surface recombination and to study the effect of temperature on carrier mobility. Surface-recombination studies reported in the literature were used as the basis for values of $y_{SR}+y_n$. It was also assumed that $\mu_p \propto T^{-1.8}$ in order to approximate to a reasonable degree the actual variation of μ_p with temperature. The effect of temperature on carrier lifetime was found to have little effect on transistor parameters at the upper end of the temperature range used. Lifetime variations do have an appreciable effect at the low end of this range, but the experimental data do not allow an accurate determination of the variation of lifetime in this temperature range.

At the quiescent operating point chosen for these tests the bandwidth of the transistor apparently is improved as temperature decreases. Pulse data show that, for a given output-current magnitude, rise time decreases as temperature decreases. With the transistor in liquid nitrogen, rise time decreases as output pulse current magnitude increases, so that large output currents can be delivered by the transistor at grounded-emitter gains that are quite acceptable in practice.

A study of this kind is, of course, the work of many people. The work has been done under the auspices of the Transistor Circuits Group of the Poughkeepsie Product Development Laboratory. To R. A. Henle and J. L. Walsh of this group are due thanks for their interest and encouragement during the progress of the study. Thanks are also due to Dr. H. P. Wolff for the use of his jigs and measuring equipment; to R. J. Domenico for many interesting and profitable discussions; to S. V. Clements and M. S. Schmookler for help with calculations and measurements; to R. Bianchi for his patient data taking; and to L. A. Harlow for his painstaking work and his ingenuity in building laboratory equipment.

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List of symbols

A_s = Surface-recombination area in cm²
α = Grounded-base current gain
$b_{cb'}$ = Collector-base barrier-susceptance in mhos
D_n = Diffusion constant for electrons in cm²/sec
D_p = Diffusion constant for holes in cm²/sec
ε = Permittivity of germanium = 1.780×10^{-9} farad/meter
I_e = Emitter current in amp
I_p = Hole current in amp
k = Boltzmann's constant = 1.380×10^{-23} joules/°K
L_n = Diffusion length for electrons in cm
L_p = Diffusion length of holes in the base in cm
Λ = q/kT in volts^{-1}
μ_n = Mobility of electrons = 3400 cm²/volt-sec at 300°K
μ_p = Mobility of holes = 1700 cm²/volt-sec at 300°K
n_n = Density of electrons
n_p = Thermal equilibrium concentration of electrons in the p region
p_n = Thermal equilibrium concentration of holes in the n region
P_o = Density of minority carriers on base side of emitter-base boundary
p_p = Density of holes
q = Charge of a carrier = 1.602×10^{-19} coulomb
s = Surface-recombination velocity in cm/sec
σ_e = Conductivity of emitter material in (ohm-cm)$^{-1}$
σ_n = Conductivity of base material in (ohm-cm)$^{-1}$
T = Absolute temperature in °K
τ_n = Lifetime of electrons in the emitter region in sec
τ_p = Lifetime of holes in the base region in sec
$V_{cb'}$ = Voltage of intrinsic collector with respect to base
$V_{eb'}$ = Voltage of intrinsic emitter with respect to base
W = Base width in cm
y_n = Admittance due to majority carrier flow in mhos
y_{SR} = Surface-recombination admittance in mhos
ω = Angular frequency

Received June 14, 1957.