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Magnetic-Recording-Head Selection Switch

Abstract: A switch for selecting one out of 100 magnetic recording heads for reading or writing is described. The recording heads are arranged in a 10 by 10 matrix and the switching is accomplished by semiconductor devices. The problem of obtaining suitably fast current rise time during writing is discussed, and the problem of crosstalk from unselected recording heads during reading is analyzed. Experimental results illustrate the performance of the switch.

Introduction

In large-scale magnetic-drum and disk storage systems using a large number of recording heads, a switch is required to allow information to be routed to or from a selected recording head. In order to reduce the number of read and write amplifiers required in the system, it is desirable to perform the switching at the recording heads so that only one read and write amplifier is required. Where rapid access to information and extreme reliability are required the switching must be done electronically.

With presently available transistors and diodes it is possible to build a compact, efficient and reliable switch. To demonstrate this a switch was constructed using 30 transistors and 200 diodes for selecting one out of 100 recording heads associated with a magnetic-disk memory.

Circuit description

A simplified circuit diagram of the switch is shown in Fig. 1. The recording heads are arranged in a 10 by 10 matrix and a head is selected by grounding the appropriate X and Y selection lines. A balanced configuration was chosen for the switch since it appeared to have several advantages over a single-ended configuration. A balanced configuration together with a differential-type read amplifier allows cancellation of extraneous-noise and common-mode switching transients. A balanced configuration considerably simplifies the design of the switch and associated write amplifier and also permits the use of unidirectional write currents.

The transistors in the switch are operated in either the saturated or cutoff region depending on whether the associated selection line is at ground potential or at $+20$ volts. This type of operation insures that only the transition time of the switch will depend upon the cutoff frequency and storage time of the transistors.

The voltages shown for the selection lines in Fig. 1 correspond to the selection of head H_{00}. Y-select transistor T_{21} is saturated, raising the potential of the row Y_0 bus to $+15$ volts. Since all other rows remain at -5 volts, only the diodes associated with the heads in row Y_0 will be forward-biased. All other diodes will be back-biased by 20 volts. X-select transistors T_1 and T_2 are also saturated and complete the low-impedance path from head H_{00} to the read lines. All other paths are blocked either by the back-biased diodes or the cut-off X-select transistors. It is clear, then, that a read signal induced in head H_{00} will appear on the read lines while the read signals from all other heads will be blocked.

Transistors T_{31} and T_{32} represent the output stage of the write amplifier. They are not part of the switch but are shown here for completeness. For reading, both T_{31} and T_{32} are cut off, while for writing they are driven between cutoff and saturation in a push-pull fashion. Resistors R_4 are chosen to limit the write current to the desired value, while the diodes associated with T_{31} and T_{32} limit the peak collector voltage on T_{31}, T_{32} and all unselected X-select transistors to $+15$ volts. Since the path of the write current includes transistors T_{21}, T_1, and T_2, these transistors must be supplied with sufficient base current to insure that they will remain in saturation even when passing the relatively large write current.

Construction

The 100-position selection switch is shown in Fig. 2. It

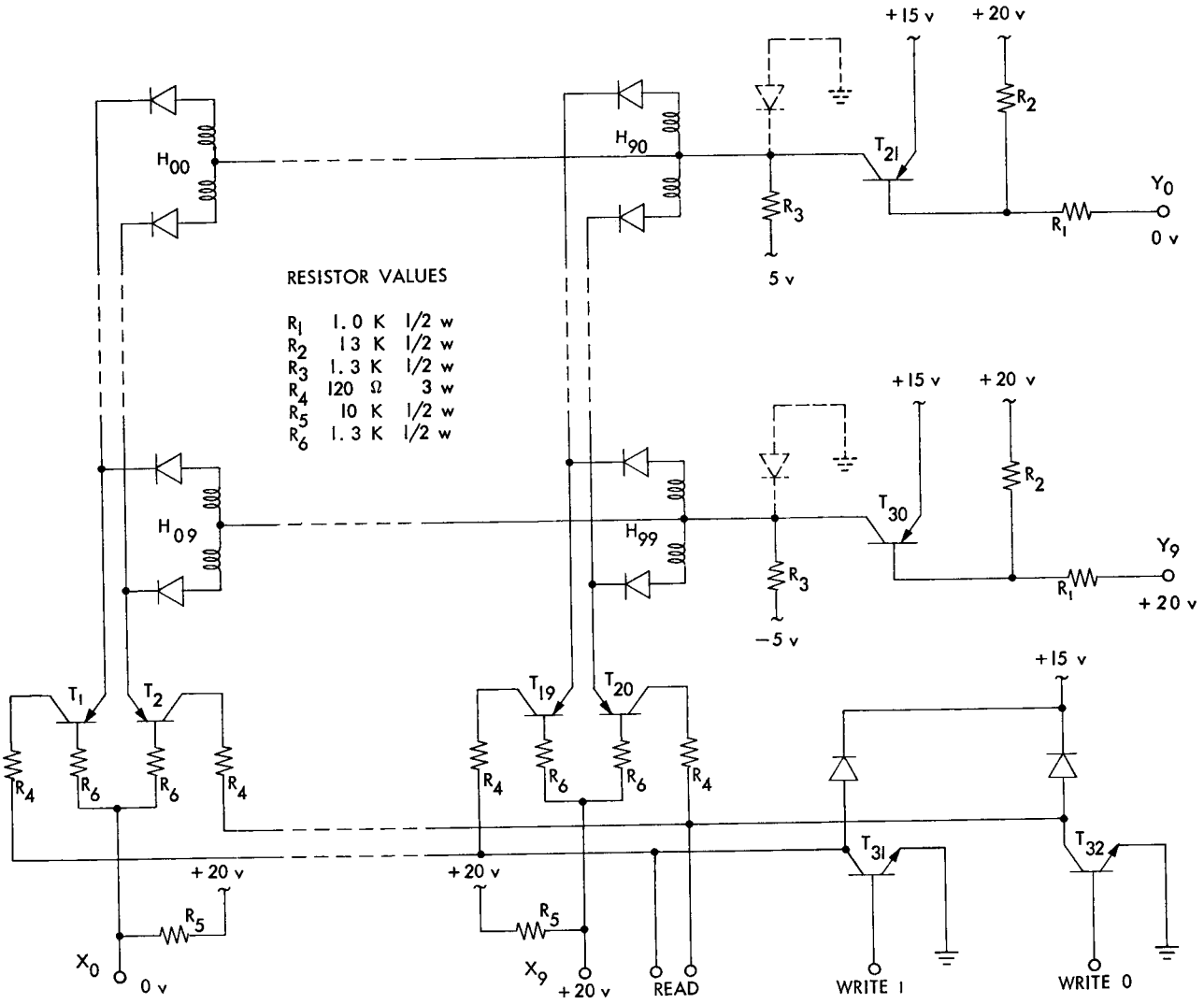
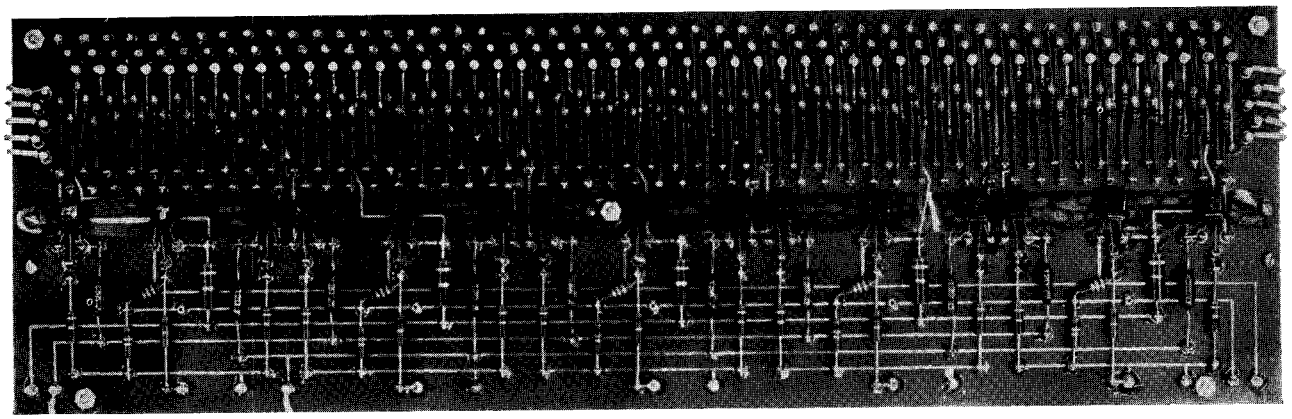


Figure 1 **Simplified schematic diagram of recording-head selection switch.**

Figure 2 **One half of 100-position recording-head selection switch.**



is made up of two identical printed-circuit boards mounted back-to-back with the necessary interconnections. The complete package occupies a volume of 1 in. by 5 in. by 16 in. The boards were laid out with the head terminals 0.3 in. apart; this spacing corresponds with the head spacing in the accompanying storage system so that cabling from the heads to the switch may be short and direct to minimize noise pickup and capacitive loading. Since the read signal is in the 10-millivolt range, it was felt that good reliability could only be obtained by using soldered connections throughout the switch.

Component specifications

Only one type of transistor is used in the switch and its pertinent specifications are listed in Table 1. IBM Type 01 transistors were selected to meet these specifications. In general the Type 01 transistor easily met all the specifications except those for punch-through and collector breakdown. Both the punch-through and collector breakdown voltage ratings could be reduced by five volts if the collectors of the Y-select transistors were clamped at ground potential as shown by the dotted lines in Fig. 1. Since selection to meet the existing specifications was easily accomplished, however, this expedient was not used. The diodes used were Transitron Type T7G germanium point-contact units. Their specifications are briefly summarized in Table 2. While the T7G diode exhibits good reverse recovery, it is not a requirement in this application. The characteristics of the recording head used in conjunction with the switch are listed in Table 3. Since the center-tapped coil of the head is always treated in a push-pull fashion, the mutual inductance between the two halves of the coil need not be treated as a separate parameter, but may be conveniently lumped in with the self inductance. An equivalent circuit which adequately represents the head at the frequencies of interest is shown in Fig. 3. Non-return-to-zero (NRZ) recording at 500,000 bits per second was specified.

Table 1 **P-n-p transistor specifications**

Punch through	$V_{cE} \geqq 25$v
Collector breakdown	$V_{cB} \geqq 30$v
Emitter breakdown	$V_{eE} \geqq 10$v
Current gain at $I_c = 100$ ma	$\beta \geqq 15$
Saturation current at 50°C	$I_{co} \leqq 17.5\mu$a

Table 2 **Diode specifications**

Forward current at +1v	$I_f \geqq 200$ma
Inverse current at −50v	$I_r \leqq 100\mu$a
Maximum inverse voltage	$E_r = 75$v
Maximum dc forward current	$I_{f_{dc}} = 100$ma

Table 3 **Recording-head characteristics**

Write current	$I_w = 100$ma
Read signal	$E_S = 10$mv, peak-to-peak
Resonant frequency	$f_r = 1$mc

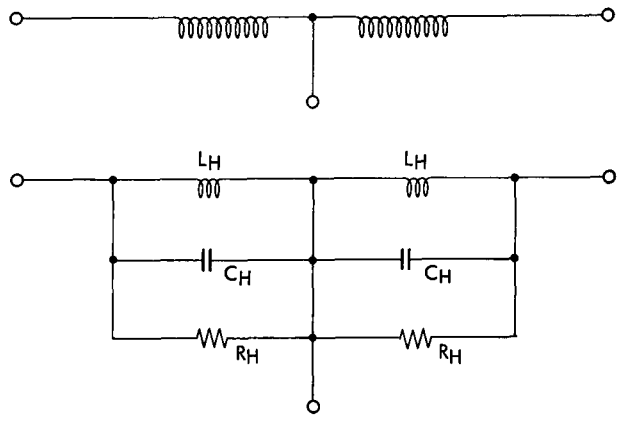


Figure 3 **Recording-head equivalent circuit.**
$L_H = 256\mu h$
$C_H = 100\mu\mu f$
$R_H = 2730\Omega$

DC design

The dc design of the switch was executed in a manner that would insure a minimum write current of 100 ma, saturation of the ON transistors, and a reverse emitter bias of at least 0.2 volt on the OFF transistors. "Worst-case" combinations of 5% power-supply variations, 15% resistor variations, 0.1 ma end-of-life I_{co} and 100,000-ohm end-of-life diode back resistance were also design criteria.

Switch peformance

- *Current rise time*

In order to record information at a 500-kc rate with the NRZ recording system, it is necessary that the write current be switched from one side of the head to the other in less than two microseconds. Initial testing of the switch indicated that the current rise time was 2.25 μsec while the current fall time was 1.80 μsec. Since these times were marginal at best it seemed desirable to find some way to speed up the current switching. An obvious approach was to increase the positive supply voltages while holding the write current constant. Since the rate of change of current in the head inductance is proportional to the voltage across the inductance, this voltage increase would result in a direct increase in speed. Since it was already necessary to select transistors to meet the existing voltage requirements, however, this was not deemed a satisfactory solution. An alternate solution to the problem is to maintain the peak voltage across the head for a longer time so that the current rise time approaches a sawtooth rather than an exponential wave shape. This longer maintenance of peak voltage will result in a speedup of current rise time of better than two to one, without changing the supply voltage, and can be accomplished by shunting the current-limiting resistors, R_4, with suitable capacitors. Experiments demonstrated that 0.005-μf capacitors resulted in the optimum current rise time without producing secondary overshoot. It will be

Table 4 **Definition of equivalent circuit parameters**

Element	*Definition*	*Value*	*Element*	*Definition*	*Value*
C_D	Diode shunt capacitance at −20v	0.1 $\mu\mu$f	R_6	Base-current-limiting resistor	See Fig. 1
R_D	Dynamic diode back resistance at −20v	11 meg	R_4	Write-current-limiting resistor	See Fig. 1
R_E	Dynamic emitter junction resistance at −5v	50 meg	C_W	Write-current-speedup capacitor	0.005 μf
R_C	Dynamic collector junction resistance at −5v	10 meg	C_S	Stray shunt capacitance	185 $\mu\mu$f
C_E	Emitter junction capacitance at −5v	8.5 $\mu\mu$f	C_H, R_H, L_H	Recording-head parameters	See Fig. 3
C_C	Collector junction capacitance at −5v	20.2 $\mu\mu$f			

recognized that a large primary overshoot can be tolerated in write current because of the saturation characteristic of normal recording surfaces. Fig 4 shows the current wave forms for no shunting capacitors and 0.005-μf shunting capacitors.

To check the effect of the shunting capacitor under actual recording conditions, the read-back signal was checked as a function of the recording-bit rate with no shunting capacitor and with a 0.005-μf shunting capacitor. The results of this test are shown in Fig. 5. With the shunting capacitors the switch easily meets the 500-kc bit-rate requirements.

• *Crosstalk*

In any recording-head selection switch one must initially consider crosstalk during reading between the unselected positions and the selected position as a possible source of trouble. In the switch described here, crosstalk occurs along two main paths. The first path is through the back impedance of the diodes associated with the nine unselected heads in the selected column (X). The second path is from the nine unselected heads in the selected row (Y), through the OFF impedance of the nine unselected X-select transistors (considering only one side of the double-ended switch). Noise contributed by the other 81 unselected heads is insignificant. In the worst case it was considered that the read signals at all unselected positions were in phase so that the crosstalk was additive. The circuit used in calculating the crosstalk is shown in Fig. 6, which represents one side of the balanced switch. A definition of the elements in Fig. 6 along with their average values is given in Table 4.

The noise voltages, e_{ND} and e_{NT}, were solved as a function of frequency in a straightforward manner using superposition in order to obtain a separate solution for each noise path as well as a complete solution. Both R_E and R_C were large enough that their effect could be ignored in the frequency range of interest. Similarly, the impedance of the R_4 and C_W combination is small enough to be ignored.

The solutions for the two noise components are:

For diode path:

$$\frac{e_{ND}}{e_N} = \frac{9[G_D G_G - \omega^2 C_D C_T + j\omega(G_D C_T + G_G C_D)]}{A}.$$

For transistor path:

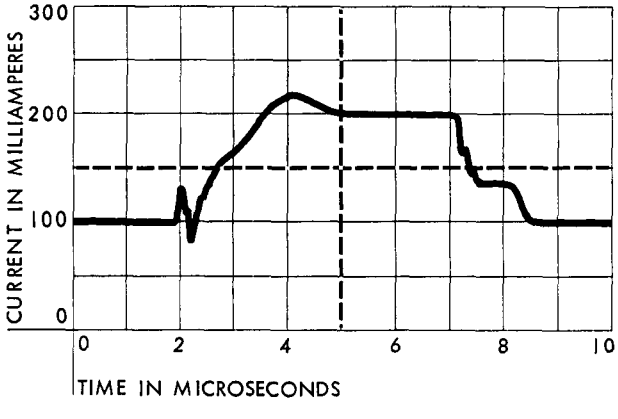
$$\frac{e_{NT}}{e_N} = \frac{-9\omega^2 C_C C_E}{A}$$

where

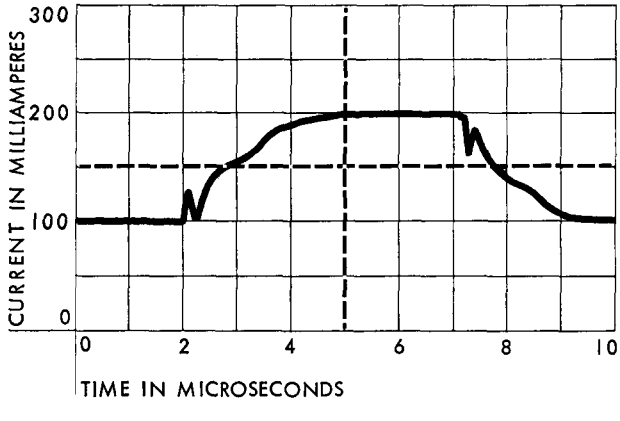
$$A = \left[G_G(G_G + G_H) + \frac{C_T}{L_H} - \omega^2(C_T C_H + C_T C_S) + j\omega \left(9G_G C_C + G_G C_H + G_G C_S + G_H C_T + G_G C_T - \frac{G_G}{\omega^2 L_H} \right) \right]$$

and $C_T = C_C + C_E$.

Figure 4 **Write-current wave forms.**
a) 0.005-μf shunting capacitor.



b) No shunting capacitor.



The results of this solution are plotted in Fig. 7 along with the crosstalk, measured experimentally by driving the 99 unselected positions with a test oscillator and measuring the induced noise across a recording head at the selected position. The agreement between calculated and experimental results appears adequate. As shown in Fig. 7, the majority of the noise at high frequencies comes through the collector and emitter junction capacitances of the X-select transistors, the second path mentioned above.

The actual read signal closely approximates the function,

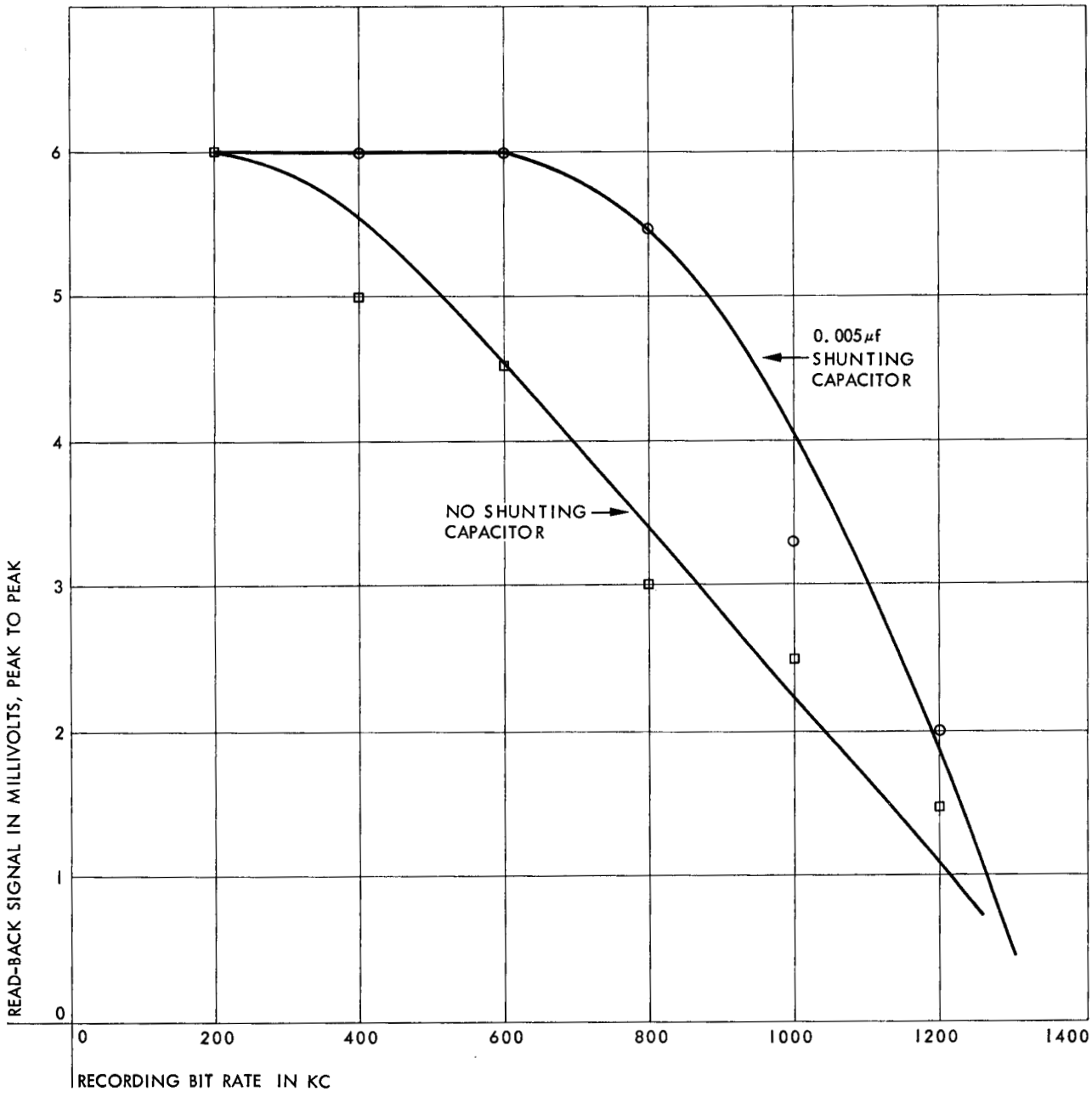
$$f(t) = A + A \cos(\omega t) \quad \text{for } -\pi/\omega < t < +\pi/\omega$$

$$f(t) = 0 \quad \text{for } +\pi/\omega < t < -\pi/\omega$$

where $\omega = 2\pi\,(250{,}000)$.

Since the main frequency components of this wave form occur below 500 kc, the noise rejection illustrated in Curve ($\times$) of Fig. 7 was considered adequate for the job at hand. An attempt was made, however, to improve the noise rejection at high frequencies by cross-neutralizing the emitter junction capacitance as shown in Fig. 8. This resulted in the improvement shown in Curve (∇) of Fig. 7.

Figure 5 **Read-back amplitude vs. recording bit rate.**



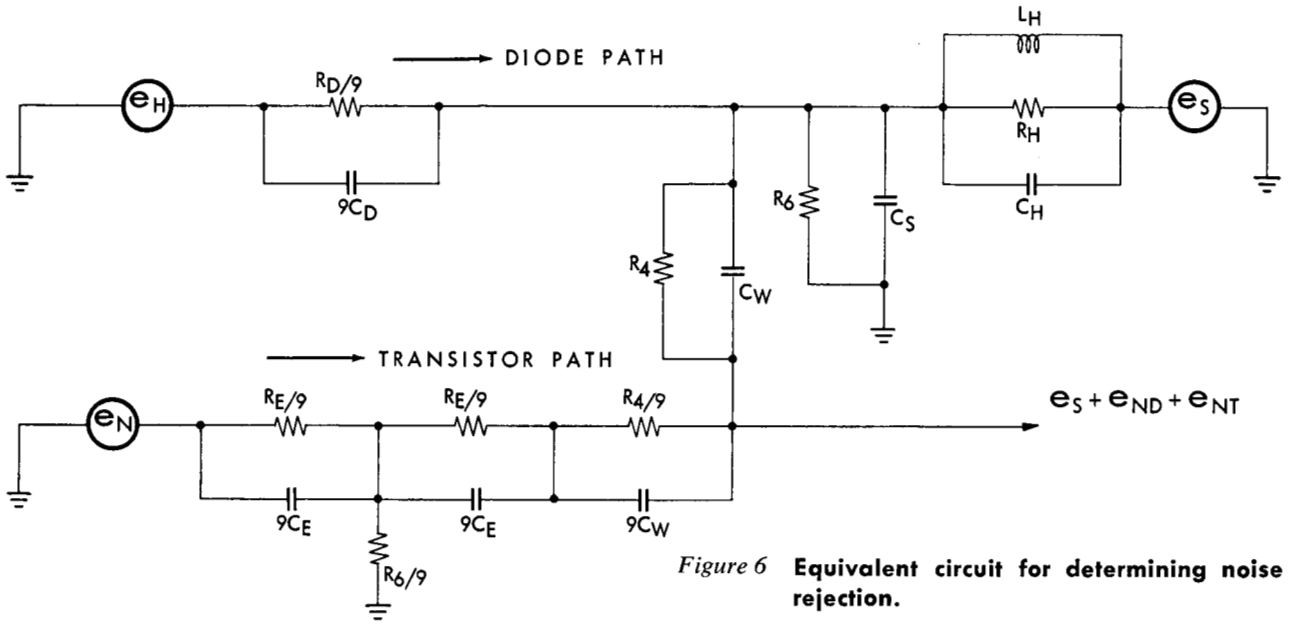
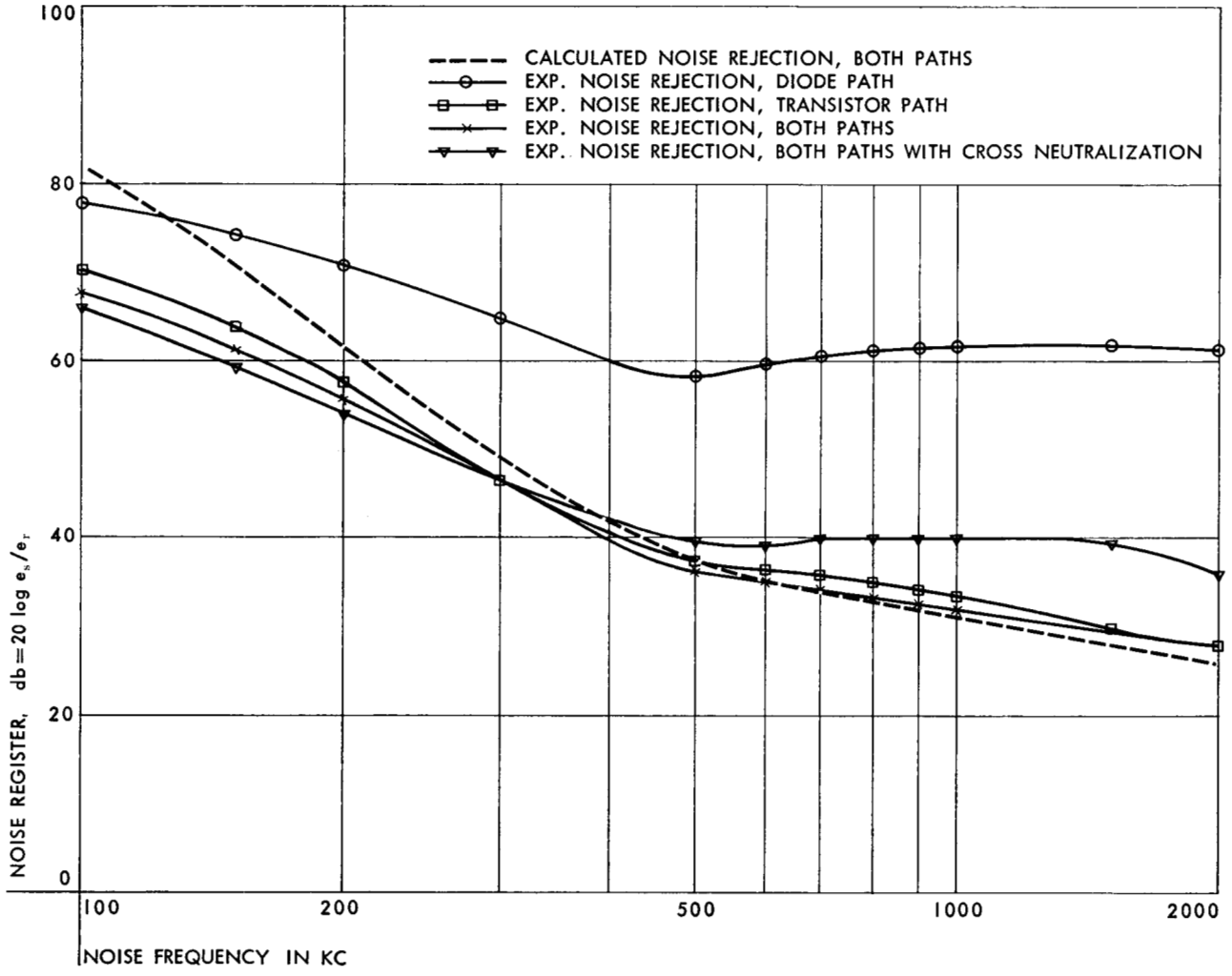


Figure 6 **Equivalent circuit for determining noise rejection.**

Figure 7 **Plot of noise rejection for recording-head switch.**



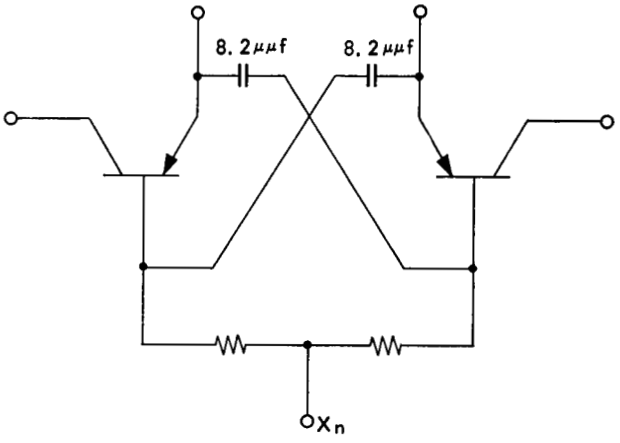


Figure 8 **Cross-neutralization of transistor emitter junction.**

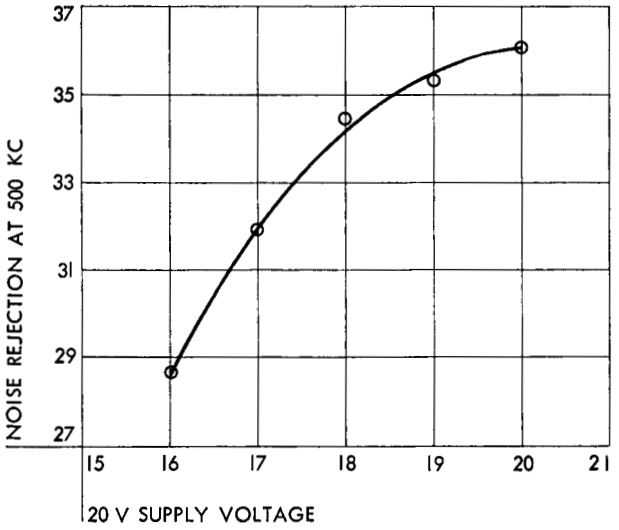


Figure 9 **Transistor noise rejection vs. supply voltage.**

Cross-neutralization might be of use in a case where the crosstalk reached an objectionable level.

Since the junction capacitance of transistors is a function of the junction voltage, it was expected that the crosstalk at high frequencies would be a function of the back bias on the X-select transistors. This supposition was verified experimentally by measuring the crosstalk at 500 kc while reducing the 20-volt supply voltage. The results of this test are shown in Fig. 9. Even when the transistor back bias is reduced to one volt, the noise rejection at the highest frequency of interest is more than 28 db.

Switching time

The transition time of the switch during reading is limited by the fact that the transistors are heavily saturated and are driven from what is essentially a current source so that the storage time is appreciable. With the particular transistors used in the switch, the transition time was approximately 8 μsec. To determine the overall switching time, the recovery time of the associated read amplifier must be added to the switch transition time. For this reason it is desirable to keep the switching transients to a minimum. The switching transient exhibited by the switch consists of two parts—a short spike of about one-volt amplitude and one-microsecond duration and a dc pedestal of less than 160 millivolts. The spike is caused by the inductance of the heads, while the pedestal is due to the difference in voltage drop across pairs of diodes, X-select transistors, and current-limiting resistors (R_4).

In general, read amplifiers may be easily designed, using standard amplitude-limiting techniques, which will not overload on short-duration spikes of relatively large amplitude. The dc pedestal however, presents a more basic problem which is not easily solved in the read amplifier. Recovery from a pedestal is primarily a function of the amplitude of the pedestal and the low-frequency response of the amplifier. If the read amplifier is to satisfactorily amplify the normal read signal, its low-frequency response cannot be restricted beyond a certain point, so that in order to obtain very short recovery times it may be necessary to place a limit on the maximum value of the pedestal. In the switch described in this article it is possible, owing to the balanced nature of the switch, to reduce the pedestal to less than 50 millivolts by matching appropriate pairs of diodes, transistors, and resistors.

Conclusion

While the switch described here has not undergone rigorous life tests, it is believed that the functional tests which have been performed are indicative of highly satisfactory performance. One out of one hundred heads may be selected for reading or writing at a 500-kc bit rate using only 200 diodes and 30 transistors.

Acknowledgment

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