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# An Experimental 50-Megacycle Arithmetic Unit

**Abstract:** An experimental 50-megacycle arithmetic unit has been built which performs a repetitive multiplication program and checks the results for errors. The unit uses pulse circuitry which has been developed to perform digital operations at a 50-megacycle pulse-repetition rate. This paper describes the arithmetic system and the circuits which perform the required functions. These circuits include a full binary adder, a phase-locked frequency divider which provides a 3.125-megacycle secondary timing source, a reshaping and retiming circuit using germanium diodes and capacitive storage, a high-speed shift register, a high-speed indicator register, and a binary word generator.

Various novel features of a digital system operating at these high speeds are described. These include the use of coaxial delay lines for the distribution of signals and as storage elements, and the use of secondary emission tubes in amplifier and multivibrator circuits.

In a 50-megacycle system the interdependence of the space and time dimensions is marked, and although this introduces problems which are not ordinarily encountered in computing systems, it may be used advantageously to provide features such as the variable-phase clock system used in the arithmetic unit.

The performance and reliability of the arithmetic unit are discussed as well as the reliability of the components and circuits which make up the system. Although the techniques and circuitry discussed here have been applied only to a relatively simple arithmetic unit, it is felt that they could be useful in a variety of high-speed computing and measurements applications.

**Contents**

## 1. System operation

• *a) Introduction*

A research investigation into the possibility of performing digital operations at VHF pulse-repetition rates has resulted in the development of a 50-mc arithmetic unit which repetitively performs a multiplication program and checks the results for errors. The unit uses commercially available components, and the basic techniques and circuits which have been developed for use in this system are described in a recent publication.[1] The present paper will describe in detail the experimental arithmetic unit, shown in functional block diagram form in Fig. 1

The system is timed by a crystal-controlled 50-mc sine-wave clock source which supplies 50-mc power through 52Ω coaxial lines to other units of the system for purposes of reshaping and retiming. Numbers in the system are represented in binary-coded form and are handled serially. The word size is 16 bits, with successive bits occurring at 20-millimicrosecond intervals. The representation of binary numbers in the system is shown in Fig. 20. A 16-to-1 frequency-divider chain, fed from the 50-mc clock, provides a synchronizing pulse which marks the beginning of each word, i.e., one for each 16th clock pulse. This synchronizing pulse has a width of 10 millimicroseconds.

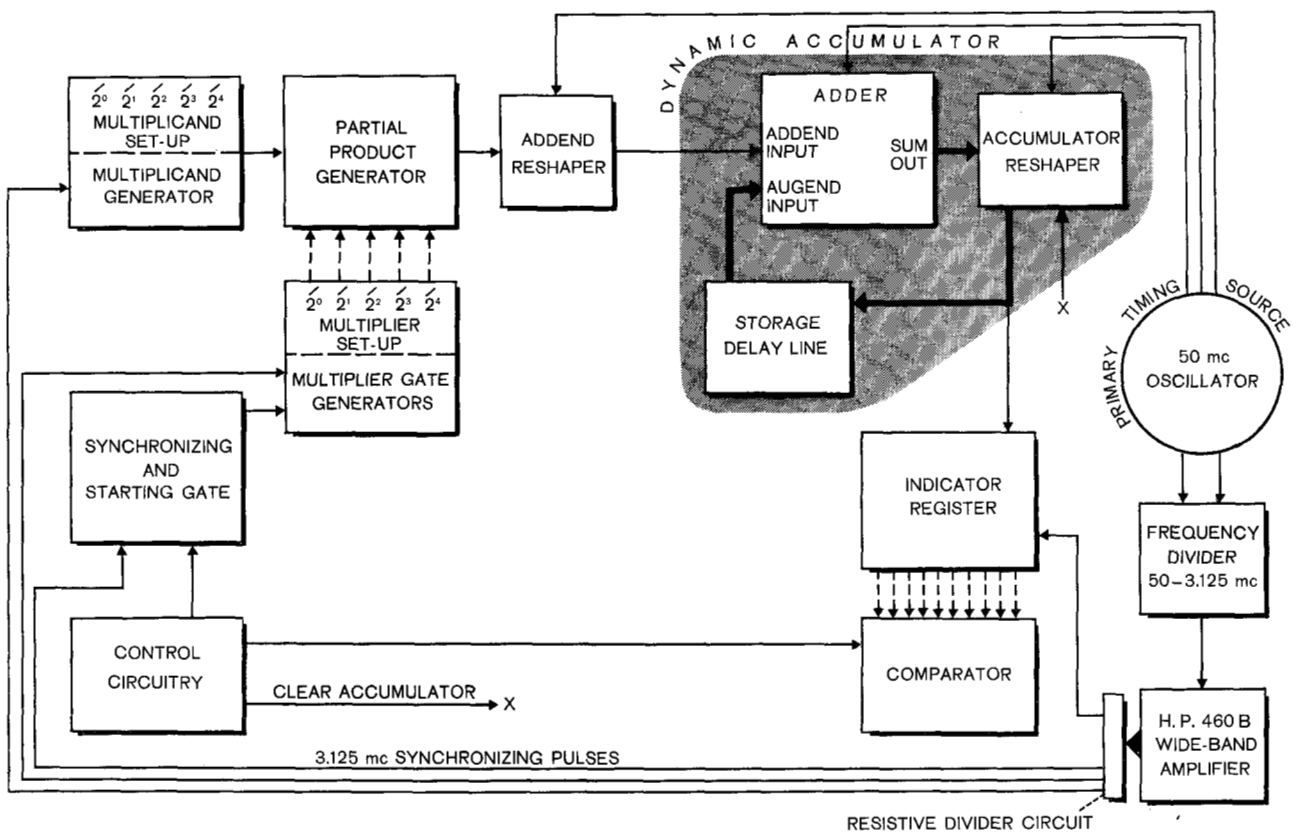
In the multiplicand generator, the synchronizing pulse is fed into a delay line which has output taps at 20-millimicrosecond intervals. The multiplicand set-up switches determine which taps will be connected into a buffer circuit; the output of this buffer provides a sequential train of pulses representing the binary multiplicand.

The partial-product generator provides means for gating and column-shifting the multiplicand under the control of the successive multiplier digits. Column-shifting is performed by a tapped line similar to the one used in generating the multiplicand. A set of gates permits selecting the output from any one of five taps; the enabling of these gates is controlled by the multiplication sequence and the value of the multiplier.

The output of the partial-product generator is reshaped by the 50-mc clock pulses in the addend reshaper before being entered into the addend input of the adder. The output of the adder is fed through a reshaper and a coaxial line of approximately 0.3 μsec time delay, back into the augend input of the adder. This normally closed loop through the adder, reshaper and delay line constitutes a dynamic accumulator register.

The system normally operates with a fixed repetitive program in which a 5 × 5 binary-digit multiplication is performed in five successive 0.32 μsec add cycles. The result of the multiplication is then allowed to circulate in

*Figure 1* **Block diagram of the experimental 50-megacycle arithmetic unit.**
*The system is broken down into functional blocks, and the distribution of the timing signals is shown.*



the accumulator register for 300 add cycles after which the accumulator is automatically cleared for the repetition of the multiplication program.

During the storage period when the product is circulating in the accumulator, a serial-to-parallel converter is operative which displays the contents of the accumulator on a visual indicator panel. The result is also fed into a comparator, which compares it bit by bit with the precomputed correct result, and registers any errors. Separate error indication for each digit position makes it possible not only to determine the period of error-free operation, but also to obtain information about the nature and location of any errors which occur.

• *b) Timing*

The primary timing source in the arithmetic unit is the 50-mc sine-wave clock signal which is distributed to the various points in the system through 52Ω RG-58/U coaxial cable. Thirteen and a half feet of RG-58/U coaxial line has a time delay equal to the 20-millimicrosecond period of the clock, and it is therefore possible to introduce the correct clock-phase for re-timing a signal in any part of the system by cutting the clock-distribution line to a suitable length. The 50-mc oscillator and its associated distribution cables therefore constitute a variable-phase clock-signal source for the arithmetic unit. This may be compared to other computing systems in which a number of discrete phases of the clock are provided throughout the system. In such systems it is necessary to delay the signal in the computer to meet a particular phase of the clock when re-timing is required.

A secondary timing source is provided in the arithmetic unit by the synchronizing pulses which occur at a pulse repetition rate of 3.125 mc and are phase-locked to the 50-mc sine-wave clock. These pulses are produced in the frequency divider circuit, amplified in a Hewlett-Packard 460B distributed amplifier, and then fed into a resistive divider circuit from which six 93Ω RG-62/U coaxial cables may be driven. The pulses which are distributed around the arithmetic unit by these 93Ω coaxial cables have negative polarity, an amplitude of approximately 12 volts and a width of 10 millimicroseconds (Fig. 2). Here the plates of a Tektronix Type 531 oscilloscope are driven through the RG 62/U, 93-ohm coaxial cable directly from the resistive divider circuit. The sweep speed is 100 millimicroseconds per centimeter for the upper waveform and 20 millimicroseconds per centimeter for the lower waveform. The vertical deflection sensitivity is approximately 13 volts per centimeter.

The repeated program of multiplication which the system performs is started by a two-tube astable multivibrator, referred to as the control multivibrator, located in the control circuits (Fig. 3). The multivibrator provides a clearing pulse for the accumulator register through a resistive divider and tube $V_8$, and, in conjunction with the synchronizing pulses, drives the synchronizing and starting gate generator ($V_9$, $V_{10}$, $V_{11}$, $V_{12}$ and $V_{13}$) and the circuits (tubes $V_1$, $V_2$, $V_3$, $V_4$ and $V_5$) which provide

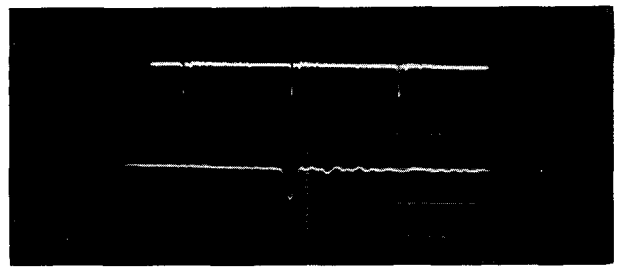


*Figure 2* **Oscilloscope photograph of the synchronizing pulses used as a secondary timing source in the arithmetic unit.**

the sampling pulses for the comparator circuit. This multivibrator is asymetrical, with tube $V_1$ "OFF" (nonconducting) for approximately 2 μsec and "ON" for approximately 100 μsec. The accumulator is cleared during the 2-μsec period and the synchronizing and starting gate is triggered to start the multiplication program at the end of this period. This control multivibrator runs at approximately 10 kc and therefore allows approximately 300 storage cycles in the computer after the multiplication is completed.

The circuits which produce the partial products for entry into the addend reshaper are timed by the synchronizing pulses. One synchronizing-pulse line, in conjunction with the 10-kc multivibrator, drives the synchronizing and starting gate circuit while another line is fed to the multiplier-gate generators to produce the "sync" and "clamp" pulses for the "Havens-delay" type[2,3] shift register. Coincidence of a sync pulse and the synchronizing and starting gate pulse starts the shift register. A fourth synchronizing-signal line fed to the multiplicand generator produces, for each synchronizing pulse, a sequence of pulses representing the multiplicand. The only timing requirement in this part of the system is that these four synchronizing-pulse lines should be cut to suitable lengths so that each of the five multiplier gates (in the partial-product generator) coincides in time with only one multiplicand.

The reshaper circuit, which will be described subsequently, requires that the signal to be reshaped should occur approximately four millimicroseconds before the clock input to the reshaper; accordingly, the clock line to the addend reshaper is cut to give this timing relationship between the clock signal and the input from the partial-product generator.

The timing requirements in the dynamic accumulator (which consists of the adder, accumulator reshaper and storage delay line) are that the storage delay line and the clock lines to the adder and the accumulator reshaper should be cut to obtain simultaneous entry of all three adder inputs (carry, augend and addend), and to insure a constant time difference between the signal and clock inputs to the reshaping network in the accumulator reshaper. This timing relationship is dependent on the relative phase between the clock waveforms at the inputs to

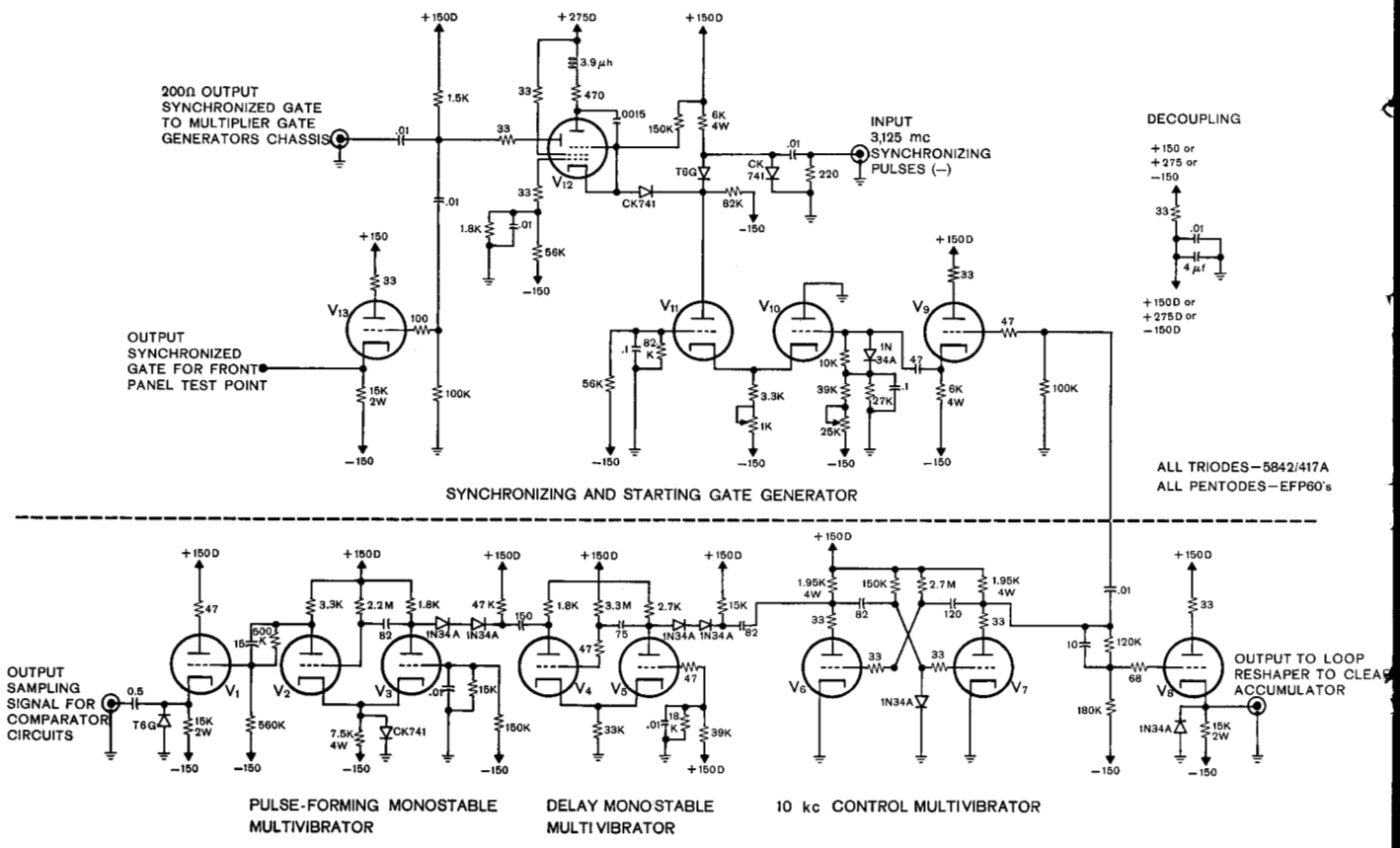



*Figure 3* **Control circuits and the synchronizing and starting gate generator.**

the three reshapers (addend, accumulator and carry) and the total accumulator loop delay. This timing may be accomplished as follows:

The system is programmed with the multiplicand set-up switches to read-in only one partial product, and the clock line to the accumulator reshaper is cut to obtain a 4-millimicrosecond time difference between the clock and signal at the inputs to the reshaper network in the accumulator on the *first* appearance of the signal at this reshaper. The 93Ω RG-62/U storage delay line is then cut so that after its first circulation in the accumulator the signal will reappear at the accumulator reshaper approximately 4 millimicroseconds ahead of the clock, i.e., the total physical delay around the accumulator loop, from the output of the reshaper network to the input of the reshaper network, is (320 minus 4) millimicroseconds. This assures simultaneous appearance of the addend and augend inputs to the adder and a fixed time difference between the signal and the clock in the accumulator reshaper during both the multiplication and storage times.

The clock line to the reshaping network in the carry loop of the adder is then cut to bring the carry signals into the adder simultaneously with the other two inputs. The additional delay in the carry loop is then adjusted to bring the carry signals into the carry reshaper network 4 millimicroseconds ahead of the clock input to this network.

The contents of the accumulator enter the indicator register through 93Ω coaxial cable driven from the output amplifier of the accumulator reshaper. Timing in the indicator is accomplished by adjusting the length of this line and the synchronizing signal line to the indicator so that the synchronizing signal and the $2^0$ digit pulse appear simultaneously at the $2^0$ tap of the indicator distribution lines. The sampling pulse for the comparator is produced by two monostable multivibrators (Fig. 3) driven by the control multivibrator. The first multivibrator provides sufficient delay so that the sampling pulse, which is formed in the second multivibrator, occurs at the end of the storage cycle.

## 2. Components

The components used in this system have been extensively described in the companion paper[1] and will therefore be only briefly described here.

The Philips EFP-60 secondary-emission pentode is used exclusively in the amplifier circuits in the unit. The EFP-60 has a nominal secondary-emission ratio of five, a transconductance from grid to plate of 25 ma/volt, a transconductance from grid to dynode of 20 ma/volt, and

a transconductance from grid to cathode of 5 ma/volt. The grid base of the tube is 3.5 volts when the plate and screen voltage are +275v and the dynode voltage is +150v. The maximum allowable plate, dynode and screen dissipations are 2 watts, 1 watt and 0.4 watt, respectively. Two useful features of the EFP-60 are that the dynode may be used as an active output element and that the tube has current gain as a grounded-grid amplifier. Since non-inverting amplification is obtainable from grid to dynode or from cathode to plate, a variety of multivibrator circuits may be built with a single EFP-60 tube.

*By using the grid and dynode as the input and output electrodes, respectively, in EFP-60 amplifier configurations, it is possible to use positive pulses throughout the system.* The advantages which derive from this unique feature of the EFP-60 tube are evident when one considers the requirements for handling negative pulses at these speeds and impedances. A cathode follower, for example, would have to be operated with a quiescent current of 50 ma in order to be able to drive 10-volt negative pulses into a 200Ω coaxial line. This feature also allows one to operate all amplifiers in a normally cutoff condition. This minimizes power dissipation and allows unwanted low-level signals to be eliminated.

The Western Electric 417A/5842 tube is used as a cathode follower in the high-speed circuitry of the system. The 5842 is a triode with a transconductance of 25 ma/volt and a maximum allowable plate dissipation of 4.5 watts. As a cathode follower it has an output impedance of 40 ohms, which suits it to pulse work at high frequencies where low impedances must be used to obtain the required rise and fall times.

The diode types used in the system are CK741/1N308,* T6G and 1N34A. The CK741 is a germanium gold-bonded diode with a dynamic forward impedance of less than 10 ohms, a reverse resistance of 25 to 100 kilohms at 3 volts reverse bias and a reverse breakdown voltage of approximately 10 volts. It is used almost exclusively in the logical circuitry of the system; its use in these circuits is dictated by its fast forward and reverse recovery times. From conducting 30 ma in the forward direction, the CK741 will recover to approximately 600 ohms in 5 millimicroseconds after the application of 10 volts reverse bias. For smaller currents the recovery is even faster.

The T6G diode is used in applications where reverse voltages of more than 10 volts are likely to be encountered. The 1N34A has very good reverse recovery characteristics, but its use in logical circuitry is prohibited by its high forward impedance. It is used to some extent in dc restorer circuits where its performance is comparable to that of the 1N308 diode.

The remainder of the components are standard resistors, capacitors and chokes. The tube type 12AT7 is used as a cathode follower in low-speed and biasing circuitry. The 2N44 PNP germanium transistor is used in the comparator circuits.

*No longer in production.

### 3. Design of individual units in the system

• *a) Introduction*

As this is an experimental system, the units which were designed at the beginning of the project have not been redesigned to utilize the more sophisticated techniques which have evolved through experience gained in operating the system.

For this reason, and also because many units are merely combinations of previously described circuits, the descriptions of units presented below vary in length and detail. The phase-locked frequency divider is a recently completed unit and is therefore described in greater detail than some of the other units.

• *b) 50-megacycle clock oscillator*

The 50-mc crystal-controlled oscillator employs conventional VHF transmitter design techniques. The output from an 8.33-mc crystal oscillator is tripled and then doubled to obtain the 50-mc frequency. A 2E26 tetrode power amplifier is coupled to a load consisting of seven 50Ω coaxial lines in parallel which feed the 10-to-15-volt peak 50-mc sine-wave clock signal to the points in the system shown in the block diagram (Fig. 1). A sine-wave clock is used because of the simplicity of making a sinusoidal signal available throughout the system without waveform distortion.

• *c) Frequency divider*

The frequency-divider circuit shown in Fig. 4 and described below provides the synchronizing pulses used in this system. These synchronizing pulses have a pulse-repetition rate of 3.125 mc and are phase-locked to the 50-mc clock. This is accomplished by blocking out every 15 cycles of the clock input and picking off and amplifying the peak of every sixteenth cycle.

The first stage of the frequency divider is a modified regenerative pulse generator[4] which divides the input by four and whose output is used to trigger an EFP-60 monostable multivibrator through a diode clamping circuit. This second stage also divides by four and produces a 20-millimicrosecond gating waveform at a 3.125-mc repetition rate which is phase-locked to the clock input. In the third stage the output of the second stage drives one leg of a diode AND circuit and gates through every sixteenth cycle of the 50-mc clock waveform applied to the other leg of the AND circuit. The output of the AND circuit is stripped and amplified by an EFP-60 amplifier.

*Stage 1*

The modified regenerative pulse generator has a diode reshaping network interposed in the feedback loop to allow synchronization of the pulse generator by the sinusoidal clock input. Its operation is as follows:

If the output of the cathode follower were connected directly to the grid of the EFP-60, this circuit would

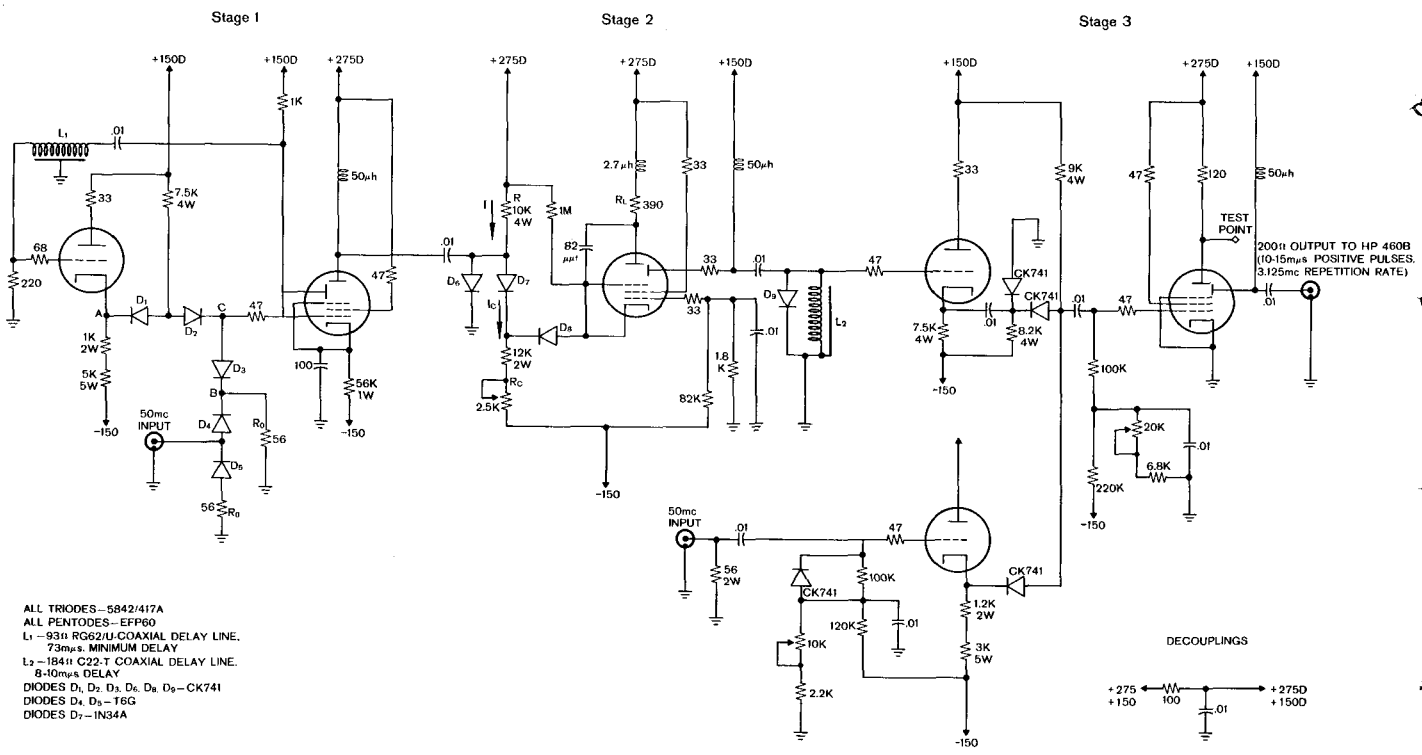



*Figure 4* **Phase-locked frequency divider.** *A 16:1 divider ratio provides a secondary timing source (referred to as the synchronizing pulses) from the 50-mc sine wave clock. These synchronizing pulses occur at a 3.125-mc repetition rate and are phase-locked to the clock signal.*

"free-run." The repetition rate of the output pulses would then be determined by the total delay through the tube and the coaxial delay line, and the width of the pulses would be determined by the bandwidth of the amplifier and delay line. The *RC* combination at the cathode of the EFP-60 is an automatic-gain-control circuit which, together with the curvature in the plate voltage *vs* grid voltage characteristics of the tube, tends to amplify the peaks of large signals and to attenuate small signals circulating in the loop. The result is that, with a proper choice of average tube current, bias builds up on the cathode, adjusting the loop gain to unity and allowing only one pulse to circulate in the loop. The average currents of the pulse trains at the dynode and the plate are determined by the cathode-resistor current and the secondary-emission ratio of the tube.

This divider stage could be synchronized by feeding in the clock signal at the cathode, but the use of the diode reshaping network provides synchronization with accurate phase lock between the clock input and the output of the circuit. Furthermore, in the absence of the clock input at one leg of the reshaping network, the loop gain is less than unity and there is no output from the circuit.

Diodes $D_4$ and $D_5$, together with the two resistors, $R_0$, allow the input line to be matched, but allow only the positive half of the clock waveform to appear at point *B*. Diodes $D_1$, $D_2$, and $D_3$, the 7.5K resistor to +150v and the input capacitance to the tube constitute the reshaping and retiming circuit used in this system. The action of this circuit is such that if pulses appear at both inputs, with the pulse at input *A* occurring before the pulse at *B*, but overlapping the rise of the pulse at *B*, the output will be identical to the pulse at *B*. This operation is accomplished through storage in the capacitor at the output of the network and is similar in function to that obtained with a regenerative broadening circuit.

If then, for the division from 50 mc to 12.5 mc required in this application, the line is cut so that the circuit would normally run with a period of 78 millimicroseconds, the addition of the 50-mc sine wave and the diode retiming circuit will introduce 2 millimicroseconds additional delay and make the circuit run with an 80-millimicrosecond period in synchronism with the 50-mc input. In other words, if a clock pulse gets through to the grid at time $t_0$, this pulse will appear at point *A* 78 millimicroseconds later and allow the fourth cycle of the sine wave after time $t_0$ to appear on the grid. This process continues and the circuit has in effect selected every fourth clock pulse. This pulse is then amplified and appears at the plate, which is not used as an active element in the pulse-generator circuit and is therefore an isolated output point. The plate supplies a 60-ma current pulse of 10 millimicroseconds duration.

The cathode follower is not essential to the operation of the circuit but its low output impedance increases the

signal-to-noise ratio at the grid of the EFP-60 and, because of the isolation it provides, the 93Ω delay line may be terminated with a 220Ω resistor to increase the open-loop gain of the circuit. The resultant reflections do not affect the operation of the circuit. It may be noted that the operation of this circuit is similar in principle to the operation of the dynamic accumulator register.

*Stage 2*

The second stage (Figs. 4, 5, 6) is an EFP-60 monostable multivibrator which is triggered from the previous stage through a diode-clamping circuit. The multivibrator configuration used here has ac-coupling from plate to cathode and operates in a manner similar to that of a blocking oscillator. No transformer is needed, however, as current amplification without signal inversion occurs within the tube.

In the quiescent state, point $A$ is clamped to ground by the difference current $(I-I_C)$ flowing through $D_6$. The cathode of the tube is therefore held at ground and the tube is biased off by the voltage divider at the grid, which holds it approximately at $-4$ volts. When a negative current pulse is applied from the first stage to the diode-clamping circuit, diodes $D_6$ and $D_7$ are back-biased and the current $I_C$ flows through $D_8$, $C$ and $R_L$, turning the tube on. Because the gain from cathode to plate in this tube is greater than unity, the tube regenerates and the plate and cathode voltages drop until the tube reaches a quasistable state in the positive grid-bias region (see Appendix). $D_8$ is then back-biased, isolating the tube from the low impedance at point $A$ during the regeneration period.

After this transition, $C$ starts to discharge, more and more of the plate current comes through $R_L$ and the grid bias decreases because less current flows through $C$. This continues until the plate "bottoms." The tube then regenerates in the direction to turn it off and the cathode voltage rises above ground by approximately the amount that $C$ has discharged during the "ON" time ($\Delta E_2$ in Fig. 5).

The negative side of the capacitor then starts charging toward $-150$ volts with a time constant $(R_L+R_C)\,C$. Since the charging current, $I_C$, is practically constant during the recharge, the time for the capacitor to charge to zero volts is $T\cong\Delta E_2 C/I_C$. During this time $D_7$ is back-biased, and pulses from the first stage cannot get through to the second stage. When the negative side of the condenser reaches ground level, the tube is ready to be triggered again. At this time there is a small period of indefinite triggering due to the fact that the positive side of the condenser has to charge to $+275$v from $(275-I_C R_L)$ volts. The current through $D_7$, which is the current $(I_T)$ available for triggering the tube is then

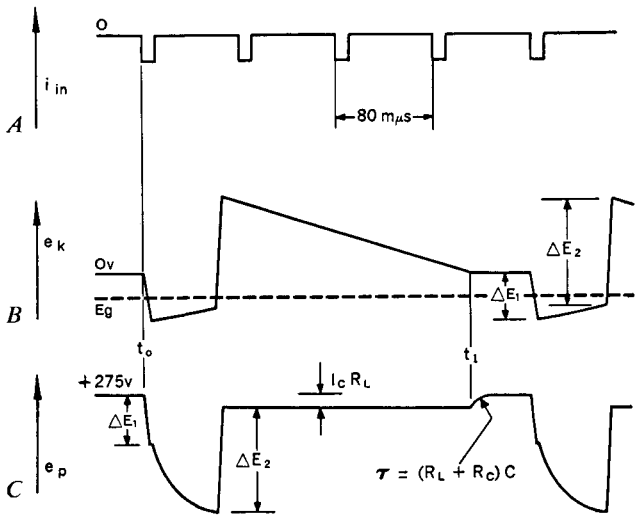
$$I_T = 0, \qquad t < t_1$$

$$I_T = I_C\left[1-\exp\left\{\frac{-(t-t_1)}{R_L C}\right\}\right]; \qquad t > t_1$$

where $t_1$ is the time at which the negative side of $C$ reaches ground level, $R_L$ is the plate-load resistor, and $C$ is the plate-to-cathode coupling capacitor. The waveforms are shown in Fig. 5.

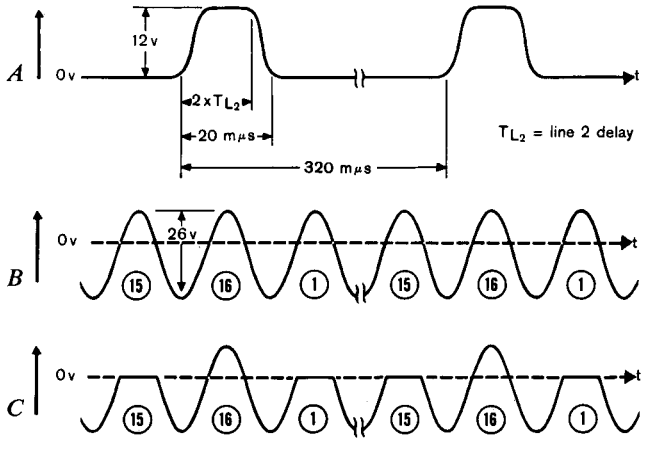
In this application of the circuit the timing is arranged so that the tube fires on every fourth pulse, and the pulses

*Figure 5* **Waveforms of the EFP-60 monostable multivibrator used in the second stage of the frequency divider.**




*A Negative current pulses from Stage 1 applied through the diode-clamping network to trigger the EFP-60 multivibrator.*
*B Voltage waveform at cathode of the EFP-60 tube.*
*C Voltage waveform at plate of the EFP-60 tube.*

*Figure 6* **Waveforms of the AND circuit in the frequency divider.**




*A 50-mc clock applied to the dc-coupled leg of the AND circuit.*
*B Gating waveform from the previous stage applied to the ac-coupled leg of the AND circuit.*
*C Output of the AND circuit.*

appearing at the free dynode have a repetition rate of 3.125 mc. The dynode is isolated from the single-shot proper except that a change of average dynode voltage will change the amplification of the tube and therefore the timing. For this reason a coil is used in the dynode and the load is ac-coupled. The dynode load is an 8-to-10-millimicrosecond shorted coaxial line which reduces the width of the dynode pulse to 20 millimicroseconds for use as a gate in the next stage. The diode $D_9$ shorts out the negative reflections which would appear at the end of the "ON" period of the tube. The rise time of the dynode pulse, shown in Fig. 6, is determined primarily by the 3-to-4-millimicrosecond transit time of the EFP-60 tube, and the tube characteristics are such that the amplitude of the pulse is limited to about 12 volts.

The timing in this stage is dependent on $R_L$, $C$, and to a smaller extent on the tube characteristics. It has been found, however, that even with a count-down of 4:1 the tube characteristics may vary over a wide range without affecting the circuit operation or reliability. The timing and frequency-division ratio is adjusted by changing the cathode resistor, and hence the charging current. A minimum $I_C$ of 10 ma is needed to trigger the tube. The inductance in the plate decreases the rise and fall times and increases the triggering sensitivity.

*Stage 3*

The output of Stage 2 is fed through a cathode follower and into one leg of an AND circuit. This leg is ac-coupled and clamped to ground; the low impedance presented at this point by the clamping diode serves to increase the signal-to-noise ratio at the output of the AND circuit.

The other leg of the AND circuit is dc-coupled from a cathode follower which is driven by the 50-mc sine wave from a 50Ω line. The input is ac-coupled into the grid of the cathode follower and provision is made to adjust the dc bias on this grid. This allows the dc level of this leg of the AND circuit to be adjusted, allowing control of the portion of the sine wave which rises above ground potential to be gated through the AND circuit. The current, $I_C$, flowing in the cathode resistor of this cathode follower consists of the tube current and, for a large part of the cycle, the AND circuit current. $I_C$ therefore has to be large enough to allow the cathode to follow the grid when the gird is going negative. That is, the time rate of change of the cathode voltage when the tube is cut off, which is approximately the difference between $I_C$ and $I_{AND}$ divided by the stray cathode capacity, should be greater than the maximum rate of change of the input (grid) voltage.

$$\frac{dV_K}{dt} = \frac{I_C - I_{AND}}{C_K} > \left[\frac{d(E_P \sin\omega_0 t)}{dt}\right]_{max} = E_P W_0.$$

Therefore, for a 50-mc sinusoidal input with a peak amplitude of 13 volts and 5 $\mu\mu$f stray cathode capacity, the excess of cathode-resistor current over AND-circuit current should be 20 ma.

From the waveforms shown (Fig. 6) it can be seen that the positive peak of every sixteenth cycle is gated through to the output amplifier, and that the gating signal may drift as much as ±5 millimicroseconds without changing the phase between the 50-mc input and the output. Drifts larger than this are unlikely and they would change the ouput of the frequency divider radically, giving a positive indication that something was wrong. The overlap of the 50-mc input and the gating waveform in this stage is accomplished by cutting the 50Ω input line to a suitable length.

*Figure 7* **Output waveform of the synchronizing and starting gate generator.**

The output of the AND circuit is fed into an EFP-60 amplifier which is normally biased-off and can be adjusted to amplify any part of the waveform appearing at the output of the AND circuit. Positive and negative current pulses of approximately 10 millimicroseconds duration are available from the dynode and plate respectively. The dynode pulse has an amplitude of approximately 60 ma, the plate pulse an amplitude of 80-100 ma. The positive output pulse from the dynode drives a 200Ω line which feeds a distributed amplifier, while the plate is left free as a test point.

● *d) Synchronizing and starting gate*

In order to enter the high-speed system it is necessary that a method of synchronization be provided between an external, non-synchronous source of commands and the internal timing. The schematic of the synchronizing and starting-gate generator is shown in Fig. 3. This circuit is an application of the plate-cathode-coupled monostable multivibrator with diode clamping used in the frequency-divider unit. Here, however, the available triggering current is controlled to provide coincidence between the randomly timed start pulses from the free-running control multivibrator and the synchronizing pulses of the arithmetic system.

In the quiescent state, the grid of the tube $V_{10}$ is at a higher potential than the grid of tube $V_{11}$, and the current in their common cathode resistor flows from ground through tube $V_{10}$. The available triggering current for the EFP-60 circuit is then just the current flowing through the 82K resistor to −150 volts and it will not respond to the synchronizing pulse input.

At the end of the 2-$\mu$sec "OFF" (non-conducting) period of tube $V_7$ in the control multivibrator — that is, after the accumulator register has been cleared — a

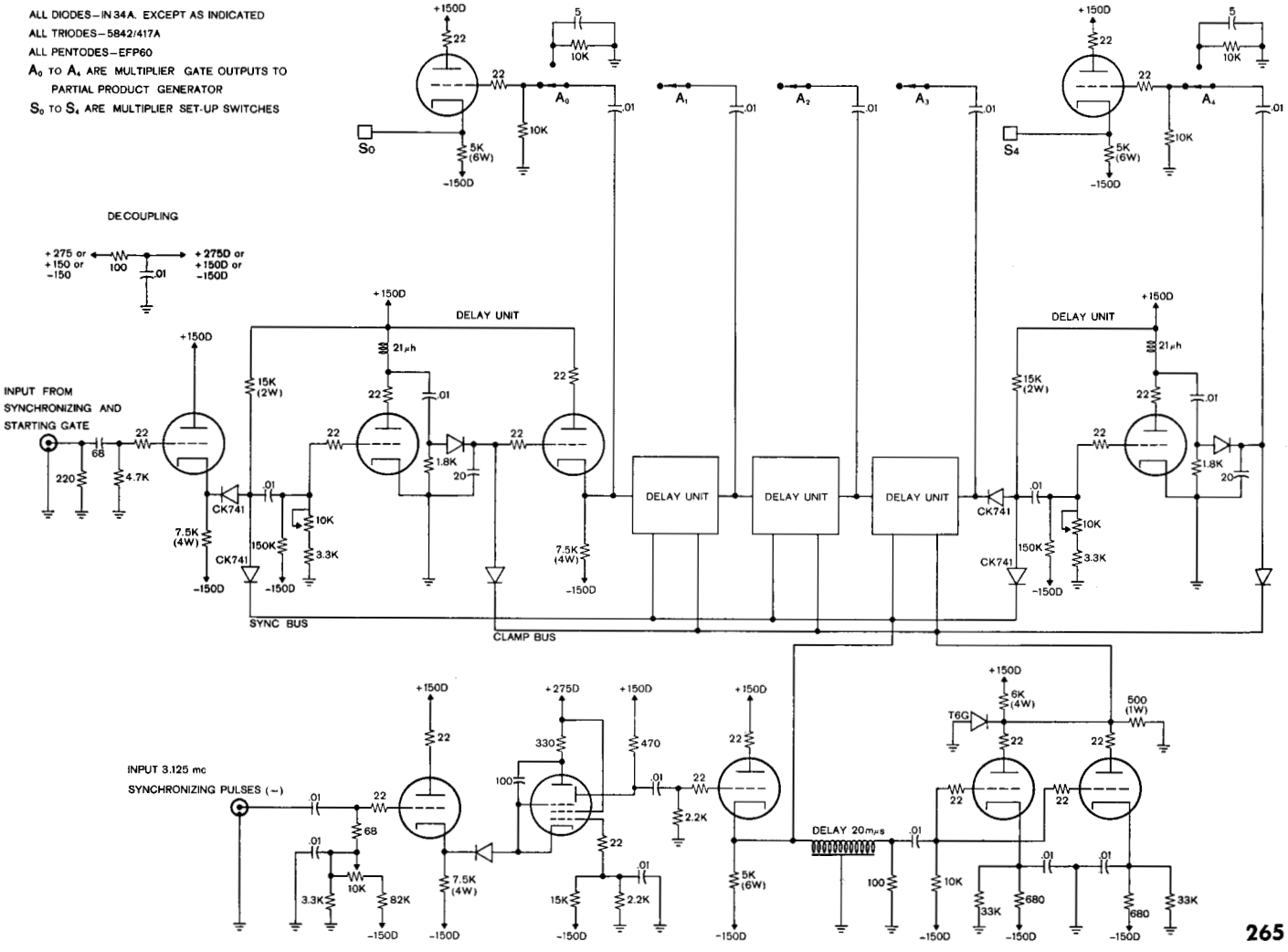
negative-going waveform, which falls approximately 80 volts at a rate of one volt/millimicrosecond, is applied to the grid of tube $V_{10}$ through a cathode follower ($V_9$). This drives the grid voltage of $V_{10}$ below that of tube $V_{11}$ and switches the common cathode-resistor current into $V_{11}$ in approximately 2 millimicroseconds. This current, which has an amplitude of approximately 15 ma, flows into $V_{11}$ from the diode-clamping circuit. The first synchronizing pulse which appears after this transition back-biases the diode-clamping circuit and forces the current to flow through the plate-load and coupling capacitor in the monostable multivibrator circuit (tube $V_{12}$), thereby triggering it to its "ON" state. A pulse which is synchronized with the internal timing of the arithmetic unit therefore appears at the dynode of the multivibrator.

To ensure coincidence of the starting pulse from the control multivibrator with at least one synchronizing pulse, the common cathode-resistor current of tubes $V_{10}$ and $V_{11}$ is made available for triggering the monostable multivibrator for a time greater than the period of the synchronizing pulses (320 millimicroseconds). This time is set by the differentiating circuit and bias control at the grid $V_{10}$ and is adjusted to be about 0.6 $\mu$sec. The blocking action of the monostable multivibrator circuit assures that only one output pulse will be produced on each cycle of the control multivibrator. The output of this circuit is shown in Fig. 7. A Tektronix Type 517 oscilloscope was used, having a 50-millimicrosecond-per-centimeter sweep speed and a vertical sensitivity of 5 volts per centimeter.

### *e) Multiplier-gate generators*

Figure 8 is a schematic diagram of the multiplier-gate generators. It shows a sequence of five units of the Havens-delay type[2,3] arranged as a five-stage shift regis-

*Figure 8* **Multiplier gate generators.**
*Shown are the 5-stage shift register with the individual Havens delay units, the sync and clamp waveform generators for the delay units, and the multiplier set-up switches ($A_0$ through $A_4$).*



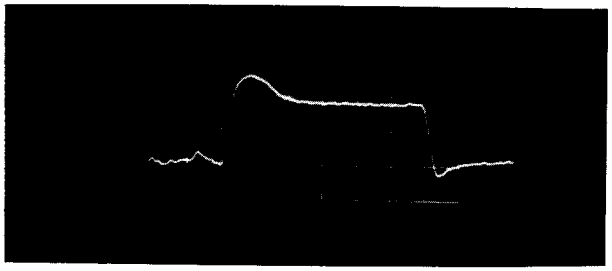


*Figure 9* **Output waveform of high-speed Havens delay unit.** *A Tektronix Type 517 oscilloscope was used, having a 50-millimicrosecond-per-centimeter sweep speed and vertical sensitivity of 5 volts per centimeter.*

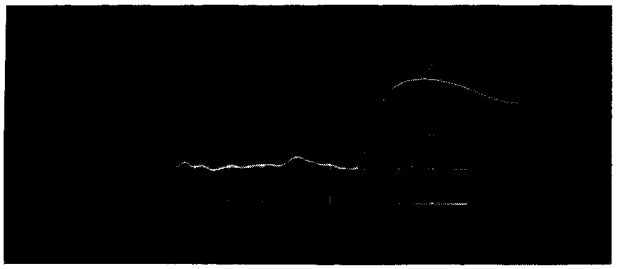


*Figure 10* **Rise time of the output waveform of the Havens delay unit.** *A Tektronix Type 517 oscilloscope was used, having a 20-millimicrosecond-per-centimeter sweep speed and a vertical sensitivity of 5 volts per centimeter. The rise time is approximately 8 millimicroseconds.*

ter. The lower row of five tubes in the schematic diagram is the circuit for generating the "sync" and "clamp" pulses for the delay units. Each negative-polarity synchronizing pulse is fed through a cathode follower to trigger an EFP-60 monostable multivibrator. The 20-millimicrosecond, 10-volt positive pulse from the dynode goes through a cathode follower and is used directly as the "sync" pulse. This pulse is also passed through a 20-millimicrosecond delay line and inverted by the two triodes connected in parallel to give a negative clamp pulse. A T6G diode is connected from the paralleled plates of the triode inverted to ground to limit the negative swing of the clamp pulse.

The shift register is started by coincidence between a synchronizing pulse and the starting gate in the first delay-unit AND circuit. The shifting in the register is at the 3.125-mc synchronizing pulse rate, so that the first delay unit stores this input signal for 0.32-$\mu$sec and then shifts it into the second delay unit, where it stays an equal length of time, and so on. The upper-left-hand output cathode follower thus receives a positive signal, starting shortly after the input signal is received. This positive signal lasts for approximately 0.30 $\mu$sec. The next output cathode follower receives a positive signal during the next synchronizing pulse period and so on. The switches ($A_0$ through $A_4$) shown in the grid circuits of the output cathode followers are those used to set up the value of the multiplier. If these switches are in the position shown on the diagram (all closed) the multiplier is 11111. Any one of the 1's may be changed to a 0 by opening the switch associated with that cathode follower. The delay units are identical in principle with the standard Havens' microsecond delay unit, but are capable of being operated at well above the 3.125-mc rate and have rise and fall times of less than 20 millimicroseconds. The major difference in our units is the use of the high-transconductance 5842 triode and some changes found in the circuit constants. The waveforms of the multiplier gates are shown in Figs. 9 and 10.

• *f) Multiplicand generator*

The multiplicand is generated from the 3.125-mc synchronizing pulses as shown in Fig. 11. The negative synchronizing pulses are fed down a 93Ω coaxial cable which is tapped at 20-millimicrosecond intervals. The signal from each tap is fed to the grid of a cathode follower which is rendered conducting or cut off, depending upon the position of the associated multiplicand set-up switch (i.e., $B_0$ through $B_4$). The selected negative pulses are combined in the combination cathode follower/diode OR circuit and fed into the cathode of an EFP-60 grounded-grid amplifier. The diodes in the OR circuit serve to isolate the cathode followers from each other so that the signal out of one cathode follower need not drive the output impedance of the other cathode followers. The neon bulbs appear on the front panel and indicate which bits of this multiplicand are "one's" as determined by the switches $B_0$ through $B_4$.

The positive pulses at the dynode of the grounded-grid amplifier are fed to a limiter-amplifier and then to a cathode follower which feeds the partial-product generator.

• *g) Partial-product generator*

The output from the multiplicand generator is fed into the partial-product generator, shown schematically in Fig. 12. The pulses representing the multiplicand are fed down a 93Ω coaxial cable tapped at 20-millimicrosecond intervals. The multiplicand then appears at each successive tap delayed by an additional 20 millimicroseconds (i.e., integral multiplies of the pulse period). Each tap feeds a cathode follower which drives one leg of an AND circuit. The other leg of the AND circuit is driven by a multiplier-gate. Thus, in every position where a multiplier gate appears at the points $S_0$ through $S_4$, the appropriately shifted multiplicand is gated into the following cathode-follower/diode OR circuit. The OR circuit output is amplified and fed to the ADDEND reshaper from a cathode follower. Thus, multiplication is performed by

examining each bit of the multiplier in turn; for each bit of the multiplier which is a "one" (as determined by the multiplier set-up keys) a multiplier gate is fed to the partial-product generator to gate the shifted multiplicand into the adder where it is added to the product being formed in the accumulator.

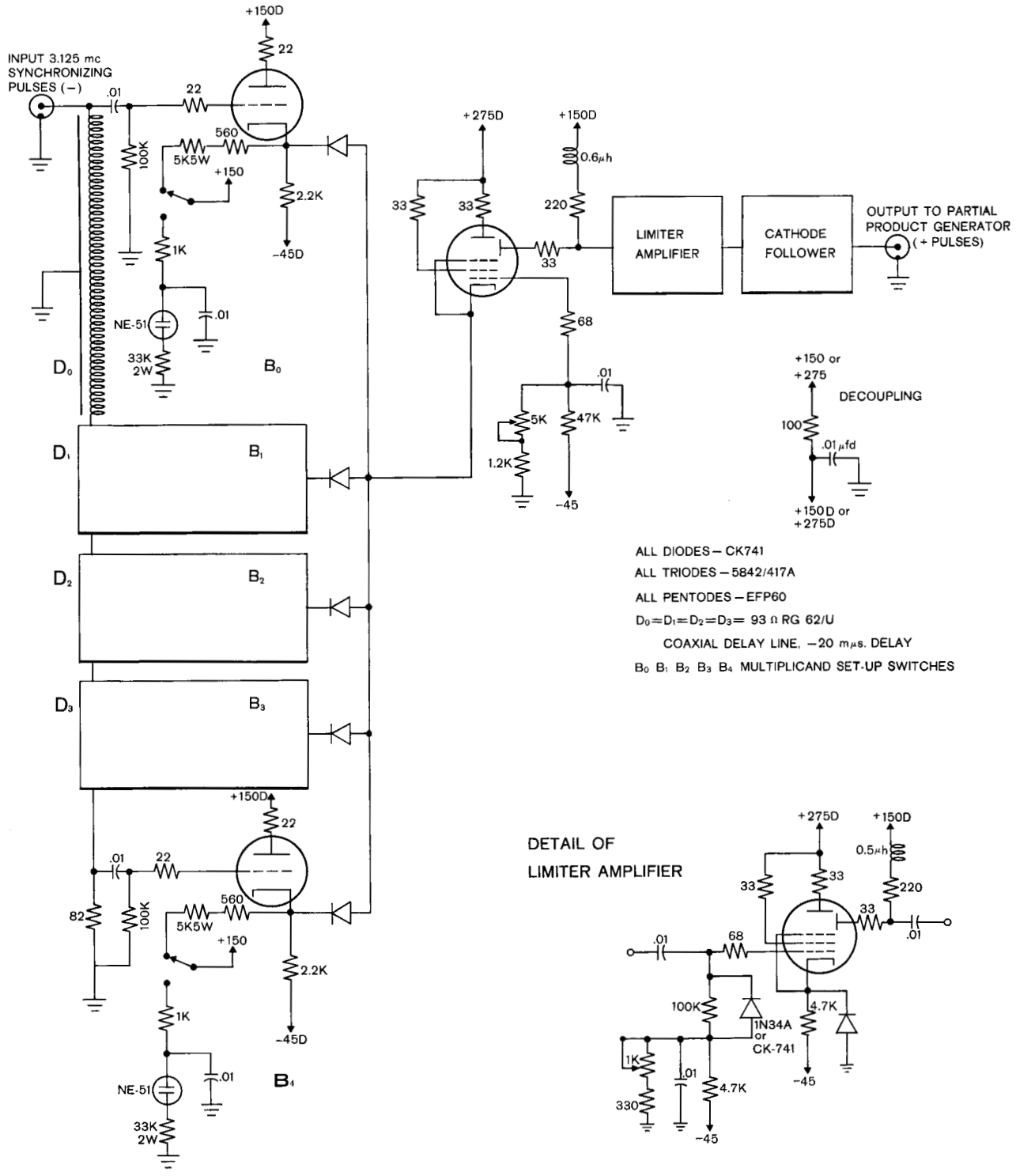



*Figure 11* **Multiplicand generator.**
*The serial 5-bit output is determined by the set of five switches $B_0$ to $B_4$. The output occurs at a 3.125-mc repetition rate.*

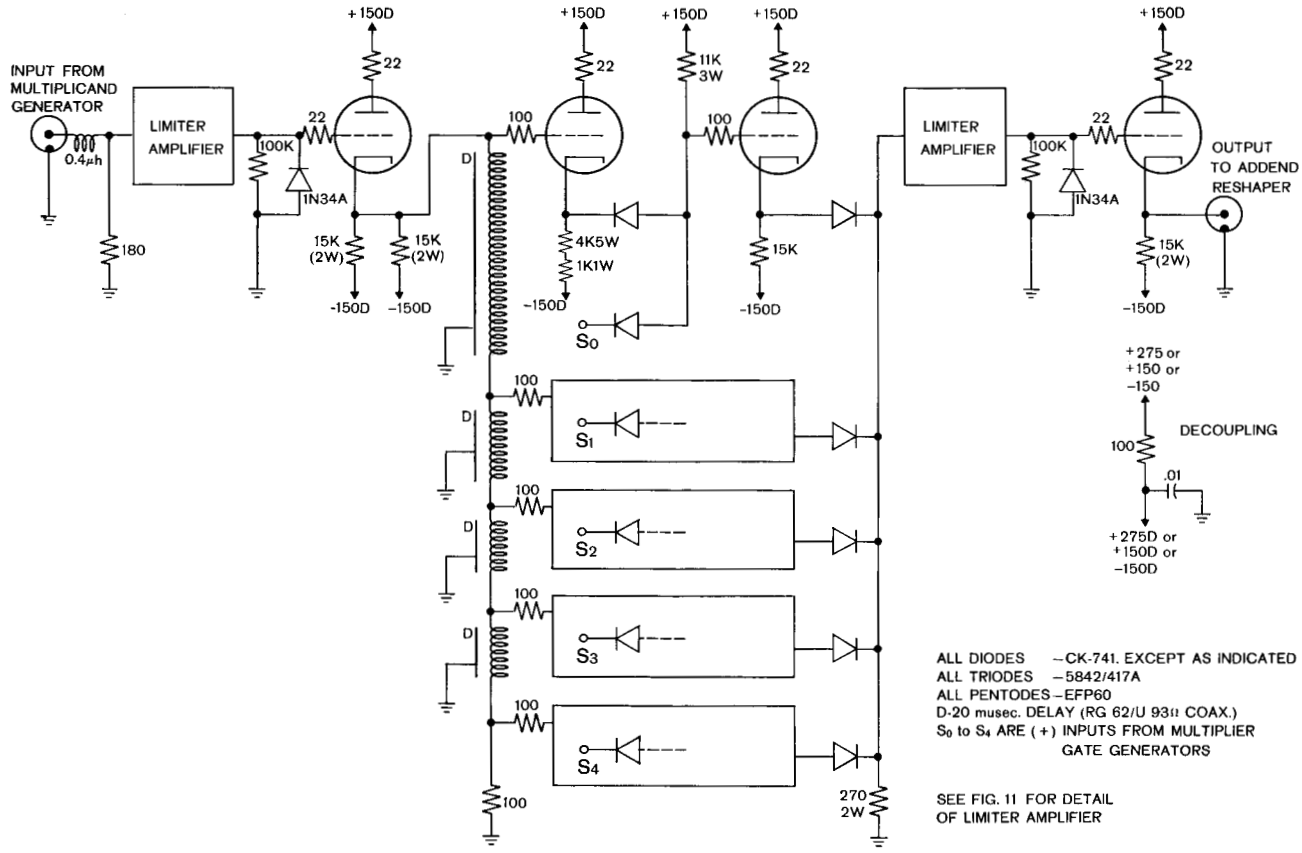



*Figure 12* **Partial product generator.**
*The input from the multiplicand generator is gated to the adder by the multiplier inputs $S_0$ to $S_4$ on consecutive synchronizing pulse periods when the multiplication program is started by the control oscillator.*

• *h) Reshapers*

The ideal reshaping requirements may be expressed by stating that in order to eliminate deterioration of pulse-coded information due to dispersion and attenuation in a system, it is necessary to check periodically the pulse information and to replace the checked pattern with a pattern containing the same information, but consisting of new, retimed pulses. These requirements imply a source of standard or clock pulses and circuitry which reproduces a clock pulse in response to entry of the deteriorated input pulse.

Since the input pulse has a non-ideal rise-time, it must be present before the arrival of the clock pulse to which it is to be retimed. At the same time, it cannot generally be assumed that the input pulse will be present during the entire clock pulse. It is therefore necessary that an output be generated which rises with the clock pulse, if an input pulse is present at the time the clock pulse rises, and that this output, if present, be held until the end of the clock pulse.

We use a notation where $X = AB$ means that $X$ occurs *if and only if* both $A$ and $B$ occur, where $X = A + B$ means $X$ occurs *if either A or B or both* occur. With these definitions, the reshaping function may be written:

$$X = CI + CX, \tag{1}$$

where:
$X$ = reshaped pulse,
$C$ = clock pulse,
$I$ = input pulse.

Several embodiments of this reshaping equation which have been used in the past are shown in Figs. 13a and 13b, with the primary differences being in the method in which the HOLD operation implicit in the $CX$ term of equation (1) is obtained. In the circuit[5,6,7] of Fig. 13a, this is done by feeding $CI$ through an amplifier and using a positive feedback path through a second AND circuit. This method fails when the delay time through the amplifier, $\tau$, becomes comparable with the pulse width, as can be seen by writing the reshaping equation for "a" including this effect:

$$X(t) = C(t)\, I(t) + C(t)\, X(t - \tau)$$
$$= C(t)[I(t) + X(t-\tau)].$$

One sees that $X(t)$ falls when $I(t)$ falls unless $t > \tau$ at this time, where it is assumed that $t = 0$ at the rise of $C$,

that $I$ falls before $C$, and that $X(t-\tau) = 0$ for $t-\tau < 0$.

In Fig. 13b the HOLD operation is performed by a multivibrator circuit which triggers "ON" with $CI$ and which triggers "OFF" with the fall of $C$. This configuration is limited by the frequency at which multivibrators can easily be triggered and reset, and again fails at the frequency range of interest here.

Figure 13c shows the reshaping circuit used in this system. The AND circuit provides the $CI$ term of equation (1), while diodes $D_1$ and $D_2$, with $C$, provide the HOLD implicit in the $CX$ term of the equation. A limiting amplifier is usually used to compensate for losses in the logical circuitry and to provide a limited output amplitude. In this circuit we see that the speed limitation is set by the logical circuitry and the amplifiers available, but is not affected by delay through the amplifier, as was the case in Figs. 13a and 13b where regeneration was required. Fig. 13d shows a circuit equivalent to Fig. 13c with a reduction of one diode. This reshaper circuit, together with limiter-amplifiers and cathode followers, makes up the addend reshaper, shown in Fig. 14, and the accumulator reshaper units in the system.

• *i) Binary adder*

A block diagram of the full binary adder is shown in Fig. 15 and schematically in Fig. 16. The logic is seen from the block diagram to be that of a conventional full-binary adder; however, the use of high-speed circuitry and the availability of the reshaped carry pulse at the input of the adder 20 millimicroseconds after the occurrence of the pulses which produced it, allow the adder to be used at a 50-mc pulse-repetition rate. The sum output to the accumulator reshaper occurs 29 millimicroseconds after the occurrence of the input pulses. The individual component circuits which allow for these high-speed operations, such as the EFP-60 limiter-amplifier circuit and the high-speed diode AND and OR circuits, have been described previously. The schematic of Fig. 16 shows the application of these component circuits to the adder.

In Fig. 15 the outputs of limiter-amplifier circuits 1, 2 and 3 are ac-coupled and dc-restored to a voltage of approximately $-5$ volts, so that the output voltages from cathode followers 4, 5, 6, 7, 8 and 9 are at approximately $-3$ volts with no input signals to the adder. The output

*Figure 13* **Reshaping circuits.**
*a) Conventional, regenerative reshaping circuit.*
*b) Multivibrator reshaping circuit.*
*c) and d) Diode reshaping circuits used in the 50-mc system.*

*Fig. 13a*

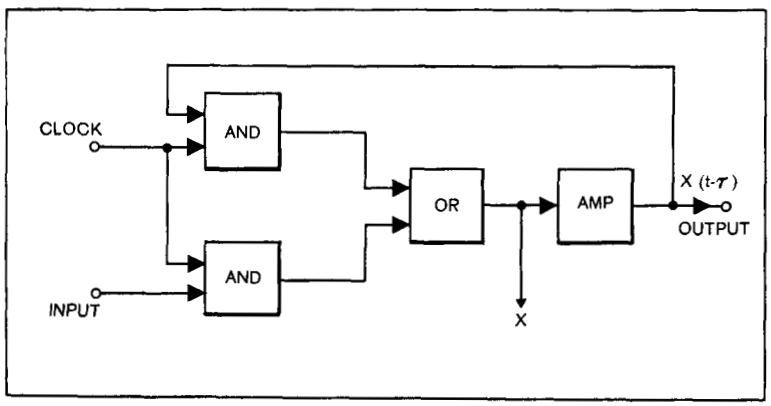
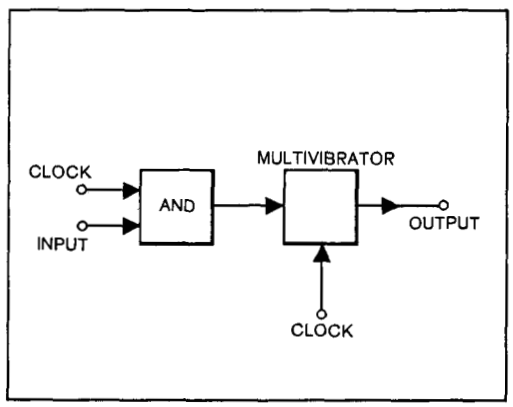



*Fig. 13b*



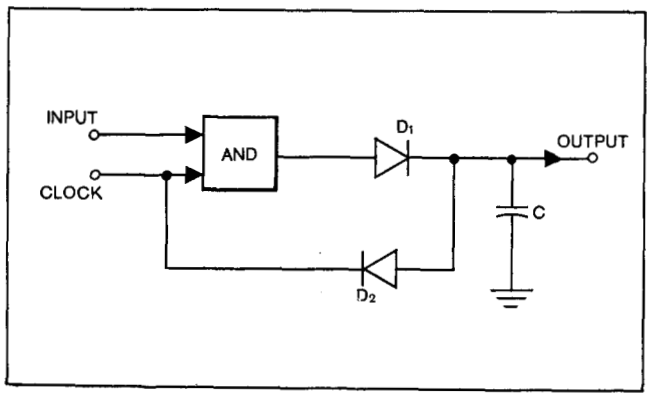




*Fig. 13c*

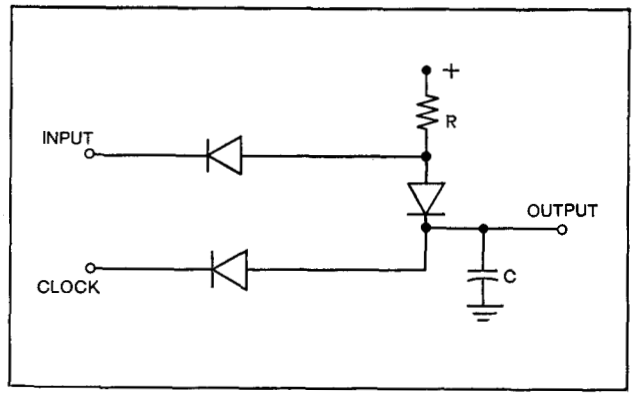



*Fig. 13d*

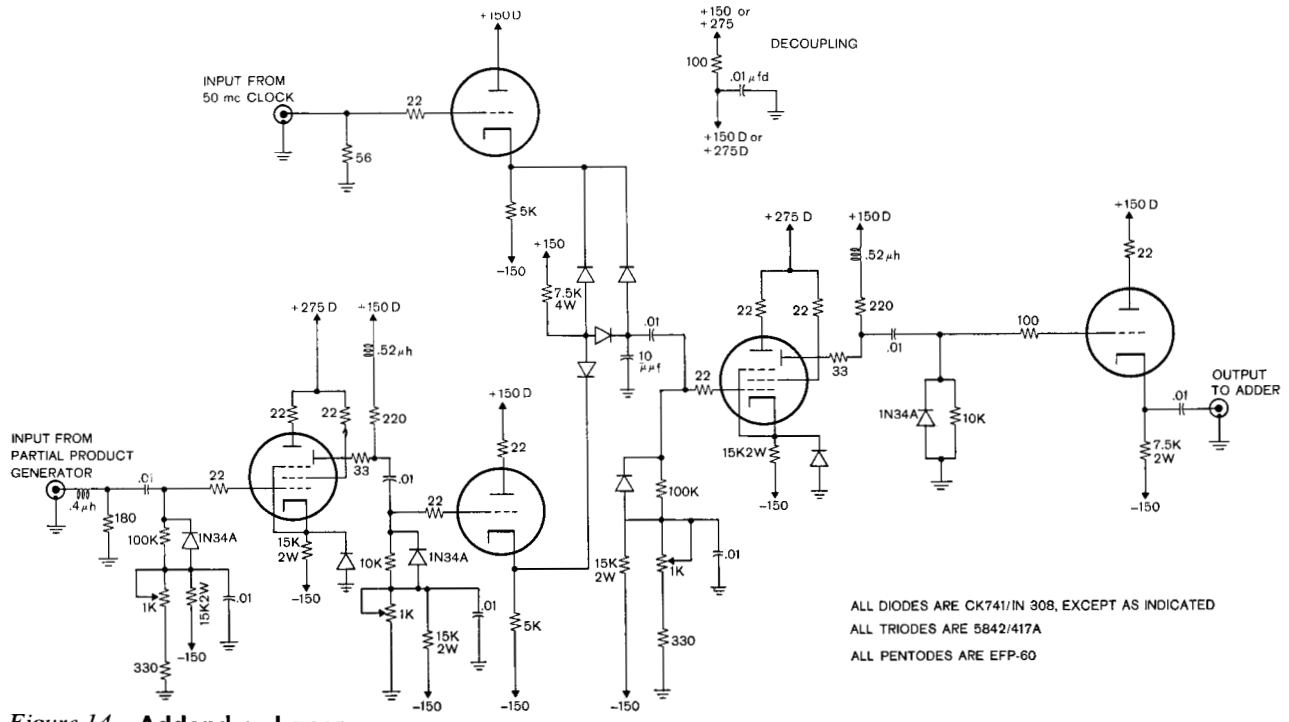



*Figure 14* **Addend reshaper.**
*This schematic shows the combination of the limiter amplifier circuit and the diode reshaper network which makes up the reshaper blocks shown in Figure 1.*

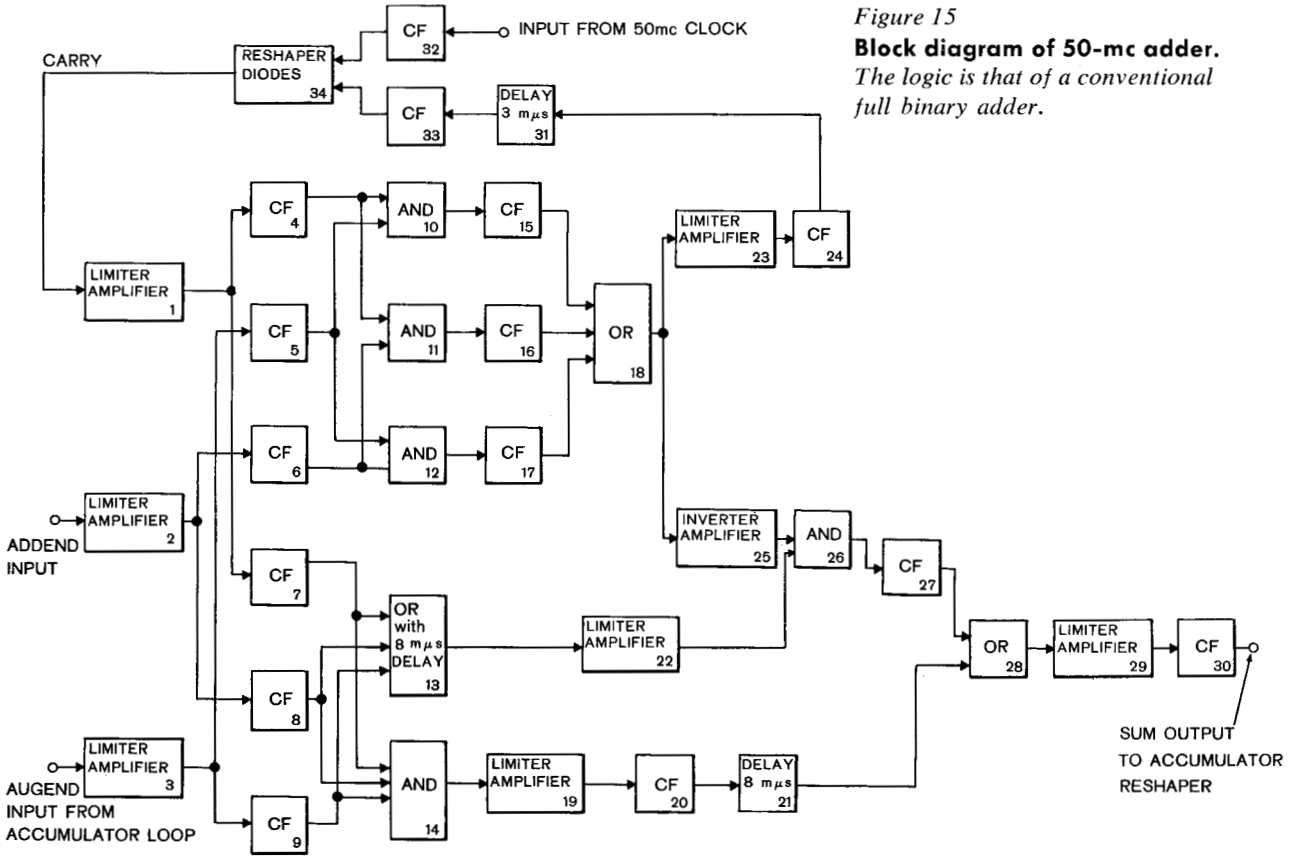


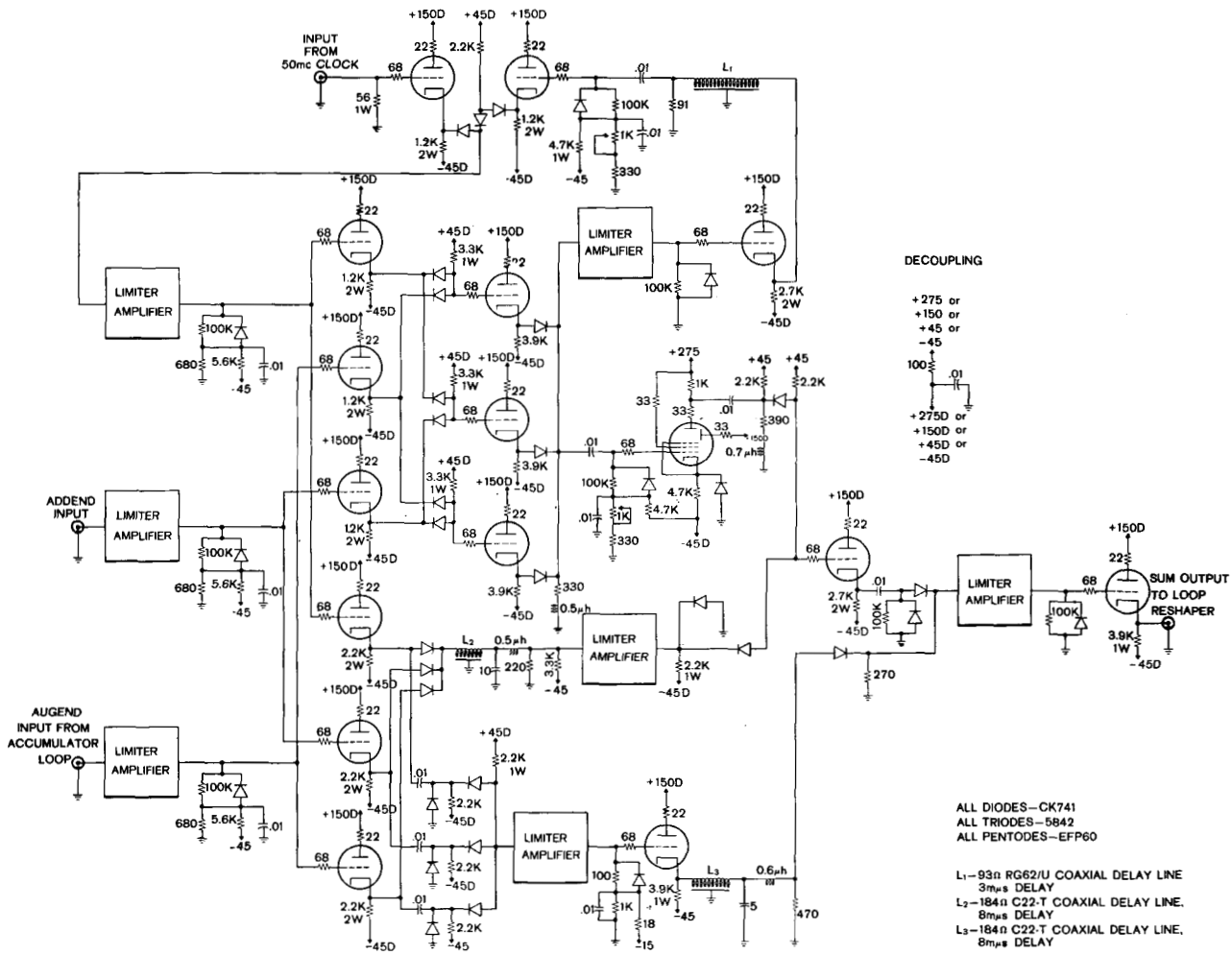

*Figure 15*
**Block diagram of 50-mc adder.**
*The logic is that of a conventional full binary adder.*

of OR circuit 13 is biased at approximately —2 volts. Thus the diodes of OR circuit 13 are normally back-biased by one volt, and an output is therefore obtained from the circuit only for input signals with a peak amplitude greater than 1 volt. In this way low-level unwanted signals due to line reflections, overshoots due to shunt-peaking, spurious responses due to signals being shunted around resistors or diodes through stray capacities, and spurious responses from diode circuitry due to recovery characteristics, are all eliminated. OR circuit 18 is also operated in this manner, the output voltage of cathode followers 15, 16 and 17 being at about —1 volt. The primary method of eliminating unwanted low-level spurious signals, however, is by operating all the EFP-60 limiter-amplifiers biased below cut-off so that a minimum amplitude signal of from 0.5 to 3 volts is required to bring the tube into conduction. Sections of coaxial delay line are used (e.g., $L_2$, $L_3$) to adjust for differences in circuit delay time.

The carry signal which appears at the output of 3-way OR circuit 18 is amplified and reshaped in the carry loop (circuits 23, 24, 31, 32, 33 and 34), and appears at the input to the adder one pulse period after the pulses at the input which produced it, as is required when performing serial arithmetic.

The upper leg of AND circuit 26 is biased so that an output is obtained from the AND circuit whenever there is an output pulse from limiter-amplifier 22 but no carry signal. Whenever a carry signal is presented at the output of OR circuit 18, however, a negative pulse is fed from the plate of inverter-amplifier 25 to inhibit the output from AND circuit 26. In order that the negative pulse out of inverter-amplifier 25 be effective in inhibiting the output from AND circuit 26 it must completely overlap the

*Figure 16* **Schematic of 50-mc full binary adder.**
*This shows how the basic circuits and components, e. g. limiter amplifier, diode reshaper network, cathode followers and coaxial delay lines, are combined to perform full binary adder logic at a 50-mc pulse repetition rate.*



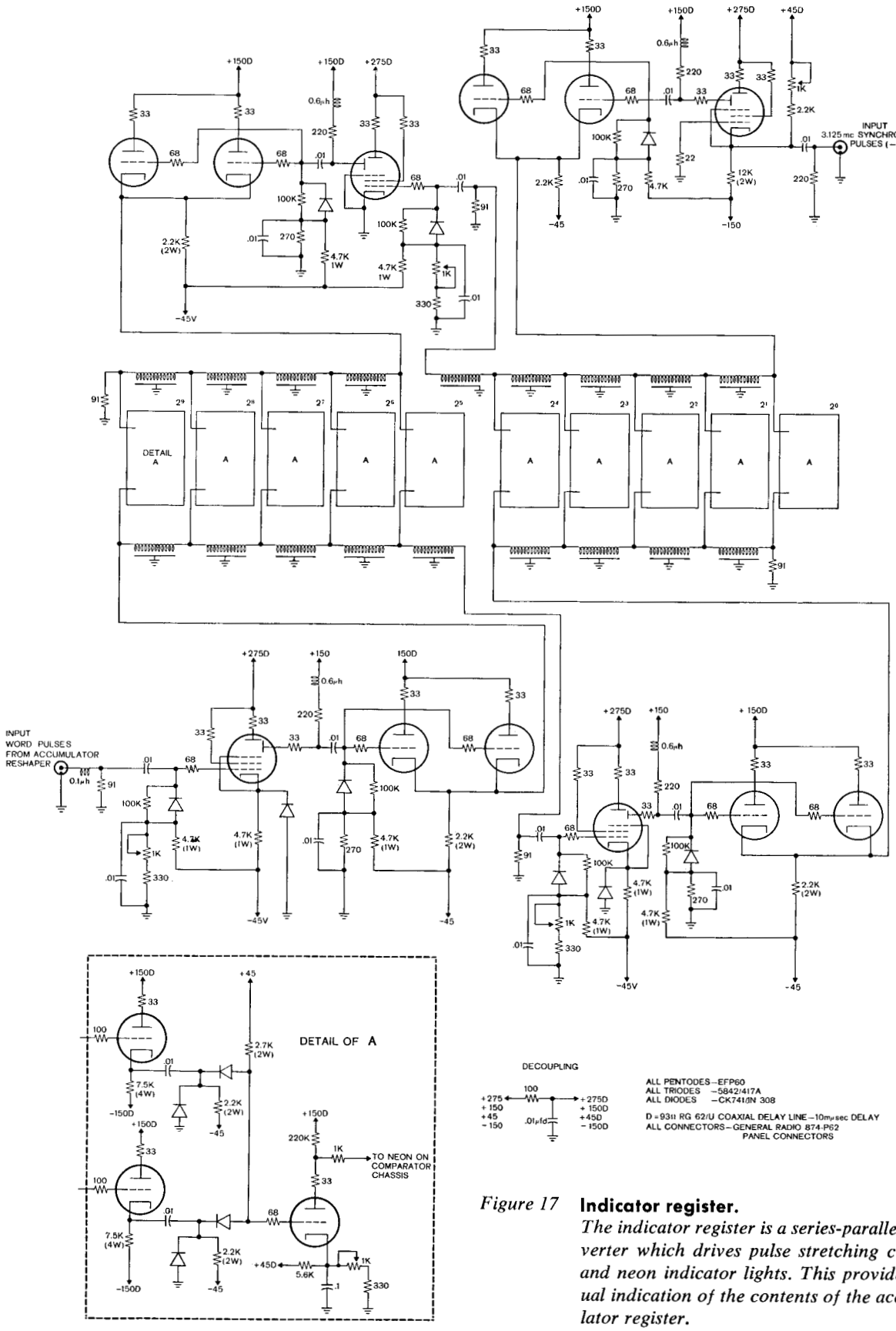



*Figure 17* **Indicator register.**
*The indicator register is a series-parallel converter which drives pulse stretching circuits and neon indicator lights. This provides visual indication of the contents of the accumulator register.*

output signal from limiter-amplifier 22. That is, it must be down before the pulse from limiter-amplifier 22 begins to rise and must not rise again until the pulse from limiter-amplifier 22 has fallen. This is accomplished by adjusting the length of the delay line in OR circuit 13 so that the output of inverter-amplifier 25 falls before the pulse from limiter-amplifier 22 rises, and by using a relatively large anode load in the inverter-amplifier to increase both the amplitude and width of its output so that it completely overlaps the output from amplifier 22. The width of the inverter-amplifier output is held within the 20-millimicrosecond pulse period so as not to interfere with subsequent pulses.

• *j) Indicator register and comparator circuits*

An indicator register and a comparator circuit are provided in the system in order to obtain a visual indication and a check of the contents of the dynamic accumulator register.

The indicator register (Fig. 17) is a series-parallel converter whose outputs drive pulse-stretching circuits which in turn drive neon lights to indicate the contents of the accumulator register.

The series-parallel converter consists of two distribution lines tapped at 10-millimicrosecond intervals, with corresponding taps connected through cathode followers to ac-coupled AND circuits. The contents of the accumulator are amplified and fed into one distribution line at the $2^9$ position of the converter, while the computer synchronizing pulses are fed into the other line at the $2^0$ position by an inverter amplifier. Limiter-amplifiers are provided in the middle of the distribution lines to make up for the decrease in signal amplitude brought about by the loading of the cathode follower connected at each tap point. If the timing of the inputs to the converter is arranged so that the synchronizing pulse and the $2^0$ bit of the stored word appear simultaneously at the $2^0$ tap points of the two distribution lines, the synchronizing pulse will sample and read out each digit position of the word at successive 10-millimicrosecond intervals.

In conventional computer circuitry, series-parallel conversion is performed by feeding the serial signal into a line which is tapped at intervals corresponding to the period of the pulses in the serial signal, and sampling all the tap points simultaneously at the appropriate time. This is not practical, however, when working with 50-mc pulse repetition rates, because the time to propagate a signal along a chassis two or three feet in length is comparable to the time between successive pulses. "Simultaneous" sampling is therefore impractical and other methods, such as the one described above, have to be used.

The output of each AND circuit in the series-parallel converter is applied to the grid of a 5842 amplifier which is biased to be normally non-conducting. The incoming pulse, which re-occurs every 320 millimicroseconds during the storage part of the computer multiplication, is amplified and then integrated by the 220K plate load resistor and the output capacity of the tube. After approximately 5 $\mu$sec or 15 input pulses, the plate drops sufficiently to fire the neon indicating lamp. The plate voltage then remains constant, with the amplified input pulses supplying the maintaining current for the neon lamp.

The comparator circuit is intended to indicate errors in each separate digit position, and consists of ten of the sections shown in Fig. 18, one for each digit position. The 2N44 germanium transistors used in this circuit have a maximum allowable collector-to-base voltage of 45 volts. Each comparator section is driven from the associated neon digit indicator and the voltage swing at the neon is divided down by the resistive divider, $R_1$ and $R_2$, and fed into a cathode follower. The cathode follower in turn drives a transistor inverter and the switch $S_1$ *is* connected to the output of either of these circuits depending on what the contents of the accumulator register should be. The design of the resistive divider is such that when a digit is stored in the accumulator register and the neon is lit, the grid voltage of the cathode follower is sufficiently negative for the cathode to be held at ground potential by the CK741 diode, and when the neon is not lit the cathode voltage is more positive than $V_1$ and the inverter is cut off.

The leg of the AND circuit connected to $S_1$ is therefore held at ground potential so long as the switch is in the correct position and there is no error in the stored word. The other leg of the AND circuit is driven by a 10-volt, 10-$\mu$sec pulse which is derived from the control circuit and occurs just before the end of each storage cycle. This pulse is restored to ground potential on entering the comparator chassis.

The latch-up error-indicator circuit is a transistor flip-flop in which $T_1$ is normally set on by the manual reset circuit in the base return of $T_2$. When both AND circuit diodes become back-biased, on the coincidence of the sampling pulse and an error signal, the current in the 220K AND circuit resistor switches into the flip-flop circuit and triggers it to its other stable state. $T_1$ is then cut off and the front panel error-indicator neon is lit. The circuit remains in this position until it is manually reset. The neon lamp connected to the collector of $T_2$ serves only to limit the voltage applied to this collector.

## 4. Physical and construction problems

Figure 19 shows the completed system mounted in a closed relay rack. The units in the front of the rack are, reading from top to bottom, the 50-mc clock oscillator with its associated meters, the dc and ac power control, the comparator unit with 10 indicator lights at the top and the error-indicator lights with their associated set-up switches below, the 5 multiplicand set-up switches and indicator lamps, and the combined multiplier gate-partial product generator chassis with its 5 multiplier switches. The rest of the circuitry is mounted in the remaining front panel positions and on the sides of the rack. The unit is cooled by a rotary fan mounted at the top of the rack.

The distribution of signals from chassis to chassis in this system is through coaxial cables, and at these speeds the signal distribution becomes an integral part of the timing of the system. In other words, it is no longer pos-

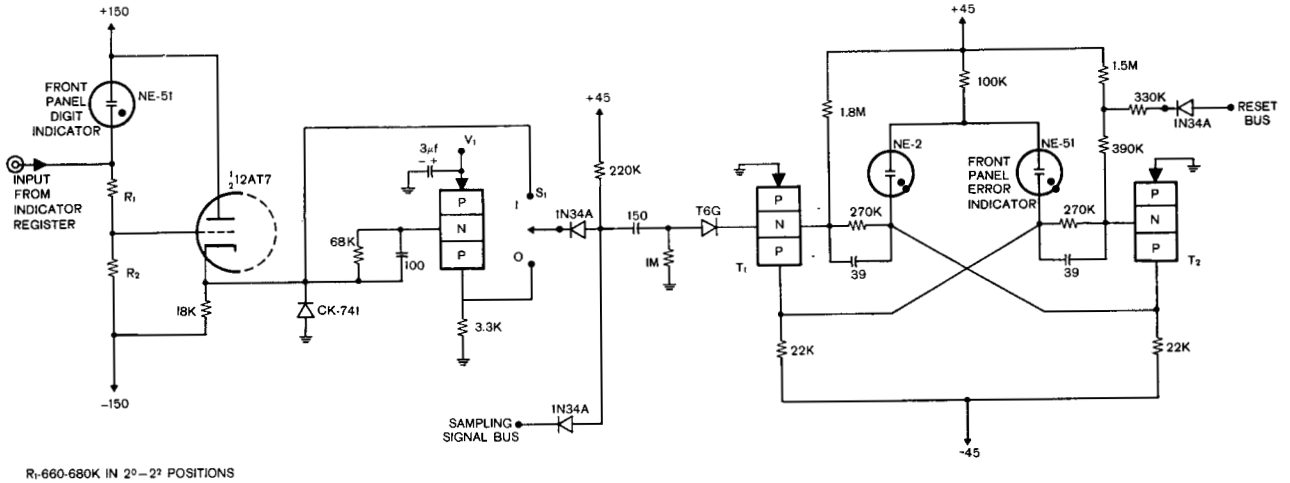
sible to assume that a signal which is fed from a unit at one instant of time arrives at its destination at the same instant of time. It is possible, however, to make use of this interdependence between time and space (e.g. in the continuously variable clock-phase aspect of the system), so that it becomes one of the attractive features of this system and in many ways leads to an overall simplification in the circuitry.

The cables used for signal distribution are RG-58/U 52Ω coax, RG-62/U 93Ω coax, and Transradio Type C-22-T 184Ω coax. This last type is used for short time-delay distribution of signals between chassis because it is physically small (O. D. of 0.44") and has an impedance which is close to the maximum allowed by signal-rise-time considerations and which will allow the line to be driven to the required signal amplitudes with the available tubes. That is, a 10-volt signal on the line requires 55 ma of current, which is just within the current capabilities of the 417A/5842 cathode follower circuit. Connectors are available from Transradio for this cable.

Line reflections were at one time a major problem in this system. The best solution to this problem was found to be the introduction of a lumped-parameter delay section between the cable connector and the following tube circuit, with the connector and tube capacitances making up the pi-section capacitances. Examples of these terminations may be seen in the circuit diagrams (e.g., Adder schematic, Fig. 16).

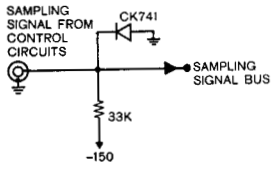
In the construction of the circuitry, the only precautions which have been taken are the usual ones for high-frequency circuits, i.e., dc-voltage decoupling, parasitic resistors, filament by-passing and a single ground point, if possible, for each sub-circuit. The circuitry is kept as compact as possible to avoid propagation delay troubles; the only point where this has been really bothersome is in the indicator register.

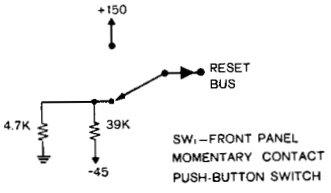
*Figure 18* **The comparator section.**
*The comparator circuit, consisting of ten of the above sections, checks for errors in each separate, digit position on every multiplication performed in the arithmetic unit.*



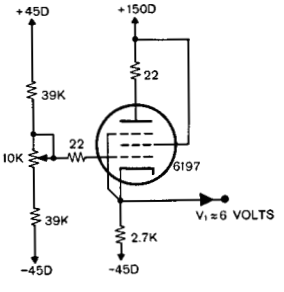

R1-660-680K IN $2^0-2^2$ POSITIONS
630-650K IN $2^3-2^9$ POSITIONS
R2-930-950K
ALL TRANSITORS-G.E. 2N44

COMPARATOR SECTION FOR ONE DIGIT POSITION
One section for each digit position from $2^0$ to $2^9$




SW1-FRONT PANEL MOMENTARY CONTACT PUSH-BUTTON SWITCH



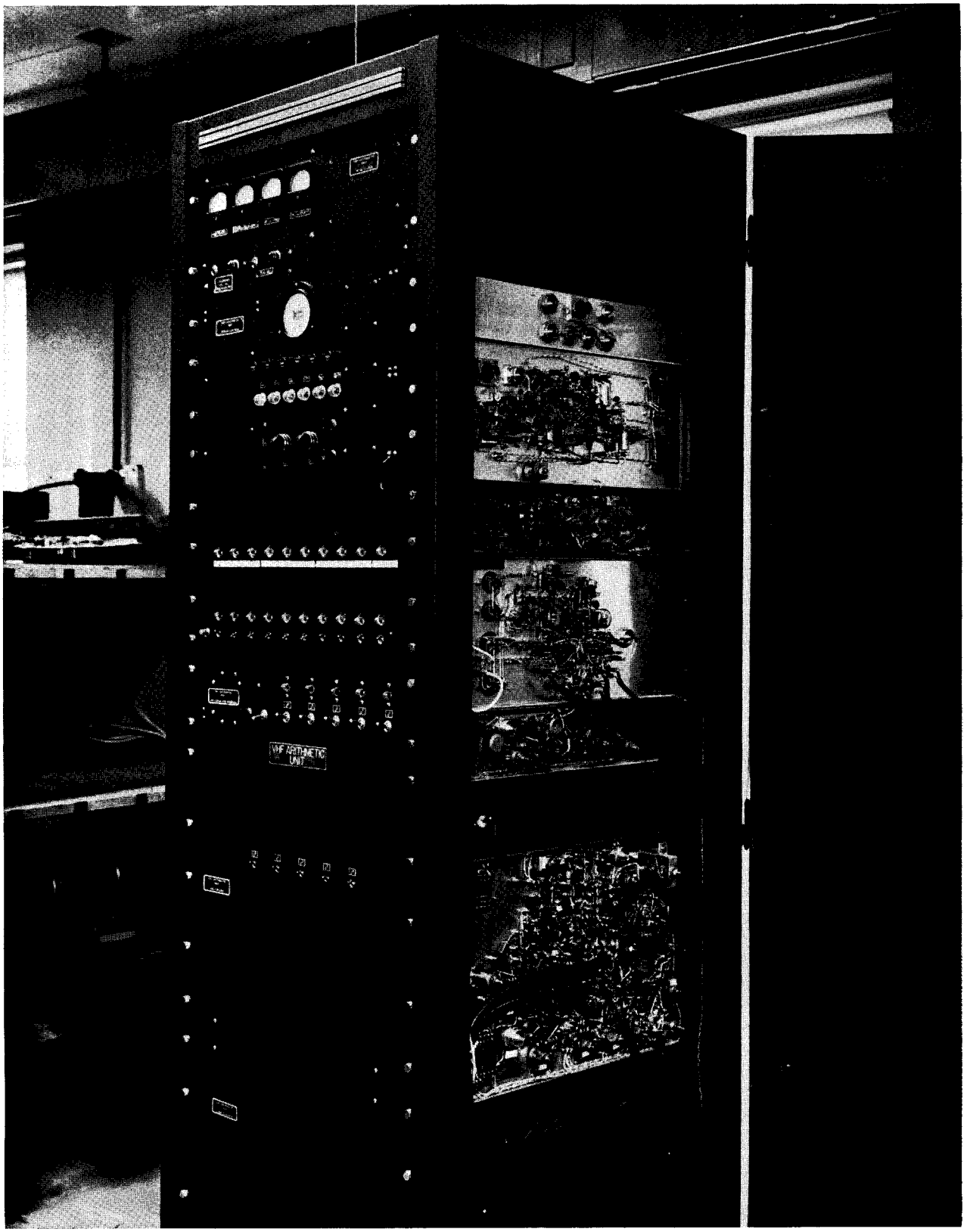



*Figure 19* **The complete system.**

| | $2^0$ | $2^1$ | $2^2$ | $2^3$ | $2^4$ | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | ↓ | ↓ | ↓ | ↓ | ↓ | | | | | |
| 1st Partial Product | 1 | 0 | 1 | 1 | 1 | | | | | 1st Adder Output |
| 2nd Partial Product | 0 | 1 | 0 | 1 | 1 | 1 | | | | |
| | 1 | 1 | 1 | 0 | 1 | 0 | 1 | | | 2nd Adder Output |
| 3rd Partial Product | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| | 1 | 1 | 1 | 0 | 1 | 0 | 1 | | | 3rd Adder Output |
| 4th Partial Product | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 4th Adder Output |
| 5th Partial Product | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | |
| Product | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 5th Adder Output |

Multiplicand = 10111 = $2^0 + 2^2 + 2^3 + 2^4 = 29$
Multiplier = 11011 = $2^0 + 2^1 + 2^3 + 2^4 = 27$
Product = $27 \times 29 = 783$
Product = $2^0 + 2^1 + 2^2 + 2^3 + 2^8 + 2^9 = 783$

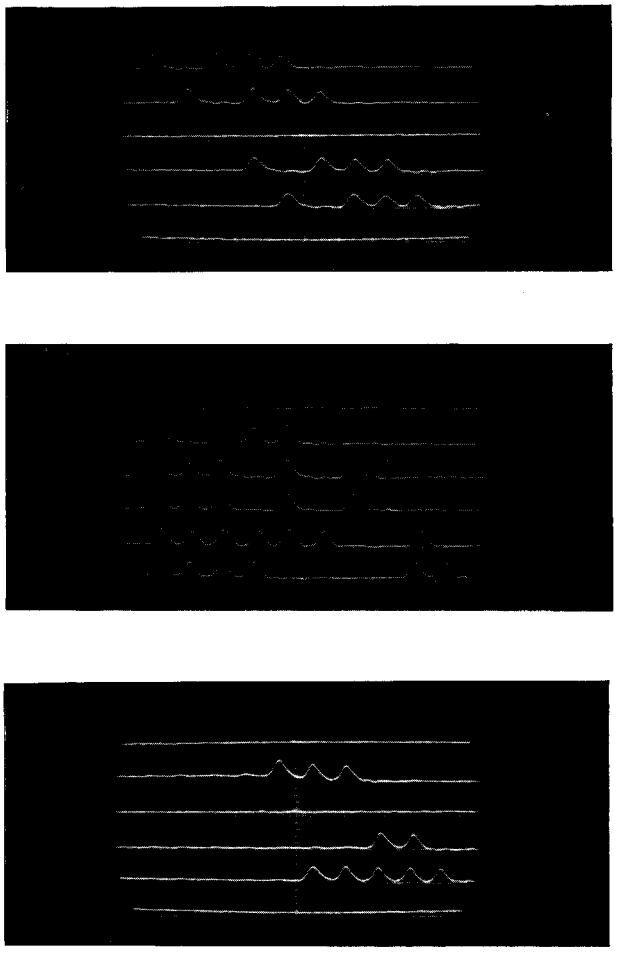



*Figure 20* **Performances of a typical multiplication program in the arithmetic unit.**
*a) Partial product at addend input of adder.*
*b) Augend input to adder from storage delay line*
*c) Carry input to adder.*

## 5. Performance and reliability

• *a) Illustrated system operation*

The oscilloscope photographs shown in Figs. 20 and 21 illustrate the system waveforms and the performance of a typical multiplication program (10111 × 11011). The multiplication is calculated above for reference; the binary numbers are shown as they would appear on the face of an oscilloscope, i.e., the lowest order digit ($2^0$) is on the left, and addition is started from the left with the remainder being carried to the next highest digit on the right.

The photographs in Fig. 20, reading from top to bottom, show waveforms during the first six add cycles after initiation of the multiplication program at the points (*a, b, c*) listed in the caption. The photograph of Fig. 21, reading from top to bottom, shows the waveforms at points $S_0$ to $S_4$ in the partial product generator schematic at the beginning of a multiplication program.

The viewing equipment used with this system and for these photographs is shown in Fig. 22. The attenuator is necessary because an input at the grid of the cathode follower greater than three or four volts will cause grid current to flow, and will therefore clip the input signal. The capacitive loading of the circuitry by the probe is on the order of 3 $\mu\mu$f. The photographs were taken with sweep speeds of 20 m$\mu$sec/cm (Fig. 20) and 200 m$\mu$sec/cm (Fig. 21). The oscillopscope vertical sensitivity is 25 volts/cm.

• *b) Evaluation of components and basic circuits*

Of the two tubes which we have chosen as the best com-

mercially available types for use in the millimicrosecond-pulse circuitry discussed above, the Western Electric 417A/5842 triode has proved to be reliable in the circuits in which it has been used. On the other hand, the circuits using the EFP-60 tube are not as reliable due to differences between individual EFP-60's and also because of variations in their characteristics with use. A real evaluation of these tubes is difficult because there are apparently variations in characteristics between different lots of these tubes which we have received from the manufacturer. The reliability of a circuit using the EFP-60 is dependent upon the circuit itself. For example, the monostable multivibrator in the frequency-divider unit functions reliably over fairly wide variations in EFP-60 characteristics. In other circuits, such as the limiter-amplifier, the output level is directly related to the grid-dynode transconductance of the EFP-60, and the output-signal amplitude has been found to vary considerably during the lifetime of the tube and also from one tube to another.

The other component of major consequence in this system is the germanium diode. With hermetically sealed units the failure rate is zero for all practical purposes. However, the reverse recovery characteristics of even the best available gold-bonded units are only barely within the specifications required for logical operations with 10-millimicrosecond pulses. It seems reasonable to assume, however, that a great improvement could be obtained if a concerted effort were made by the manufacturers of germanium diodes to produce a unit specifically for use with millimicrosecond pulses. In particular, if the recent techniques used for the production of high-frequency drift transistors were applied to the manufacture of diodes, we feel that superior units could be obtained.

The system uses a total of 27 EFP-60 tubes, 121 417A/5842 tubes, and 169 diodes.

• c) *Evaluation of individual units*

The most marginal units in this system are those which use the greatest amount of diode logical circuitry and limiter-amplifier circuits. This is a direct consequence of the discussion in Section b above. We have found in general that the units which are composed primarily of

*Figure 21* **Multiplier gates.**

multivibrator circuits and also the units which operate at the 3.125-mc rate are the most reliable. The delay-unit shift register, for example, has operated without failure during the time that the system has been in operation. The requirements on the individual units are much more stringent for those units within the dynamic accumulator register.

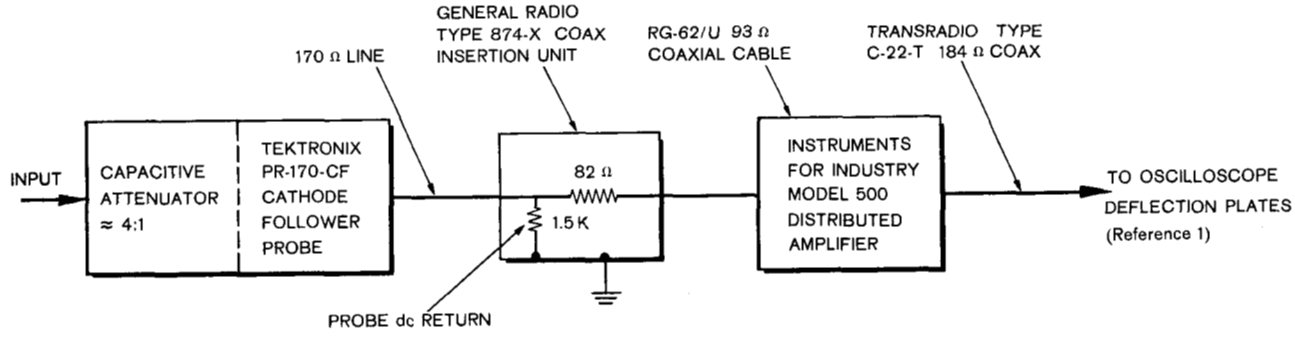
Another problem encountered in the system is the variation in bias levels at the inputs to the limiter-amplifiers due to the non-ideal dc restoration. These bias levels are a function of the number of pulses appearing at the dc restoration point. Typically, the bias levels in the accumulator register with no pulses stored will be one volt different from the bias levels with 8 pulses stored. This one-volt shift is quite significant when compared to the 3.5v grid base of the EFP-60 tube and the amplitude of the pulses. The reliable operation of this system is very much dependent upon a constant phase lock between the 50-mc clock and the 3.125-mc synchronizing signal. The frequency-divider circuit which accomplishes this phase lock has been found to be very reliable even though it makes use of diodes whose characteristics are far from ideal.

• d) *Tests on system reliability*

The system has been tested for reliability. The details of the tests which had been completed at the writing of this paper are given below.

The adjustments in the system were optimized, and all weak components were replaced. The system was then run continuously on six successive days for periods of

*Figure 22* **Viewing equipment.**
*The vertical sensitivity using a Tektronix Type 535 oscilloscope is 2½ volts per millimeter. The input admittance is that of a capacitor of 3μμf shunted by a resistor of 12 megohms.*



from six to ten hours, performing a different multiplication on each day. The tests were run with the arithmetic unit operating on a multiplication program with a 10-kilocycle repetition rate. This represents $3.6 \times 10^7$ multiplications per hour and approximately $10^{10}$ storage circulations in the accumulator register per hour.

The average period of error-free operation during this six-day test was found to be four hours. This represents, on the average, $1.44 \times 10^8$ error-free multiplications and $4 \times 10^{10}$ error-free storage circulations in the accumulator register. On two days no errors occurred; on one of them the system performed the multiplication program illustrated above ($10111 \times 11011$) and had not made any errors when it was shut down at the end of a ten-hour period. The gain in the accumulator-register storage loop was adjusted slightly after three days of operation because the storage of eight consecutive pulses was becoming marginal.

Although these results show that the system is capable of very reliable operation, it should be emphasized that the operating margins, particularly in the adder and the accumulator register, are not large. The adder, primarily because of the dc-restoration problem, has to be carefully adjusted if the system is to perform any one of the possible multiplication programs. In the dynamic-accumulator-register loop, which consists of the accumulator-reshaper, the storage delay line and the adder "straight-through" path, there are seven EFP-60 limiter amplifiers, a diode 3-way OR circuit, two delay lines and a reshaping network, so that it is quite sensitive to changes in characteristics of the secondary-emission tubes.

## 6. Conclusions

Millimicrosecond pulse techniques were first investigated and developed by workers in the field of nuclear instrumentation, and since that time a great deal of literature has become available on the subject. This literature deals mainly with individual circuits, and to a large extent with the variety of multivibrator circuits which can be built with the EFP-60 secondary emission tube. The experimental project which is described in this paper took these techniques as its starting point.

The results presented in this paper add to and extend these techniques and furthermore show that they may be applied to large-scale digital systems with a reasonable expectation of reliable operation. More important though, they show that it is possible to perform diode logic at pulse repetition rates far in excess of those which are usually used. A great deal of work still remains to be done in the field, however, both in circuit design and on obtaining new and better components. While there is very little doubt that better diodes could be developed for work at these speeds, there do not seem to be any tubes available or under development at present which are better suited to this work than the EFP-60 secondary emission tube. The development of really high-speed transistors seems to offer the only possibility of obtaining a component which will offer an improvement over this tube.

The application of the arithmetic system described in this paper to computing problems would be very much dependent on the nature of the problem. It is entirely possible that it could be useful in applications where extreme speeds are needed and can be paid for in terms of increased cost and power consumption.

## Appendix: Quasi-stable operating point of the plate-cathode-coupled multivibrator

When the EFP-60 plate-cathode-coupled monostable multivibrator is triggered, the cathode and plate voltages drop until, because of nonlinearities in the tube characteristics, the gain falls below unity and the following equation is satisfied:

$$i_p = i_{R_L} + i_K = i_{R_L} + (i_p - i_d) + i_g, \qquad (1)$$

where $i_{R_L}$ and $i_K$ are the currents in the plate load resistor and the feedback capacitor, respectively. This equation can be solved if the plate and grid characteristics of the tube for positive grid bias are known. These may be approximated as follows:

When the EFP-60 with a plate and screen voltage of +275v and a dynode voltage of +150v is driven to positive grid bias, the grid-to-plate transconductance decreases (the plate current being about 100 ma and increasing only slightly with a further increase of grid voltage), the dynode current falls off slightly, and the cathode current increases linearly with a transconductance (under pulsed conditions) of approximately 10 ma/volt. In the negative bias region, the grid-to-cathode transconductance is approximately 8 ma/volt so that for positive grid bias the grid-to-cathode circuit may be represented approximately by a 500Ω resistor.

Equation (1) then becomes, to an approximation:

$$100 = \frac{\Delta E_1}{0.390} + 8(E_{cc}) + 10(\Delta E_1 - E_{cc}), \qquad (A)$$

where $\Delta E_1$ is the initial plate swing (Fig. 5), and the grid bias is $-E_{cc} = -4$v.

Substituting $E_{cc} = 4$ volts in equation A, we find $\Delta E_1 = 8.5$ volts. Hence $E_{gk} = \Delta E_1 - E_{cc} = +4.5$ volts. This agrees with observed voltages.

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