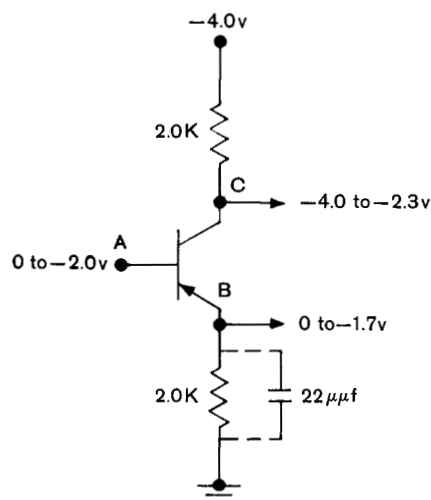


J. L. Walsh

A Symmetrical-Transistor Steering Circuit*

Figure 1 Waveforms for conventional phase inverter.



A bilateral transistor phase-inverter has application in digital computer switching circuits. In the circuit shown in Fig. 1, the emitter and collector load are equal; and when the input is at zero, the transistor is virtually cut off, leaving the collector and emitter at -4.0 and 0 volts, respectively. If an input of -2.0 volts were applied to the base from some voltage source, then the emitter potential would drop from 0 to -2.0 volts (less the drop across the emitter base diode). The drop across the 2.0 K emitter load resistor would fix the current flowing into the emitter, and the collector potential would rise from -4.0 volts to some value determined by αI_e and the 2.0 K collector load resistor. Since α in a junction transistor is close to unity, one would expect the collector to rise to a value close to -2.0 volts. The transistor is now close to saturation. If the base input were made more negative, the collector potential would attempt to rise above the base input level and collector clamping or saturation would occur. In short, for an input-voltage swing less than that which would cause saturation, the emitter and collector outputs are close to being equal, differing only by the variation caused by α being less than unity. When the transistor is driven into saturation, the collector output is much smaller, being limited to the difference in the collector supply voltage and the base input. Some pic-

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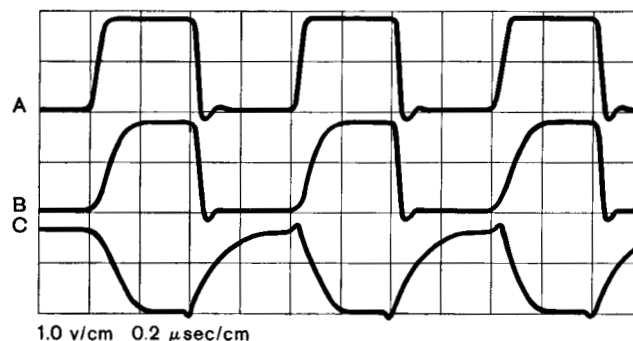


Fig. 1(a) A Input from pulse generator
B Output at emitter
C Output at collector

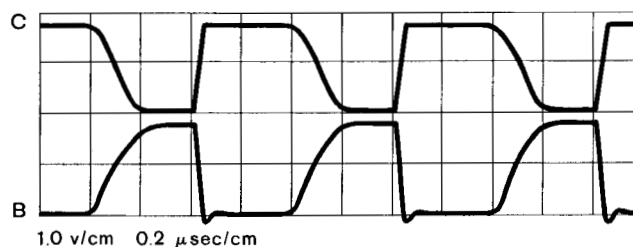


Fig. 1(b) C Output at collector with overdrive capacitor
B Output at emitter with overdrive capacitor

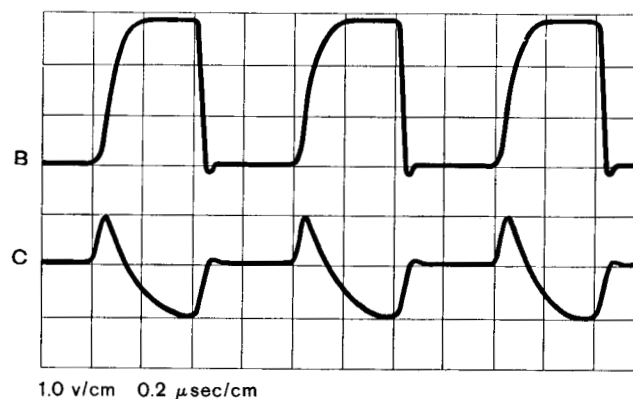


Fig. 1(c) B Output at emitter for 3.0v input
C Output at collector

tures of the response of the circuit are shown in Figure 1. Note, in Figs. 1(a) and 1(b), that the transistor is not driven into saturation. In Fig. 1(c), the input signal has been increased to -3.0 volts. A full output is obtained at the emitter, but the collector output is limited by saturation to the difference between the -4.0 volt power supply and the -3.0 volt input, approximately 1.0 volt. Note the large positive spike coupled through from emitter to collector during the time the transistor is in saturation but after the positive turn-off pulse has been applied.

The circuit, as it has been shown, is well known and commonly used. An interesting variation is possible due to the symmetrical nature of the junction transistor. If by some external means the collector and emitter power supplies were interchanged, the normal emitter would become a collector and the normal collector an emitter. Then, if the transistor were perfectly symmetrical, that is, normal α and normal ω equal to inverted α and inverted ω , one would expect no difference in the response of the circuit. Many commercially available transistors exhibit good inverted properties. An example is shown in Fig. 2.

One simple application of the bilateral phase inverter can be made in triggering the conventional Eccles-Jordan flip-flop shown in Fig. 3. In the circuit shown, the phase-inverter load resistors are returned to the collectors of

the flip-flop. Depending on the state of the flip-flop, the phase inverter will have its normal collector returned to -4.0 volts (cut-off side of flip-flop) or to approximately -0.03 volts (saturation drop across the "on"-side transistor). Application of a negative input from some voltage source to the base of the phase inverter will produce a positive-going output at the reversed biased junction of the phase inverter and a negative-going output at the forward biased junction. These output signals pass through the $33 \mu\mu\text{f}$ coupling condensers to the bases of the flip-flop and simultaneously turn off the "on" side of the flip-flop and turn on the "off" side. The phase-inverter load resistors act to sense the condition of the flip-flop and to steer the correct polarity pulses to the flip-flop bases. The circuit takes advantage of the bilateral nature of the junction transistor in that each junction of the input transistor will alternately serve as an emitter or a collector for successive input pulses. In this particular flip-flop, overdrive capacitors could be eliminated because of the simultaneous-triggering feature of the input circuit. The absence of the overdrive capacitor would tend to increase the rise time slightly but significantly improves the fall time. Such an arrangement results in a more symmetrical output, that is, an output of more equal rise and fall time. Waveforms of the circuit are shown in Fig. 3.

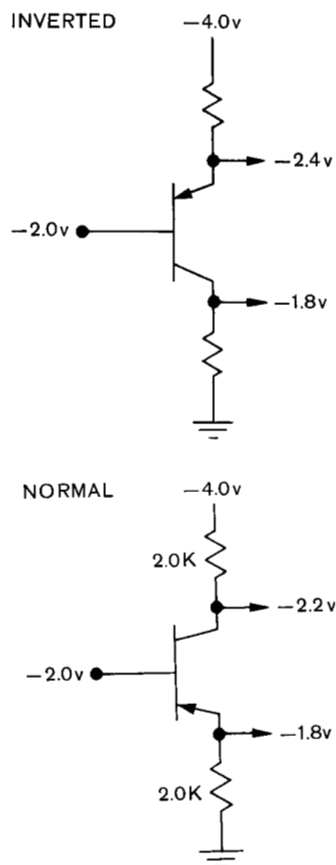
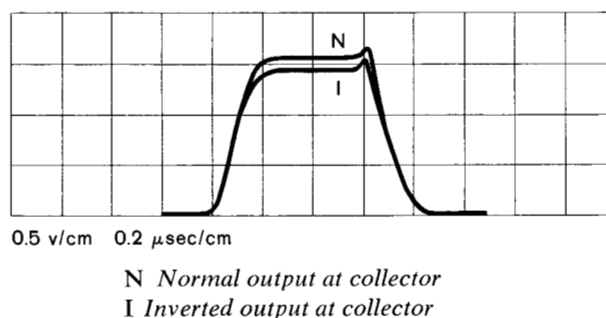


Figure 2 Output of phase inverter.



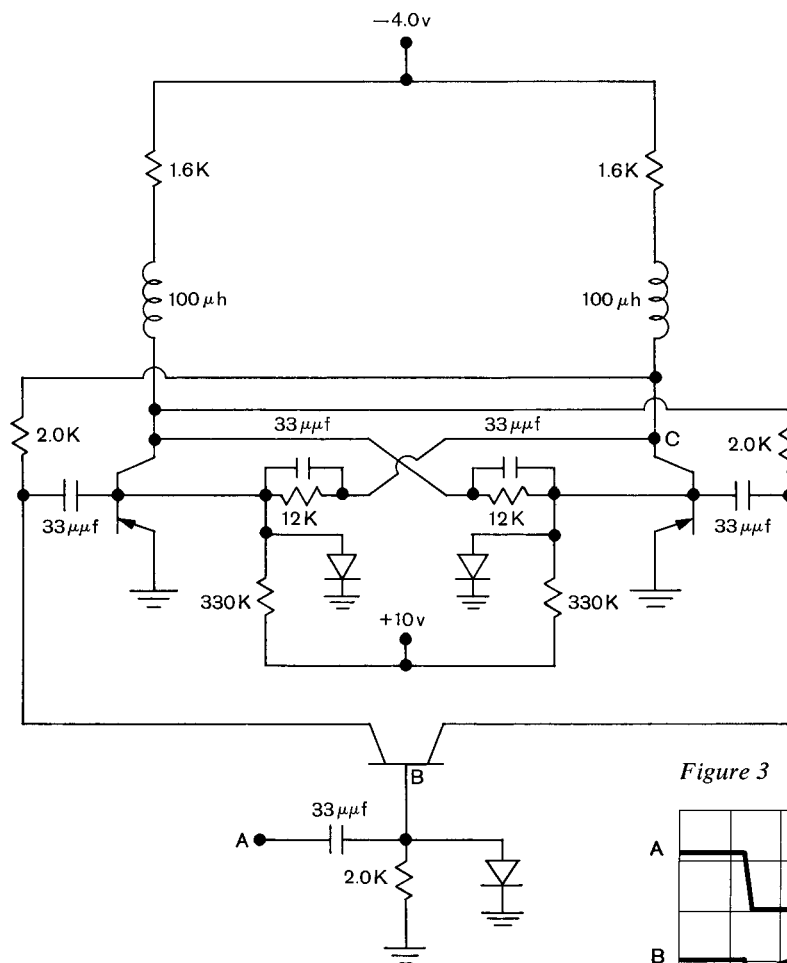
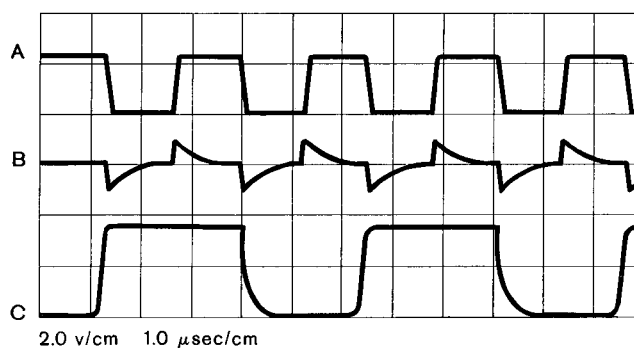


Figure 3 Binary Eccles-Jordan flip-flop.



A Input
B Input at base of symmetrical transistor
C Output at collector

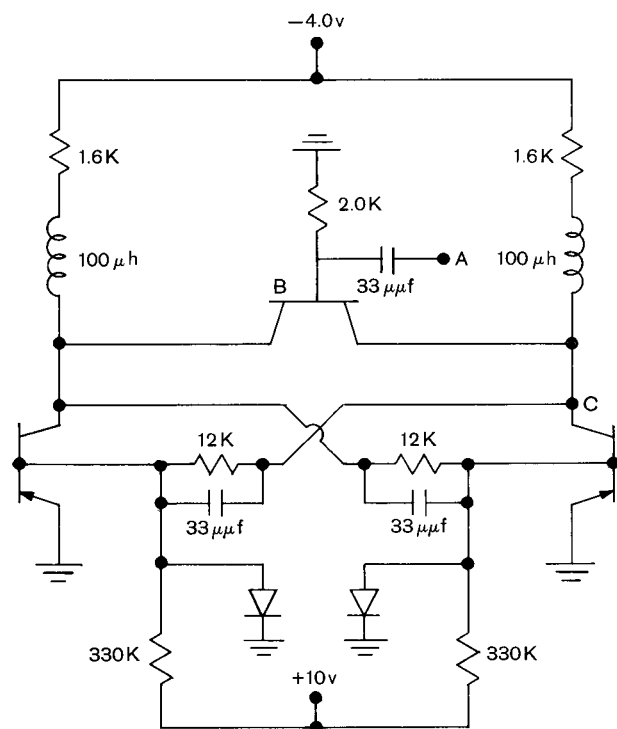
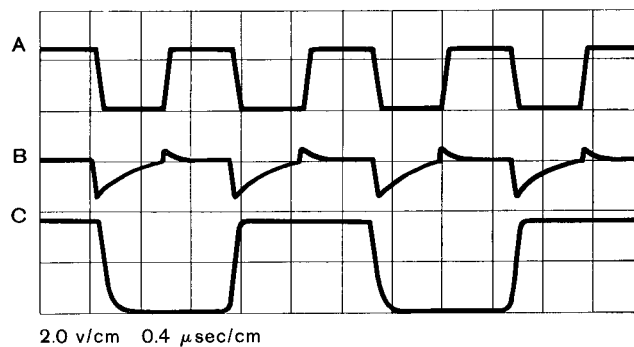


Figure 4 Binary Eccles-Jordan flip-flop.



A Input
B Input at base of symmetrical transistor
C Output at collector

CLOSED RING

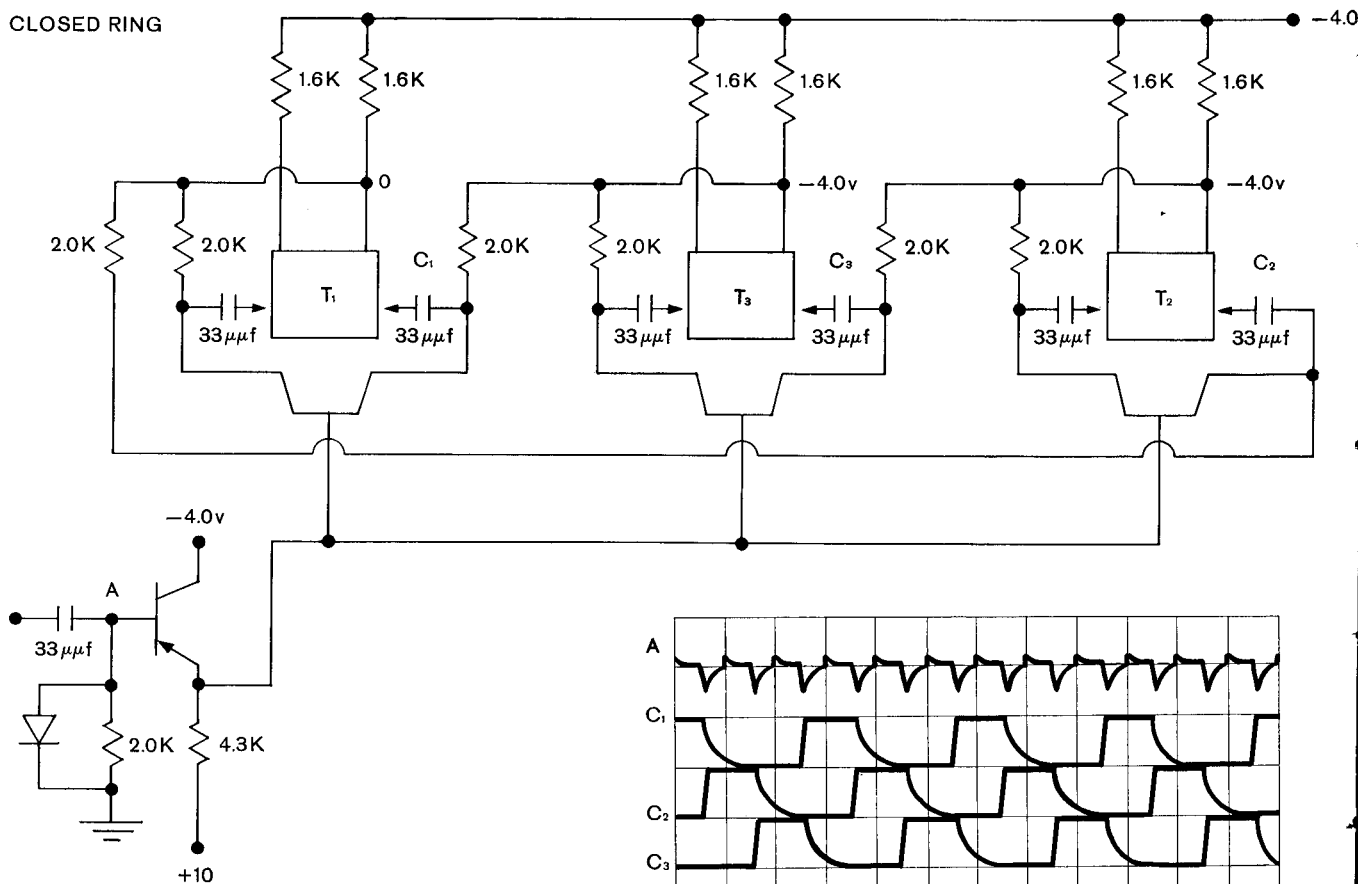


Figure 5 Ring counter.

In another arrangement due to J. C. Logue,* the symmetrical transistor is tied directly between collectors, as shown in Fig. 4. In this arrangement, application of a negative input will divert current from the "on" side of the flip-flop to the "off" side through the symmetrical transistor. As in the previous arrangement, application of successive input pulses causes the normal emitter and collector junctions to reverse their roles, being alternately emitter or collector, depending on the state of the flip-flop. Waveforms are shown in Fig. 4.

This type of circuit might find application in rings, counters, shifting registers, or any system composed largely of flip-flops. One possible small system is the closed ring shown in Fig. 5. As shown here, only three stages are used. This is not a restriction and more could be added if desired. Initially, the first stage is "on" and the others are "off". Gates 1 and 2 are conditioned, but gate 3 is deconditioned; that is, its load resistors are both returned to -4.0 volts (off sides of T_2 and T_3). The first input pulse turns off T_1 and turns on T_2 , and the

second input pulse turns off T_2 and turns on T_3 . The third input pulse completes the cycle, turning off T_3 and turning on T_1 . Waveforms of the ring are shown in Fig. 5. In this particular ring, the simultaneous triggering feature of the input circuit is retained. The parameters of the trigger are the same as those shown in previous figures.

Conclusions

1. The greatest advantage of the circuit as far as binary triggering is concerned seems to be that simultaneous triggering at both bases can be used. This reduces the regeneration time in the flip-flop.
2. The circuit is quite sensitive to changes in input level. This can be overcome by application of a bias at the input which is greater than the anticipated noise level.
3. The symmetrical circuit finds application wherever flip-flops are used, including rings, counters and shifting registers.

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