L. D. Seader

A Self-Clocking System for Information Transfer

Summary

This paper describes a circuit which generates a continuous train of clock pulses bearing a fixed phase relationship to information pulses. By switching two gated oscillators, the information pulses continuously correct the phase of the clock pulses.

Introduction

In digital data-storage and transfer systems, a clock signal is required in order to detect the absence or presence of information bits. The clock signal is merely a train of pulses of uniform spacing which has a fixed phase relationship with the information bits. Coincidence between a clock pulse and an information pulse indicates a "one" bit while anti-coincidence indicates a "zero" bit for the bit slot corresponding to that particular clock pulse.

In some synchronous systems, such as a magnetic-drum storage system, it is possible to generate the clock signal so that it inherently maintains the proper phase relationship with respect to the information bits. In some asynchronous systems, such as a magnetic-core storage system, the phase and frequency of the information bits is determined by an independently generated clock signal. In addition, however, there are some systems where it is either inconvenient or impossible to use an independently generated clock signal. These systems require that the clock signal be derived from the information bits. The purpose of this report is to present a method of deriving clock pulses from information bits which has proved to be both simple and reliable. The circuit is called a phased clock-pulse generator.

Block diagram description

A block diagram of the circuit is shown in Fig. 1 and the idealized waveforms are shown in Fig. 3. A binary corrected trigger is driven by the information pulses so that every time a pulse is received, the trigger changes status. The two outputs of the trigger are used to gate two oscillators such that one oscillator is on and the other oscillator is off. An incoming information pulse reverses conditions and the oscillator which was previously on is turned off and vice versa. The oscillators are of a type which start with a known phase so that phase correction is inherent in the switching of the oscillators. The outputs of the two oscillators are mixed in an "or" circuit to provide a continuous train of clock pulses, and the overdriven amplifier serves to square up the half-sinusoidal output of the "or" circuit. The output of the circuit, then, is a continuous train of square clock pulses which maintain a fixed-phase relationship with the information pulses.

Detailed circuit description

The phased clock-pulse generator was originally developed to overcome certain clock-phasing problems associated with the IBM random-access memory. Because of the mechanical tolerances in the access mechanism a proper phase relationship between the data and a recorded clock track could not be maintained over long periods.

Figure 2 is a detailed circuit diagram of the phased clock-pulse generator as it is used in the RAMAC 305 computer in conjunction with the random-access memory. The circuits are designed for a nominal clock frequency of 80 kc. NRZI recording is used.

Figure 1 **Block diagram of the circuit.**

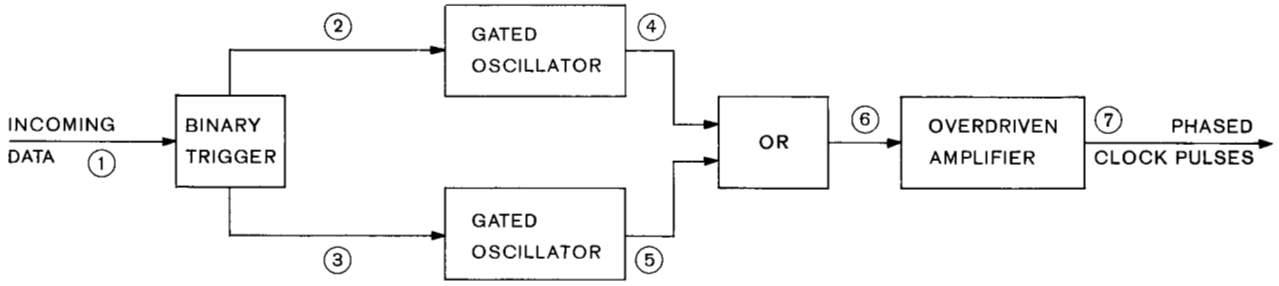
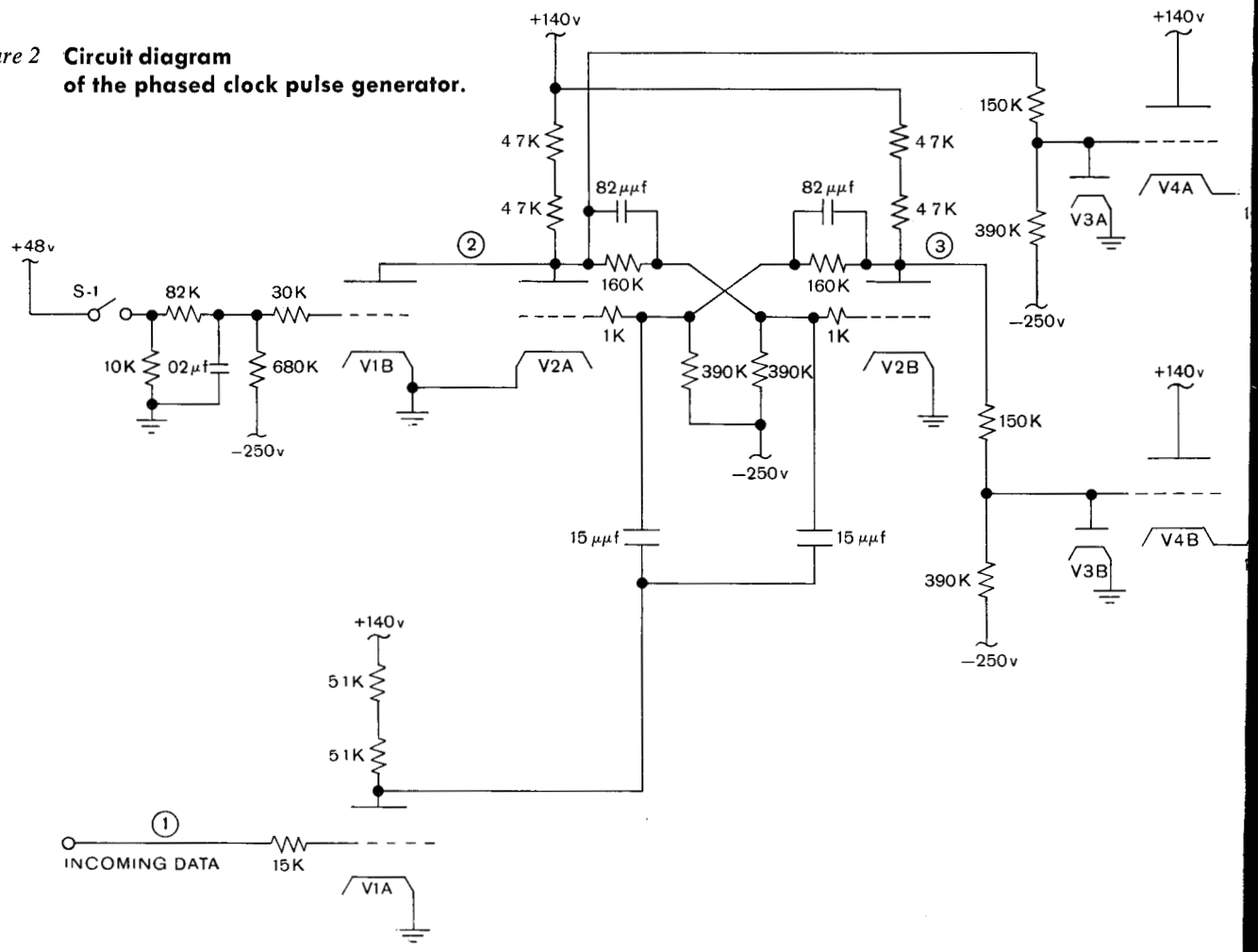


Figure 2 **Circuit diagram of the phased clock pulse generator.**



Reading

For reading information out of the memory relay point $S-1$ is open. V1B is, therefore, cut off and does not affect the operation of the trigger. Incoming data pulses are inverted by V1A and fed to the binary-connected trigger so that the trigger changes states with the leading edge of each data pulse. The trigger is a standard Eccles-Jordan type with capacitive-coupled triggering. Each plate of the trigger is d-c coupled to a gated Hartley oscillator. V4A and V4B provide the gating functions for the two oscillators while V5A and V5B provide low-impedance outputs and supply energy to the tank circuits to sustain oscillation. The initial amplitude of oscillation depends upon the L/C ratio of the tank circuit and the cathode current of the gating tube (V4) just before the tube is cut off. The relationship is given by the equation

$$V = 2I\sqrt{\frac{L}{C}}\,, \qquad (1)$$

where I is the cathode current of V4, V is peak-peak initial amplitude of oscillation.

The outputs of the two oscillators are mixed in a negative "or" circuit consisting of V6A and V6B. A negative "or" circuit is used since the gated Hartley oscillator starts in a negative-going direction. The voltage level of the "off" oscillator is such that the "or" circuit clips off the positive half of the signal. The capacitor shunting the load resistor of the "or" circuit allows a certain control over the symmetry of the clock signal by smearing the positive going edge of the half-sinusoid and thereby changing the width of the clock pulses. The half-sinusoidal signal is squared up by the overdriven amplifier consisting of V7A and V7B.

Writing

For writing information into the memory, a continuous train of clock pulses is required. This is obtained by closing relay point $S-1$. V1B, then, conducts and clamps the trigger to the state in which V2A is conducting and V2B is cut off. The clamp renders the trigger immune to any impulses from V1A. The grid voltage of V4A is about -35 volts while the grid voltage of V4B is 0 volts. Under these conditions, the Hartley oscillator associated with V5A is allowed to oscillate while the oscillator associated with V5B is highly damped and produces no signal. Sufficient feedback is provided in the Hartley oscillator for the amplitude of oscillation to build up to the point where

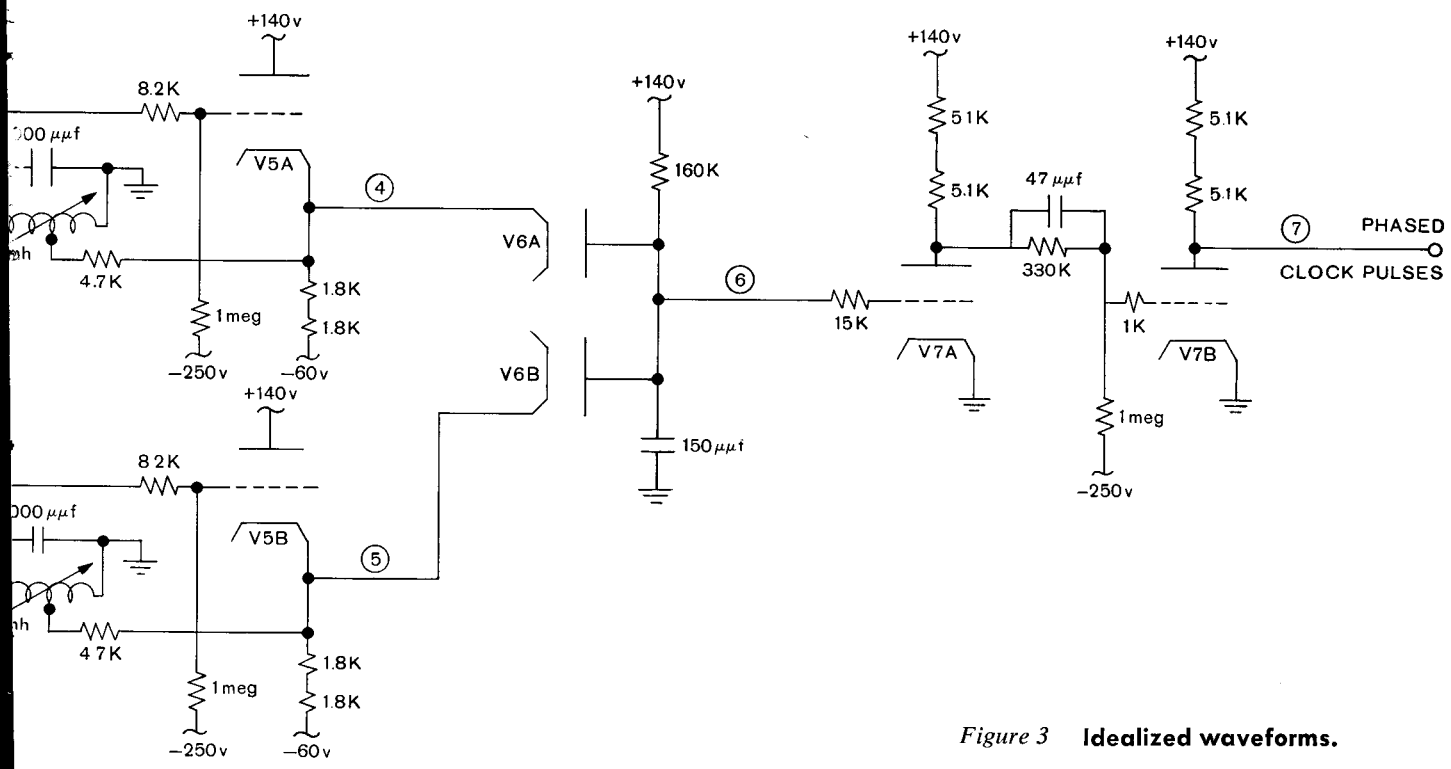
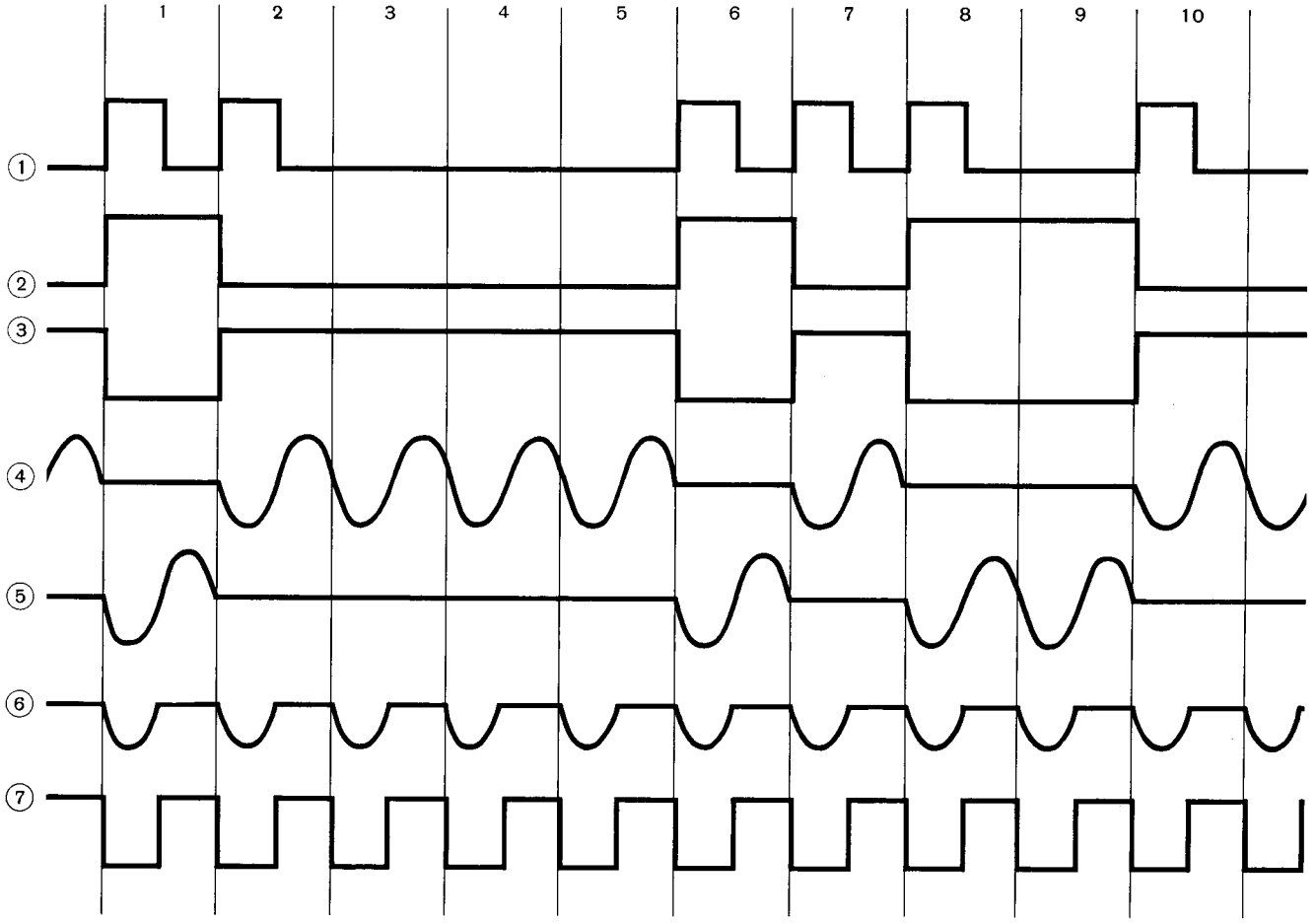


Figure 3 **Idealized waveforms.**



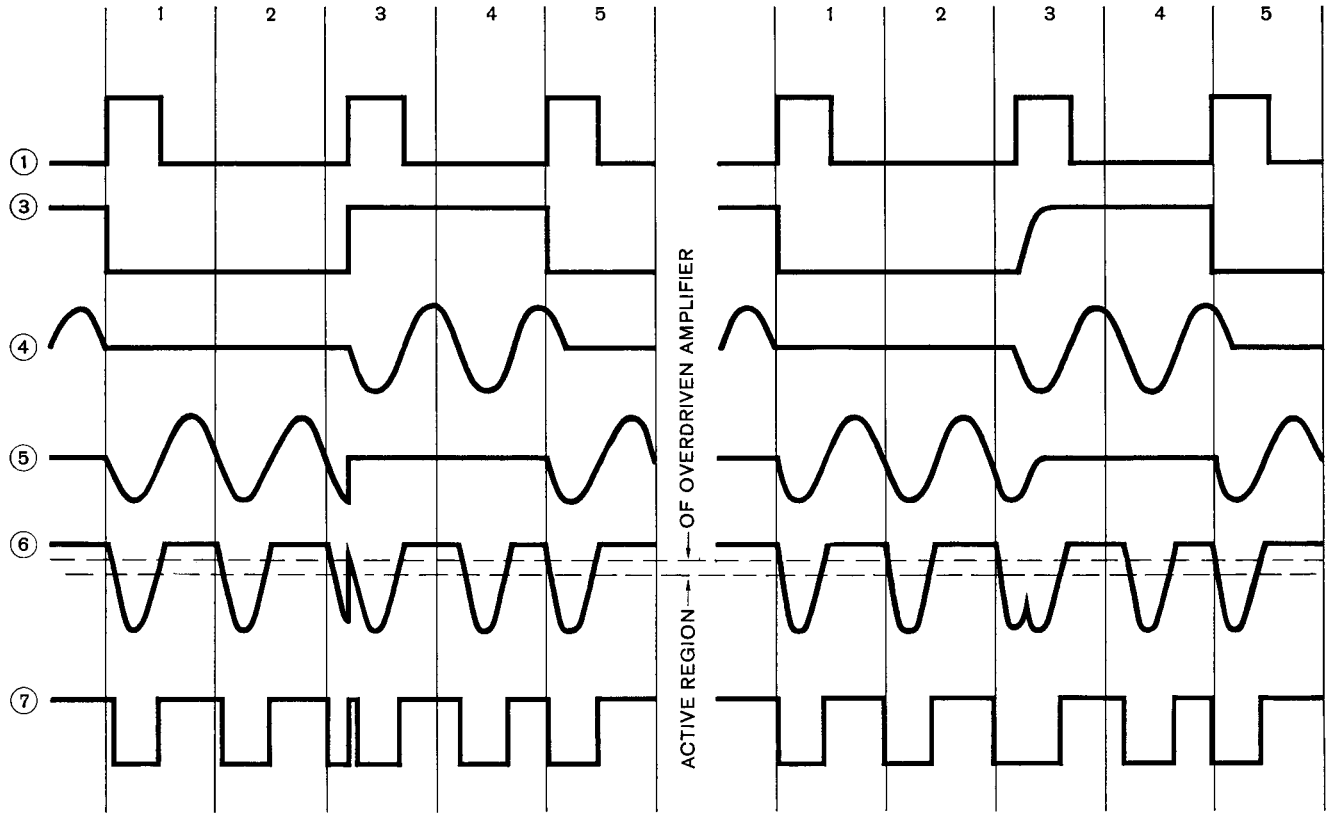


Figure 4 **Sliver elimination.**

V4A will conduct on the negative peaks and limit the buildup. The feedback is not so great, however, that any appreciable distortion occurs from the limiting action.

Special considerations

Figure 4 illustrates two special considerations which must be taken into account in the design and application of the PCPG. Both of these considerations arise from the fact that individual data pulses may be out of phase with respect to adjacent pulses.

In the left half of Fig. 4, it will be noted that the data pulse in slot 3 is lagging in phase. As a result of this, oscillator (5) generates an extra fraction of a cycle which operates the overdriven amplifier. Assuming the ideal waveshape shown at (3), oscillator (5) is abruptly shut off at the leading edge of the data pulse while oscillator (4) is turned on and starts down at a sinusoidal rate. It is seen, therefore, that a sliver will be generated equal in width to the time it takes oscillator (4) to get through the active region of the overdriven amplifier.

The solution to the sliver problem is shown in the right half of Fig. 4. By slowing down the rise time of the waveform at (3) so that oscillator (4) crosses the active region before oscillator (5) recrosses the active region the sliver is eliminated. In the circuit of Fig. 2, the rise time of the trigger is inherently poor with respect to the fall time because of the 82 $\mu\mu$f compensating capacitors.

The second special consideration is seen in the waveform of (7) in the right half of Fig. 4. It will be noted that when a data pulse is out of phase the negative going edge of the clock pulse bears no fixed relationship to the leading edge of the data pulse, but the positive going edge always occurs half a bit time after the leading edge of the data pulse. Any data standardizing system using the PCPG must take this fact into account for reliable operation.

While the PCPG will tolerate rather large phase errors in individual data bits, the long-term data rate must be held quite accurately, depending upon the maximum number of cycles which may occur in the system between data pulses. The relationship is given by the equation

$$\frac{\triangle f_{max}}{f} = \frac{.5}{N} \qquad (2)$$

where $\triangle f$ is the difference in frequency of oscillators and data, N is the maximum number of cycles between data pulses.

This is a theoretical limit and a safety factor should be employed to take into account short-term phase errors and finite rise and fall times of the circuits. When properly designed and applied, the PCPG has resulted in reliability and simplicity previously unattainable.

Received January 15, 1957