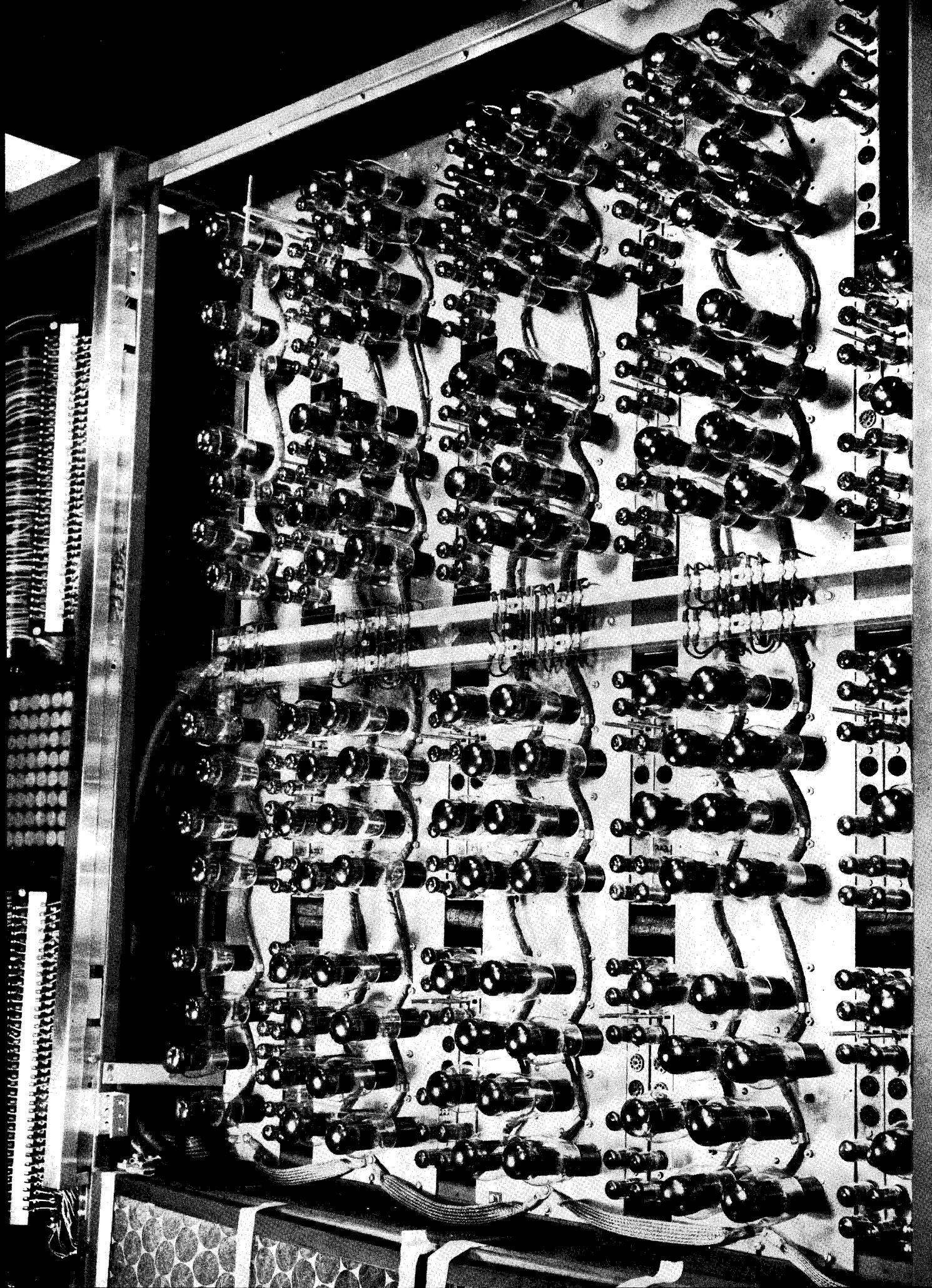




A 32,000-Word Magnetic-Core Memory

Abstract: The development of the IBM 738 magnetic core storage unit is described and associated engineering problems are discussed, including the electrical and mechanical arrangements for packaging more than one million magnetic cores and their circuits. This paper describes the driver circuits and the sense amplifier used for this system.

Introduction

Scientific and engineering computing applications on IBM 704 and 709 Data Processing Machines have pointed out a need for a larger, high-speed memory system. As a result of this need, a program was undertaken in the latter part of 1955 to develop a magnetic-core memory that would have 32,768 thirty-six-bit words of storage, eight times the existing basic memory capacity, with random access to all word addresses, and with a read-write cycle of 12 microseconds.

This memory has been designated the IBM 738 Magnetic-Core Storage Unit. The memory array size is 128 by 256 by 36 ferrite cores, which are operated in coincident current fashion and driven by switch core matrices of the anti-coincident type.

The major engineering problems that were encountered were those of driving a large array with the increased back voltages generated, minimizing delay effects which become more severe as the number of cores increases, and solving the electrical and mechanical problems of packaging 1,179,648 magnetic cores and their associated circuits in a workable and reproducible form.

Machine organization

A logical block diagram of the magnetic-core storage unit is shown in Fig. 2. The address register is used to store the address being selected by the calculator. The address decoders subdivide the 15-binary-bit address appearing in the address register into 42 lines which feed the switch core matrices and digit plane selection circuits. The wave-

form generator accepts basic timing pulses from the calculator and incorporates these into gates. These gates, along with control pulses shown in Fig. 3, control the operation of the memory. Figure 3 also shows the memory drive current waveforms and the waveform on the storage output bus. The sense amplifiers accept the small amplitude signals from the sense winding in the core array, amplify, time sample, and drive the signals to the buffer register. The buffer register and input-output switching circuits control the information flow from the computer into core storage and from storage back to the computer. The test circuits will be explained in subsequent sections.

Machine packaging

The physical layout of the machine is shown in Fig. 4. The circuits in the section labeled "logic" are packaged in eight-tube pluggable units and contain the address decoding, the memory waveform generator, the buffer register, the address register, driver selection circuits, and test circuitry which is controlled at the C. E. (Customer Engineer) panel. Directly beneath the C. E. panel is a power supply which furnishes the special voltages necessary for the transistor sense-amplifier circuits. This has been packaged as a hinged gate.

Packaging was one of the major problems encountered in the design of the core storage unit. Several layouts were considered and studied, the primary objective being to minimize cable lengths which interconnect the logic, drivers, core array, and sense amplifiers.

As is often the case in machine design, ideal cable length could not be realized because of other important factors, such as ease of access for maintenance and ease

Figure 1 The driver frame

The large core-driver vacuum tubes are on panels along with eight-tube pluggable units.

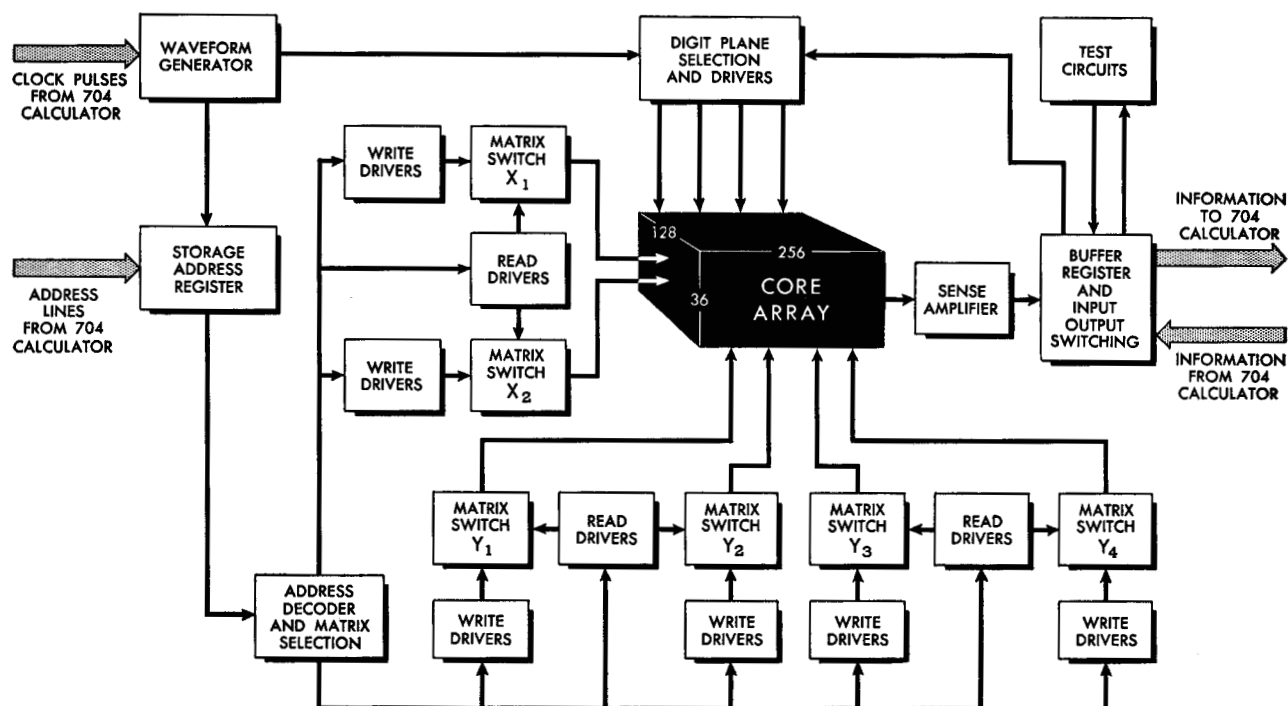


Figure 2 Logical block diagram
of the IBM 738 magnetic-core storage unit.

of disassembly for shipment. However, taking these factors into consideration, a layout was achieved which allowed reasonably short cables where necessary.

The two driver frames, each of which contains half of the drivers and half of the memory array, are arranged so that no coaxial cables are required between them. The only connections between them are two crossover planes, each containing 128 wires, one across the top and another across the bottom of the open area between frames, as shown in Fig. 5.

The driver circuit used is a current feed-back amplifier similar to that used in existing IBM memories. As shown in Fig. 1, the large core-driver vacuum tubes are on panels along with eight-tube pluggable units. These pluggable units contain the driver amplifiers. This method of packaging places the driver amplifier as close to the driver tube as possible, thereby decreasing the number of coaxial lines by 50% below that of previous designs. This arrangement was chosen primarily to insure maximum stability in the feed-back amplifier circuit.

Although the driver tubes and their associated circuits are panel mounted and the feed-back amplifier circuitry is packaged in pluggable units, all tube sockets are in the same plane for ease of cooling. All components are accessible for testing without the necessity of using a pluggable-unit extender, as is normally the case with pluggable construction.

The array was divided into two sections for a number of reasons. The primary governing factor was the selec-

tion of 64 by 128 for the physical plane size, shown in Fig. 6. This size represents a compromise between smaller planes where the number of solder connections in the array would be undesirably large, and a full logical plane of 128 by 256 where problems of quantity production would be greater. The size chosen was influenced to some extent by its adaptability to other memory applications in IBM. Two groups of planes were necessary in order to provide access to three sides of each plane for removal from the array. Another reason was that it is desirable to keep the lines from drivers to the array as short as possible. As can be seen in Fig. 5 the Y_1 , Y_2 , and X_1 , switch core matrices which are in the left frame are driven from the left drivers, while the Y_3 , Y_4 , and X_2 switch core matrices which are in the right frame are driven from the right drivers. The switch core matrices were inserted in the center of the two halves of the memory array for reasons which may be seen by referring to Fig. 5. The sections of the array have been termed "quadrants." The secondaries of the switch cores in the Y_1 matrix are all connected down to the first quadrant of the array. The secondaries of the Y_2 matrix are all connected up to the second quadrant. The secondaries of the X matrices are connected through all four quadrants. This is accomplished through the use of the crossover planes. The dotted lines in Fig. 5 show the thirty-six-bit word which would be selected if the switch core shown in the X_1 matrix and the switch core shown in the Y_3 matrix were addressed. In order to minimize space requirements, transistors mounted on etched wiring cards were utilized for the sense amplifiers. The cards plug into a group of sockets in the logic frame.

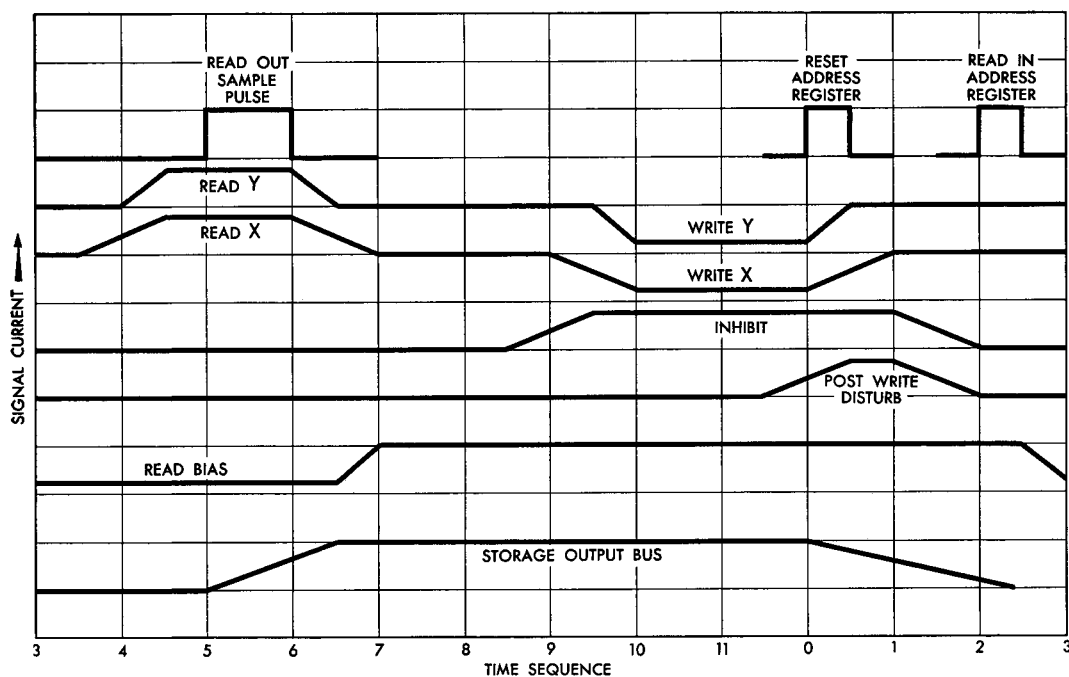


Figure 3

Figure 3 **Machine timing chart** showing the control pulses and the memory drive current waveforms.

Figure 4 **Physical layout of the IBM 738**
A: drivers; B: logic; C: core array; D: sense amplifier; E: C.E. panel; F: power supply.

Figure 5 **Diagram of core array**
The two driver frames are arranged so that no coaxial cables are required between them.

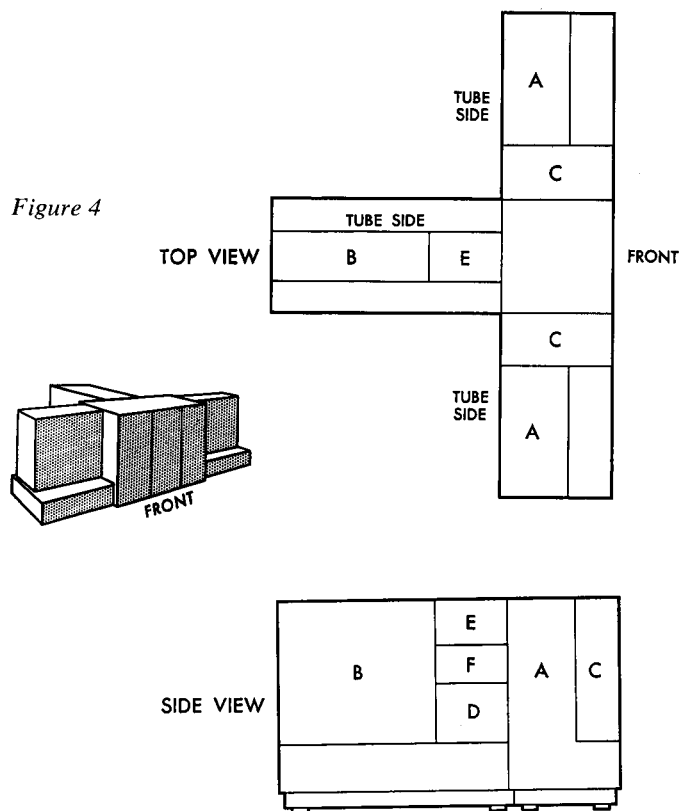
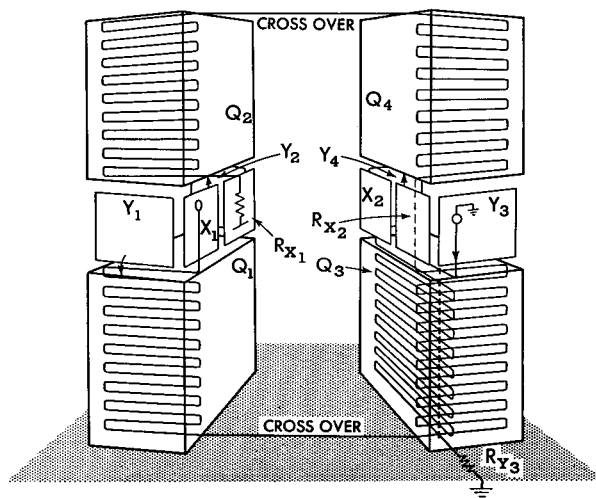


Figure 5



Driving problems

As mentioned earlier, the array contains 1,179,648 cores, or 32,768 thirty-six-bit words. There are 128 address lines in the X direction and 256 address lines in the Y direction. This means that there are 128 by 36, or 4608 cores in the secondary of each Y switch core and twice that many for each X switch core. The vacuum tube selected as a driver was Type 5998, a low-gain, twin power triode. An 8 by 16 switch core matrix was investigated and rejected on the basis that to drive the 16 switch cores required either the use of a voltage in excess of the tube rating or the use of two tubes in parallel for each line.

Two tubes used in parallel would allow more current to be switched, so that a 2-to-1 current step-down switch core could have been used. If it is assumed that this current step-down switch core would result in a voltage step-down from secondary to primary of 2 to 1, then the back voltages appearing at the primaries of the switching and non-switching switch cores would be reduced sufficiently to allow a lower plate voltage to be used for the drivers. With the given array, a selected switch core (with 9216 memory cores in its secondary and a pulse with a 1 microsecond rise of proper magnitude) will have appearing across its primary a pulse of approximately 45 volts. The non-selected switch cores in the same line each will generate back voltages of about 10 volts. This back voltage can be decreased if a 2-to-1 current step-down switch core is used, but it was found from experience that this 10 volts was reduced only to about 8 volts and, although this allowed the plate voltage to be reduced somewhat, the reduction was still not sufficient to keep within the ratings of the tube when 16 switch cores were being driven. Because of the time cycle involved, the current necessary, and the wattage rating of the Type 5998, 160 volts is the maximum that should be used for the tube plate supply. Since the drop across the tube is about 40 volts when conducting and since there is about 20 volts drop across the load resistor, 100 volts is left for the switch cores. This voltage limited the number of switch cores in series to about eight, and therefore limited X and Y matrices to 8 by 8 switch cores.

As can be seen in the timing chart of Fig. 3 the X drive currents were allowed to rise in one microsecond, while the Y drive current was expected to rise in one-half microsecond. The half-microsecond rise of Y current was specified in order to insure a signal on the sense winding of sufficient magnitude at *read* time. This current rise time was possible on the Y lines since only 4608 cores were linked per line. Without radical changes of supply voltages or driving circuitry, the same speed was not possible in the X lines, where 9216 cores are linked. This problem was solved by allowing the X drive current to start up a half microsecond before the Y drive current

and by allowing one microsecond for the X current to rise.

A complete scattering of the memory addresses was considered necessary to reduce as much as possible the effect caused by mutual inductive coupling between adjacent memory lines.

In smaller IBM core memories, the wires from the switch core matrix to the array are wired consecutively from the series strings of switch cores in the *read* direction or the *write* direction of a switch core matrix to the array. Either may be undesirable in a very large array. Consider the case of consecutively wiring to an array from a series of switch cores which all receive the same *write* current, calling this an X switch core matrix. Assume a particular memory core is selected. The memory core which is on the same Y line as the selected core and on the X memory line adjacent to the core selected can receive enough current in addition to the half select current to make it partially switch from a "zero" to a "one." This particular core receives about 400 ma from the selected Y line and receives about 100 ma from the X switch core which is in the same series string as the selected switch core, but in addition may also receive as much as 50 ma of mutually induced current from the adjacent X line. These three currents add and may drive these non-selected memory cores with enough current to switch them partially. This may make them appear to have been storing a "one" instead of a "zero" when they are next interrogated. With the system of address scattering used on the IBM 738, there is never a case where adjacent memory lines are connected to the same series string of switch cores in either the *read* or *write* direction.

A memory array exhibits characteristics of a delay line. The delay in establishing a full half select current between the first and the last cores in a string of 8192 cores is in the neighborhood of 0.2 to 0.3 microsecond. In order to minimize this delay effect, the inhibit winding was divided into four independently driven sections.

The sense winding is similarly divided. Eight independent sense windings of 4096 cores each are connected to independent pulse transformers in the sense amplifier.

Sense amplifier

The sense-amplifier circuit for the IBM 738 is of the type in which the signals are fed through a pulse transformer and then rectified before being amplified. One etched-wiring card will amplify the signals from one-half of a sense plane, or approximately 16,000 cores. The input circuit to each of the four transformers per card contain 4096 cores. As shown in Fig. 7, each transformer has a diode connected to each of its outside secondary leads. The signals from two transformers are coupled by connecting the four rectifying diodes to a common load to form an OR circuit. This signal is then applied to one emitter follower of a two-emitter-follower OR circuit, the other emitter follower receiving a signal from the other two transformers. The signal appearing at the output of this OR circuit is then amplified with a class

Figure 6 The core plane

The plane size selected for this array was
64 × 128 cores.

"A" transistor stage and then re-amplified and sampled with a combination class "C" amplifier and sampling stage. The last stage is an emitter follower to power the lines carrying this output pulse to the buffer register. Two output emitter followers are connected together to form an OR circuit in order to pick up a full 32,768 cores for each of the 36 output lines. The transistor card also contains a circuit for shaping and powering the sample pulse used in the last amplifier stage.

Recovery problems were encountered in the design of this amplifier. As can be seen in Fig. 3, the signal pulse which will occur at about the time marked "5" at the top of the chart, is preceded by the "inhibit" and "post-write disturb" pulses. The magnitude of the noise received at the input to the sense amplifier due to these two pulses may be as high as 1 volt, whereas, the circuit is designed to amplify a signal pulse of from 65 to 150 millivolts. The circuit must recover from the 1-volt noise pulse before the signal can be amplified. Proper recovery

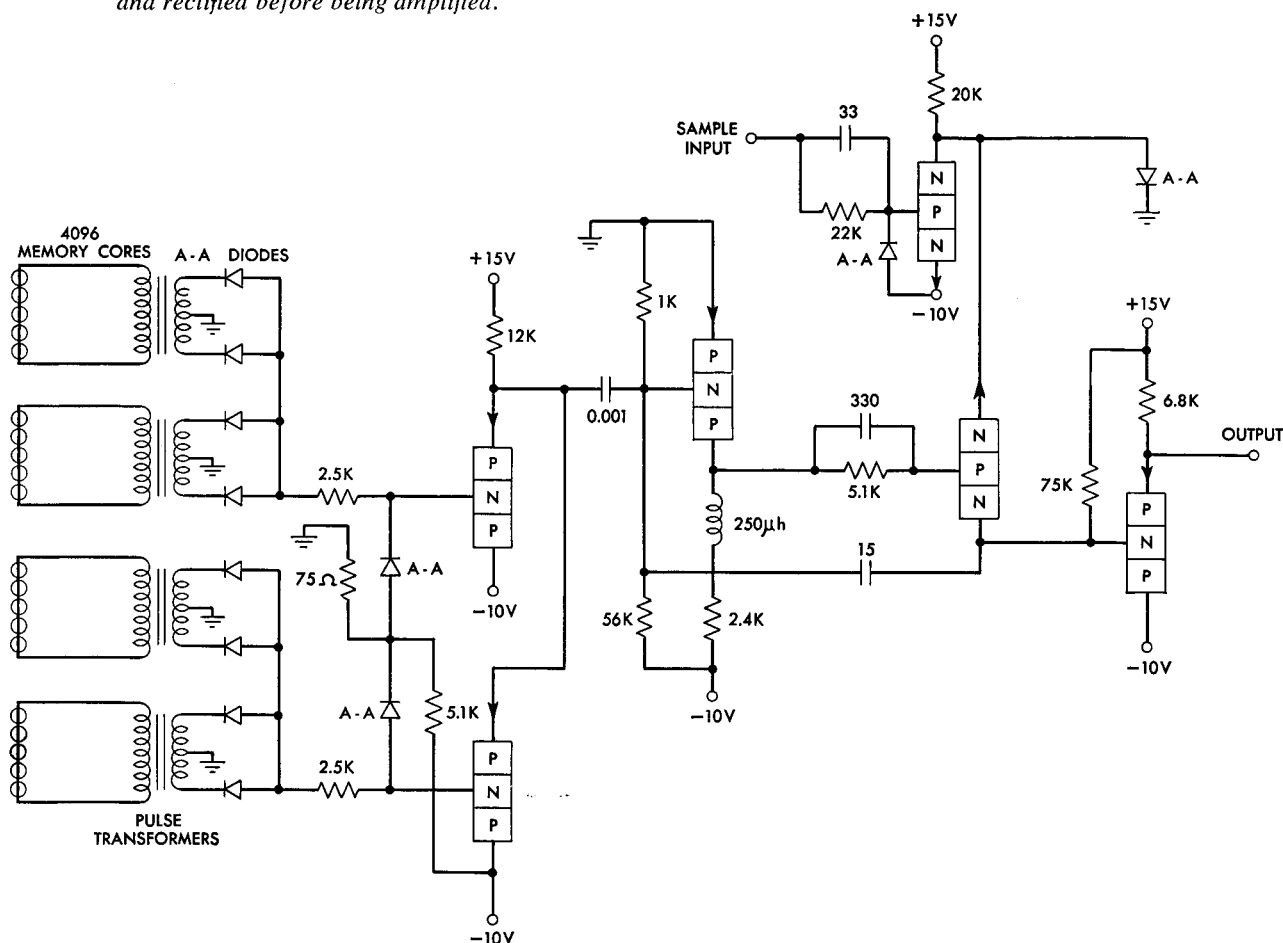
was obtained by placing a clipping circuit between the load of the rectifying diodes and the input to the emitter-follower OR circuit. The clipping level is set at about 200 millivolts. A differentiating circuit was inserted between the emitter-follower OR circuit and the first amplifier to limit the duration of the noise pulses seen by the first amplifier.

Maintenance aids

In order to facilitate maintenance of the IBM 738, memory test circuits have been incorporated in the logic section, which can be controlled on the C. E. panel to enter all "ones" or "zeros" into memory and then to test to see if these "ones" or "zeros" were retained correctly. The C. E. panel also includes indicator lights to show the address being selected and to show the information appearing on the memory output lines.

A circuit has been developed by a computer development group responsible for computer maintenance design

Figure 7 Circuit diagram of the sense amplifier
Signals are fed through a pulse transformer and rectified before being amplified.



and is included in the machine to detect filament burn-outs in all tubes contained in the pluggable units. The system monitors the amount of current flowing in the bus connecting the filament center taps back to the center tap of the filament transformer. If the amount of current changes because half a filament burns out, a relay is energized and an indicator lights on the C. E. panel.

Conclusion

In the development of this large high-speed memory, the adoption of transistors and etched wiring cards for the sense amplifier circuits has decreased the space needed for this circuitry to one-fourth of that which ordinarily would be required.

The division of the memory array so that the two halves are in different frames has made the wiring contained in the array accessible to service and has placed the array as near the drivers as possible, thereby simplifying the problems of driving such a large number of

cores. The method developed for placement of core drive amplifiers, core drivers, and switch core matrices has greatly added to the stability of this feed-back amplifier system.

The general layout of components will contribute toward ease and speed of maintenance and should reduce installation time to a minimum.

Acknowledgment

It is not possible to acknowledge here the help of all of those who have contributed directly to the design of this memory, but we wish to acknowledge particularly the contributions of Erich Bloch, who was responsible for some of the original design, and the guidance and assistance of P. W. Jackson throughout the greater part of the project.

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