IBM Maintenance Library

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8100 Information System

8130/8140 Processors

8101 Storage and Input/Output

Maintenance Information

(Volume 2 of 4)

SY27-2521-3

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Chapter 5. MAP Reference Information
Display and Printer Adapter
(AD)

Introduction

This part of the manual provides maintenance information to service the Display/Printer Attachment Feature adapter used in the IBM 8100 Information System. When used with IBM's MAP maintenance package, the MAP diagnoses display/printer problems and refers to this part for information such as hardware locations, possible-cause-of-failure lists, and wiring checks.

This part consists of five sections:

1. General Information (AD100–AD134): contains information on display/printer components, addressing, operation, and repair strategy.
2. Offline and Online Tests (AD200–AD254): contains test information and failure action plans.
3. Intermittent Failure Repair Strategy (AD300–AD358): contains information to repair intermittent failures.
4. Signal Paths (AD400–AD470): contains diagrams and charts that show wiring and signal paths.
5. Attached Devices (AD500): contains information on the devices that can be attached to the display/printer adapter.

Contents

Chapter 5. MAP Reference Information (MR)

MAP Reference Information General Outline

Wherever possible according to contents, all Chapter 5 MAP reference sections correspond to the same respective topics within each section up to XX400, and then become adapter/device dependent. The following general outline applies to all Chapter 5 MAP reference sections.

Note: *If certain sections do not apply within a particular MAP reference section, they are not included.*

XX100 General Information
- XX110 Components and Addressing
  - XX111 Hardware Components
  - XX112 Addressing
  - XX113 Configuration Table Entry
- XX120 Basic Operational Description
- XX130 Adapter—Unique Repair Strategy
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- XX210 Offline Test Routine Descriptions
  - XX211 Adapter Tests
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- XX230 Test Message Formats and Status Information
  - XX231 Adapter Test Message Formats
  - XX232 Device Test Message Formats
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- XX310 Adapter-Unique Intermittent Repair Strategy
  - XX311 Looping with MAP Interaction to Determine Failures
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  - XX313 Using the Free-Lance Utility to Determine Failures
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- XX330 Error Log Formats and Meanings Used for the XX MAP
  - XX331 DPPX Error Log Formats and Meanings
  - XX332 DPCX Condition/Incident Log Formats and Meanings
- XX340 How to Use the Error Log
  - XX341 DPPX Error Log
  - XX342 DPCX Condition/Incident Log
- XX350 Action Plan to Correct Intermittent Failures

Sections XX400 and above are unique according to the MAP reference information required.

Figures

Abbreviations

ADWA	adapter work area
AID	attention identification
CHCV	channel control vector
CHIO	channel I/O
CIL	Condition/Incident Log
DOSF	Distributed Office Support Facility
DPCX	Distributed Processing Control Executive
DPPX	Distributed Processing Programming Executive
EN	error number
EOC	end of chain
FDM	function definition module
FRU	field replaceable unit
GFI	general failure index
hex	hexadecimal
I/O	input/output
LA	logical address
MAP	Maintenance Analysis Procedure
MD	Maintenance Device
MIM	Maintenance Information Manual
PA	physical address
PA key	program attention key
PF	program function
PN	port number
RR	Routine
SCA	Secondary Component Address
SCF	System Control Facility
SERDES	serializer/deserializer
SSCF	Secondary System Control Facility

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AD100 General Information

This section contains a basic discussion of the display/printer adapter and shows the attachable devices. It enables you to understand the adapter's physical components, operation, and addressing scheme as well as any unique repair strategy used to perform fault isolation on the adapter.

For a detailed hardware discussion of the display/printer adapter and its operation, refer to section AD400.

AD110 Components and Addressing

AD111 Hardware Components

The display/printer adapter consists of six adapter cards, and one driver/receiver card for each group of four attached devices. See Section AD500 for types of attached devices. Depending on the customer's configuration, there can be from 1 to 24 devices attached to the display/printer adapter. Therefore, the minimum number of cards associated with this adapter is 7 and the maximum number of cards is 12.

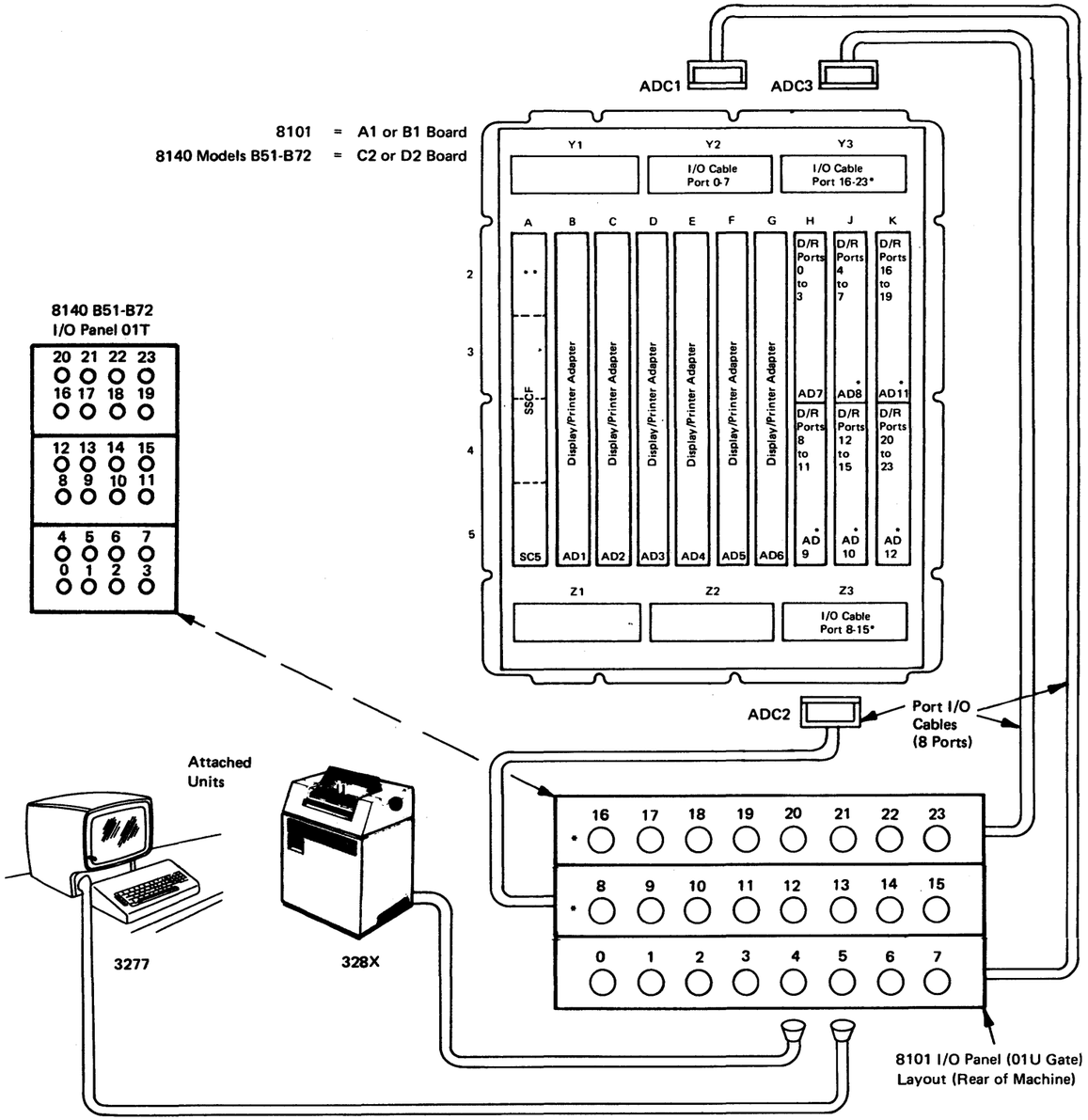
The display/printer adapter feature on the 8100 Information System, is available on either an 8101 and requires a board in either the 01A-A1 or 01A-B1 position, or an 8140 model B51—B72 and requires a board in either 01A-C2 or 01A-D2 position. Figure AD111-1 shows adapter card, cable, and I/O panel locations.

AD112 Addressing

The software addressing used for the display/printer adapter specifies a physical address (PA) and a port number (PN), which determine the attached device used for the operation to be performed.

The PA consists of two hexadecimal (hex) characters. The first hex character (P), whose value is determined by the setting of the SSCF address switches, selects the SSCF adapter group. The second hex character (A) is the adapter address within the SSCF adapter group. See the Physical Addresses table in AD113. Refer to Chapter 2 (CP210) for a discussion of addressing.

The port number (PN) is the same as the attached device port number. For example, PN 03 equals port 3.



*These driver/receiver cards (AD8-AD12), cables (ADC2 and ADC3), and I/O connectors are installed only if required by the number of attached devices.

**If the adapter is located on the A1 or C2 board, an SSCF card (SC5) is in position A2. If the adapter is located on the B1 or D2 board, SCF signal cables are in positions A2, A3, and A4.

Figure AD111-1. Display/Printer Adapter Card, Cable, and I/O Panel Locations

AD113 Configuration Table Entry

LV	PA	UTUT	OPOP OPOP
01	aa	0080	Not used
02	cc	0080	X000 0000
03	cc	0100	X000 0000 (X=8 if printer attached has Katakana feature)

LV 01 = adapter entry for adapter tests, where aa = adapter physical address and 0080 is the unit type.

LV 02* = port entry for adapter tests, where cc = device I/O port number (decimal 00–23) and 0080 is the unit type.

LV 03 = device entry for unique device tests, where cc = device I/O port number (decimal 00–23) and 0100 is the unit type.

*AD MAPs use LV 02 entries to verify and repair the adapter.

Physical Addresses

Unit	1st 8101	2nd 8101	3rd 8101	4th 8101	8140 Model B51–B72
Physical Address	1F	2F	3F	4F	5F

AD120 Basic Operational Description

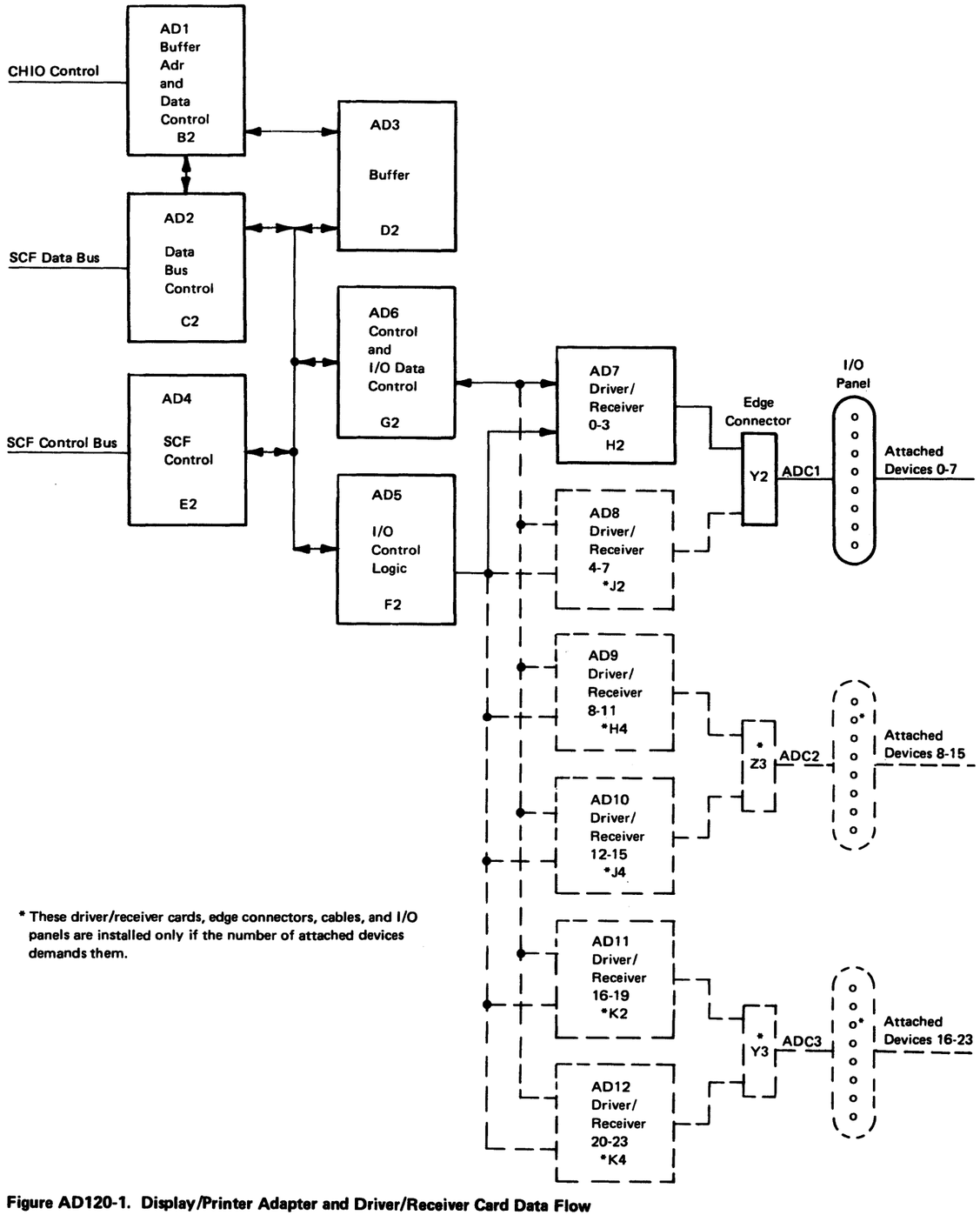
The display/printer adapter consists of six adapter cards (AD1–AD6), plus one driver/receiver card (AD7–AD12) for each group of four attached devices. See Figure AD120-1, which shows the functions of these cards and the data flow between them.

The adapter controls the operation of from 1 to 24 attached devices (see AD500 for types of attached devices), depending upon the customer's configuration. The adapter transfers information with each attached device through a single coaxial cable. The information is transmitted serially, and the width of the transmitted pulse determines whether the data is a 1- or a 0-bit.

There are three basic types of operations that occur between the adapter and its attached device: (1) poll, used to determine the status of the device; (2) read, used to receive data from the device; and (3) write, used to send data to the device.

AD121 Poll Operation

The adapter sends a poll command to the attached device, which decodes the command as a poll operation and sends device status to the adapter. There is a line turnaround time between the adapter command and the device's response. If the device does not respond with the device status before the line turnaround time is reached (a timeout condition), the adapter terminates the poll operation and indicates "device not available" status.



* These driver/receiver cards, edge connectors, cables, and I/O panels are installed only if the number of attached devices demands them.

Figure AD120-1. Display/Printer Adapter and Driver/Receiver Card Data Flow

AD122 Read Operation

The adapter sends a read command to the attached device, which decodes the command as a read operation and sends the data requested (either a 480- or 1920-byte transmission) to the adapter. There is a line turnaround time between the adapter command and the device's data. If the device does not respond (send data) to the read command before the line turnaround time is reached (a timeout condition), the adapter terminates the read operation and indicates "device not available" status.

AD123 Write Operation

The adapter sends a write command to the attached device, along with either a 480- or 1920-byte data message. Following the data message transmission, the adapter sends a poll command (see AD121 "Poll Operation" above) to the device to obtain device status to determine whether the write operation was successful.

AD130 Adapter-Unique Repair Strategy

Refer to Chapter 4 for 8100 general repair strategy. The General Failure Index (GFI) initially determines an adapter problem. If the problem can be isolated to one attached device, you are referred to Section 4 of the device's Maintenance Information Manual (MIM). The IBM 8100 Information System online and offline programs provide the tests required by these MIMs. If the problem occurs on more than one attached device, you are instructed to use the AD MAP on a maintenance device (MD) diskette to determine the cause of the failure (using offline checkout, selection A).

AD131 Offline Checkout

To perform the adapter offline checkout, obtain the 8100 from the customer. The AD MAP and offline tests are provided on MD diskette 03, which operates in the MD. Select offline checkout (selection A) from the AD MAP menu. Then run the display/printer offline test to isolate the problem to the adapter, to the attached device, or to the unit's Secondary System Control Facility (SSCF).

If the problem is isolated to the adapter, the AD MAP directs you to replace the FRU(s) causing the problem. If the problem is not corrected, you are referred to AD250 (Failure Action Plans) for further corrective action, such as replacing multiple FRUs and checking board signal paths.

If the problem is isolated to an attached device, the MAP directs you to check the I/O coaxial cable to the device. If the cable is bad, inform the customer and end the trouble call. If the cable is good, you are referred to Section 4 of the attached device's MIM. The tests required by these MIMs are provided by online and offline programs (see AD200).

If the problem is isolated to the SSCF, the AD MAP transfers control to the SC MAP, which directs you to replace the FRU causing the problem.

AD132 DPPX Online Tests

In a DPPX operating system, online device tests are provided to service the attached devices. To repair an attached device, you can use the online device tests within the DPPX operating system along with the attached device's MIM.

AD133 DPCX Online Tests

In a DPCX operating system, online tests are available to service the attached devices. To check out or repair the adapter, use the offline tests (see AD131). To repair an attached device, you can use the online device tests within the DPCX operating system along with the attached device's MIM.

AD134 Intermittent Failures

Depending on the error condition, different types of intermittent error conditions can occur:

- An intermittent failure can occur so infrequently that it cannot be detected by looping the test. You are instructed to use the system error log (AD312).
- An error also can occur at random times. This causes the generation of different error messages, thereby making the MAPs ineffective. After the MAPs detect three different test error messages, you are instructed to use the action plans in AD250.
- If an error is detected only after looping the test for more than 5 minutes, record the test error message and use the free-lance looping operation (AD313) and the action plans in AD250.

See AD300 for detailed information on intermittent failures.

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AD200 Offline and Online Tests

The display/printer adapter can be tested offline.

- Offline adapter tests reside on MD diskette 03.

Display and printer devices can be tested offline and also online when using either DPPX or DPCX.

- Offline device tests reside on MD diskette 03.
- DPPX and DPCX device tests are contained on the system-resident device, are part of the operating system, and are identical to the offline tests.

AD210 Offline Test Routine Descriptions

AD211 Adapter Tests

The offline display/printer tests verify the operation of the adapter with one of its attached devices. The test consists of 14 routines on MD diskette 03. The routines are arranged so that they test functions within the adapter in an order that isolates any failure to the FRU or FRUs most likely to be bad. The test is invoked from the MD, either by the AD MAP or by the MD free-lance utility.

When using the MAP, the test is invoked automatically when required. When using the Free-Lance Utility, the following test invocation message must be issued:

1. At 80BC or PA00, enter PAPNB.
2. At 81BC, enter SLRRB

   Where:

   PA = physical address (see AD112)
   PN = port number (see AD112) of attached device to be tested.
   S = sense option:
   - 0 = run only adapter tests, routines 01-03
   - 1 = run adapter/device tests, routines 01-0B
   - 2 = run adapter/device tests with manual intervention, routines 01-0E

   L = loop option:
   - 0 = run selected routines one time
   - 1 = loop selected routines; stop on error
   - 2 = loop selected routine; bypass error

   RR = routine number. If 00 or no entry is made, all routines for sense option are run. If a routine number is entered, only that routine is run.

   B = begin execution; enters the invocation message.

The following briefly describes each routine.

Routine 01, Test Device Independent Commands. Tests the Set, Read, Reset Status, and Reset Adapter commands.

Routine 02, Invalid Command Test. Issues all invalid adapter commands, and expects a system check/program exception for each invalid command issued. Registers 2 and 3 contain the address of the valid command table; register 1 contains the command issued.

Routine 03, Stop Idle Poll Test. Issues a Stop Poll command to a reset adapter and expects an immediate interruption.

Routine 04, Specific Poll Test. Issues a Specific Poll command to the device specified. A Specific Poll command is also issued with no device command specified to test timeout. This test simulates a nonexistent device.

Routine 05, Write Full Buffer Test. Tests the Write Full Buffer command by performing six write operations. The first five verify that the buffer size indicated in the device status is correct. The last write operation writes valid information into a buffer, and uses the same data as the Read Full Buffer test, Routine 06.

Routine 06, Read Full Buffer Test. Reads the contents of the buffer and compares the data received with the data written. During the read operation, a second read operation is attempted, and the resulting adapter status should indicate an equipment (machine) check (bit 5) condition. This test uses a fixed cursor address, depending upon the buffer size; for a 480-character buffer the address is hex 157, and for a 1920-character buffer the address is hex 6F7.

Routine 07, Channel I/O Control Register Test. Tests the Read CSCB command and the capability of the adapter to access all channel I/O register pairs.

Routine 08, Adapter Reset Test While Channel I/O Operation Is in Process. Starts a Channel I/O read operation, performs a delay, and then issues a Reset Adapter command. No interruption should occur, and the adapter status should be clear.

Routine 09, Floating Cursor Test. Floats the cursor through a pattern from one corner to the other, then floats an attribute character in the opposite direction. Data is checked on the read pass.

Routine 0A, Test Timeout on Read Command. Attempts a Read operation with no device command specified to test the adapter timeout circuits. An error occurs for any status indication without timeout.

Routine 0B, Printer Test. Checks the adapter paths to the printer or 129 Card Recorder (RPQ MK6956) and is bypassed when a display is attached.

Routine 0C, Idle Poll Test 1. This display-only manual intervention routine tests that the specified display's ENTER pushbutton stops idle polling and indicates pending information in the device status.

Routine 0D, Idle Poll Test 2. This manual intervention routine runs on the specified device port being tested. The routine checks that going from a not available to an available state causes an interruption and presents the proper device status.

Routine 0E, Stop Idle Poll Test. Starts an idle poll operation and then issues a Stop Idle Poll command. Only the Enable and Interruption bits of the basic status are expected.

AD212 Offline Device Tests

The display/printer offline/online device tests aid in maintaining devices attached to the 8100 through the display/printer adapter. If the attached device is a display (3277), the tests consist of eight routines; if the attached device is a printer (3284, 3286, 3287, 3288), the tests consist of three routines. The tests reside on MD diskette 03 and require that the entire system be obtained from the customer before running. The tests are invoked from the MD using the free-lance utility and use the following invocation message:

1. At 80BC or PA00, enter PAPNSAB.
2. At 81BC, enter SLRRB

Where:

PA = physical address (see AD112).
PN = port number (see AD112) of attached device to be tested.
SA = device address, which is the same two-digit entry as PN.
S = sense option:
0 or 1 = run routines with no manual intervention (routine 01 only)
2 = run device tests: 01, A1-A4 (if a display); 01, 02, 03 (if a printer)
L = loop option:
0 = run selected routines one time.
1 = loop selected routine; stop on error.
2 = loop selected routine; bypass error.
RR = routine number. If 00 or no entry is made, all routines for sense option are run. If a routine number is entered, only that routine is run. Note that routines A5—A7 are only run when specifying the RR option.
B = begin execution; enters the invocation message.

Display Tests

The following describes the eight routines used to test attached displays:

Routine 01. Tests the basic data flow required to operate with the attached device.

Routine A1. Generates test pattern 1*, which displays all available characters. The pattern contains protected-data fields, numeric fields, high-intensity fields, nondisplay fields, and selector-pen-detectable fields. The routine also tests the audible alarm feature (if installed).

Routine A2. Generates test pattern 2* or 3*, depending on the display model, and displays all data at normal intensity. The audible alarm, if installed, sounds when this pattern appears on the screen.

Routine A3. Generates test pattern 5*. It loads the display station buffer with all available uppercase and lowercase character codes. The audible alarm, if installed, sounds when this pattern appears on the screen.

Routine A4. Tests the operation of the following keys on the keyboard: PA1, PA2, ENTER, and TEST REQUEST.

Routine A5 (selectable routine).** Tests the operation of the PF1 through PF12 keys on the keyboard.

Routine A6 (selectable routine).** Tests the operation of the badge reader feature.

Routine A7 (selectable routine).** Tests the operation of the additional attention-generating keys (PF1—PF5, and PA3) associated with the data entry keyboard.

Printer Tests

The following describes the three routines used to test attached printers:

Routine 01. Tests the basic data flow required to operate with the attached device.

Routine 02, Control Character Test. Tests the capability of the printer to perform the new line (NL) and end of message (EOM) control character functions.

Routine 03, Formatted Line Test. Tests the capability of the printer to format lines of 40, 64, and 80 character lengths.

*For a description of the test patterns, see the *8100-3277 Attachment*, Form SY27-2522.

**Test routines A5, A6, and A7 are for features on the 3277 display and must be individually selected with the invocation message.

AD220 Online Test Routine Description

AD221 DPPX

There are no online display/printer adapter tests in the DPPX operating system. To check or repair the adapter, you must use the offline tests (see AD131).

The DPPX online display/printer device tests are identical to the offline device tests (see AD212 for routine descriptions). They are part of the DPPX operating system, and can be run in conjunction with the customer's operation. The tests can be invoked by another attached I/O device (see *8100-3277 Attachment,* Form SY27-2522). The DPPX online device tests use a different invocation message than the offline device tests. Refer to Chapter 2, CP720, which explains the invocation of online device tests.

Notes:

1. *All routines except routine 01 must be individually selected with the VERIFY command.*
2. *Any error detected by the DPPX operating system is recorded in the error log.*

AD222 DPCX

There are no online display/printer adapter tests in the DPCX operating system. To check or repair the adapter, you must use the offline tests (see AD131).

The DPCX online device tests for 3277 displays and 3284, 3286, 3287, 3288 printers are identical to the offline device tests (see AD212). They are part of the DPCX operating system and can be run in conjunction with the customer's operation. The tests can also be invoked by another attached device (see *8100-3277 Attachment,* Form SY27-2522). The DPCX online device tests use the same invocation message as the offline device tests. Refer to AD212 for a discussion of the device tests.

For DPCX/DOSF operating systems, online device tests are provided for the 3732 display and 3736 printer. The tests are part of the DOSF operating system and can be run in conjunction with the customer's operation. The tests are invoked via SYSTCM, which is part of DPCX, and uses the same invocation message as the offline device tests (AD212). There are 4 test routines for the 3732 display and 15 routines for the 3736 printer. (See *8100–3732*, SY33-0048, and *8100–3736,* SY33-0050, for descriptions of these test routines.)

For the 129 Card Data Recorder attachment (RPQ MK6956), only DPCX online tests (4 routines) are provided. For a description of these test routines, see *8100-129 Attachment,* Form SY27-2552.

Note: *DPCX online device tests only loop five times.*

AD230 Test Messages and Status Information

AD231 Offline Display/Printer Adapter Tests

The following messages are generated while running the offline display/printer adapter tests:

- **PA00** = successful test completion.
- **PA70** = manual intervention stop. To continue, press the ENTER key on the attached display.
- **PA71** = manual intervention stop. To continue, turn power off then on at the attached display, or disconnect then reconnect the I/O coaxial cable of the attached display.
- **PA80** = error detected in the adapter data flow circuitry.
- **PAF0** = display/printer test is running.
- **PAXE** = error detected. Refer to the following test error message formats:

  Type 1. PAXE RREN
  Type 2. PAXE RREN 00BS
  Type 3. PAXE RREN MC00
  Type 4. PAXE RREN MC00 ADDR
  Type 5. PAXE RREN 00BS DSDS
  Type 6. PAXE RREN 00BS EXPD RECD
  Type 7. PAXE RREN 00BS EXPD RECD DSDS

Where:

- **PA** = physical address or port number
- **X** = level indication.
  If 1, PA = physical address.
  If 2, PA = port number of device being tested.
- **E** = error. Indicates that the three preceding digits are an error format and that the next four digits are RREN.
- **RR** = failing routine number (01 through 0E)
- **EN** = error number which defines the type of error (see AD240)
- **00** = always zero (not used)
- **BS** = basic adapter status
- **MC** = machine check indicator
- **ADDR** = address stored when machine check occurred
- **DSDS** = device status: 1st DS is device status byte 1; 2nd DS is device status byte 2.
- **EXPD** = expected data
- **RECD** = received data

Note: *When entering PAXE test error messages into the MD for MAP menu selection 'C', do not use spaces.*

AD232 Device Tests

The display/printer device tests generate the following messages:

- **PN00** = successful completion of requested test
- **PN01 through PN29** = manual intervention stops; service representative action required to continue (see *8100-3277 Attachment,* Form SY27-2522)
- **PNF0** = Device test in progress
  PN = port number of device being tested.
- **PN3E** = Error detected according to the following formats:

  Type 1. PN3E RREN CCBS D1D2
  Type 2. PN3E RREN CCBS EXAC
  Type 3. PN3E RREN CCBS

Where:

- **PN** = port of device being tested
- **3E** = error indicator
- **RR** = failing routine number (01, A1-A7, 02, 03)
- **EN** = error number which defines type of error
- **CC** = completion code
- **BS** = adapter status
- **D1** = device status byte 1
- **D2** = device status byte 2
- **EX** = expected AID (Attention Identification) or data
- **AC** = actual AID or data

Note: *Error format type 2 only occurs when testing a display and the CC of the message is 08. Offline device tests use error format type 1 and 3.*

AD233 Status and Sense Bytes

The display/printer adapter uses a basic/adapter (hardware/software) status byte and two sense (device status) bytes. Each bit of the status and sense bytes identifies specific actions or functions. The test error messages (AD231) and the error log (AD330) indicate these status and sense bytes in hexadecimal (hex). To determine the active status and sense bits, you must convert the hex value to a decimal value; see Appendix A for hex-to-decimal conversion.

Basic Adapter Status Information

Basic Status - BS (Hardware); Adapter Status - AS (Software)

Bits	0	1	2	3	4	5	6	7	
BS	Overrun	Parity Error	Not Avail	Busy	Not Used	Machine Check	Enabled	Interruption Request	BS
AS				Not Used			Idle Poll	Invalid Operation	AS

Note: *The meaning of each bit is the same for basic and adapter status unless otherwise noted.*

Bit	Meaning
0	Overrun - Adapter buffer data was either not sent to the device for a write operation, or not stored in processor storage for a read operation. The new data overlaid the old data in adapter buffer storage.
1	Parity Error - An inbound parity error occurred either between the adapter and the attached device, or from the adapter's buffer.
2	Not Available - The attached device is not available.
3	BS: Busy - The adapter is performing a function. AS: Not used.
4	Not used.
5	Machine Check - The attached device caused a machine check.
6	BS: Enabled - The attached device can cause an interruption. AS: Idle Poll - An idle poll operation is being performed.
7	BS: Interruption Request - The attached device has an interruption condition. AS: Invalid Operation - An invalid function was requested.

Sense (Device Status) Information

Bits	0	1	2	3	4	5	6	7	
Sense Byte 1	Device Check	Transmit Check	Info Pending	Attention Ident (AID) Code					Display
				Not Ready	Not Used	Equip Check	Not Used	Not Used	Printer
Sense Byte 2	Device Busy	Device Model	0	Device Port Address					Display
			1						Printer

Note: *The meaning of each bit is the same for a display or a printer unless otherwise noted.*

Sense Byte 1 (Device Status Byte 1)

Bit	Meaning
0	Device Check - The attached device detected incorrect parity in its buffer, or a display detected a cursor check.
1	Transmit Check - The attached device detected incorrect parity on data received from the adapter.
2	Information Pending - Either the operator generated an attention or a device check occurred.

Bits 3 through 7 have a different meaning depending on whether the attached device is a display or a printer. For a display, bits 3 through 7 is the AID code:

3277 Display						3732 Display					
Bits						Bits					
3	4	5	6	7	Meaning	3	4	5	6	7	Meaning
0	0	0	0	0	No AID generated	0	0	0	0	0	No AID generated
0	0	1	1	0	Magnetic card reader	0	0	0	0	1	End (screen modified)
0	1	0	0	0	129 is not reading cards	0	0	0	1	0	SCR advance (screen modified)
0	1	0	0	1	Reserved	0	0	0	1	1	Page advance (screen modified)
0	1	0	1	0	Reserved	0	0	1	1	1	IMM command (screen modified)
0	1	0	1	1	PA3 key	0	1	0	0	0	Enter (screen modified)
0	1	1	0	0	PA1 key	0	1	0	0	1	Top (screen modified)
0	1	1	0	1	CLEAR key	0	1	0	1	0	SCR return (screen modified)
0	1	1	1	0	PA2 key	0	1	0	1	1	Page return (screen modified)
0	1	1	1	1	Reserved	0	1	1	0	0	Adjust (screen modified)
1	0	0	0	0	TEST REQUEST key	0	1	1	0	1	Line delete (screen modified)
1	0	0	0	1	PF1 key	0	1	1	1	0	Print (screen modified)
1	0	0	1	0	PF2 key	0	1	1	1	1	Sent delete (screen modified)
1	0	0	1	1	PF3 key	1	0	0	0	0	Cancel (screen modified)
1	0	1	0	0	PF4 key	1	0	0	0	1	End
1	0	1	0	1	PF5 key	1	0	0	1	0	SCR advance
1	0	1	1	0	PF6 key	1	0	0	1	1	Page advance
1	0	1	1	1	PF7 key	1	0	1	0	1	Block insert (screen modified)
1	1	0	0	0	PF8 key	1	0	1	1	0	Block move (screen modified)
1	1	0	0	1	PF9 key	1	0	1	1	1	IMM command
1	1	0	1	0	PF10 key	1	1	0	0	0	Enter
1	1	0	1	1	PF11 key	1	1	0	0	1	Top
1	1	1	0	0	PF12 key	1	1	0	1	0	SCR return
1	1	1	0	1	ENTER key	1	1	0	1	1	Page return
1	1	1	1	0	Selector pen	1	1	1	0	0	Block copy (screen modified)
						1	1	1	0	1	Block delete (screen modified)
						1	1	1	1	0	Block return (screen modified)
						1	1	1	1	1	Help (screen modified)

Note: *Screen modified means either the cursor is moved or data is changed after the screen is received but before an AID is pressed.*

For a printer:

Bit	Meaning
3	Not Ready - The cover is not closed or the printer is out of paper.
4	Not used.
5	Equipment Check - Error detected.
6	Not used.
7	Not used.

Sense Byte 2 (Device Status Byte 2)

Bit	Meaning
0	Device Busy - The device is executing a keyboard, selector pen, ID card, or write printer operation.
1	Device Model - Buffer size of attached device: if a 0, the device has a 480-character buffer; if a 1, a 1920-character buffer.
2	Device Type - Type of attached device: if a 0, the device is a display; if a 1, a printer.

Bits 3 through 7 designate the port address of the attached device reporting the failure:

Bits						Bits					
3	4	5	6	7	Port	3	4	5	6	7	Port
0	0	0	0	0	00	0	1	1	0	0	12
0	0	0	0	1	01	0	1	1	0	1	13
0	0	0	1	0	02	0	1	1	1	0	14
0	0	0	1	1	03	0	1	1	1	1	15
0	0	1	0	0	04	1	0	0	0	0	16
0	0	1	0	1	05	1	0	0	0	1	17
0	0	1	1	0	06	1	0	0	1	0	18
0	0	1	1	1	07	1	0	0	1	1	19
0	1	0	0	0	08	1	0	1	0	0	20
0	1	0	0	1	09	1	0	1	0	1	21
0	1	0	1	0	10	1	0	1	1	0	22
0	1	0	1	1	11	1	0	1	1	1	23

Note: *It is possible for a failing attached device to respond to a poll for another device or to respond with the wrong port address.*

AD240 Test Error Messages and Descriptions

Every display/printer offline test error message (such as PAXE RREN has an error number (EN). This error number indicates the type of failure detected and the additional status information available in the test error message format. The routine number and the error number determine the error message formats.

The following table lists, for each routine, the error numbers and their meaning. For test message formats, see AD230.

RREN	Format Type	Meaning	Type of Failure and Possible Cause
0102	4	Unexpected machine check interruption.	Adapter failure: 1. Board voltages 2. Adapter cards (in order of probability of being bad): AD2, AD4, AD3, AD5, AD1, AD6 3. SSCF (SC5) card See Action Plan in section AD251.
0104 to 010D	2	Received incorrect basic status.	
0202	4	Unexpected machine check interruption.	Adapter failure: 1. Adapter cards (in order of probability of being bad): Routine 02: AD2, AD4, AD6 Routine 03: AD4, AD5, AD2 2. SSCF (SC5) card See Action Plan in section AD251.
020E	1	Invalid operation accepted.	
020F	3	Valid operation rejected.	
0302	4	Unexpected machine check interruption.	
0310	2	Missing interruption for stop poll operation.	
0311	2	Incorrect status for stop poll interruption.	
0401	2	Unexpected attached device interruption.	Adapter's first operation using the attached device: 1. Coaxial cable 2. Adapter cards (in order of probability of being bad): AD6, AD5, AD1, AD3, AD4, AD2, AD7-12 See Action Plan in section AD252.
0402	4	Unexpected machine check interruption.	
0403	2	Attached device interruption cannot be reset.	
0412	2	Missing interruption for specific poll operation.	
0413	2	Incorrect adapter status for specific poll interruption.	
0414	2	Incorrect status for specific poll interruption.	
0415	5	Device status incorrect for specific poll operation.	(continued)
0416	5	Incorrect device status for specific poll operation.	
0417	2	Missing interruption for specific poll operation.	
0418	2	Incorrect status for specific poll interruption.	
0419	5	Device status incorrect for specific poll operation.	
0501	2	Unexpected attached device interruption.	Adapter/Attached Device Failure Adapter cards (in order of probability of being bad): AD1, AD6, AD2, AD5, AD3, AD4 See Action Plan in section AD253.
0502	4	Unexpected machine check interruption.	
0503	2	Attached device interruption cannot be reset.	
0512	2	Missing interruption for specific poll operation.	
0513	2	Incorrect adapter status for specific poll interruption.	
0516	5	Incorrect device status for specific poll operation.	
051A	2	Missing interruption for write operation.	
051B	2	Incorrect status for write operation interruption.	
051D to 0523	5	Device status incorrect for write operation.	
0524	7	Adapter data flow error.	
0525	7	Adapter data flow error.	

RREN	Format Type	Meaning	Type of Failure and Possible Cause
0601	2	Unexpected attached device interruption.	Adapter/Attached Device Failure
0602	4	Unexpected machine check interruption.	Adapter cards (in order of probability of being bad):
0603	2	Attached device interruption cannot be reset.	AD3, AD2, AD1, AD5, AD6, AD4
0612	2	Missing interruption for specific poll operation.	See Action Plan in section AD253.
0613	2	Incorrect adapter status for specific poll interruption.	
0616	5	Incorrect device status for specific poll operation.	
061A	2	Missing interruption for write/read operation.	
061B	2	Incorrect status for write/read interruption.	
0626	2	Incorrect status for write/read interruption.	
0627	2	Missing interruption for write/read operation.	
0628	2	Incorrect status for write/read interruption.	
0629	6	Read data not equal to write data.	
062A	6	Read data not equal to write data.	
0701	2	Unexpected attached device interruption.	Adapter/Attached Device Failure
0702	4	Unexpected machine check interruption.	Adapter cards (in order of probability of being bad):
0703	2	Attached device interruption cannot be reset.	AD2, AD3, AD5, AD6
0712	2	Missing interruption for specific poll operation.	See Action Plan in section AD253.
0713	2	Incorrect adapter status for specific poll interruption.	
0716	5	Incorrect device status for specific poll operation.	
071A	2	Missing interruption for write/read operation.	
071B	2	Incorrect status for write interruption.	
0723	5	Device status incorrect for write operation.	
0724	7	Adapter data flow error.	
0725	7	Adapter data flow error.	(continued)
0727	2	Missing interruption for write/read operation.	
0731	6	Read data not equal to write data.	
0801	2	Unexpected attached device interruption.	Adapter/Attached Device Failure
0802	4	Unexpected machine check interruption.	Adapter cards (in order of probability of being bad):
0803	2	Attached device interruption cannot be reset.	AD4, AD5, AD6
0812	2	Missing interruption for specific poll operation.	See Action Plan in section AD253.
0813	2	Incorrect adapter status for specific poll interruption.	
0816	5	Incorrect device status for specific poll operation.	
0832	2	Incorrect status after reset.	
0901	2	Unexpected attached device interruption.	Adapter/Attached Device Failure
0902	4	Unexpected machine check interruption.	Adapter cards (in order of probability being bad):
0903	2	Attached device interruption cannot be reset.	AD5, AD6
0912	2	Missing interruption for specific poll operation.	See Action Plan in section AD253.
0913	2	Incorrect adapter status for specific poll interruption.	
0916	5	Incorrect device status for specific poll operation.	
091A	2	Missing interruption for write/read operation.	
091B	2	Incorrect status for write/read interruption.	
0923	5	Device status incorrect for write operation.	
0924	7	Adapter data flow error.	
0925	7	Adapter data flow error.	
0927	2	Missing interruption for write/read operation.	
0929	6	Read data not equal to write data.	
092A	6	Read data not equal to write data.	
0939	2	Incorrect status for write/read interruption.	
093B	6	Read data not equal to write data.	

RREN	Format Type	Meaning	Type of Failure and Possible Cause
0A01	2	Unexpected attached device interruption.	Adapter/Attached Device Failure
0A02	4	Unexpected machine check interruption.	Adapter card: AD5
0A03	2	Attached device interruption cannot be reset.	See Action Plan in section AD253.
0A12	2	Missing interruption for specific poll operation.	
0A13	2	Incorrect adapter status for specific poll interruption.	
0A16	5	Incorrect device status for specific poll operation.	
0A3D	2	Missing interruption for read operation.	
0A3E	2	Incorrect status for read operation.	
0B01	2	Unexpected attached device interruption.	Adapter/Attached Device Failure
0B02	4	Unexpected machine check interruption.	Adapter cards (in order of probability of being bad):
0B03	2	Attached device interruption cannot be reset.	AD6, AD5, AD4, AD3, AD7-AD12
0B12	2	Missing interruption for specific poll operation.	See Action Plan in section AD253.
0B13	2	Incorrect adapter status for specific poll interruption.	
0B16	5	Incorrect device status for specific poll operation.	
0B3F	5	Continuous interruptions from attached devices.	
0B46	2	Missing interruption for write operation.	
0B47	2	Incorrect status after write operation.	
0B48	5	Device status incorrect.	
0B49	2	Missing interruption for write operation.	
0B4A	5	Device status incorrect.	
0B50	5	Incorrect device address.	
0C01	2	Unexpected attached device interruption.	Adapter/Attached Device Failure
0C02	4	Unexpected machine check interruption.	Adapter cards (in order of probability of being bad):
0C03	2	Attached device interruption cannot be reset.	AD6, AD5, AD4, AD3, AD7-AD12
0C12	2	Missing interruption for specific poll operation.	See Action Plan in section AD253.
0C13	2	Incorrect adapter status for specific poll interruption.	
0C16	5	Incorrect device status for specific poll operation.	
0C1A	2	Missing interruption for write operation.	
0C1B	2	Incorrect status for write interruption.	(continued)
0C3F	5	Continuous interruptions from attached devices.	
0C40	2	Incorrect status from enter interruption.	
0C41	5	Device status incorrect.	
0C50	5	Incorrect device address.	
PA70	–	Manual intervention stop. Press ENTER key on device to continue.	
0D01	2	Unexpected attached device interruption.	Adapter/Attached Device Failure
0D02	4	Unexpected machine check interruption.	Adapter cards (in order of probability of being bad):
0D03	2	Attached device interruption cannot be reset.	AD6, AD5, AD4, AD3, AD7-AD12
0D12	2	Missing interruption for specific poll operation.	See Action Plan in section AD253.
0D13	2	Incorrect adapter status for specific poll interruption.	
0D16	5	Incorrect device status for specific poll operation.	
0D1A	2	Missing interruption for write operation.	
0D1B	2	Incorrect status for write interruption.	
0D3F	5	Continuous interruptions from attached devices.	
0D41	5	Device status incorrect.	
0D50	5	Incorrect device address.	
PA71	–	Manual intervention stop. Turn power off then on to continue.	
0E01	2	Unexpected attached device interruption.	Adapter/Attached Device Failure
0E02	4	Unexpected machine check interruption.	Adapter card: AD5
0E03	2	Attached device interruption cannot be reset.	See Action Plan in section AD253.
0E12	2	Missing interruption for specific poll operation.	
0E13	2	Incorrect adapter status for specific poll interruption.	
0E16	5	Incorrect device status for specific poll operation.	
0E44	2	Missing interruption for stop poll operation.	
0E45	2	Incorrect status for stop poll interruption.	

AD250 Failure Action Plans

This section provides action plans for the failures detected by the display/printer test. The failing routine number indicated by the test error message (see AD230) determines the type of failure detected.

Failing Routine (RR)	Type of Failure	Go to Action Plan Section
01 through 03	Adapter failure	AD251
04	Adapter's first operation using the attached device	AD252
05 through 0E	Adapter/attached device failure	AD253

Other Test Error Messages	Type of Failure	Go to Action Plan Section
PA70	Adapter did not detect that the ENTER key was pressed.	AD253
PA71	Adapter did not detect that the display has become ready.	AD253
PA80	Adapter failed to initiate a data transfer.	AD251
XXBC	Adapter failure (machine check).	AD251

Determine the type of error and go to the indicated action plan section to correct this type of failure.

Note: *When the AD MAP sends you to this section to perform an action plan, verify the repair action by pressing FWD on the MD keypad to run the test.*

AD251 Adapter Failure Action Plan

For a list of cards that could cause this failure as determined by the test error message (Routines 01, 02, 03, or test error messages XXBC or PA80), see AD254.

A failure was detected in the adapter circuitry. The failing operation was not related to operations involving the attached device, as only adapter bus control circuits were being used. Proceed as follows:

1. Measure the board voltages (see AD111):
   a. F2D03 = +4.5V to 5.5V dc
   b. F2B11 = +7.7V to 9.3V dc
   c. F2B06 = –4.5V to –5.5V dc

   If any are missing or out-of-tolerance voltages, go to the PA MAP.
2. Exchange all possible adapter cards that could cause the failure (see AD254).
3. Exchange the SSCF (SC5) card.

Machine Type	Model	SC5 Location
8101	All	A1A2
8140	B51–B72	C2A2

4. Check the board signal path (see AD410) and correct if necessary.
5. Run all adapters in the SSCF address group (use group address P of PA); exchange any failing adapter.
6. Perform either of the following:
   a. If the test error message was 92BC, return to the Chapter 1 Action Plan that sent you here and proceed with the next step.
   b. For all other messages, request aid.

AD252 Adapter/Device First Operation Failure Action Plan

For a list of cards that could cause this failure as determined by the test error message (Routine 04), see AD254.

A failure was detected when the adapter initiated its first operation involving an attached device. Proceed as follows:

1. Ensure that the test is run on an attached device that is connected to the adapter and that the device has power on. Correct, if necessary, and rerun the test.
2. Go to AD253 (Adapter/Device Failure Action Plan) and perform that action plan (Routines 05 through 0E and test error messages PA70 and PA71).

AD253 Adapter/Device Failure Action Plan

For a list of cards that could cause this failure as determined by the test error message, see AD254.

A failure was detected during an adapter-to-device operation. Proceed as follows:

1. Isolate the failure to the adapter or to the attached device by swapping the attached devices on the port being tested.
   - If the device is failing, check its coaxial I/O cable. Then go to the device's MIM to initiate a repair action.
   - If the adapter is failing, exchange the adapter cards associated with the test error message. See AD254 for the AD card replacement list.
2. Check the board signal path associated with the test error message. See AD410 for the board wiring chart.
3. Request aid.

AD254 Adapter Card Exchange Table

The following table shows the cards associated with a test error message. The YY designation can be any error number. The card most likely bad is designated 1, the next most likely bad is designated 2, and so on. XX = the display/printer adapter board location as follows:

Machine Type	Model	Board (XX)	Note
8101	All	A1 or B1	If 8101 has a B1 board, the adapter resides in that board.
8140	B51–B72	C2 or D2	If 8140 has a D2 board, the adapter resides in that board.

AD Test Error Message	AD1 XXB2	AD2 XXC2	AD3 XXD2	AD4 XXE2	AD5 XXF2	AD6 XXG2	AD7–AD12*
92BC or 97BC or AXBC	–	5	4	1	2	3	–
PAXE 01YY	5	1	3	2	4	6	–
PAXE 02YY	–	1	–	2	–	3	–
PAXE 03YY	–	3	–	1	2	–	–
PAXE 04YY	3	6	4	5	2	1	7
PAXE 05YY	1	3	5	6	4	2	–
PAXE 06YY	3	2	1	6	4	5	–
PAXE 07YY	–	1	2	–	3	4	–
PAXE 08YY	–	–	–	1	2	3	–
PAXE 09YY	–	–	–	–	1	2	–
PAXE 0AYY	–	–	–	–	1	–	–
PAXE 0BYY	–	–	4	3	2	1	5
PAXE 0CYY	–	–	4	3	2	1	5
PAXE 0DYY	–	–	4	3	2	1	5
PAXE 0EYY	–	–	–	–	1	–	–
**PA70	–	–	3	4	2	1	–
**PA71	–	–	3	4	2	1	–
PA80	1	2	6	5	3	4	–

*Exchange only the driver card (AD7–AD12) associated with the failing port. See Driver Card Exchange Table below.

**PA70 or PA71 are errors only if manual intervention does not continue after a stop condition.

Driver Card Exchange Table

Card Location	Associated Ports	Card Location	Associated Ports
XXH2	0 through 3	XXJ4	12 through 15
XXJ2	4 through 7	XXK2	16 through 19
XXH4	8 through 11	XXK4	20 through 23

AD300 Intermittent Failure Repair Strategy

Note: *Intermittent failures can possibly be detected by looping the display/printer off-line tests or by examining the system error log.*

AD310 Adapter-Unique Intermittent Repair Strategy

AD311 Looping with MAP Interaction to Determine Intermittent Failures

The display/printer tests can be looped using AD MAP selection A if you answer "yes" to the question: "DO YOU WANT TO CHECK FOR INTERMITTENT FAILURE BY LOOPING AD TEST?" The tests loop continuously, displaying "PAF0 TEST LOOPING" on the MD, until either detecting an error or you terminate the tests by entering an "F" at the MD.

If detecting an error while looping, the MAP diagnoses and directs repairs of the failure in the same manner as a solid failure. Once you perform a repair action, the MAP loops the tests to verify the repair.

Note: *If the MAP does not detect an error within 5 minutes while looping on the test, or if the error detected occurs randomly (test error messages vary), the MAP operation is ineffective. Use the free-lance looping operation described in AD313.*

AD312 Using the System Error Log to Determine Intermittent Failures

The IBM operating systems (DPPX and DPCX) use error logs to record any adapter failure that occurs during system operation. Obtain all error log records associated with the display/printer adapter (see AD320). Then examine the log (see AD340) to determine both the type of failure and the action plan used to correct the failure. If no conditions or incidents were recorded in the log, no failures occurred during system operation.

To verify a repair action, ensure that the adapter operates correctly by running the test using the free-lance utility. To do this, enter PAPNB at 80BC and 20B at 81BC (see AD211). Then return the system to the customer. After the customer has used the system, examine the error log for any display/printer adapter failures. If the error log indicates the same failure, perform the next step in the action plan. If the log contains no failures, end the repair action.

AD313 Using the Free-Lance Utility to Determine Intermittent Failures

You can loop the display/printer tests by using the free-lance utility. To do this, enter PAPNB at 80BC and 11B at 81BC (see AD211). The test loops continuously until either the MAP detects an error or you terminate the test by entering an "F" at the MD.

If the MAP detected an error while looping, the MD displays the test error message (see AD231). Record this message and use the "Failure Action Plans" (AD250) to diagnose and repair the failure. Once a repair action has been taken, loop the test for at least 5 minutes to verify the repair.

Note: *If no error is detected by looping the tests, examine the system error log, described in section AD312.*

AD320 Error Log Information Needed for the Display/Printer Adapter

Refer to Chapter 2 (CP750 for DPPX and CP830 for DPCX) for procedures on how to obtain the error log. Perform two searches for log records.

1. Search for log records of the failing port using its PAPN (see AD112).
2. Search for all log records of the failing adapter using its PA (see AD112).

AD330 Error Log Formats and Meanings Used for the Display/Printer Adapter

The format of the error log depends upon the IBM operating system (DPPX or DPCX) being used by the customer. For DPPX, refer to AD331; for DPCX, refer to AD332.

AD331 DPPX Error Log Format and Meaning

The DPPX operating system generates certain class and subclass error log records according to the failure type (Chapter 2, CP740). The AD MAP uses only the class 5, subclass 1 hardware record (CP748) for fault isolation, and has an option field value of 24 and a DT (device type) field value of A. The following describes the class 5, subclass 1 DPPX error log format and meaning used for display/printer attachment.

Note: *The 'x' designations indicate the field size in bytes, where 2 x's = one byte.*

RECORD FORMAT

```
CLASS   05   SUBCLASS   01   OPTION 24
DATE  YY.DDD   TIME  HH/MM/SS
 PA xx   SCA xxxx   DT   A
 CRC xx   COMPSTAT xx   ARC xx
 DATA xxxxxxxx    RES xxxx   CNT  xxxx
 IOEP  xxxxxxxx    ADWA xxxxxxxx
 CA xx   CPR xx    FRWA xxxxxxxx
 RES xxxxxxxx

Extended Data
 D01 xxxx D02 xxxx D03  xxxx D04 xxxx
 D05 xxxx D06 xx
```

RECORD MEANING

The following describes the meaning of those DPPX error log fields used to analyze display/printer storage hardware errors. For a detailed DPPX error log analysis, refer to Chapter 2, CP740.

CLASS	=	5	=	Hardware I/O error
SUBCLASS	=	1	=	Hardware I/O error
DATE	=	YY.DDD	=	The year and Julian date of the log output
TIME	=	HH/MM/SS	=	The hour/minute/second of the log output
PA	=	XF	=	Display/printer attachment physical address
			=	5F =8140 Models B51-B72
			=	1F =1st 8101
			=	2F =2nd 8101
			=	3F =3rd 8101
			=	4F =4th 8101
SCA	=	xxxx	=	Indicates the port number of the failing attached device
DT	=	A	=	Display/printer device type
CRC	=	xx	=	Function module request code (see AD333)
COMPSTAT	=	xx	=	Completion status (see AD333)
ARC	=	xx	=	Adapter status byte (see AD333)
DATA	=	xxxxxxxx	=	Data address
RES	=	xxxx	=	Not used
CNT	=	xxxx	=	Not used
IOEP	=	xxxxxxxx	=	I/O interrupt entry point
ADWA	=	xxxxxxxx	=	Adapter work area address
CA	=	xx	=	Not used
CPR	=	xx	=	Not used
FRWA	=	xxxxxxxx	=	Not used
RES	=	xxxxxxxx	=	Not used

Extended Data

D01 = xxxx = First byte = Device command

		Format 1	Format 2
Bit 0	=	Poll	Poll
Bit 1	=	Read	Not used
Bit 2	=	Write	Prt format
Bit 3	=	Sys ready	Prt format
Bit 4	=	Unlock keyboard	Start printer
Bit 5	=	Erase unprotected	Sound alarm
Bit 6	=	Reset xmit check	End
Bit 7	=	ACK	ACK

= Second byte = Format identifier for device command in first byte
= 00 = Format 1
= 80 = Format 2

D02 = xxxx = Device command for write end poll, same format as D01

D03 = xxxx = First byte = Final device status byte 1 (see AD233)
= Second byte = Final device status byte 2 (see AD233)

Note: *Final device status is the result of a write operation ending poll sequence or of an error detected on a specific poll.*

D04 = xxxx = First byte = Device status byte 1 (see AD233)
= Second byte = Device status byte 2 (see AD233)

Note: *D04 contains device status as a result of an attention interruption.*

D05 = xxxx = First byte = Initial device status byte 1 (see AD233)
= Second byte = Initial device status byte 2 (see AD233)

Note: *D05 contains initial device status as a result of first device error on a write function request.*

D06 = xx = Record length indicator
Bit 0 = 1920-byte transfer
Bit 1 = 480-byte transfer
Bits 2-6 = Not used
Bit 7 = Perform modified data tag shift

AD332 DPCX Condition/Incident Log Formats and Meanings

The DPCX operating system generates five types of Condition/Incident Log (CIL) records according to the failure type (Chapter 2, CP840). The AD MAP uses only the type-1 and type-2 CIL records to analyze display/printer attachment hardware errors. For a detailed DPCX CIL analysis, refer to Chapter 2, CP840.

Note: *The 'x' designations indicate the field size in bytes, where 2 x's = one byte.*

TYPE-1 RECORD FORMAT

```
1-TYPE  I-REC  SEQ xxxx   NA xx   PA xx  LA xx
C-CODE xx          B-STAT xx            C-FR xx
X-STAT1 xx         X-STAT2 xx           S-FR xx
IOCB  xxxx xxxx    RC xx
D1 xxxx  D2 xxxx   D3 xxxx   D4 xxxx
```

TYPE-2 RECORD FORMAT

```
2-TYPE  I-REC  SEQ xxxx   NA xx   PA xx  LA xx
D21 xxxx xxxx          LVL xx        C-FR xx
D22 xxxx xxxx          MC xx         S-FR xx
D23 xxxx   D24 xxxx   D25 xxxx
```

RECORD MEANING

1-TYPE	=		CIL record type-1
2-TYPE	=		CIL record type-2
I-REC	=		Incident record
SEQ	=	xxxx	= A four-digit decimal value from 0001 to 4095 that identifies the relative time when the record occurred.
NA	=	xx	= Number of applications active when the error occurred.
PA	=	xx	= XF = Display/printer attachment physical address = 5F = 8140 Models B51-B72 = 1F = 1st 8101 = 2F = 2nd 8101 = 3F = 3rd 8101 = 4F = 4th 8101
LA	=	xx	= A two-digit hex number indicating the port number (PN) of the failing attached device:

Port (PN)	LA	Port (PN)	LA	Port (PN)	LA	2nd AD Feature (RPQ ML3071) Port (PN)	LA
0	14	8	26	16	3A	0	54
1	15	9	29	17	3B	1	55
2	16	10	2A	18	44	2	56
3	19	11	2B	19	45	3	57
4	1A	12	34	20	46	4	59
5	1B	13	35	21	49	5	9A
6	24	14	36	22	4A	6	9B
7	25	15	39	23	4B	7	(not used)

C-CODE	=	xx	= Completion status (see AD333)
B-STAT	=	xx	= Adapter status byte (see AD333)
C-FR	=	xx	= Function module request code (see AD333)
X-STAT1	=	xx	= Device status byte 1 (see AD233)
X-STAT2	=	xx	= Device status byte 2 (see AD233)
S-FR	=	xx	= System function request; same as C-FR
IOCB	=	xxxxxxxx	= Not used
D1-D4	=	xxxx	= Not used
MC			= System check code = 1X = Program check = 2X = Storage parity error = 4X = I/O timeout = 8X = I/O bus parity error

AD333 DPPX and DPCX Common Error Log Byte Meanings

Certain fields in the DPPX error log and the DPCX condition/incident log, although named differently, have identical bit or byte meanings. The following paragraphs explain these fields and their meanings, as well as list the field names used by each operating system.

Adapter Return Code

You can find the DPPX adapter status byte in the ARC field and the DPCX adapter status byte in the B-STAT field (AD233).

- Bit 0 Overrun (possible system throughput or code problem)
- Bit 1 Parity error (inbound parity error between the adapter and the device)
- Bit 2 Device not available (an error log entry is recorded for an attached device having power off or not connected)
- Bit 3 Busy
- Bit 4 Could not enable the adapter
- Bit 5 Machine check
- Bit 6 Idle poll active
- Bit 7 Invalid function request (possible code error)

Completion Status

You can find the DPPX completion status in the COMPSTAT field and the DPCX completion status in the C-CODE field. The following explains their meanings:

- Bits 0-3 Retry count
- Bit 4 Complete
- Bit 5 Error
- Bit 6 Exception
- Bit 7 Attention

Function Module Request Code

You can find the DPPX function module request code in the CRC field and the DPCX function module request code in the C-FR field. The following explains their meanings:

- 00 Initialize
- 15 Specific poll—restart idle poll
- 16 Write—restart idle poll
- 17 Read—restart idle poll
- 1E Write—restart idle poll
- 1F Read—without start idle poll
- 21 Specific poll—without start idle poll
- 22 Specific poll—without start idle poll
- 23 Start idle poll
- 26 Write—without start idle poll

AD340 How to Use the Error Log

The procedure for examining the error log depends upon the IBM operating system (DPPX or DPCX) being used by the customer. For DPPX, see AD341; for DPCX, see AD342.

AD341 DPPX Error Log

Examine the log records for the failing adapter. The PA indicates the physical address of the failing adapter, and the Secondary Component Address (SCA) indicates the failing port number of the attached device (see AD331).

Obtain the adapter status, found in the ARC field (9) of the log record (See AD331). Convert this hex number to binary (see Appendix A for hex-to-binary conversion). If the ARC has bit 5 on, use the "Machine Check Action Plan" (AD351) to initiate a repair action. If bit 5 is off, determine if more than one attached device (more than one SCA) is recording entries in the log. If only one device is recording entries (all entries have the same SCA), use the "Coaxial Cable or Attached Device Failure Action Plan" (AD357) to initiate a repair action. If more than one device is recording log entries, use the ARC bits that are on, in the order listed below, to determine the type of failure.

ARC Bit On	Meaning	Go to Action Plan
5	Machine Check	AD351
1	Parity Error	AD352
2	Device not available	AD353
0	Overrun/Underrun	AD354
7	Invalid Operation	AD355
None of above	Unknown-type failure	AD356

AD342 DPCX Condition/Incident Log

Examine the log records for the failing adapter. The PA indicates the failing adapter address, and the LA indicates the failing port number of the attached devices (see AD332). If any type-2 format records are found, use the "Machine Check Action Plan" (AD351) to initiate a repair action. If no type-2 records are found, examine the type-1 format records to determine the type of adapter failure. Then determine whether the problem is in the adapter or the attached device.

Obtain the BSTAT from the type-1 record and convert this hex number to binary (see Appendix A for hex-to-binary conversion). If the BSTAT has bit 5 on, use the "Machine Check Action Plan" (AD351) to initiate a repair action. If bit 5 is off, determine if more than one attached device (more than one LA) is recording entries in the log. If only one device is recording entries (all log entries have the same LA), use the "Coaxial Cable or Attached Device Failure Action Plan" (AD357) to initiate a repair action. If more than one device is recording log entries, use the BSTAT bits that are on, in the order listed below, to determine the type of failure:

BSTAT Bit On	Meaning	Go to Action Plan
5	Machine Check	AD351
1	Parity Error	AD352
2	Device Not Available	AD353
0	Overrun/Underrun	AD354
7	Invalid Operation	AD355
None of above	Unknown Adapter Failure	AD356

AD350 Action Plans to Correct Intermittent Failures

To determine the type of error-log failure, refer to "How to Use the Error Log" (AD340), which sends you to the appropriate action plan. Refer to Figures AD350-1, AD350-2 and AD350-3 for card locations.

Card	Location	Comments
AD1	XXB2	XX = board location. **Machine Type / Model / Board (XX)** 8101 / All / A1 or B1 8140 / B51–B72 / C2 or D2 If the 8101 has a B1 board, the adapter is in the B1 board. If the 8140 has a D2 board, the adapter is in the D2 board.
AD2	XXC2	
AD3	XXD2	
AD4	XXE2	
AD5	XXF2	
AD6	XXG2	

Figure AD350-1. Display/Printer Adapter Card Location Chart

Card Location	Associated Ports	Card Location	Associated Ports
XXH2	0 through 3	XXJ4	12 through 15
XXJ2	4 through 7	XXK2	16 through 19
XXH4	8 through 11	XXK4	20 through 23

Figure AD350-2. Display/Printer Driver/Receiver Card Exchange Table

Machine Type	Model	SSCF (SC5)
8101	All	A1A2
8140	B51–B72	C2A2

Figure AD350-3. SSCF Card Location Chart

AD351 Machine Check Action Plan

1. DPCX Type-2 Log Format: An adapter operation caused the processor to detect a machine hardware error, such as incorrect parity.
2. DPCX Type-1 or DPPX Log Format (BSTAT bit 5): The adapter detected a machine hardware error in the adapter bus control circuitry.

Caution: Turn power off when removing or exchanging cards or cables.

Troubleshoot this failure in the sequence listed in the following table and refer to Figures AD350-1 and AD350-3.

Probable Cause	Action	Comments
1. Incorrect voltages	Measure AD and SSCF board voltages: a. F2D03 = +4.5 to +5.5V dc b. F2B11 = +7.7 to +9.3V dc c. F2B06 = −4.5 to −5.5V dc	1. For missing or out-of-tolerance voltages, go to the power MAP.
2. Loose or defective SSCF control cable	Inspect for loose or defective cable.	See Note 1 (AD358).
3. Defective adapter card	Exchange AD4, AD5, and AD6 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
4. Defective adapter card	Exchange AD3, AD2, and AD1 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
5. Defective SSCF card	Exchange SSCF card. See SSCF card location chart, Figure AD350-3.	See Note 3 (AD358).

AD352 Parity Error Action Plan

An inbound parity error between the adapter and the attached device was detected, or a parity error was detected within the adapter's buffers. Troubleshoot this failure in the sequence listed in the following table and refer to Figures AD350-1 and AD350-2 for card locations.

Caution: Turn power off when removing or exchanging cards or cables.

Probable Cause	Action	Comments
1. Defective coaxial I/O cable grounding	Verify I/O cable grounding.	1. Open ground circuit. The I/O panel is grounded through internal I/O cables ADC1, ADC2, and ADC3 (AD111). 2. See Note 1 (AD358).
2. Out-of-tolerance voltage	Measure board voltage: C2B11 = +7.7 to +9.3V dc	For out-of-tolerance voltage, go to power MAP.
3. Defective adapter card	Exchange AD1, AD2, and AD3 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
4. Defective adapter card	Exchange AD6, AD5, and AD4 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
5. Defective I/O driver/ receiver card	Exchange I/O driver card(s) associated with the failing port(s). See Display/Printer Driver/ Receiver Card Exchange Table, Figure AD350-2.	See Note 3 (AD358).

AD353 Device-Not-Available Action Plan

A device-not-available failure indicates that the attached device did not respond to an adapter operation within an allotted time (timeout condition). Troubleshoot this failure according to the sequence listed in the following table and refer to Figures AD350-1 and AD350-2 for card locations.

Note: *Device-not-available status is recorded in the error log for any attached device whose power is off during system initialization.*

Caution: Turn power off when removing or exchanging cards or cables.

Probable Cause	Action	Comments
1. Defective I/O coaxial cable	Inspect I/O coaxial cable and internal cables ADC1, ADC2, ADC3 for loose or defective connection (see AD111).	1. If the problem is with the I/O coaxial cable, inform the customer. 2. If the problem is with the I/O panel or internal cable ADC1, ADC2, or ADC3, make necessary corrections. 3. See Note 1 (AD358).
2. Defective adapter card	Exchange AD6, AD5, and AD1 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
3. Defective I/O driver/receiver card(s)	Exchange the I/O driver/receiver card(s) associated with the failing port(s). See Display/Printer Driver/Receiver Card Exchange Table, Figure AD350-2.	See Notes 1 and 2 (AD358).
4. Defective adapter card	Exchange AD2, AD3, and AD4 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Note 3 (AD358).

AD354 Overrun/Underrun Action Plan

An overrun/underrun failure indicates that adapter buffer data was either not sent to the device for a write operation, or not stored in processor storage for a read operation. The new data overlaid the old data in adapter buffer storage. Troubleshoot this failure according to the sequence listed in the following table and refer to Figures AD350-1 and AD350-3 for card locations.

Note: *An overrun/underrun failure can be caused by system overusage or by a program error.*

Caution: Turn power off when removing or exchanging cards or cables.

Probable Cause	Action	Comments
1. Defective adapter card	Exchange AD1, AD2, and AD4 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
2. Defective adapter card	Exchange AD3, AD5, and AD6 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
3. Defective SSCF card	Exchange SSCF card. See SSCF card location chart, Figure AD350-3.	See Note 3 (AD358).

AD355 Invalid Operation Action Plan

An invalid operation failure indicates that the operation being requested cannot be performed because of the state of the adapter. Troubleshoot this failure according to the sequence listed in the following table and refer to Figure AD350-1 for card locations.

Note: *An invalid operation failure can be caused by a program error.*

Caution: Turn power off when removing or exchanging cards or cables.

Probable Cause	Action	Comments
1. Defective adapter card	Exchange AD4, AD5, and AD6 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
2. Defective adapter card	Exchange AD1, AD2, and AD3 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Note 3 (AD358).

AD356 Adapter Failure Action Plan

An unknown adapter failure was detected. Troubleshoot this failure in the sequence listed in the following table and refer to Figures AD350-1, AD350-2, and AD350-3 for card locations

Caution: Turn power off when removing or exchanging cards or cables.

Probable Cause	Action	Comments
1. Defective adapter card	Exchange AD1, AD2, and AD3 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
2. Defective adapter card	Exchange AD4, AD5, and AD6 cards with new ones. See Display/Printer Adapter Card Location Chart, Figure AD350-1.	See Notes 1 and 2 (AD358).
3. Defective I/O driver/receiver card	Exchange the I/O driver/receiver card(s) associated with the failing ports. See Display/Printer Driver/Receiver Card Exchange Table, Figure AD350-2.	See Notes 1 and 2 (AD358).
4. Defective SSCF card	Exchange the SSCF card. See SSCF card location chart, Figure AD350-3.	See Note 3 (AD358).

AD357 Coaxial Cable or Attached Device Failure Action Plan

Only one port (only one attached device) on the adapter is causing a failure. Troubleshoot this failure in the sequence listed in the following table.

Note: *If an attached device has its power off during system initialization, an error log recording is made indicating device not available status (bit 2 in BSTAT for DPCX; ARC for DPPX).*

Caution: Turn power off when removing or exchanging cards or cables.

Probable Cause	Action	Comments
1. Defective coaxial I/O cable	Inspect I/O cable for loose or defective connection	1. If the problem is with the cable, inform the customer. 2. If the problem is with the I/O panel or internal cable ADC1, ADC2, or ADC3, make necessary correction (see AD420). 3. See Note 4 (AD358).
2. Defective attached device on failing port	Record the device status bytes in the log (see AD331 or AD332). Refer to the attached device's MIM (see AD500).	See Note 5 (AD358.)

AD358 Common Action Plan Notes

1. To verify the fix: run the display/printer tests. At the 80BC message, enter PAPNB; at the 81BC message, enter 20B (see AD211). If the test fails (see AD231), record the test error message and use the AD MAP, menu selection C, to find the failure. The tests should run to successful completion (PA00). Return the system to the customer. Obtain a new error log after the customer has used the system. If the log indicates the same failure, go to the next step in the table. End repair action when there are no display/printer failures indicated in the log.
2. If this same failure occurs after exchanging cards, replace the original cards and go to the next step in the table.
3. If this same failure occurs after completing the last step in the table, replace the original cards and request aid.
4. To verify the fix: return the system to the customer. Obtain a new error log after the customer has used the system. If the log indicates that the same port is failing, go to the next step in the table. End repair action when there are no display/printer failures indicated in the log.
5. If no problem is found in the attached device, go to AD340 and determine the type of failure using either the BSTAT or ARC bit in the log.

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AD400 Signal Paths and Detailed Operational Description

AD410 Board Signal Paths

Using the test error message, check continuity between the test points indicated by the error message in the AD411 (adapter-to-SSCF), AD412 (adapter), and AD413 (adapter-to-I/O drivers) signal path lists.

AD411 Adapter-to-SSCF Signal Path Check

1. Check the continuity between the adapter test point and the related SSCF test point using the table below. [See System Control Facility (SC) section of Chapter 5 for SSCF test points.] Use machine line names to determine the point-to-point continuity check. Use the failing routine number of the test error message to determine which lines should be checked.
2. If an open circuit is found, determine whether the open is in the cable or in the board signal path. If in the cable, repair the cable (a temporary fix of the cable can be made by wire-wrapping the test points together). If the open is in the board signal path, correct by wire-wrapping.
3. To verify the fix, run the display/printer tests. At 80BC, enter PAPNB; at 81BC, enter 20B (see AD211).

Test Error Message	Line Name	Adapter Test Point
PAXE 01XX	– Data Tag	E2D02
	– Address Tag	E2D06
	– Valid Halfword	B2B05
	– Bus Bit P0	C2G04
	– Bus Bit 0	C2J06
	– Bus Bit 1	C2G05
	– Bus Bit 2	C2D09
	– Bus Bit 3	C2G02
	– Bus Bit 4	C2J02
	– Bus Bit 5	C2B10
	– Bus Bit 6	C2G03
	– Bus Bit 7	C2D12
	– Bus Bit P1	C2J12
	– Bus Bit 8	C2M04
	– Bus Bit 9	C2P04
	– Bus Bit 10	C2P02
	– Bus Bit 11	C2P07
	– Bus Bit 12	C2M02
	– Bus Bit 14	C2J11
	– Bus Bit 15	C2G13
PAXE 04XX	– Channel Request Med	B2D05
	– End of Chain	B2P09
PA80	– Channel Grant Medium	E2B08
A0BC	– IPR	E2M13
ACBC	– Bus Bit 13	C2P05
Intermittent Problems	– Halt	E2P02
	– I/O Tag Halfword	E2S03
	– System Reset	E2D04
	– Parity Valid	F2G08
	– IR/B1-7	E2M13
	– Release	C2P09

AD412 Adapter Signal Path Check

1. Check the continuity between each test point for the failing routine number in the test error message, as shown in the table below.
2. If an open circuit is found, correct by wire-wrapping the test points together.
3. To verify the fix, run the display/printer tests. At 80BC, enter PAPNB; at 81BC, enter 20B (see AD211).

Test Error Message	Test Point A	Test Point B	Test Point C	Test Point D	Test Point E
PAXE 01XX	B2D09	E2G03			
	B2G04	E2U05			
	C2B04	C2D08			
	C2B07	C2D08			
	C2D02	C2D08			
	C2D07	E2M02			
	E2J04	E2B05			
	E2P12	E2G07			
	E2P09	E2S04			
	E2U04	F2P05			
	C2M05	D2D05	E2D07	F2J07	
	C2M09	E2D11	F2U11		
	C2U05	E2B13	G2B12		
	C2M07	D2B04	E2D10	F2P11	
	B2J10	E2S05	F2S02	G2G02	
	D2M04	E2S09	F2J05		
	B2P10	E2B07	G2J11		
	C2B13	D2D11	E2U09	F2S09	
	C2B02	D2B10	E2M08	F2D05	
	C2M13	D2B07	E2P04	F2D06	
	C2G08	D2D06	E2U07	F2G10	
	C2P10	D2B05	E2D12	F2G09	
	C2B09	C2D10	D2D09	E2S08	F2S10
	C2B12	D2D10	E2P06	F2S12	
	C2M10	D2B09	E2B10	F2J10	
	C2P11	D2D04	E2D13	F2M04	
	C2M08	D2B02	E2B09	F2P06	
	C2U12	C2J04	F2D11		
PAXE 02XX	C2P12	D2B03	E2B12	F2U09	
	C2P13	D2D02	E2M03	F2G13	
PAXE 03XX	E2U04	F2P05			
	E2J07	F2M07			

Test Error Message	Test Point A	Test Point B	Test Point C	Test Point D	Test Point E
PAXE 04XX	C2M05	D2D05	E2D07	F2J07	
	C2M09	E2D11	F2U11		
	C2U05	E2B13	G2B12		
	C2M07	D2B04	E2D10	F2P11	
	B2J10	E2S05	F2S02	G2G02	
	D2M04	E2S09	F2J05		
	B2P10	E2B07	G2J11		
	B2M02	E2D02			
	B2J07	F2M09			
	B2P02	G2D12			
	B2P04	D2P06			
	B2G12	D2M08			
	B2M04	D2G05			
	B2M12	D2S03			
	B2D06	D2S04			
	B2D04	G2U09			
	B2B08	E2D05	F2B12		
	B2J05	E2U06			
	B2M07	F2B08	G2B05		
	B2G03	G2G13			
	B2S08	F2D07	G2P06		
	C2P06	E2M05	E2P05		
	D2B13	E2J13			
	D2D12	G2G03			
	D2G13	G2M02			
	D2P02	E2U12			
	D2J02	G2P04			
	D2J05	G2S03			
	D2G03	F2B05	G2U11		
	E2S07	G2J02			
	E2D09	G2G04			
	E2S12	F2G05			
	F2M08	G2M05			
	F2G07	F2J02			
	F2P02	F2P04			
	F2B07	G2S12			
	F2J09	G2M13			
	G2D04	G2U04			
	G2S02	G2S10			
	G2M09	G2B02			
	B2M10	C2S13	D2U04		
	E2J10	F2M13	G2B13		
	D2M03	F2M05	G2D13		
	F2M03	F2M12			
	F2B03	G2S13	G2S05		
	B2M05	C2S05	E2S02	F2G04	G2U02
	B2D02	E2M07	G2G10		
	B2J13	D2G04	F2D12	G2U05	G2J12
	B2B13	D2G02	G2P11		
	C2B05	D2D07	F2S13		

Test Error Message	Test Point A	Test Point B	Test Point C	Test Point D	Test Point E
PAXE 05XX	C2B13	D2D11	E2U09	F2S09	
	C2B02	D2B10	E2M08	F2D05	
	C2M13	D2B07	E2P04	F2D06	
	C2G08	D2D06	E2U07	F2G10	
	C2P10	D2B05	E2D12	F2G09	
	B2M10	C2S13	D2U04		
	E2J10	F2M13	G2B13		
	D2M03	F2M05	G2D13		
	F2M03	F2M12			
	F2B03	G2S13	G2S05		
	B2M05	C2S05	E2S02	F2G04	G2U02
	B2D02	E2M07	G2G10		
	B2J13	D2G04	F2D12	G2U05	G2J12
	B2M03	D2J09			
	B2D11	C2D06			
	B2B12	C2U02			
	B2S03	C2M12	D2B12		
	B2U12	C2G09			
	B2D10	C2P09			
	B2G02	C2U07			
	B2J12	C2J13			
	B2M08	C2S12			
	B2U11	C2M03			
	B2M13	C2D13			
	B2U02	C2J05			
	B2D07	C2S07			
	B2S07	C2S03			
	B2P06	C2D04	D2J11	E2M04	F2D10
	B2S13	D2P07	E2S10	F2M02	G2M08
	B2P07	E2U10	F2U10	G2B03	
	B2G08	G2U10			
	B2G10	D2J12	F2B09	G2S08	
	B2D13	F2J11	G2M12		
	B2G07	C2G12	G2U12		
	D2J04	F2B04			
	D2J06	F2B02			
	E2G04	G2J10			
	F2B13	G2G07			
	F2J12	G2J07			
	B2S12	D2U11			
	B2U04	D2S10			
	B2U10	D2U06			
	B2B02	C2U13	D2J13	E2G10	
	F2D04	G2B10			

Test Error Message	Test Point A	Test Point B	Test Point C	Test Point D	Test Point E
PAXE 06XX	C2M07 C2B02 C2M13 C2G08 C2P10 C2B09 C2B12 C2M10 C2P11 C2M08 C2U12 C2P12 C2P13 B2B13 C2B05 B2S12 B2U04 B2U10 B2B02 B2P05 B2J09 B2S05 B2U06 B2S04 B2U09 B2S10 B2B04 B2J02 C2B08 D2G08 F2J06 F2S03 F2D02 F2G12 G2P10 G2D02 E2B02 E2S13 E2M10	D2B04 D2B10 D2B07 D2D06 D2B05 C2D10 D2D10 D2B09 D2D04 D2B02 C2J04 D2B03 D2D02 D2G02 D2D07 D2U11 D2S10 D2U06 C2U13 C2S04 C2S02 D2U12 D2S09 D2S08 D2U10 D2U02 D2M02 C2B03 D2B08 F2D09 F2G02 F2S05 G2M03 G2D09 G2P05 G2U07 F2J13 F2J04 F2U12	E2D10 E2M08 E2P04 E2U07 E2D12 D2D09 E2P06 E2B10 E2D13 E2B09 F2D11 E2B12 E2M03 G2P11 F2S13 D2J13 F2U13 G2D07 G2P13 G2G05 G2D06	F2P11 f2D05 F2D06 F2G10 F2G09 E2S08 F2S12 F2J10 F2M04 F2P06 F2U09 F2G13 E2G10	F2S10
PAXE 07XX	C2P13	D2D02	E2M03	F2G13	
PAXE 08XX	B2J04	E2G05	F2M10	G2S09	
PAXE 09XX	D2G07	G2U13			
PAXE 0BXX	D2J07 E2G13	G2B09 F2S04			
PAXE 0CXX	E2B02 D2J07 E2G13	F2J13 G2B09 F2S04	G2P13		
PA70	F2S08	G2M04			

Test Error Message	Test Point A	Test Point B	Test Point C	Test Point D	Test Point E
PA71	F2D04 D2D13	G2B10 G2B07			
PA80	B2P10 B2M05 E2S13 B2P12 B2P11 B2G09 B2D12 B2J11 B2P13 E2B04	E2B07 C2S05 F2J04 C2S10 F2G03 C2U11 C2U10 C2U09 C2G10 G2J09	G2J11 E2S02 G2G05	F2G04	G2U02
A0BC	B2J10 D2M04 D2M05	E2S05 E2S09 F2D13	F2S02 F2J05	G2G02	
A8BC	B2B03	C2D05			
0EFF–ACBC	B2G13	G2P02			
92BC	B2D02 B2J13 E2M10 B2B07 B2U07 E2G08	E2M07 D2G04 F2U12 C2U04 C2S08 G2J13	G2G10 F2D12 G2D06	G2U05	G2J12
Intermittent Problems	B2B09 B2G05 C2U06 D2G09 E2G09 E2U13 F2U02	B2J06 C2J07 E2J02 G2G08 G2J06 G2P12 G2S04	E2B03		

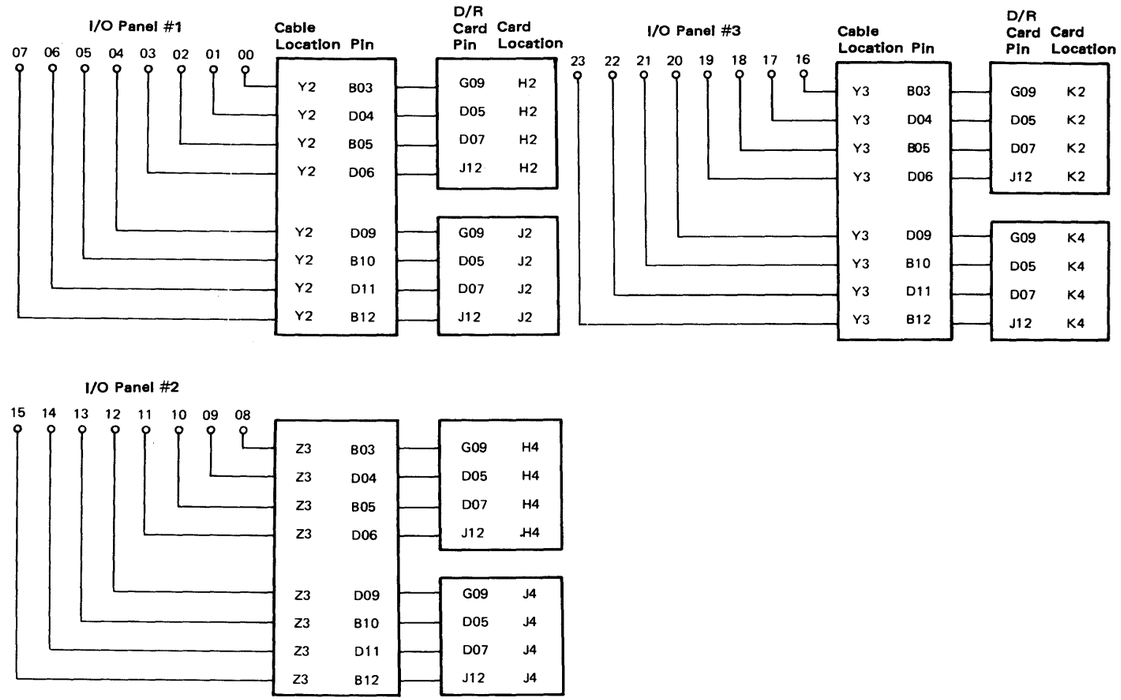
AD413 Adapter-to-I/O Driver/Receiver Signal Path Check

1. Check continuity between the source test point and the test points for the ports installed for the failing routine number in the test error message, as shown in the table below.
2. If an open circuit is found, correct by wire-wrapping together the source test point and the related port test points.
3. To verify the fix, run the display/printer tests. At 80BC, enter PAPNB; at 81BC, enter 20B (see AD211).

Test Error Message	Source Test Point	Ports 0–3	Ports 4–7	Ports 8–11	Ports 12–15	Ports 16–19	Ports 20–23
PAXE 04XX	F2P12	H2D10	J2D10	H4D10	J4D10	K2D10	K4D10
or	F2P13	H2B12	J2B12	H4B12	J4B12	K2B12	K4B12
PAXE 0CXX	G2G12					K2D09	K4D09
	G2P09	H2D09	J2D09	H4D09	J4D09		
	G2P07	H2D06	J2D06	H4D06	J4D06	K2D06	K4D06
	A2B13	H2D13	J2D13	H4D13	J4D13	K2D13	K4D13
PAXE 04XX	F2P09			H4B02	J4B02		
or	F2P10		J2D02		J4D02		K4D02
PAXE 0BXX	F2U06	H2B02	J2B02			K2B02	K4B02
or	F2U07	H2D02		H4D02		K2D02	
PAXE 0CXX	F2P07					K2B03	K4B03
or	F2U04	H2B03	J2B03	H4B03	J4B03		
PAXE 0DXX							
PAXE 0BXX	G2B04	H2B08	J2B08	H4B08	J4B08		
or	G2D05					K2B08	K4B08
PAXE 0CXX	G2B08	H2J07	J2J04	H4J07	J4J07	K2J07	K4J07
or	G2D10	H2G08	J2G08	H4G08	J4G08	K2G08	K4G08
PAXE 0DXX	G2D11	H2B10	J2B10	H4B10	J4B10	K2B10	K4B10
	G2M07	H2G10	J2G10	H4G10	J4G10	K2G10	K4G10

AD420 Adapter-to-Port Signal Path Check

1. Check the continuity from the center of the I/O panel coaxial socket to the driver/receiver pin, shown in the figure below. Check the I/O socket ground by checking continuity from the outer part of the I/O panel coaxial socket to any D08 pin on the display/printer adapter board.
2. If you find an open circuit, determine whether the open circuit is in the cable or in the board signal path.
   a. If the open is in the cable, repair the cable.
   b. If the open is in the board signal path, correct by wire-wrapping.



AD450 Display/Printer Adapter Detailed Description and Data Flow

Sections AD451, AD452, and AD453 describe the read, write, and CHIO control operations. See Figure AD450-1 for data flow.

AD451 Read Operation

A program-function request initiates a read operation. An Initiate CHIO command passes a channel control vector (CHCV), the device address, the record length (480 or 1920 bytes), and the function to be performed, to the adapter hardware. The adapter then makes a channel request (using the CHCV) to obtain the Read command from a control area in processor storage. The Read command is written into the adapter buffer and then loaded into the data-out register; from there it is loaded into the SERDES (serializer/deserializer) and transmitted serially-by-bit to the device.

At this point the hardware starts a timeout function. If the device responds before the timeout occurs, the timeout function is reset. If the timeout occurs (no response from the device), the read operation is terminated; bit 7 of the basic status byte is set and an I/O interruption is requested.

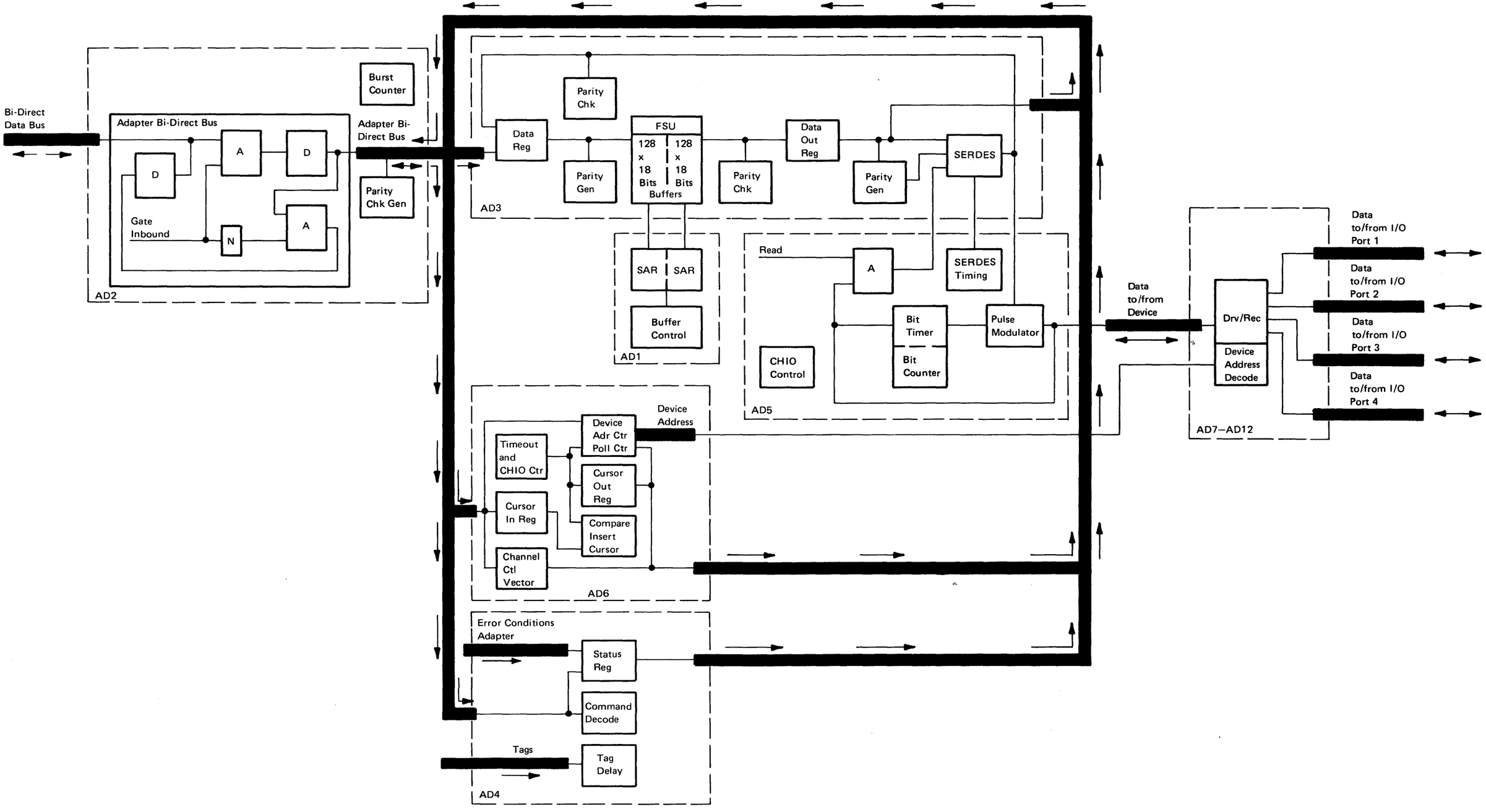


Figure AD450-1. Display/Printer Adapter Functional Diagram

Data is transmitted from the device serially-by-bit and shifted into the SERDES from the serial-data-in line. When 26 bits have been accumulated in the SERDES, certain bits such as busy, data/control, and parity are removed and the remaining 16-bit halfword is transferred to the data-in register. A buffer storage cycle is initiated, and the contents of the data-in register are stored into the appropriate alternate buffer. (A halfword is written into a buffer about every 22 usec.) Because this is a synchronous operation, any outstanding asynchronous storage request to the other alternate buffer to read data to the processor is temporarily suspended.

The acceptance of data continues until the alternate buffer is full (256 bytes). At this point, the hardware does two things. First, the hardware switches to the other alternate buffer and loads that buffer with either the next 256 bytes from the device for a 1920-byte transfer or with the final message increment of 224 bytes for a 480-byte transfer. Second, and concurrent with the first, the hardware makes a channel request (using the channel control vector originally presented) and transfers the contents of the first alternate buffer (from the data-out register) to a data area in processor storage. This transfer is done in burst mode (data chaining) according to the value in the burst length counter (see AD453).

When the contents of this alternate buffer have been completely transferred to the processor, the data transfer stops until the other alternate buffer is full of data (256 bytes or the final message increment), at which time data transfer starts again. This buffer alternating action continues until the complete message (480 or 1920 bytes) has been transferred to processor storage.

After the last data transfer has occurred, the adapter makes another channel request (using the original channel control vector) to store the cursor record pointer (which has been stored in the cursor-in register) in processor storage at the next halfword location following the Read command. The adapter then generates an interruption (by setting bit 7 in the basic status byte) to indicate to the program that the function requested (read) has been completed. The program then issues a Read Basic Status command to determine if the read operation was completed without an error. The data-in register receives the status from the device. The status is stored in one of the empty alternate buffers and is then available to be read into processor storage by a CHIO operation.

AD452 Write Operation

A program-function request initiates a write operation. An Initiate CHIO command passes a channel control vector (CHCV), the device address, the record length (480 or 1920 bytes), and the function to be performed, to the adapter hardware. The adapter then makes a channel request (using the CHCV) to obtain the Write command and the cursor pointer from a control area in processor storage. The Write command is written into the adapter buffer and then loaded into the data-out register. The cursor pointer is loaded into the cursor-out register. The adapter then makes another channel request (using the CHCV) to obtain the message from a data area in processor storage.

A CHIO operation loads data from processor storage into the halfword data-in register. A buffer storage cycle is initiated, and the contents of the data-in register are stored in the appropriate alternate buffer. This operation may stop temporarily if there is an outstanding synchronous storage request to the other alternate buffer to read data out of that buffer for transmission to the device (from the data-out register and the SERDES).

The first 256 bytes of the message are written into one of the alternate buffers. This transfer is done in burst mode (data chaining) according to the value in the burst length counter (see AD453). When this buffer is full (256 bytes), the adapter does two things. First, the Write command, which is still in the data-out register, is loaded into the SERDES and transmitted serially-by-bit to the device. The first halfword of the message is read from the alternate buffer into the data-out register and then loaded into the SERDES. After the last bit of the Write command has been transmitted, a halfword is read from the alternate buffer to the SERDES about once every 33 usec. Second, and concurrent with the first, the adapter switches to the other alternate buffer and makes a channel request to load that buffer with either the next 256 bytes for a 1920-byte transfer or with the final message increment of 224 bytes for a 480-byte transfer. This buffer alternating action continues until the complete message (480 or 1920 bytes) has been transmitted to the device.

When the last halfword of the message has been loaded into an alternate buffer and as soon as one of the buffers becomes available (that is, its contents have been transferred to the SERDES), the adapter makes a channel request (using the CHCV) to obtain a Poll command from processor storage, which is the next halfword following the cursor pointer. This Poll command, which is written into the buffer and transmitted to the device immediately following the 480- or 1920-byte message, is an end-of-record signal to the device. The device status is sent to the adapter and stored in one of the alternate buffers. The adapter then makes a channel request and stores the device status in processor storage in the next halfword location following the Poll command. The adapter then generates an interruption (by setting bit 7 in the basic status byte) to indicate to the program that the function requested (write) has been completed. The program then issues a Read Basic Status command and examines both adapter and device status to determine if the write operation was completed without an error.

AD453 CHIO Adapter Operation

The adapter initiates and terminates all channel operations. A burst length counter, which is set for 128 halfwords (256 bytes), provides for data chaining under one channel grant signal. The burst length count specifies the minimum number of halfwords to be transferred between the channel grant signal and the end-of-chain (EOC) signal. An active release signal causes the adapter to prematurely end the operation and respond to the data tag signal with EOC. If the adapter detects the release signal when the data tag is active, the adapter responds to that data tag with a valid signal (assuming this transfer is not the last data transfer) and then responds to the next data tag with EOC. Once the adapter has responded to the data tag signal with EOC, it leaves its channel request signal on (assuming there is more data to be transferred), and waits for a channel grant signal to resume the CHIO operation.

AD470 Card Logic Signals

Figures AD470-1 through AD470-6 show the logic signals for cards AD1 through AD6, respectively; Figure AD470-7 shows cards AD7 through AD12.

AD2	+	Ending Lth 2	S07	AD1 B2	J07	+	Invert Bit 6	AD5
AD4	–	Ch Grant Low	P10		P12	–	Data Mode 1 Pwr	AD2
AD5	+	1920 or 480 Byte Xfer	M07		P11	–	TN Wr Cursor	AD5
AD2	+	B Busy	M08		P02	+	SERDES Osc	AD6
AD2	–	End of Data Lth	P13		G09	–	Wr Dev	AD2
AD4	+	Invert Bit 6	J05		M10	+	Wr Bfr Mode (–Rd Mode)	AD2–AD3
AD5	+	CHIO CB Bit 0 On	P07		P04	–	Ld Bfr in Reg	AD3
AD4	–	Reset	J04		G12	–	Ld Bfr Out Reg	AD3
AD6	+	Load Data Out Regs	G08		M03	–	Gate Dev Status	AD3
AD6	+	Wrt Poll Latch Set	G10		M04	–	Gate Xmit	AD3
AD6	+	Adapt Channel I/O Time	J10		D09	+	Parity Error	AD4
AD2	+	A Busy	J11		D05	–	Ch Req Low (CHIO Req)	SC5
AD2	–	A Full	G02		P09	–	EOC	SC5
AD2	–	B Full	J12		B05	–	Valid Halfwd to Wc	SC5
AD6	+	Channel I/O Request	G13		D11	+	Break In	AD2
AD6	–	End of Chain	G03		B12	+	T1	AD2
AD2	+	Buffer EOC Lth	J02		D12	+	T3	AD2
AD4	–	Valid Halfword	G04		S03	+	T6	AD2
AD4	+	Osc	B08		S02		Unused	
AD2	–	Parity Error	G05		B03	–	Rd Out Cmd	AD2
SC5	–	Data Tag	M02		U12	+	Partial Fullset EOD	AD2
AD6	+	Bit Counter 10	D13		D10	+	Hi Buff Adr	AD2
AD6	+	In Reg Ctr 1	B13		M12	–	Res to FSU	AD3
AD6	+	Load Data Latch Set	J13		D06	–	Sel to FSU	AD3
AD2	+	480 Xfer	U02		U05	–	Step Up SAR Tp	
AD2	+	1920 Xfer. 7 B Act	M13		D04	–	CHIO Grant	AD6
AD2	+	B Active	U11		B02	+	CHIO Req 1	AD4
	–	2 Byte Xfer Tie On	J06–B09		B04	–	CHIO Not CHIO Grant	AD3
AD4	–	Set Dev Cmd CHIO Req	M05		B10		Unused	
AD4	+	Wrt Sample SS On	D02		B07	–	Bfr Val	AD2
AD6	+	Command Loaded	G07		U07	+	EDC	AD2
AD2	–	Ending Latch 1	D07		M09	–	SAR Out TP 1	
AD6	–	Cmd Response Set CHIO Req	S08		U13	–	SAR Out TP 2	
AD2	–	Ovrn/Undrn	P06		S13		Unused	
AD2	+	Busy Exit	P05		S09		Unused	
AD5	+	Channel I/O Ctr 0	S13		S05	–	SAB Bit 0	AD3
AD2	+	Early Busy Reset	J09		U06	–	SAB Bit 1	AD3
					S04	–	SAB Bit 2	AD3
					S12	–	SAB Bit 3	AD3
					U04	–	SAB Bit 4	AD3
					U10	–	SAB Bit 5	AD3
					U09	–	SAB Bit 6	AD3
					S10	–	SAB Bit 7	AD3

Figure AD470-1. AD1 Card Logic Signals

SC5	–	Data Bit P0	G04	AD2 C2	B13	–	Adapter Bus Bit 0
SC5	–	Data Bit 0	J06		B09	–	Adapter Bus Bit 1
SC5	–	Data Bit 1	G05		B12	–	Adapter Bus Bit 2
SC5	–	Data Bit 2	D09		B08	–	Adapter Bus Bit 3
SC5	–	Data Bit 3	G02		B05	–	Adapter Bus Bit 4
SC5	–	Data Bit 4	J02		B02	–	Adapter Bus Bit 5
SC5	–	Data Bit 5	B10		M13	–	Adapter Bus Bit 6
SC5	–	Data Bit 6	G03		G08	–	Adapter Bus Bit 7
SC5	–	Data Bit 7	D12		M05	–	Adapter Bus Bit 8
SC5	–	Data Bit P1	J12		M10	–	Adapter Bus Bit 9
SC5	–	Data Bit 8	M04		P10	–	Adapter Bus Bit 10
SC5	–	Data Bit 9	P04		P12	–	Adapter Bus Bit 11
SC5	–	Data Bit 10	P02		P13	–	Adapter Bus Bit 12
SC5	–	Data Bit 11	P07		P11	–	Adapter Bus Bit 13
SC5	–	Data Bit 12	M02		M07	–	Adapter Bus Bit 14
SC5	–	Data Bit 13	P05		M08	–	Adapter Bus Bit 15
SC5	–	Data Bit 14	J11		U07	–	A Full
SC5	–	Data Bit 15	G13		U09	+	A Busy
SC5		Select Low (Feature Bd)	D10		J13	–	B Full
AD1	+	T1	U02		S12	+	B Busy
AD1	+	T3	U10		M03	+	B Active
AD1	+	T6	MD		D13	+	1920 Xfer. 7 B Act
AD1	–	Rd Out Cmd	D05		G10	–	End of Data Lth
AD1	+	Break In	D06		B03	+	Buffer EOC Lth
AD1	+	EOC	S08		J05	+	480 Xfer
AD1	+	CHIO Req 1	U13		J07	–	Parity Error
AD1	+	Wr Bfr Mode (–Rd Mode)	S13		P06	–	Ovrn/Undrn
AD1	–	Wr Dev	U11		D07	–	Address Compare
AD1	–	Data Mode 1 Pwr	S10		S07	–	Ending Latch 1
AD1	+	Partial Fullset EOD	G09		D11	+	5 Volt Tie Up – 2K
AD1	+	Hi Buff Adr	P09		S03	+	Ending Lth 2
AD4	–	Reset	S05		U06	–	Data in Parity Chk
AD4	–	Set Dev CMD CHIO Req	D04		S02	–	Burst=0 Set EOC TP
AD4	+	Load CHIO CB	M09				
AD6	+	Command Loaded	G12				
AD5	–	Gate Inbound	J04–U12		S04	+	Early Busy Reset
						+	Busy Exit
AD1	–	Bfr Val	U04		D08	–	Ground
AD4	+	Data Tag Delayed	U05				
SC5	–	Release	S09				
	+	Tie Up Bit 1	J09				
	+	Tie Up Bit 2	J10				
	+	Tie Up Bit 4	G07				
	–	Address Bit 5	B04				
	–	Address Bit 6	B07				
	–	Address Bit 7	D02				

AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD3 – AD5
AD3 – AD5
AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD3 – AD5 – AD4
AD1
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AD1 – AD4
AD1 – AD4
AD4
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AD1
AD4
AD1
AD1

Figure AD470-2. AD2 Card Logic Signals

AD2	–	Adapter Bus Bit 0	D11
AD2	–	Adapter Bus Bit 1	D09
AD2	–	Adapter Bus Bit 2	D10
AD2	–	Adapter Bus Bit 3	B08
AD2	–	Adapter Bus Bit 4	D07
AD2	–	Adapter But Bit 5	B10
AD2	–	Adapter Bus Bit 6	B07
AD2	–	Adapter Bus Bit 7	D06
AD2	–	Adapter Bus Bit 8	D05
AD2	–	Adapter Bus Bit 9	B09
AD2	–	Adapter Bus Bit 10	B05
AD2	–	Adapter Bus Bit 11	B03
AD2	–	Adapter Bus Bit 12	D02
AD2	–	Adapter Bus Bit 13	D04
AD2	–	Adapter Bus Bit 14	B04
AD2	–	Adapter Bus Bit 15	B02
AD1	–	SAB Bit 0	U12
AD1	–	SAB Bit 1	S09
AD1	–	SAB Bit 2	S08
AD1	–	SAB Bit 3	U11
AD1	–	SAB Bit 4	S10
AD1	–	SAB Bit 5	U06
AD1	–	SAB Bit 6	U10
AD1	–	SAB Bit 7	U02
AD1	+	T6	B12
AD6	+	In Reg Ctr 1	G02
AD6	+	Load SERDES	G03
AD6	+	Load Data Latch Set	G04
AD1	–	Gate Xmit	G05
AD6	–	Reset Load Data Latch	G07
AD6	–	Set Ser Int Chk	G09
AD6	+	Data Ser In	J02
AD5	–	Insert Cursor 1	J04
AD5	–	Insert Cursor 2	J06
AD6	+	Xmit or Rec Shift Serdes	J05
AD1	–	Gate Dev Status	J09
AD6	+	Wrt Poll Latch Set	J12
AD1	–	Ld Bfr Out Reg	M08
AD1	–	Ld Bfr in Reg	P06
AD1	–	Res to FSU	S03
AD1	–	Sel to FSU	S04
AD1	+	Wr Bfr Mode (–Rd Mode)	U04
AD1	–	CHIO Not CHIO Grant	M02
AD6	–	Gate Dev Status to Bus	M03
AD4	+	Gate CHIO CB to Bus	M04
AD1	+	CHIO Req 1	J13
AD4	–	Overrun	J11
AD5	+	Channel I/O Ctr 0	P07

AD3
D2

B13	–	Bad Parity OR'ed	AD4
D12	+	Bad Serdes Parity	AD6
D13	+	Avail and Ready	AD6
G08	+	SERDES Out Bit 20	AD5 – AD6
G13	+	Serial Out Bit On	AD6
J07	+	SERDES Out Bit 23	AD6
M05	+	Gate Data or CHIO CB to Bus	AD5
S12		Bfr in Bit P1 TP	
M09		Bfr in Bit 0 TP	
P09		Bfr in Bit 1 TP	
M10		Bfr in Bit 2 TP	
P10		Bfr in Bit 3 TP	
S13		Bfr in Bit 4 TP	
U13		Bfr in Bit 5 TP	
M12		Bfr in Bit 6 TP	
P12		Bfr in Bit 7 TP	
P13		Bfr in Bit P2 TP	
S02		Bfr in Bit 8 TP	
P11		Bfr in Bit 9 TP	
S07		Bfr in Bit 10 TP	
U09		Bfr in Bit 11 TP	
S05		Bfr in Bit 12 TP	
U05		Bfr in Bit 13 TP	
U07		Bfr in Bit 14 TP	
M13		Bfr in Bit 15 TP	

Figure AD470-3. AD3 Card Logic Signals

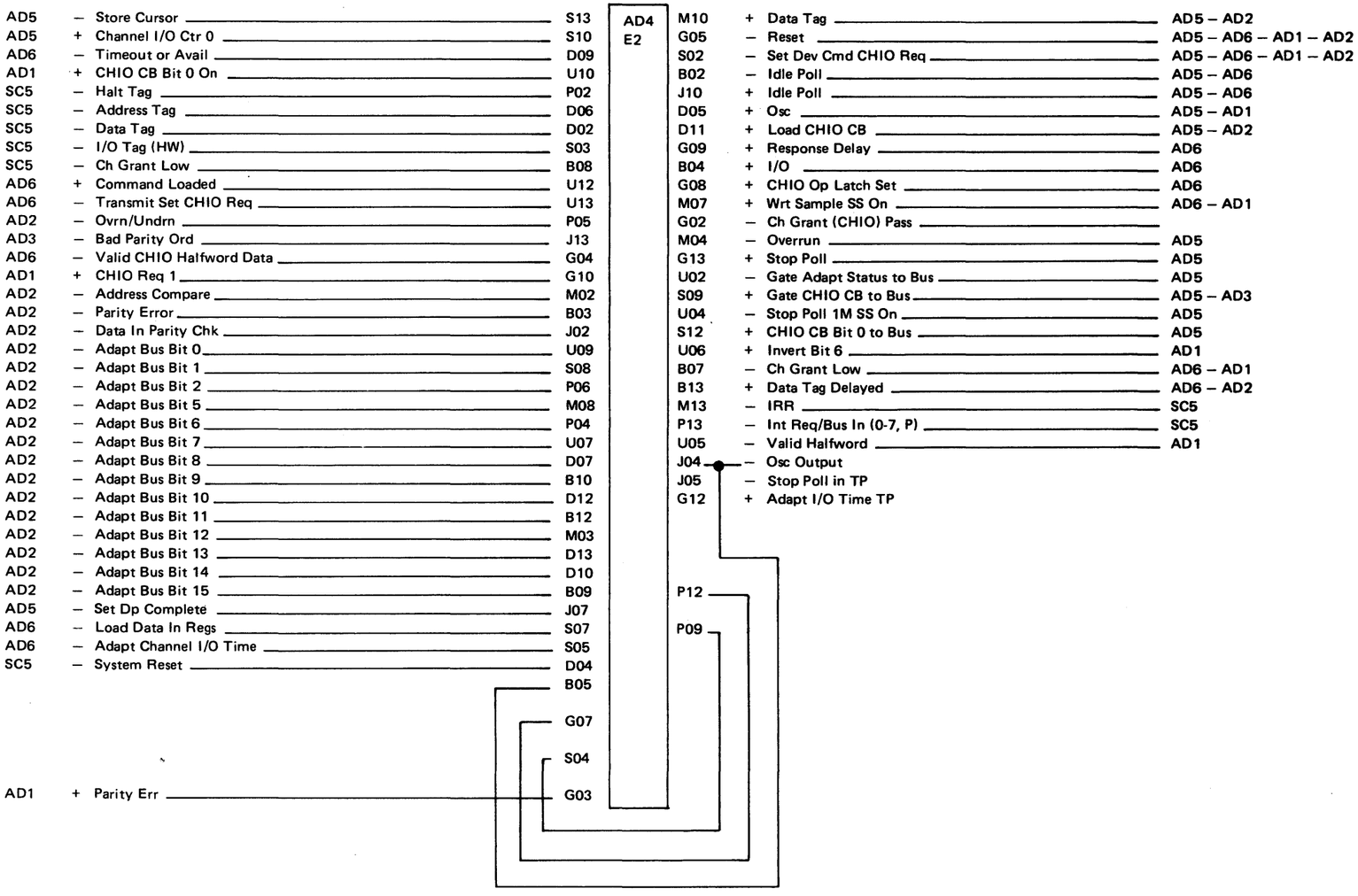


Figure AD470-4. AD4 Card Logic Signals

AD3	+	Gate Data or CHIO CB to Bus	D13	AD5	B04	–	Insert Cursor 1		AD3
AD2	–	Adapt Bus Bit 0	S09	F2	B02	–	Insert Cursor 2		AD3
AD2	–	Adapt Bus Bit 1	S10		D11	–	Gate Inbound		AD2
AD2	–	Adapt Bus Bit 2	S12		B08	+	1920 or 480 Byte Xfer		AD6 – AD1
AD2	–	Adapt Bus Bit 3	U13		S08	–	Step Poll Ctr Up		AD6
AD2	–	Adapt Bus Bit 4	S13		U02	+	AD Response Latch Set		AD6
AD2	–	Adapt Bus Bit 5	D05		D04	–	Idle Poll Strobe Dev Status		AD6
AD2	–	Adapt Bus Bit 6	D06		M07	–	Set Op Complete		AD4
AD2	–	Adapt Bus Bit 7	G10		J04	–	Store Cursor		AD6 – AD4
AD2	–	Adapt Bus Bit 8	I07		M02	+	Channel I/O Ctr 0		AD6 – AD4 – AD1 – AD3
AD2	–	Adapt Bus Bit 9	J10		M08	–	Timeout		AD6
AD2	–	Adapt Bus Bit 10	G09		U10	+	CHIO CB Bit 0 On		AD6 – AD4 – AD1
AD2	–	Adapt Bus Bit 11	U09		G08	–	Parity Valid		SC5
AD2	–	Adapt Bus Bit 12	G13		G07	+	Carry 2048		
AD2	–	Adapt Bus Bit 13	M04		J06	+	Borrow 2048		
AD2	–	Adapt Bus Bit 14	P11		P13	–	3277 Dev Adr Bit 1 On		AD7 – AD12
AD2	–	Adapt Bus Bit 15	P06		P12	–	3277 Dev Adr Bit 2 On		AD7 – AD12
AD6	+	Clear Channel I/O Counter	B07		P10 (A)	+	3277 Dev Adr Bit 4 On	(A)	AD8 – AD10 – AD12
AD6	–	Load Out Regs	D02						
AD6	+	Transmit	B03		P09 (B)	+	3277 Dev Adr Bit 8 On	(B)	AD9 – AD10
AD6	+	Rec Bit Timer 8	J09						
AD6	+	Bit Counter 10	J11		P07 (C)	+	3277 Dev Adr Bit 16 On	(C)	AD11 – AD12
AD6	–	Wrt Load CHIO Ctr	B13						
AD6	–	Cmd Response Set CHIO Req	D07		U07 (D)	–	3277 Dev Adr Bit 4 On	(D)	AD7 – AD9 – AD11
AD1	–	TN Wr Cursor	G03						
AD6	–	Xmit Step CHIO Ctr	G12		U06 (E)	–	3277 Dev Adr Bit 8 On	(E)	AD7 – AD8 – AD11 – AD12
AD6	+	Wrt Poll Latch Set	B09						
AD6	+	Load SERDES	B05		U04 (F)	–	3277 Dev Adr Bit 16 On	(F)	AD7 – AD8 – AD9 – AD10
AD6	–	Wrt Load Cursor Adr Reg	J12						
AD6	–	Gate Dev Status to Bus	M05		S03	+	Rd Timeout SS On		
AD6	+	Load Data Latch Set	D12						
AD6	+	Adapt Channel I/O Time	S02		P02				
AD4	–	Overrun	D10						
AD4	+	Stop Poll	S04		M03				
AD4	–	Gate Adapt Status to Bus	B10						
AD4	+	Gate CHIO CB to Bus	J05						
AD4	–	Stop Poll 1M SS On	P05						
AD4	+	CHIO CB Bit 0 to Bus	G05						
AD1	+	Invert Bit 6	M09						
AD4	+	Load CHIO CB	U11						
AD4	+	Data Tag	U12						
AD4	+	Reset	M10						
AD4	–	Set Dev Cmd CHIO Req	G04						
AD4	–	Idle Poll	J13						
AD4	–	Idle Poll	M13						
AD4	+	Osc	B12						
AD3	+	SERDES Out Bit 20	D09						

S05

J02

G02

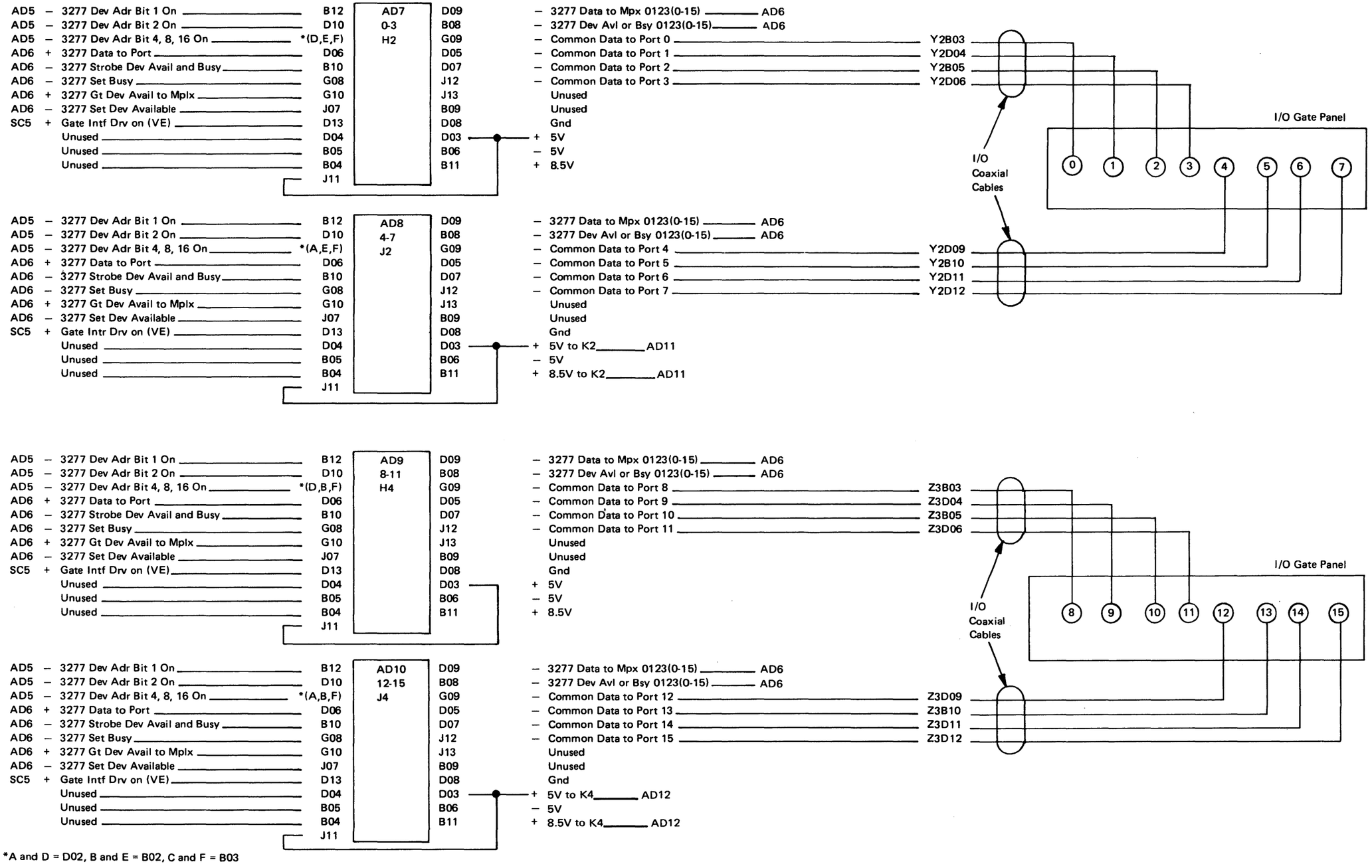
P04

M12

Figure AD470-5. AD5 Card Logic Signals

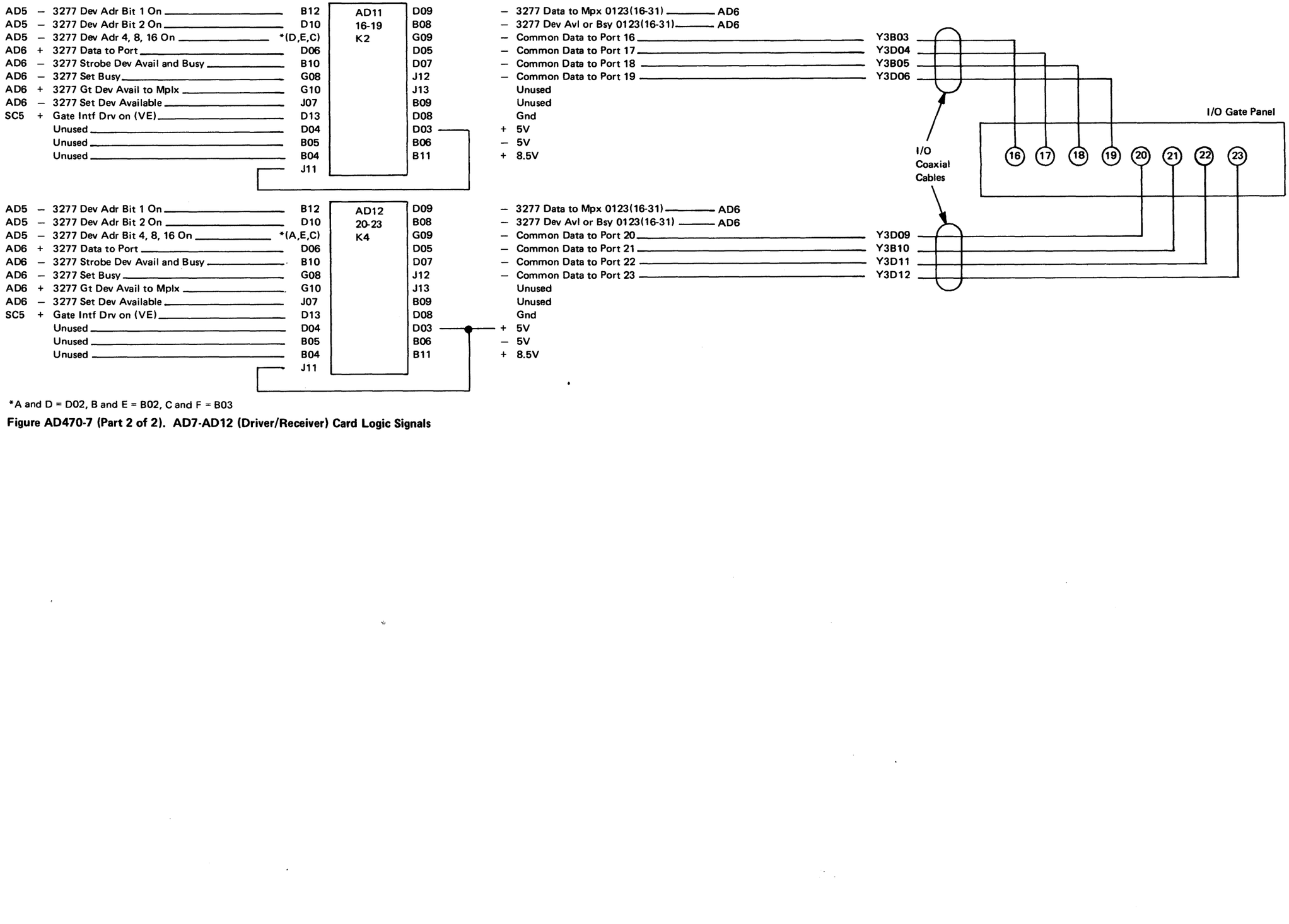
AD7 – AD12	–	3277 Data To Mpx 0123 (0–15)	P09	AD6 G2	P07	+	3277 Data to Port	AD7 – AD12
AD7 – AD12	–	3277 Dev Avl or Bsy 0123 (0–15)	B04		D11	–	3277 Strobe Dev Avail and Busy	AD7 – AD12
AD7 – AD12	–	3277 Data to Mpx 0123 (16–31)	G12		D10	–	3277 Set Busy	AD7 – AD12
AD3	+	Bad SERDES Parity	G03		M07	+	3277 Gt Dev Avail to Mplx	AD7 – AD12
AD3	+	Avail and Ready	B07		B08	–	3277 Set Dev Available	AD7 – AD12
AD3	+	SERDES Out Bit 23	B09		G13	–	End of Chain	AD1
AD3	+	Serial Out Bit On	M02		U10	+	Load Data Out Regs	AD1
AD3	+	SERDES Out Bit 20	D07		P04	+	Data Ser In	AD3
AD5	+	1920 or 480 Byte Xfer	B05		U13	–	Reset Load Data Latch	AD3
AD5	–	Step Poll Ctr Up	M04		S03	+	Xmit or Rec Shift SERDES	AD3
AD5	+	Rd Response Latch Set	S04		J04	–	Gate Data to Bus	
AD5	–	Idle Poll Strobe Dev Status	B10		P11	+	In Reg Ctr 1	
AD5	–	Store Cursor	G05		S08	+	Wrt Poll Latch Set	AD5 – AD1 – AD3
AD5	+	Channel I/O Ctr 0	M08		U11	+	Load SERDES	AD5 – AD3
AD5	–	Timeout	M05		J07	–	Wrt Load Cursor Adr Reg	AD5
AD5	+	CHIO CB Bit 0 On	B03		D13	–	Gate Dev Status to Bus	AD5 – AD3
AD4	+	Response Delay	J06		U05	+	Load Data Latch Set	AD5 – AD1 – AD3
AD4	+	I/O	J09		J02	–	Load Data In Regs	AD4
AD4	+	CHIO Op Latch Set	J13		S12	+	Clear CHIO Counter	AD5
AD4	+	Wrt Sample SS On	G10		M03	–	Load Out Regs	AD5
AD4	–	Ch Grant Low	J11		S13	+	Transmit	AD5
AD4	+	Data Tag Delayed	B12		M13	+	Rec Bit Timer 8	AD5
AD4	+	Data Tag	D06		M12	+	Bit Counter 10	AD5 – AD1
AD4	–	Reset	S09		G07	–	Wrt Load CHIO Ctr	AD5
AD4	–	Set Dev Cmd CHIO Reg	U02		P06	–	Cmd Response Set CHIO Req	AD5 – AD1
AD4	–	Idle Poll	P13		P10	–	Store Cursor Adr CHIO Req	
AD4	+	Idle Poll	B13		D09	–	Xmit Step CHIO Ctr	AD5
AD1	+	SERDES Osc	D12		G02	+	Adapt Channel I/O Time	AD5 – AD4 – AD1
AD1	–	CHIO Grant I	U09		U12	+	Command Loaded	AD4 – AD1 – AD2
AD7 – AD12	–	3277 Dev Avl or Busy 0123 (16–31)	D05		P12	–	Transmit Set CHIO Req	AD4
					G08	–	Set Ser Int Chk	AD3
			J12		J10	–	Valid CHIO Halfword Data	AD4
			S05		P02	+	Channel I/O Request	AD1
			P05		D04	–	Reset Bit Counter SS On	
			U04		D02	–	Idle Poll Set Xmit Latch	
			U07		J05	–	Xmit Reset Bit Counter TP	
			S10		G04	–	Timeout or Avail	AD4
			B02		S02			
					M09			

Figure AD470-6. AD6 Card Logic Signals



*A and D = D02, B and E = B02, C and F = B03

Figure AD470-7 (Part 1 of 2). AD7-AD12 (Driver/Receiver) Card Logic Signals



*A and D = D02, B and E = B02, C and F = B03

Figure AD470-7 (Part 2 of 2). AD7-AD12 (Driver/Receiver) Card Logic Signals

AD500 Attached Device Information

The following devices can be attached to the display/printer adapter:

- Displays:

  3277 Display Station, Model 1 (480-character display)
  3277 Display Station, Model 2 (1920-character display)
  3732 Text Display Station

- Printers:

  3284 Printer, Models 1 and 2 (up to 40 cps)
  3286 Printer, Models 1 and 2 (up to 66 cps)
  3287 Printer, Models 1 and 2 (desk top printer)
  3288 Line Printer, Model 2 (132 characters per line; up to 155 lpm)
  3736 Printer

- 129 Card Data Recorder (RPQ MK6956)

When these devices are attached to an 8100, the basic device MIM contains changed or additional pages. These pages alter that MIM to reflect attachment to an 8100. The title on the cover page designates the presence of these changes, as well as the following form numbers:

Attached Device	Basic MIM	Attachment Pages*
3277-1, -2	SY27-2314	SY27-2522
3284-1, -2	SY27-2315	SY27-2523
3286-1, -2	SY27-2315	SY27-2523
3287-1, -2	SY27-0171	SY27-2524
3288-2	SY27-2401	SY27-2525
3732	SY33-0048	–
3736	SY33-0050	–
129(RPQ MK6956)	–	SY27-2552

*Pages added to the basic MIM that provide online test information for the 32XX when attached to an IBM 8100 System.

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Chapter 5. MAP Reference Information
Bring Up
(BU)

Introduction

This part of the manual contains information relating to the processor instruction/execution (I/E) unit, storage, and basic operator panel (BOP) of the 8130/8140 Processor. It describes the basic and extended bringup (BU) tests and how to run them to verify correct processor and BOP functions. When used in conjunction with the BU MAP, it enables you to perform fault isolation for failures caused by components of the 8130/8140 processor I/E unit, floating-point processor (if present), storage, BOP, and BOP adapter.

This information is divided into five sections:

1. General Information (BU100–130): Contains information related to processor I/E unit, processor storage, BOP hardware components, and physical addressing. It also contains basic operational theory as well as repair strategy unique to the BU MAP and its associated reference information.
2. Bringup and Basic Operator Panel Tests (BU200–260): Contains test information, certain unique test procedures, and lists action plans for failures not readily detected by the BU MAP.
3. Intermittent or Random Failure Strategy (BU300–350): Discusses intermittent or random failures and the action plans used to repair them.
4. Signal Paths and Detailed Operational Description (BU400–480): Uses diagrams and charts to show wiring and signal paths, and contains a detailed description of the processor I/E unit and processor storage, as well as the basic operator panel.
5. Adjustment, Removal, Replacement, and Voltage Check Procedures (BU500–532): Contains reference information used for FRU replacement, troubleshooting, repair procedures, and voltage checks.

Contents

Figures

Abbreviations

ACV	address control vector
AOM	address overlay mask
BAR	buffer address register
BOP	basic operator panel
BSTAT	basic status
BU	bringup
CHIO	channel I/O
CLA	carry lookahead
CSU	customer setup
DAR	dynamic address relocation
DAT	dynamic address translation
DPCX	Distributed Processing Control Executive
DPPX	Distributed Processing Programming Executive
ECC	error correction coding
EFP	expanded function panel
EIRV	error interrupt request vector
EN	error number
FP	floating-point
FRU	field-replaceable unit
GFI	General Failure Index
hex	hexadecimal
I/E	instruction/execution
I/O	input/output
IPL	initial program load
LED	light-emitting diode
MAP	Maintenance Analysis Procedure
MD	Maintenance Device
MDDR	Maintenance Device Data Register
PEC	program execution code
PIC	program information code
PIO	programmed I/O
PIRV	program interrupt request vector
PSCF	Primary System Control Facility
PSV	program status vector
ROS	read-only storage
R/W	read/write
SAB	stack address bus
SCF	System Control Facility
SDC bus	system direct control bus
SDI	storage data in
SDO	storage data out
SSCF	Secondary System Control Facility
TTE	Translation Table Entry
TTEA	Translation Table Entry Address

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BU100 General Information

This section contains a basic discussion of the processor instruction/execution unit, storage, storage control, and the basic operator panel (BOP) of the 8130/8140 Processor. It enables you to understand their physical components and operation, as well as the BOP physical addressing scheme. It also enables you to understand any unique repair strategies involved when performing fault isolation on these components. For a detailed hardware description, including point-to-point logic signals, refer to the BU400 section.

BU110 Components and Addressing

BU111 Hardware Components

The following describes and shows components of the processor, processor storage, storage control, and BOP hardware. Refer to this section whenever necessary to determine the processor, BOP, and BOP adapter card locations.

Processor, Storage, and Storage Control

The 8130 processor uses six cards for instruction/execution and three cards for storage control and addressing functions, which are located in the 01A-A1 board. The first, or basic, storage card position contains 256K bytes of read/write storage, the second card position (feature) can contain either 128K or 256K bytes of read/write storage, and the third and fourth card positions (feature) can each contain 256K bytes. The storage control card contains the 4K ROS area and can also contain part of the ECC logic.

The processor instruction/execution (I/E) unit of the 8140 also uses six I/E cards and three storage control cards located in the 01A–A1 board to perform processing and storage addressing functions. All card locations vary between models (see Figures BU111-5 through BU111-15).

- In 8140 Models A3X, A4X and A5X, the first storage card position contains 4K ROS and 28K bytes of read/write storage, and all remaining storage cards contain 32K bytes of read/write storage.
- 8140 Models A6X, A7X, and BXX use storage cards containing 128K bytes of read/write storage, and the 4K ROS area resides on a separate card.

8140 Models A6X, A7X, and BXX also use two ECC (Error Correction Coding) cards as a part of storage control. Floating-point, available in Models A4X and BXX, uses two cards that also plug directly into the 01A–A1 board.

Refer to the appropriate figure in this section for all 8130 and 8140 processor, storage, and storage control card locations.

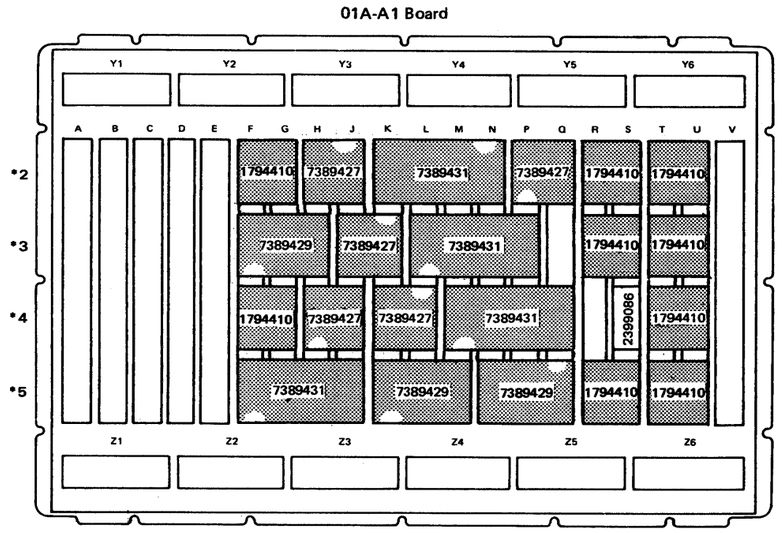
Basic Operator Panel (BOP)

The BOP mounts on a subframe located at the top and toward the front of the 8130/8140 frame. The BOP adapter card, located inside the 8130/8140 front covers and mounted on a bracket attached to the right side cover, controls BOP operations. The following functional FRUs relate to the BU MAP:

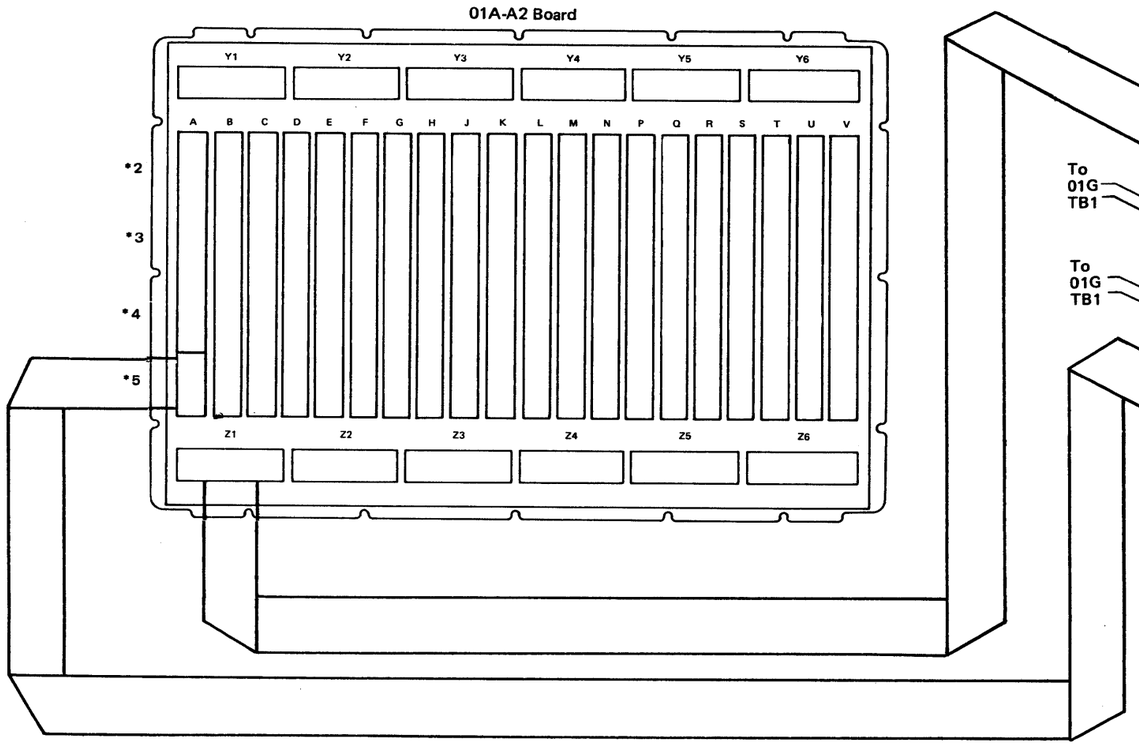
- BOP adapter card
- LED indicator card
- Data/Function pushbutton card
- IPL Mode switch
- BOP cable assembly
- Keylock switch (feature)

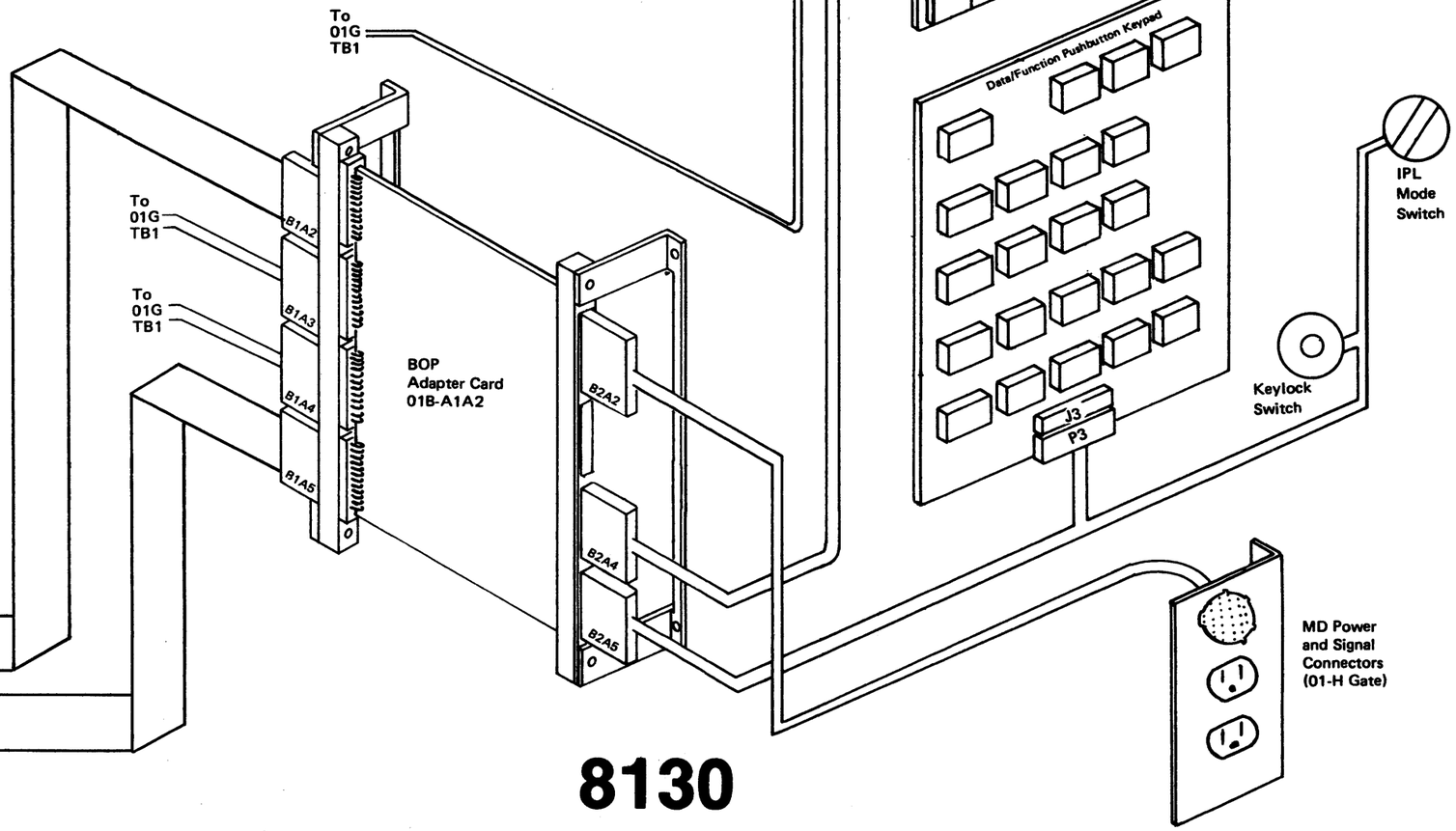
8130 and 8140 Component Locations Relating to the BU MAP

Figures BU111-1 through BU111-15 show the 8130 and 8140 Processor and BOP hardware components and locations. It also shows the size (2-, 3-, or 4-wide) and placement of the processor I/E unit top card connectors.



Note: *The 12 polarized top card connector key positions are indicated by semi-circular cutouts.*





*Top card connector locations W, X, Y, and Z correspond to card rows 2, 3, 4, and 5 respectively.

Figure BU111-1. 8130 BOP, BOP Adapter Card, 01A-A2 Board Cables, and 01A-A1 Board Connectors

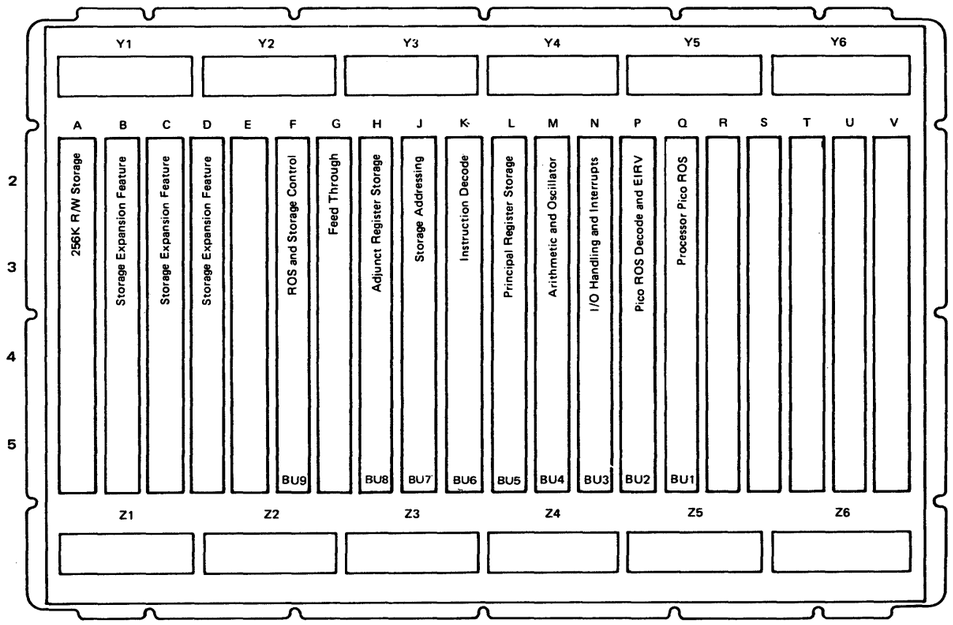
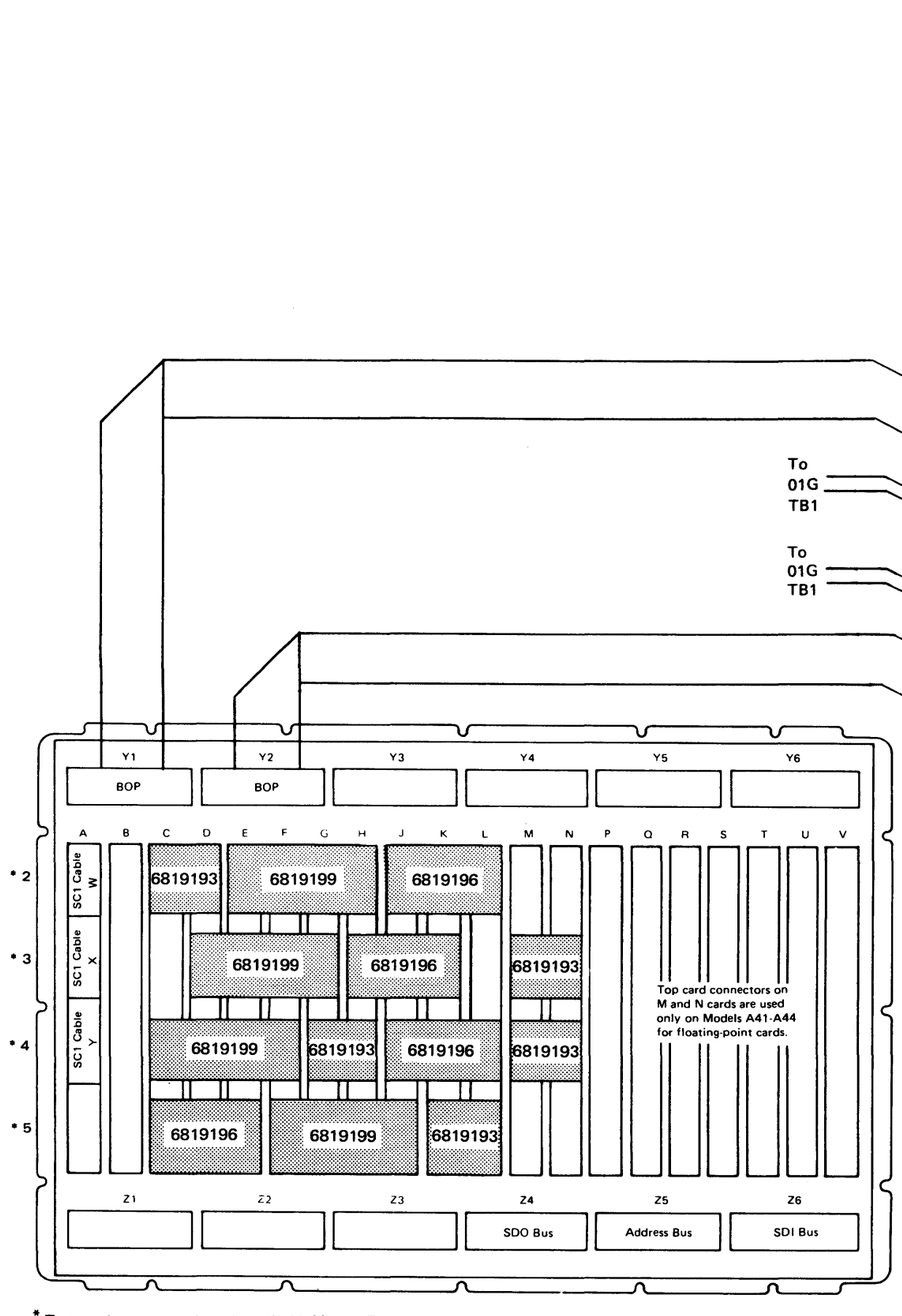
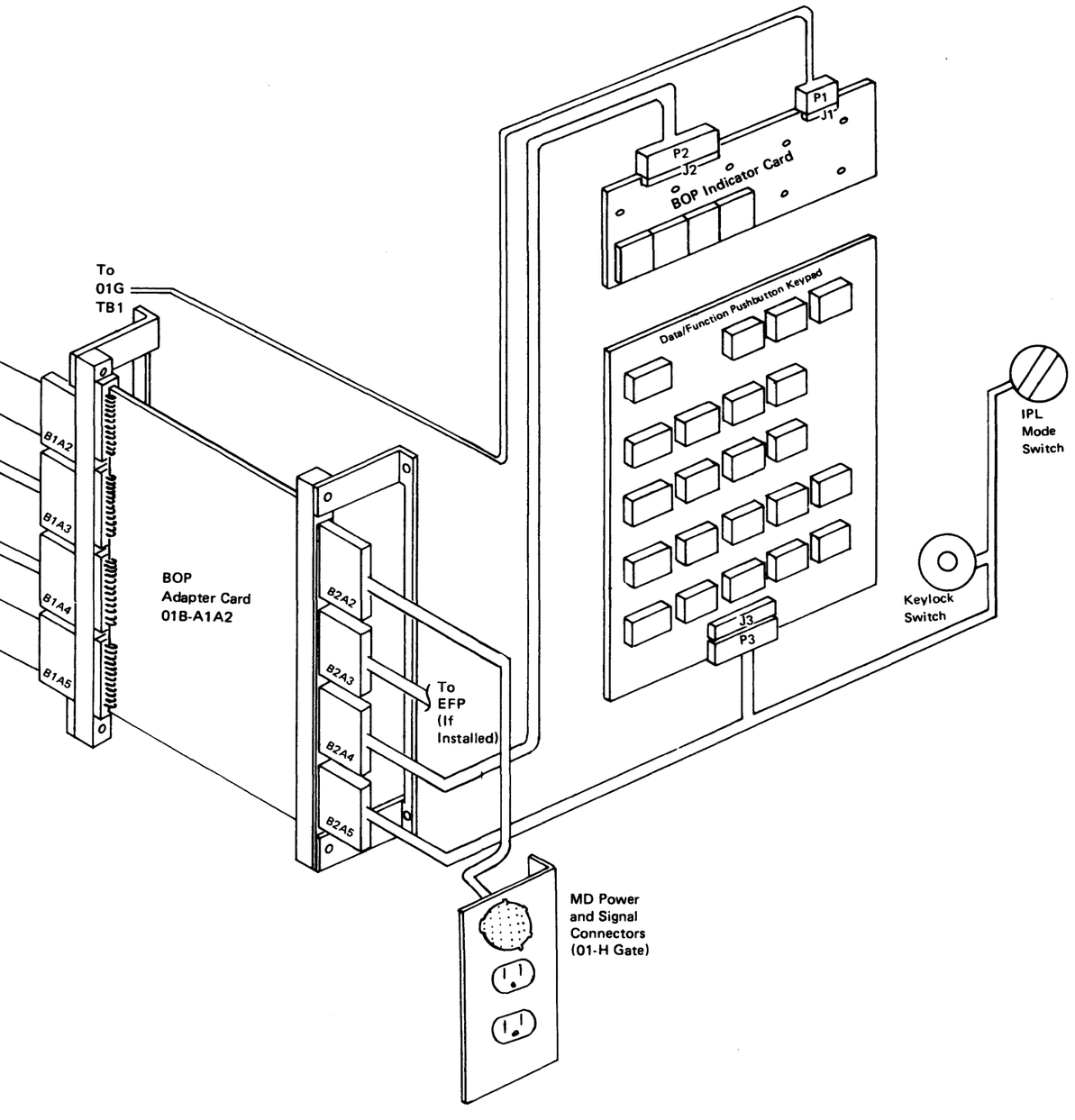


Figure BU111-2. 8130 Models A21–A24 (256K, 384K, 512K, 768K, or 1024K) 01A-A1 Board Card Locations

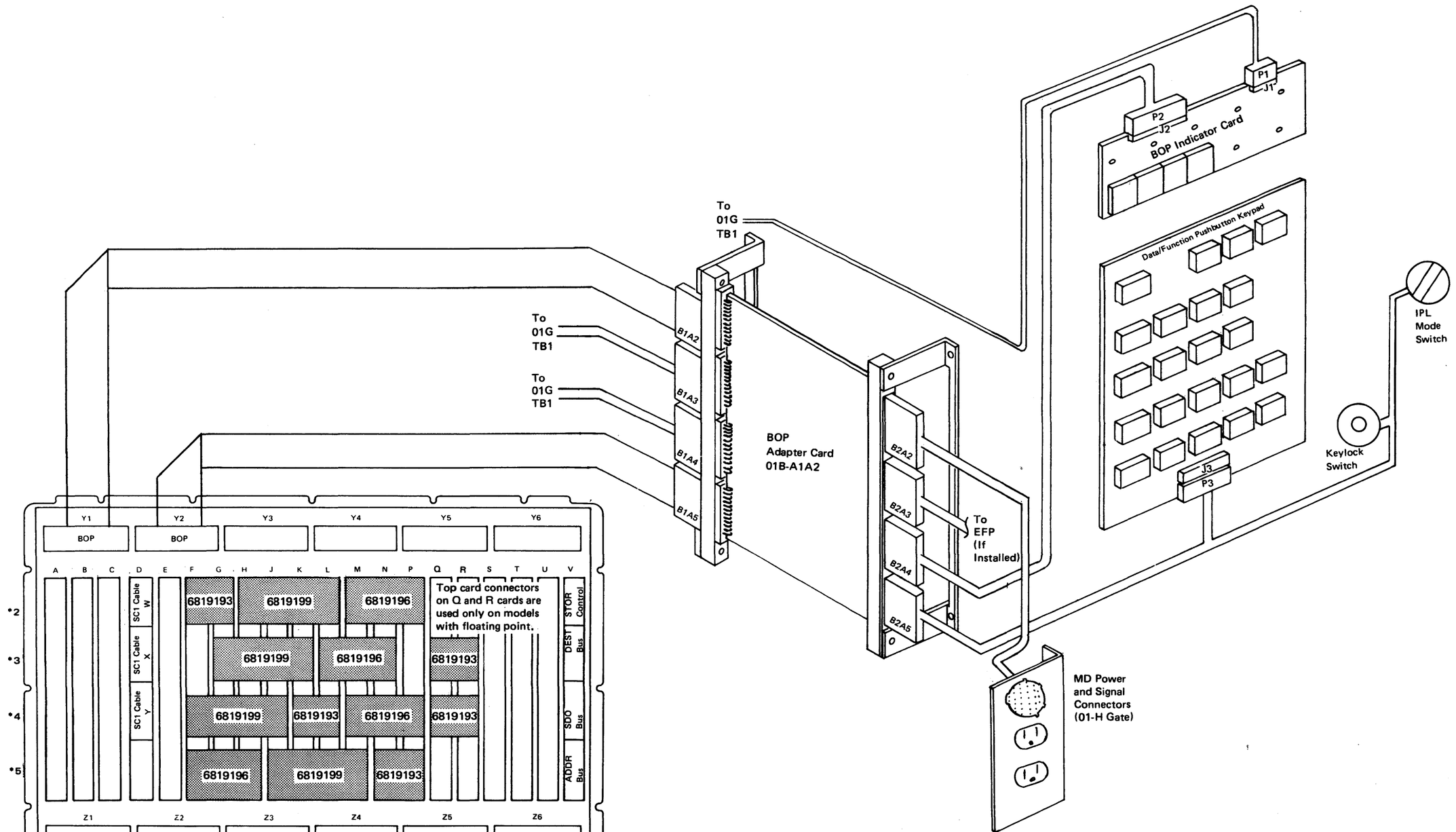


* Top card connector locations W, X, Y, and Z correspond to card rows 2, 3, 4, and 5, respectively.

Figure BU111-3. 8140 Models AXX BOP, BOP Adapter Card, and 01A-A1 Board Cables and Connectors



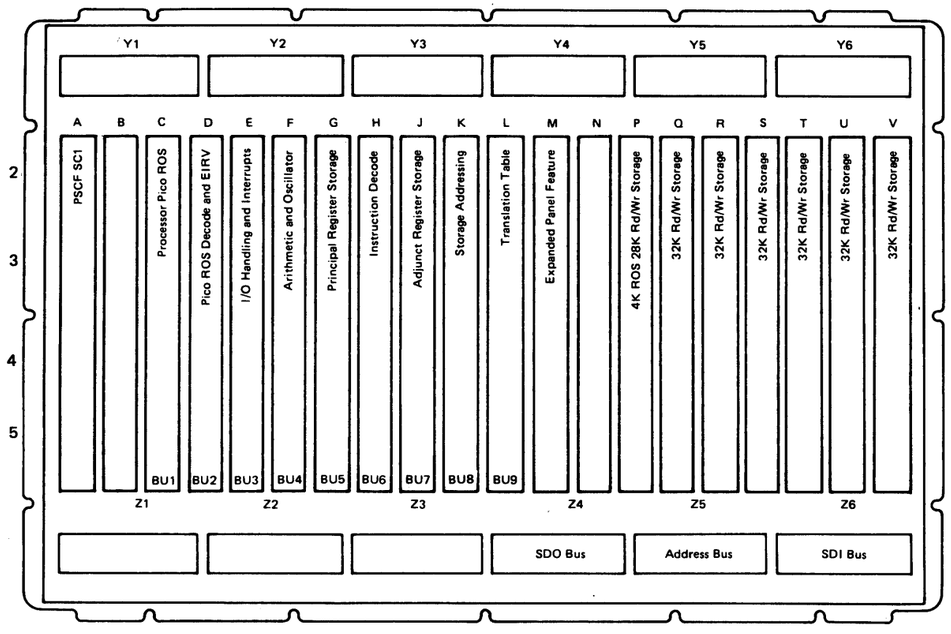
8140 Models AXX

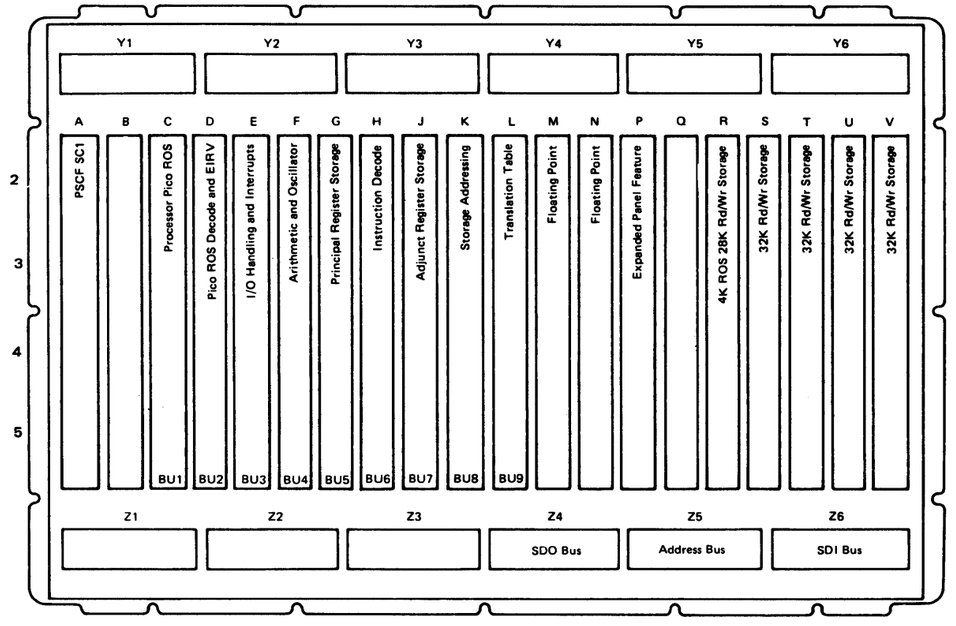


8140 Models BXX

* Top card connector locations W, X, Y, and Z correspond to card rows 2, 3, 4, and 5, respectively.

Figure BU111-4. 8140 Models BXX BOP, BOP Adapter Card, and 01A-A1 Board Cables and Connectors





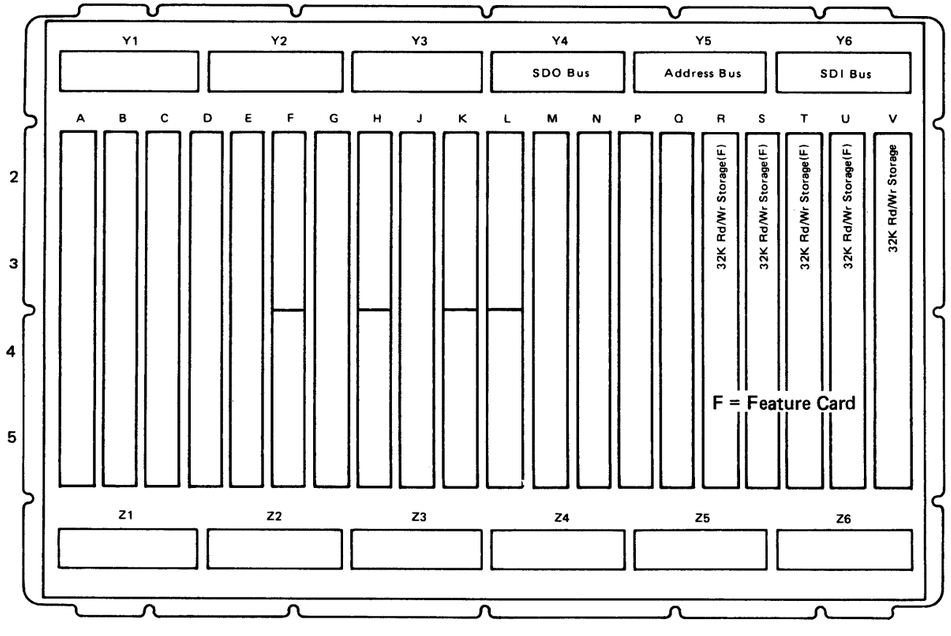


Figure BU111-5. 8140 Models A31–A34 (256K or 384K) A1 Board Card Locations and A2 Board Storage Card Locations

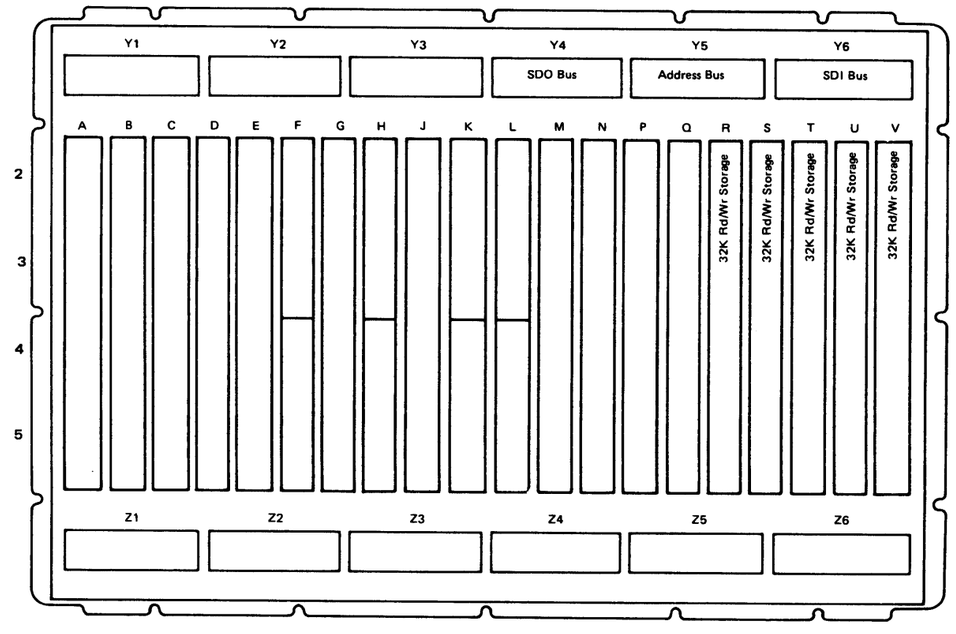
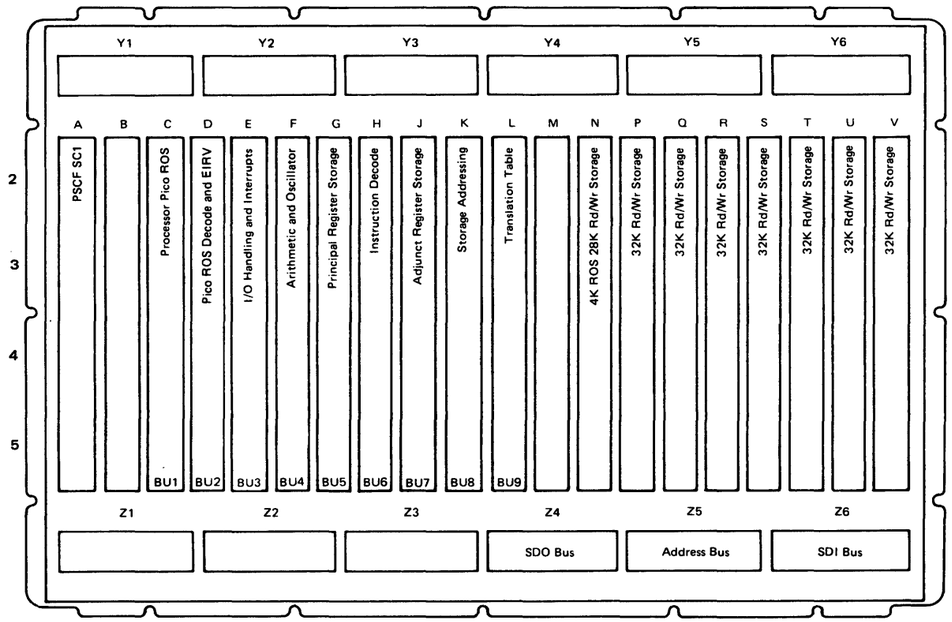


Figure BU111-6. 8140 Models A41–A44 (320K) A1 Board Card Locations and A2 Board Storage Card Locations



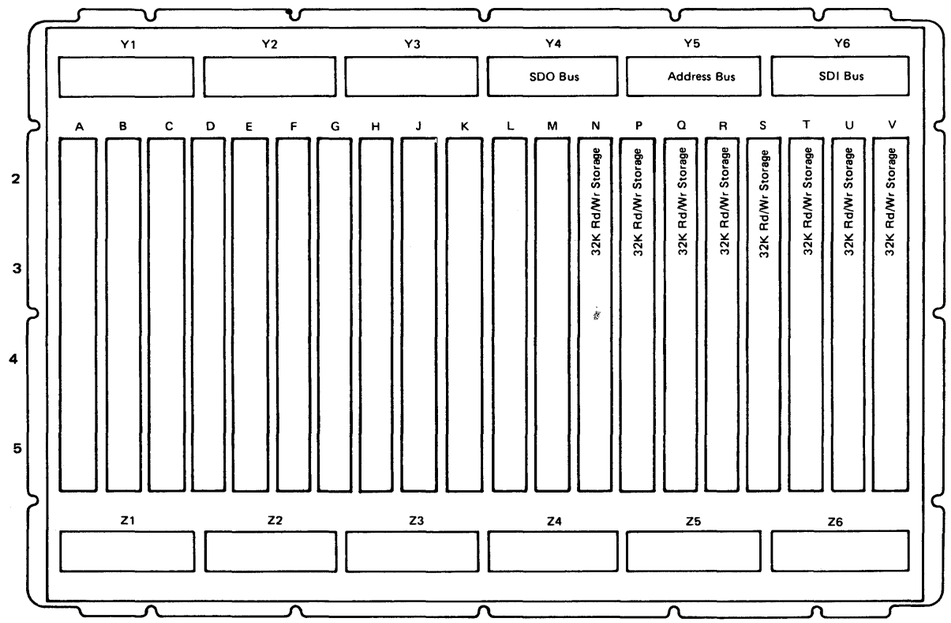


Figure BU111-7. 8140 Models A51—A54 (512K) A1 Board Card Locations and A2 Board Storage Card Locations

Storage Block Number	Address Range		Card Location	Range Check Jumpers*		
	Hex	Decimal		RCJ8 (M09)	RCJ4 (S13)	RCJ2 (U13)
00—07	0000—3FFFF	0—256K	A1A2	1	0	0
08—0B	40000—5FFFF	256K—384K	A1C2	0	1	0
08—0F	40000—7FFFF	256K—512K	A1C2	1	1	0
10—17	80000—BFFFF	512K—768K	A1B2	1	0	1
18—1F	C0000—FFFFF	768K—1024K	A1D2	1	1	1

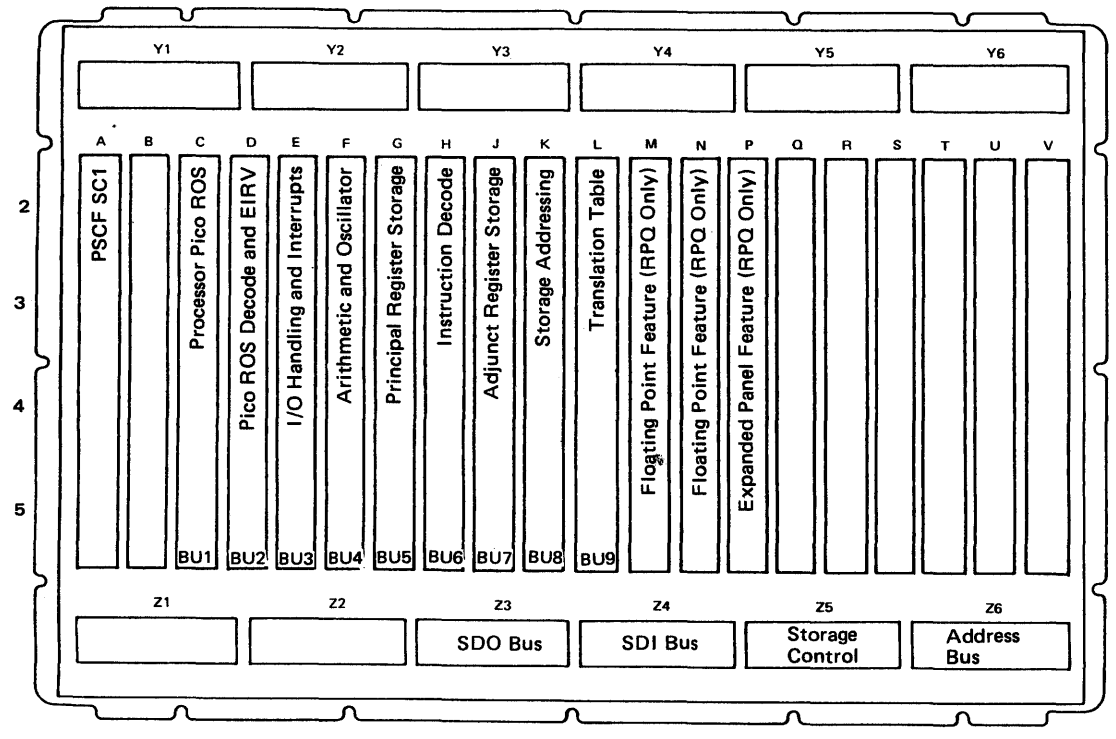
*The range check jumpers are at card location F2 on the 01A-A1 board. A "1" indicates that a jumper to ground is required. A "0" indicates that no jumper is required.

Figure BU111-8. 8130 Storage Card Locations, Address Ranges, and Range Check Jumpers

Storage Block Number	Address Range		Card Location		
	Hex	Decimal	Model A3X	Model A4X	Model A5X
00	0000—7FFF	0—32K	*A1P2	*A1R2	*A1N2
01	8000—FFFF	32K—64K	A1Q2	A1S2	A1P2
02	10000—17FFF	64K—96K	A1R2	A1T2	A1Q2
03	18000—1FFFF	96K—128K	A1S2	A1U2	A1R2
04	20000—27FFF	128K—160K	A1T2	A1V2	A1S2
05	28000—2FFFF	160K—192K	A1U2	A2V2	A1T2
06	30000—37FFF	192K—224K	A1V2	A2U2	A1U2
07	38000—3FFFF	224K—256K	A2V2	A2T2	A1V2
08	40000—47FFF	256K—288K	A2U2(f)	A2S2	A2V2
09	48000—4FFFF	288K—320K	A2T2(f)	A2R2	A2U2
0A	50000—57FFF	320K—352K	A2S2(f)		A2T2
0B	58000—5FFFF	352K—384K	A2R2(f)		A2S2
0C	60000—67FFF	384K—416K			A2R2
0D	68000—6FFFF	416K—448K			A2Q2
0E	70000—77FFF	448K—480K			A2P2
0F	78000—7FFFF	480K—512K			A2N2

*4K ROS and 28K read/write storage
(f) = Feature cards

Figure BU111-9. 8140 Models A3X, A4X, and A5X Storage Card Locations and Address Ranges



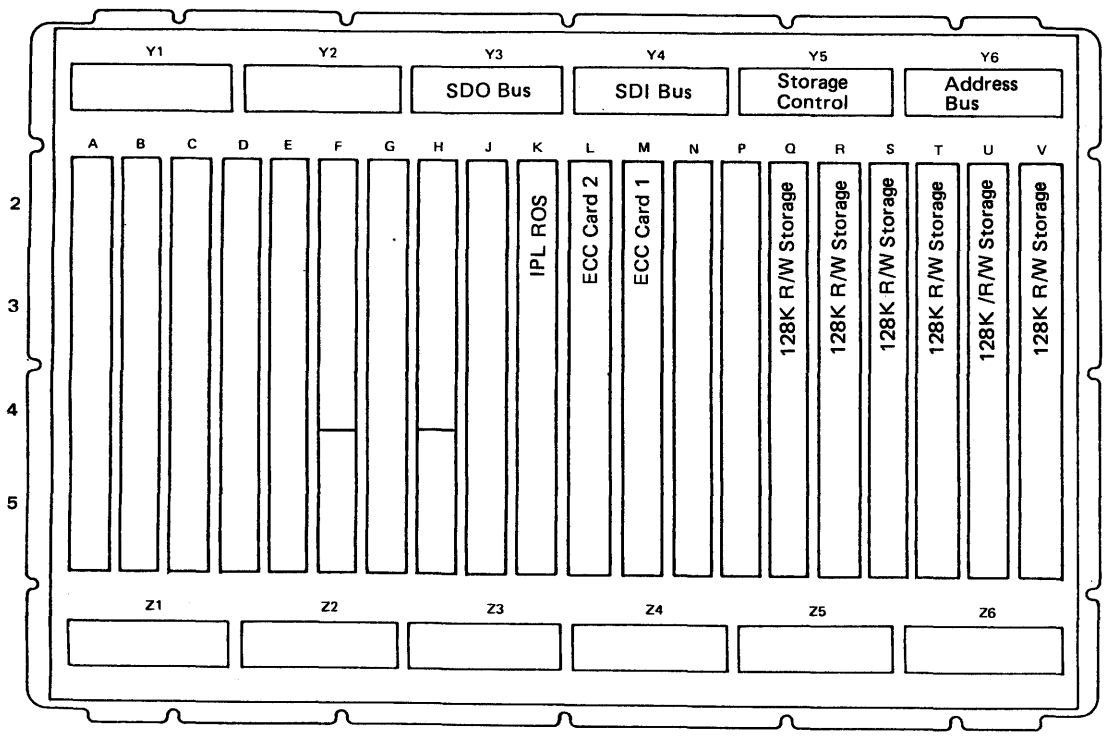
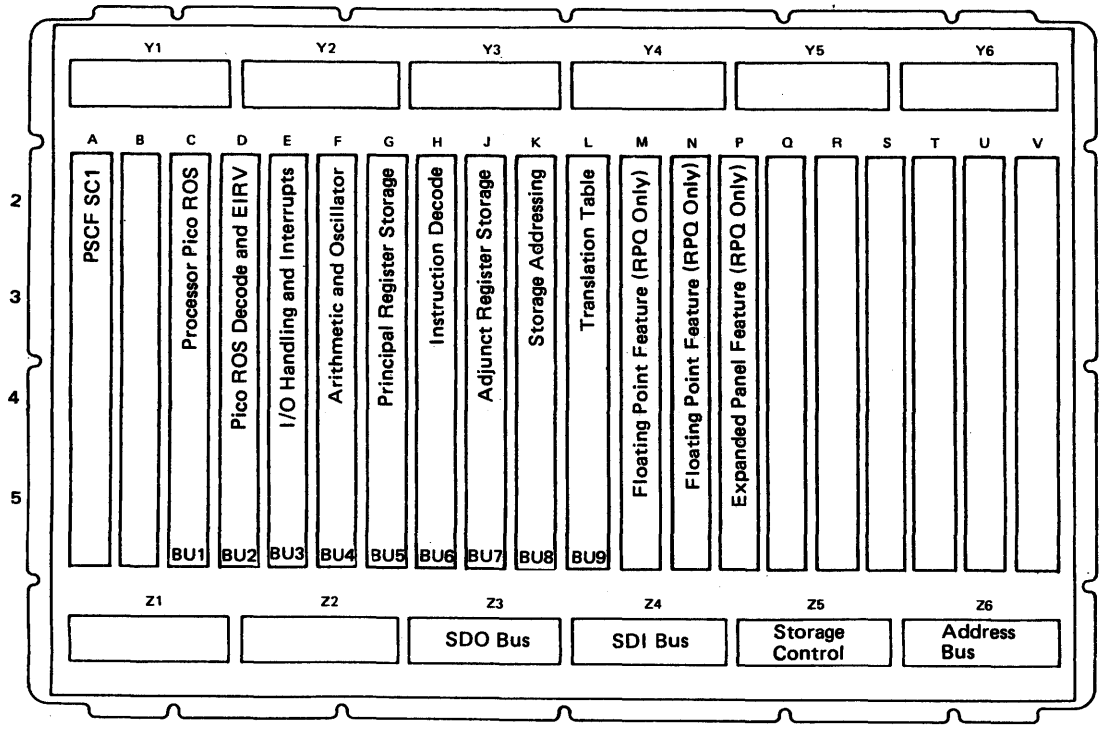


Figure BU111-10. 8140 Models A61-A62 (768K) A1 Board Card Locations and A2 Board Storage and ECC Card Locations



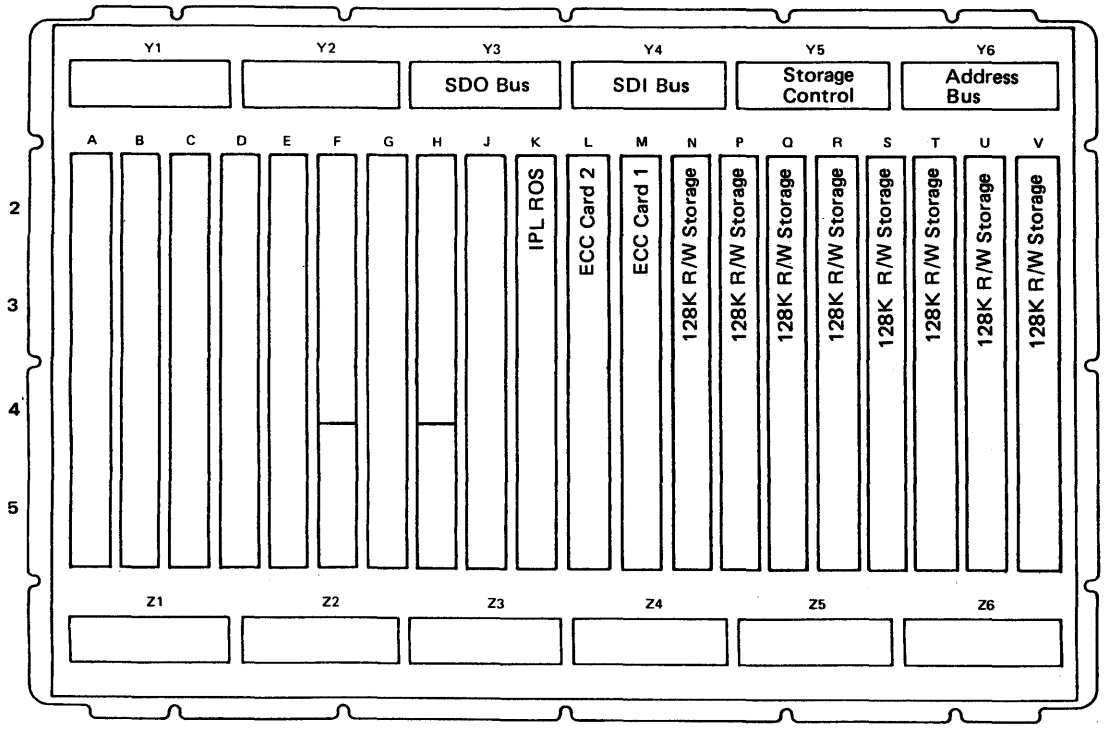
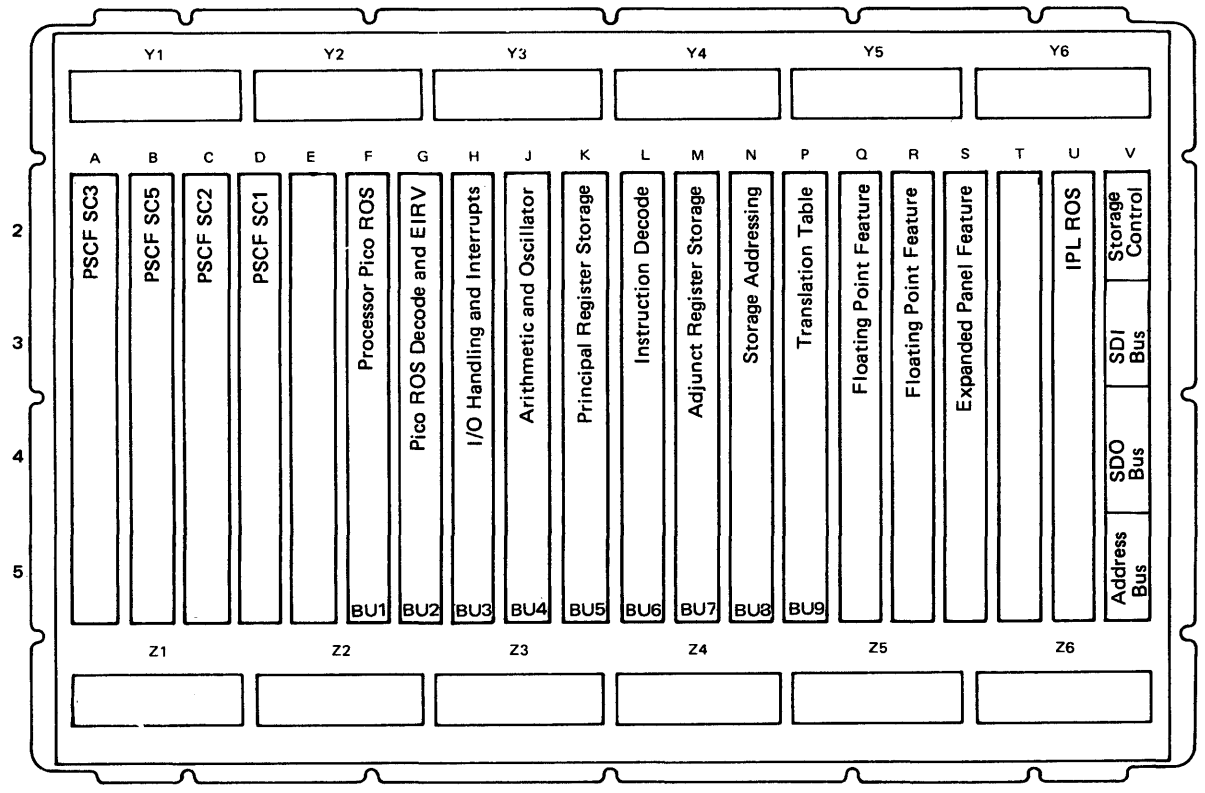


Figure BU111-11. 8140 Models A71-A72 (1024K) A1 Board Card Locations and A2 Board Storage and ECC Card Locations



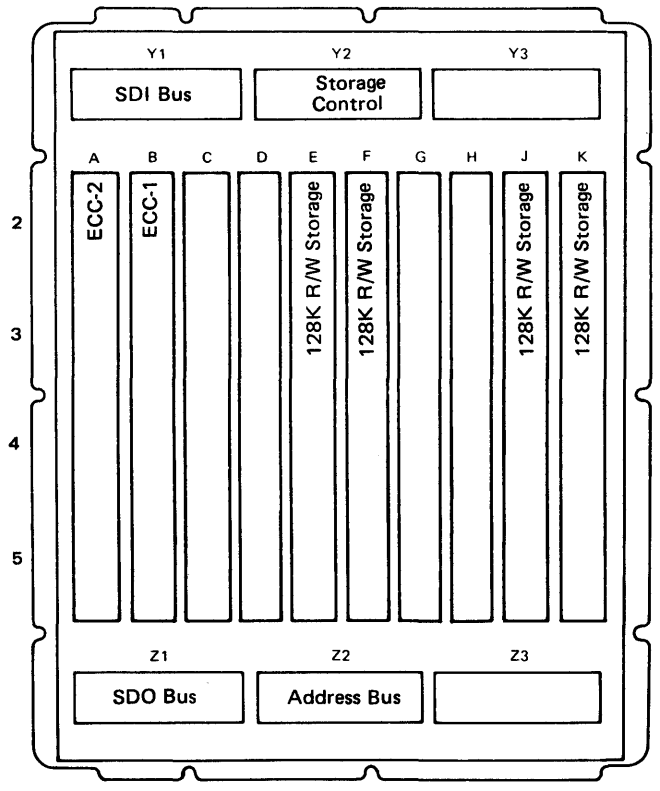
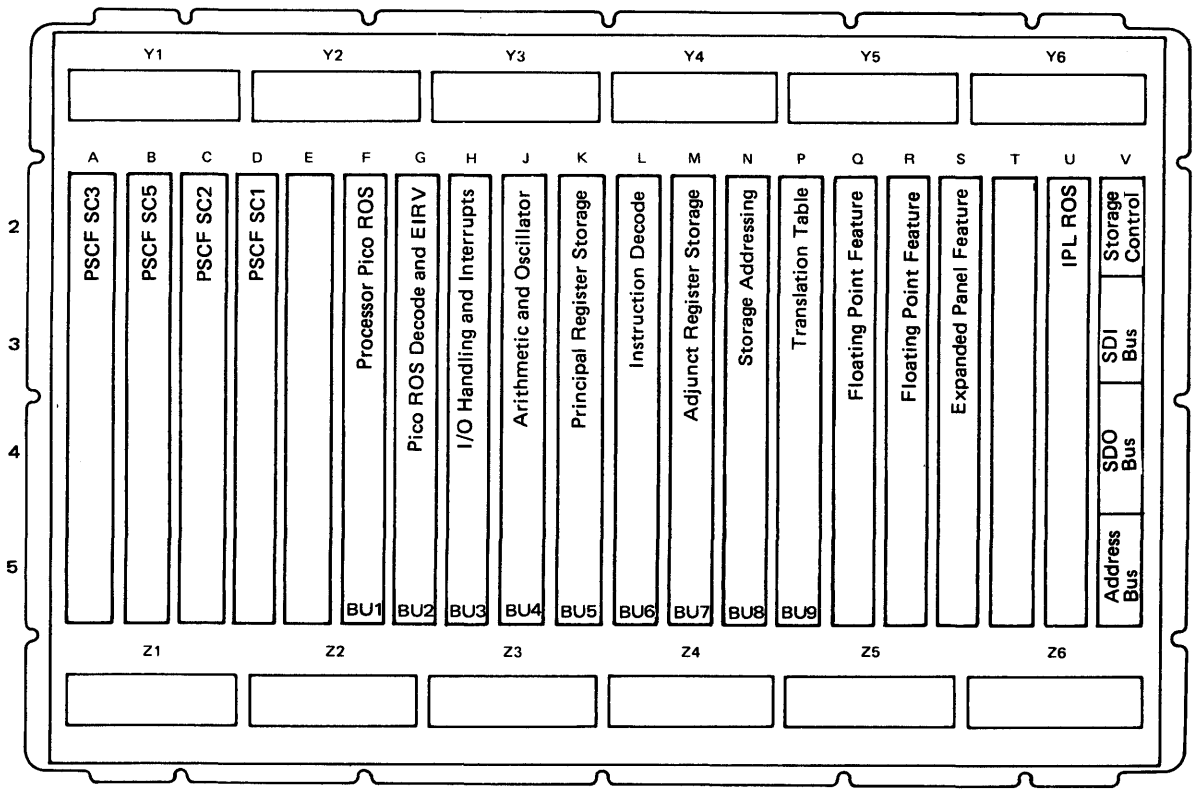


Figure BU111-12. 8140 Models B51-52 (512K) A1 Board Card Locations and C1 Board Storage and ECC Card Locations



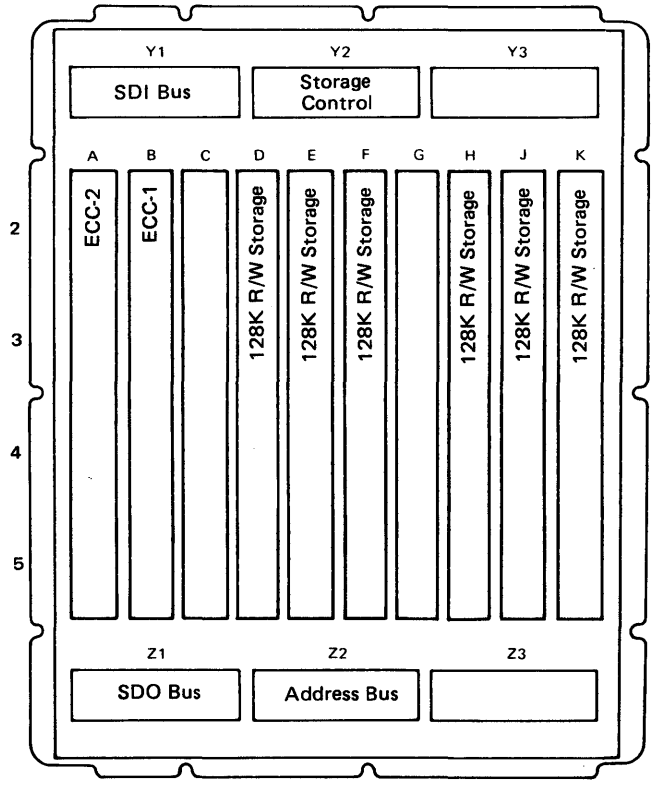
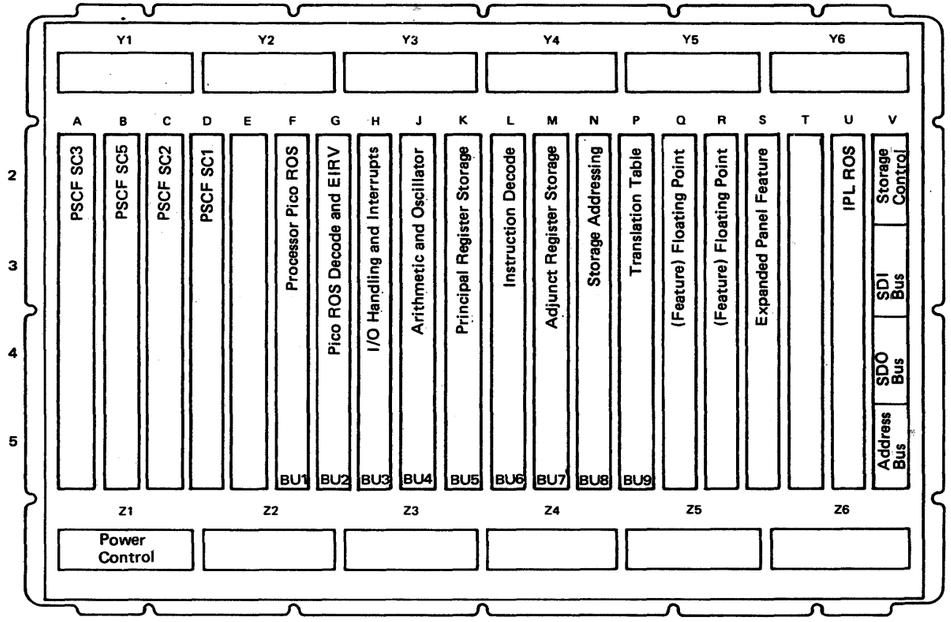


Figure BU111-13. 8140 Models B61-62 (768K) A1 Board Card Locations and C1 Board Storage and ECC Card Locations



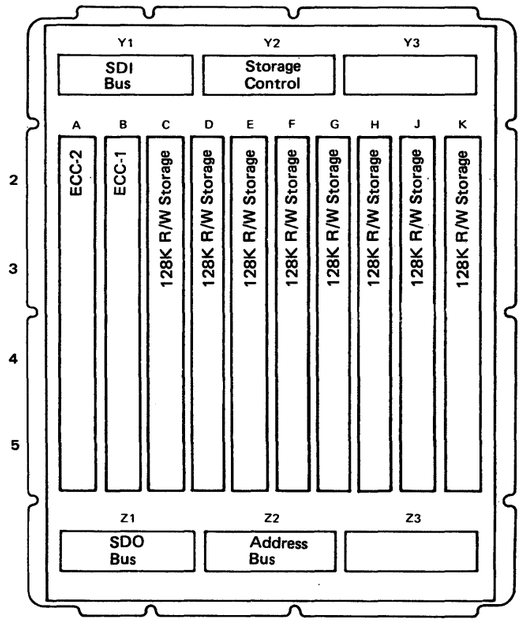


Figure BU111-14. 8140 Models B71-72 (1024K) A1 Board Card Locations and C1 Board Storage and ECC Card Locations

Storage Block Number	Address Range		Card Location*				
	Hex	Decimal	A6X	A7X	B5X	B6X	B7X
00–07	0000–3FFFF	0–256K	A2V2 A2U2	A2V2 A2U2	C1F2 C1K2	C1F2 C1K2	C1F2 C1K2
08–0F	40000–7FFFF	256K–512K	A2T2 A2S2	A2T2 A2S2	C1E2 C1J2	C1E2 C1J2	C1E2 C1J2
10–17	80000–BFFFF	512K–768K	A2R2 A2Q2	A2R2 A2Q2		C1D2 C1H2	C1D2 C1H2
18–1F	C0000–FFFFF	768K–1024K		A2P2 A2N2			C1C2 C1G2

*Full word storage locations are split in half between the two cards listed for the storage block numbers. Bytes 0 and 1 are physically located on the first of the pair of storage cards and bytes 2 and 3 are located on the second.

Figure BU111-15. 8140 Models A6X, A7X, and BXX Storage Card Locations and Address Ranges.

BU112 Addressing

The BOP adapter has a fixed physical address of hex 09, and appears to the processor as a halfword adapter on the programmed I/O (PIO) bus, as do most other 8100 devices. The processor uses this bus for information transfer to and from the SCF. The SCF then uses the system direct control (SDC) bus to transfer information to the BOP adapter.

The BOP logic either recognizes its own address during IPL and information transfer, or permits maintenance device (MD) information transfer to occur if BOP basic status register bit 4 (MD enabled) is on the BOP adapter decodes an MD command.

BU113 Configuration Table Entry

The processor configuration table entry defines the processor type, storage size, model number and also if floating point is installed. It uses the following standard format:

LV PA UTUT OP(1*) OP(2*) OP(3*) OP(4*), where:

LV = 0C

PA = 99

UTUT = 0F00

*OP(1) = 02 = No floating-point, No ECC
03 = Floating-point installed, No ECC
12 = No floating-point, ECC installed
13 = Floating-point and ECC installed

*OP(2) = 08 = 256K
0A = 320K
0C = 384K
10 = 512K
18 = 768K
20 = 1024K

*OP(3) = XX = 8130/8140 model number (21-24, 31-34, 41-44, 51-54, 61, 62, 71, 72)

*OP(4) = 00 = Models A3X-A5X
A0 = Models A6X-A7X
B0 = Models BXX

*These fields are physically represented in the format OPOP OPOP. The numbers in brackets are only used to explain the entry values.

BU120 Basic Operational Description and Data Flow

This section describes the basic operation and data flow of the processor and BOP. It also describes the BOP switches, pushbuttons, indicators, and their function or meaning. Refer to section BU450 for a detailed description of processor operation, BU460 for processor storage, BU470 for the BOP, and BU480 and for floating point.

Figure BU120-1 shows the 8130/8140 processor basic data flow. The numbers within the black squares indicate how many bits are used for that particular bus, and the arrows show the direction of bus information transfer.

BU121 Processor I/E Unit and Storage

The 8130/8140 processor is a general purpose, interrupt-driven controller that uses 2's complement arithmetic on byte and halfword data fields, and which also controls systems of I/O devices.

The nine-card processor instruction/execution unit includes, and is logically organized around, the following functional elements or subsystems:

- ROS and ROS control
- Arithmetic and logical unit
- Register storage
- Storage control
- Functional storage unit
- I/O control
- 8130/8140 external function control
- Floating-point (basic on 8140 Models A41-A44, an RPQ on 8140 Models A6X and A7X, and a feature on 8140 Models BXX)

The functional storage unit provides program and data storage. In 8140 Models A3X, A4X, and A5X, each card contains 32K bytes of storage up to a maximum of 512K, depending on model. In 8140 Models BXX, A6X, and A7X, each card contains 128K bytes of storage up to a maximum of 1024K, again depending on model. In the 8130, the first, or basic, storage card contains 256K bytes of storage, the first feature card can contain either 128 or 256K bytes, and the second and third feature cards contain 256K bytes. The processor executes programs that have been placed in this storage area from an external input source.

Buses permit information transfer between all functional elements, which are logically connected by control lines originating from the ROS control subsystem.

The 8130/8140 uses previously established forms of error detection and data protection to maintain data integrity and security, some of which are:

- Parity checking on data and control paths
- Check character processing
- Format checking of instructions and control fields within the hardware
- Validity checking of storage addressing
- Storage protection
- ECC logic in the processor to storage data paths, to correct single bit failures and detect double bit failures (not available on 8140 Models A3X, A4X, or A5X).

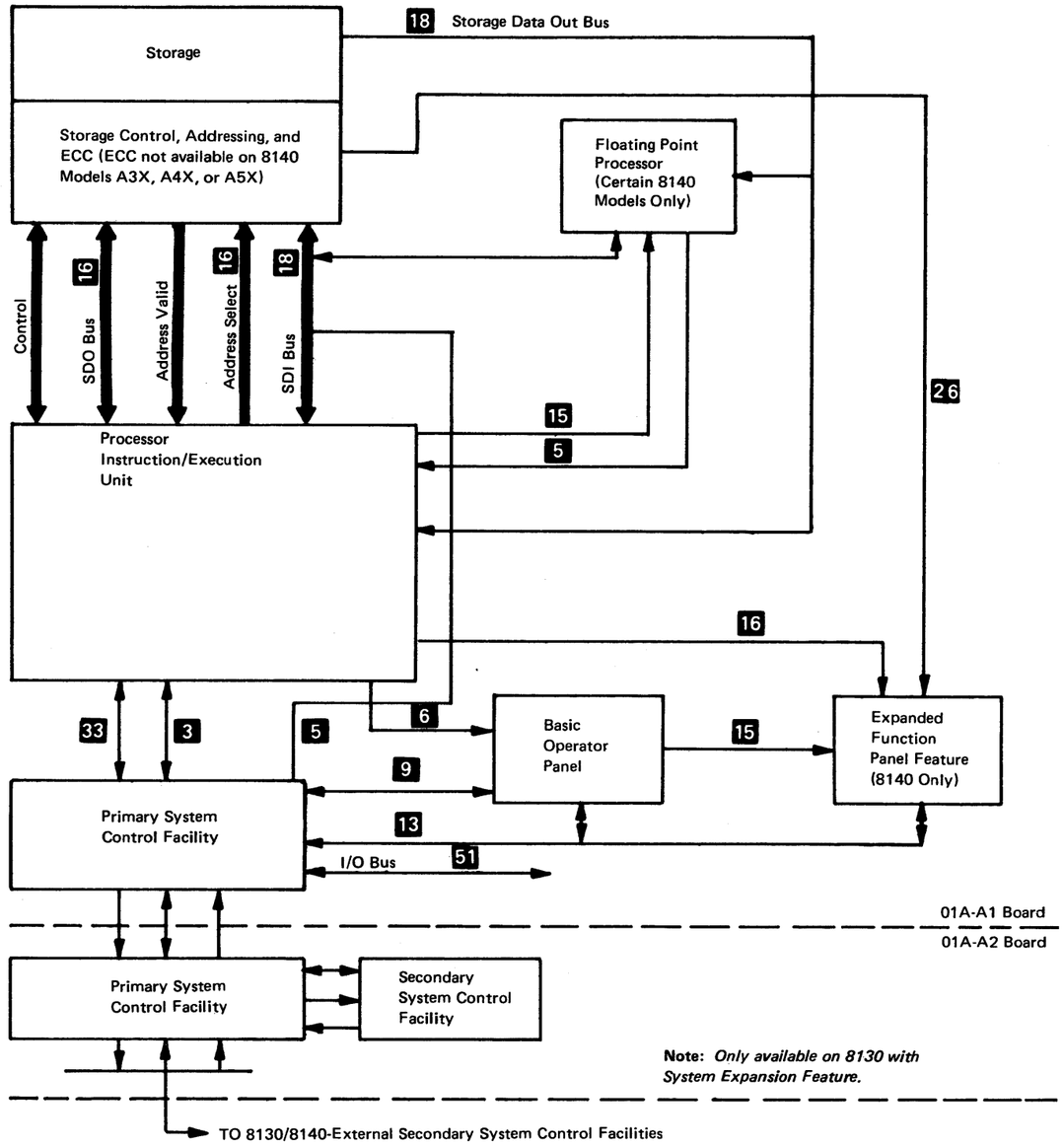


Figure BU120-1. 8130/8140 Basic Data Flow

BU122 Basic Operator Panel (BOP)

The processor transfers information with the BOP and the MD through the BOP adapter by using the I/O halfword instruction. This specifies the BOP address (hex 09) and the command to be executed. The BOP adapter decodes the instructions to determine the operation and to which (BOP or MD) it applies. These programmed 16-bit transfers also permit the processor to analyze and alter the BOP control vector and the contents of the display, status, and MD registers.

The BOP permits the user to exert manual control over the system by:

- Entering data parameters
- Entering function parameters
- Establishing IPL selection parameters
- Initiating a system reset, which results in an automatic IPL sequence
- Providing keylock security for power control and operator panel input functions (if the feature is installed)

The BOP also provides:

- System or test information either through indicators, or the four-position hexadecimal display
- Indication of proper or improper power operation
- The logical signal attachment and control of the MD
- 8130/8140 power on/off control

Figure BU122-1 shows the basic operator panel.

The following text describes the switches, pushbuttons, and indicators of the basic operator panel, and explains their function or meaning.

Power Controls and Indicators

Power On/Power Off switch — A two-position, binarily marked rocker switch that, when placed in the Power On position, initiates an 8130/8140 power-on sequence. If any attached 8101 or 8809 power switches are on, it also initiates power sequencing to these units. During the power-on sequence (approximately 70 seconds), the BOP indicators and hexadecimal display do not contain valid information and should be ignored. When the power-on sequence completes, the indicators assume the status that they would normally have as a result of a reset/IPL sequence, and the IPL function then begins. When placed in the Power Off position, turns off 8130/8140 power.

Power On indicator — On during initial power sequencing (approximately 70 seconds), and remains on to indicate completion of a successful power-on sequence. The 5V voltage sense line determines the indicator status.

Power On Disabled indicator — On when the normal power-on sequence is disabled by executing a programmed power-off command, and also when removing and restoring utility power after a power/thermal check. In addition, if the keylock feature is installed, the indicator is on if power was removed with the keylock switch in the Secure position. To reset the indicator, turn the keylock switch (if installed) to the Enable or Power Only position and the power switch to Power Off.

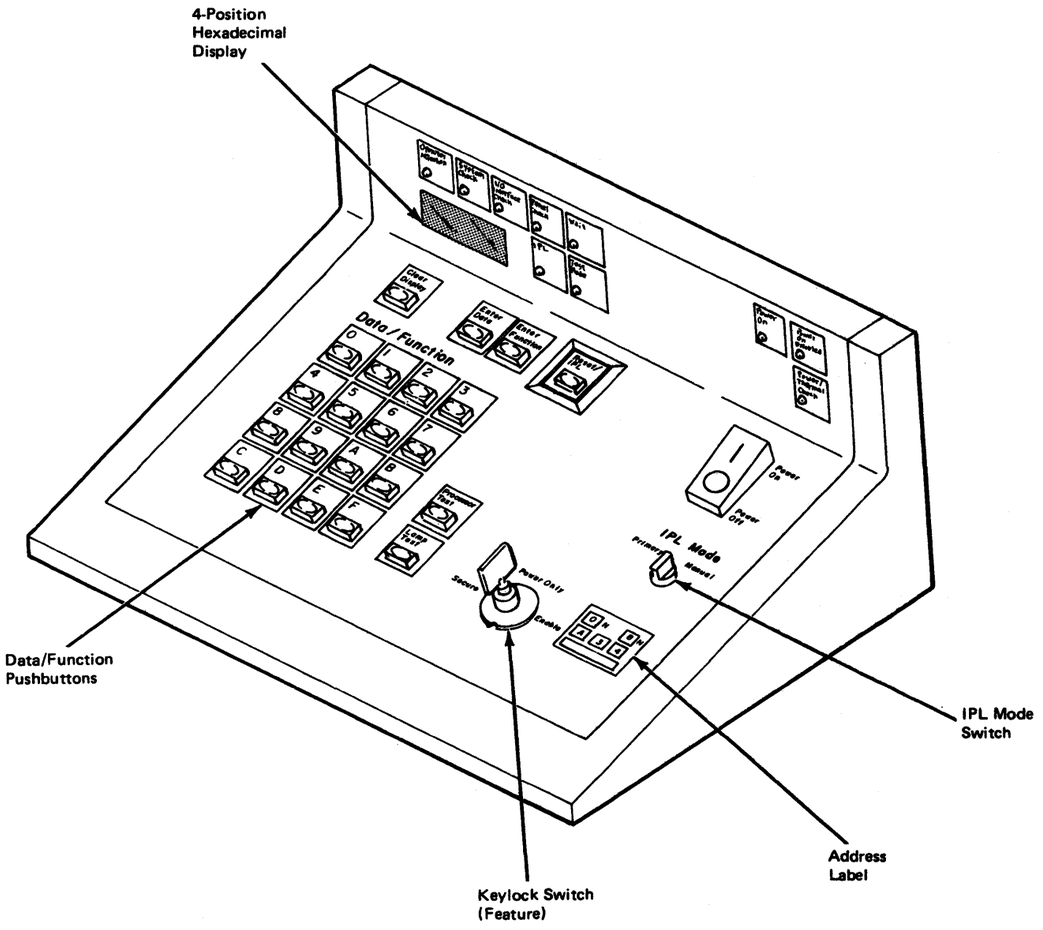


Figure BU122-1. Basic Operator Panel (BOP) with Keylock Feature Installed

Power/Thermal Check indicator – Turns on when a power-off sequence has occurred for one of the following reasons:

- An undervoltage or overvoltage condition
- Receiving the brake applied signal from disk storage
- An excessive temperature condition in the processor
- Opening of the disk storage interlock lever switch

After fault isolation, the indicator can be reset by turning the power switch to Power Off then Power On.

Refer to the power MAP (PA) for power/thermal repair actions.

IPL Mode Switch: Providing the keylock switch (if installed) is in Enable, permits the user to (1) enter IPL parameters from the Data/Function pushbuttons when set to Manual, or (2) select a previously set parameter value in either the PSCF programmable register or the PSCF hardware switches when set to Primary. Refer to Chapter 2, CP520, for a detailed description of IPL modes.

Keylock Switch (Feature): This key-activated, three-position switch restricts functional operation of the BOP pushbuttons and system power controls. The following describes the positions and their meaning.

- Secure – Disables all panel pushbutton functions, but power can be turned off. If the 8130/8140 is powered off, this position will not permit a power-on sequence.
- Power Only – Disables all panel pushbuttons except the Power On/Power Off switch. The IPL mode switch defaults to primary mode.
- Enable – Enables all power and panel pushbutton functions.

Note: *Without this feature, the system defaults to the Enable position.*

Display: The BOP uses a four-position hexadecimal display to indicate:

- BOP to processor input/output information.
- System message numbers (SMNs).
- System error information.

The user manually enters four hexadecimal characters that appear starting at the left of the display. Any more than four characters entered are ignored, and any input error can be corrected by the Clear Display pushbutton and subsequent reentry of the correct values. Bit 4 of the BOP control register, if on, does not permit information transfer between the display register and the processor and causes a blank (dark) display.

Indicators

Operator Attention – Functions under program control, and when on, the processor expects input from the keypad. BOP control register bit 0 determines the indicator status.

System Check – On when any of the following conditions occur:

- A processor instruction/execution unit hardware error
- An I/O error
- A program error associated with a channel I/O operation
- A program exception while using a primary PSV.

It is reset either by a BOP Reset Adapter command, processor logic, or otherwise removing the error condition.

I/O Interface Check – Functions under program control, and when on, the processor detected that it could not access any adapters. This error occurs during either an IPL error recovery or a channel I/O operation. The BOP basic status register bit 12 (IPL) must be off to turn this indicator on, and a system reset or a BOP Reset Adapter command turns this indicator off.

Panel Check – The program detected an error either in the BOP adapter or on the panel bus. If on, all other indicators are unreliable. This error can be caused by the adapter, a logic card, a defective cable or improper cable seating, or other adapter-to-panel malfunctions. A system reset or a BOP Reset Adapter command turns this indicator off.

Note: *If the indicator is on because of an incomplete signal path in the three cables containing the BOP cable interlock circuitry, these methods do not reset this indicator.*

Wait – On when the processor is not executing instructions, and reset either when the processor begains instruction execution or by a system reset.

IPL – Processor is executing an IPL. Turned on either by a power-on reset, pressing the Reset/IPL pushbutton, or performing a programmed IPL instruction, and turned off either by the program or logic. BOP status register bit 12 determines the indicator status.

Test Mode – On during IPL or bringup testing, and blinks twice each second when displaying bringup test error messages of 0100 or above. BOP control register bit 1 determines the indicator status, and bit 2 determines if it blinks.

Pushbuttons

Clear Display – Resets the BOP display register to zeros. This pushbutton does not affect other BOP registers or request a processor interruption.

Enter Data – Pressing this pushbutton after entering information into the Data/Function pushbuttons specifies to the program that the values should be used as data rather than function input. It also turns on the data entry bit (8) and the interrupt request bit (15) in the BOP basic status register.

Enter Function – Pressing this pushbutton after entering information into the Data/Function pushbuttons specifies to the program that the values should be used as a function input rather than data. It also turns on the function entry bit (9) and the interrupt request bit (15) in the BOP basic status register.

Reset/IPL – Performs a system reset and initiates an IPL sequence. The keylock (if installed) and IPL switch settings operate in conjunction with this pushbutton.

Processor Test – When pressed, the rightmost position of the BOP hex display indicates whether a parity error occured within any of four processor cards. See BU249 for more detailed information.

Lamp Test – Activates all BOP indicators except the 4-position hexadecimal display. Also activates all expanded panel (if installed) indicators except the 8-position hexadecimal display and the Current or Last Level indicator.

Data/Function pushbuttons – Enter either hexadecimal data or function information to the operator panel display register. These pushbuttons are functionally unlocked only when the processor and program permit input, and only with the keylock switch (if installed) in the Enable position.

BU123 Floating Point

Floating-point instructions are used to perform calculations on operands that use many significant digits, and to yield results designed to maintain precision. This function is basic on 8140 Models A41–A44, is an RPQ on 8140 Models A6X and A7X and is a feature on 8140 Models BXX.

The floating-point (FP) function uses two cards. These cards logically contain an FP processor, as well as the data and control lines to the processor instruction/execution and storage cards. The pico ROS card (BU451) controls FP functions. Data can be in either 32-bit (short precision) or 64-bit (long precision) formats. The floating-point control card contains eight sets of registers used only for FP operation, each register set containing four 64-bit registers.

Note: *The processor I/E cards control the system check and condition value decodes for the FP function.*

BU130 BU MAP Unique Repair Strategy

Use the Chapter 1 General Failure Index (GFI) for initial 8130/8140 fault isolation. The GFI then refers you to the appropriate MAP according to the failure indication, where you then perform repair actions relating to the failure. When the GFI directs you to the BU MAP because of a bringup failure, you are instructed to run the BU tests. To do this, insert MD diskette 01 and select diskette MAP menu option 1, BU tests.

This displays the BU MAP menu, where you can select A to run the BU tests, B to use a BU test error message, or C to perform the BOP basic checkout procedures.

- UNLESS INSTRUCTED OTHERWISE, YOU SHOULD ALWAYS SELECT MENU OPTION "A", which provides a step-by-step procedure used to perform both basic and extended BU testing and also isolate BOP problems. If the MAP determines that the BOP caused the error, the MAP then automatically invokes the BOP checkout procedures used for option C.
- Option B uses a test error message to generate a list of FRUs that could cause the failure. This option does NOT consider that the operator panel could cause the error message, in which case the message might not be a valid indication. Selection B could be used if you have an error message resulting from an intermittent repair strategy and want to know the cards that could cause this error.
- Option C (8140 only) allows you to quickly analyze failures caused by the BOP.

The BU MAP uses certain flag bits, which are transparent to the user, to logically step the procedures. If you press RESET on the MD, you reset these flag bits and interrupt this logical flow, and the MAP then starts at the beginning. For example, these flag bits can be used to indicate where the MAP continues after you perform a repair action. If you exchanged a card as directed by the MAP and a new error occurs, the MAP retains the logical sequence of the action performed, according to your input to the MD. It then may instruct you to verify the fix by checking card and cable seating, checking the part number, or other methods. If you verified the fix and the same new error occurs, the MAP considers this failure to be unrelated to the previous failures and proceeds accordingly.

The MAP might only isolate BOP component failures to a FRU group rather than a particular FRU. In this instance, the MAP then directs you to the maintenance reference information for further FRU isolation, and you can decide if you should perform this isolation.

BU200 Offline and Online Bringup and Basic Operator Panel Tests

Bringup (BU) tests are logically grouped into basic and extended routine sections. They check the functional capability of the processor instruction/execution unit, storage, storage control, part of the primary system control facility, and also the BOP. Neither the basic nor the extended tests can operate concurrently with the customer application, but the extended tests can be requested, loaded from disk storage, and executed if the system uses either the DPPX or the DPCX operating systems. No MAP interaction occurs, however, when loading from disk storage.

- Basic BU tests occur during every 8100 powerup and also when pressing the Reset/IPL pushbutton. This test verifies part of processor storage, as well as all other hardware necessary to correctly load additional data.
- Extended BU tests always occur during a power-on primary IPL sequence. Refer to CP520 in Chapter 2 for an explanation of IPL modes. The tests can also occur during a reset/IPL sequence if specified by the IPL parameters, provided the 8100 uses either the DPPX or DPCX operating systems. If run from the MD, the MD must be connected with MD diskette 01 loaded. It completes processor testing and checks proper operation of all processor storage not tested by the basic BU tests.

Basic Bringup Tests

The basic BU tests are an integral part of the physical 8130/8140 Processor and reside in the 4K read-only-storage (ROS) area.

Note: *Neither the service representative nor the customer can access this area.*

The tests run automatically when:

- Pressing the Reset/IPL pushbutton.
- A power-on sequence initiated by the Power Off/Power On switch occurs.
- An automatic system power restoration after a utility outage occurs.
- Executing a programmed IPL sequence.

The test verifies part of processor storage, as well as those portions of the processor instruction/execution cards, system control facility, and BOP needed to load from an IPL device. Test options enable you to select BOP display and keypad tests, display the PSCF hardware switch values, display the PSCF programmed IPL register contents, or select run and loop options for extended BU testing.

The test, structured by routine, uses each routine to verify specific operations. Where possible, testing occurs on each instruction, function, or logical component before incorporating them into another routine. As testing progresses from reset to device load, ROS reports test status through the BOP display register. These indications reflect either (1) test progress (BOP display values 0000 to 00FF), (2) error messages, or (3) prompting messages.

The initial testing phase uses a KDO instruction to increment the last two BOP display characters. Starting at address hex 0000, as each operation completes successfully, the display increments to the next higher value. If this progress value does not change within 5 seconds, the display value indicates successful completion to that point, and is used as the test error message entry for BU MAP operation. Errors that occur after initial SCF and BOP testing result in a four-character message on the BOP display.

Successful completion of the basic BU tests enable ROS to determine the IPL device type specified, and to load the selected program from the device. This program can be either (1) the extended BU tests, (2) a test control monitor, (3) a control program, or (4) a utility, depending on the IPL parameters specified.

Extended Bringup Tests

Because the basic BU tests check only enough logic to permit correct initial program loading, the extended BU test should be performed to ensure full processor functional capability. The tests reside on disk storage when using either DPPX or DPCX, and MD diskette 01 when using the MD. Unless performing the extended BU offline under MAP control, the MD does not have to be connected. In either case, IPL parameter bits 2 and 3 must be on.

Note: *The initial PSCF switch setting does not permit extended BU test execution when using primary IPL mode.*

These tests check the remainder of the instruction set not tested by the basic BUs, as well as testing real and logical storage addresses and addressing facilities, processor storage, register storage, level switching functions, and PSV swapping capabilities. Certain routines also test the floating-point functions on certain 8140 Models, if installed.

BU201 How to Invoke the Basic Bringup Tests

The basic BU tests require complete system dedication. Obtain the system from the customer and do the following to perform an IPL in manual mode:

1. Set keylock switch (if installed) to Enable.
2. Set IPL Mode switch to Manual.
3. Press the Reset/IPL pushbutton to initiate the test.

A prompt message of 0200 in the BOP display indicates successful completion of the basic BU test.

BU202 How to Invoke the Extended Bringup Tests

The extended BU tests can be run offline on systems using either DPPX or DPCX, but should normally be invoked under MAP control from the MD. By using the MD, the tests load and automatically run from the MD by prompting you to perform specific steps while using the MAPs.

How to Invoke the Extended BU Tests from the MD Under Map Control

To invoke the extended bringups under MAP control, obtain the system from the customer and do the following:

1. Open the 8130/8140 front covers and locate the 01H gate (bracket) on the right.
2. Attach the MD signal cable to the 25-pin socket, and insert the MD power plug into either convenience outlet directly below it.
3. Power on the MD, insert MD diskette 01, and IPL the MD.
4. At the MD diskette 01 menu, enter '1' to select the BU MAP.
5. At the BU MAP menu, enter 'A' to select offline checkout.

The MAPs then prompt you to perform the procedures necessary for BU testing, which also includes loading and running the extended BU tests according to the MAP results. Successful completion of the extended BU tests displays 3F00 in the BOP.

How to Invoke the Extended BU Tests without MAP Control

The extended BU tests can be invoked without using MAP control by either of two methods:

- To invoke the extended BUs from the MD without MAP control, refer to Chapter 2, under CP523, "How to Run Bringup Tests Using the MD Free-Lance Utility.
- To invoke the extended BUs from disk storage without MAP control, the 8100 must operate using either DPPX or DPCX. Obtain the system from the customer and perform the following steps at the BOP:
  1. IPL the system in manual mode (see BU201).
  2. At successful completion of the basic BU tests (BOP prompt message 0200), enter 33PA and press Enter Data on the BOP, where PA is the system-resident disk physical address.
  3. At prompt message 0201, enter '00FF' and press Enter Function.

The extended BU tests now load and execute from disk storage and, if successful, result in a 3F00 message in the BOP display. If any errors occur, invoke the BU tests using MAP control. Refer to Chapter 2, CP500, for more detailed information concerning initial program load and parameter meanings.

BU203 How to Loop the Extended BU Tests

The extended BU tests can be looped without using MAP control by either of two methods:

- To select and loop extended bringups from the MD without MAP control, refer to Chapter 2, under CP523, "How to Run the Bringup Tests using the MD Free-Lance Utility".
- To select and loop the extended tests from the disk storage without MAP control, the 8100 must operate using either DPPX or DPCX. Obtain the system from the customer and perform the following steps at the BOP:
  1. IPL the system in manual mode (see BU201).
  2. At successful completion of the basic BU tests (BOP prompt message 0200), enter 33PA and press Enter Data, where PA is the system-resident disk physical address.
  3. At prompt message 0201, enter a test option according to the following format, then press Enter Function.

Option	Description
00RR	Run the selected routine (RR) of the extended tests once. Refer to section BU213 for routine descriptions. This option runs extended test routine RR one time. A BOP display value of 3F00 indicates successful completion.
01RR	Loop the selected routine (RR) of the extended tests. This option loops the selected routine. Terminate this option by pressing Reset/IPL.
00FF	Run all extended tests once and stop when any error occurs. A BOP display value of 3F00 indicates successful completion.
01FF	Loop all extended BU tests. This option loops all extended bringup tests and stops on any error. Terminate this option by pressing Reset/IPL.

The test then executes according to the options selected. If any errors occur, invoke the BU tests using MAP control.

BU204 How to Invoke the BOP Manual Intervention Tests

The following describes the procedures necessary to perform the manual intervention routines used to test the BOP.

Basic Keypad/Display Test

1. IPL the system in manual mode (see BU201).
2. At successful completion of the basic BU tests (BOP prompt message 0200), enter 33PA and press Enter Data on the BOP, where PA is the system-resident disk physical address.
3. Again press Clear Display, followed by Enter Data. This test places 0000 in the BOP display, and increments this value by hex 1111 until the display indicates hex FFFF.
4. When the prompt message 0202 appears, enter any four hex characters from the BOP keypad and press Enter Data.
5. When prompt message 0203 appears, press Enter Data. The four characters entered in step 4 should then appear in the BOP display.
6. To return to the 0202 prompt message for further testing, press Enter Data.
7. To exit the routine, press Reset/IPL.

If any failures occur:

1. IPL the MD using MD diskette 01.
2. At the MD diskette 01 menu, enter '1' to select the BU MAP.
3. At the 8140 BU MAP menu, enter 'C' to select the BOP checkout option; at the 8130 BU MAP menu enter 'A' to select the offline checkout option.

BOP Indicator Test — Routine 3B

This test must be selected and requires manual intervention. If the 8100 does not use either DPPX or DPCX, it must be loaded offline from the MD using the Free-Lance Utility. Refer to Chapter 2, under CP523, "How to Run Bringup Tests Using the MD Free-Lance Utility".

Routine 3B tests the ability to turn all indicators off and on under system control. It assumes that all indicators operate correctly using the Lamp Test pushbutton. If any indicator fails from the Lamp Test pushbutton, use either 8140 BU MAP menu selection C and perform the BOP checkout procedure, or 8130 BU MAP menu selection A and perform the offline checkout.

To invoke the test:

1. IPL the system in manual mode (see BU201).
2. At successful completion of the basic BU tests (BOP prompt message 0200), enter 33PA and press Enter Data on the BOP, where PA is the system-resident disk physical address.
3. At prompt message 0201, enter '003B' and press Enter Function.

The test now loads from disk storage and begins by displaying '3B00'. To proceed through the test, press Enter Function while observing the display and indicator lights. Every time you press Enter Function, an indicator should change status and a corresponding message should be displayed. Refer to Figure BU204-1 for correct indicator status according to the displayed message. Press Reset/IPL to exit the routine.

If the repair actions in Figure BU204-1 do not correct the error:

1. Perform either the defective indicator card or cable wiring test in the BOP Indicator Checkout Procedure (BU254).
2. Perform the Cable Interlock Checkout Procedure (BU254).

Display	Correct Indicator Status	Failure Repair Action for Incorrect Indicator Status
Blank	All indicators off except Power On.	1. Exchange BOP adapter card.* 2. If Panel Check indicator is on, perform cable interlock checkout procedure in BU254.
3B01	Operator Attention on	Exchange BOP adapter card.*
3B02	System Check on	1. Exchange BOP adapter card.* 2. Check for continuity between 01B–B1A5B06, 01A–A1F1B13, and 01A–A1D2J07 (8140 AXX) or 01A–A1G2J07 (8140 BXX).
3B03	I/O Interface Check on	Exchange BOP adapter card.*
3B04	Panel Check on	1. Exchange BOP adapter card.* 2. Check for cable jumper continuity at 01B–B1A3B04. 3. If present, check for continuity between 01B–B1A5D11, 01A–A2A5D04, and 01A–A2G2M10 in an 8130, or between 01B–B1A5D11, 01A–A1E1B11, and 01A–A1A2M10 (8140 AXX) or 01A–A1D2M10 (8140 BXX).
3B05	IPL on	Exchange BOP adapter card.*
3B06	Test Mode on	Exchange BOP adapter card.*
3B07	Operator Attention off	Exchange BOP adapter card.*
3B08	System Check off	Exchange BOP adapter card.*
3B09	IPL off	Exchange BOP adapter card.*
3B0A	Test Mode blinking	Exchange BOP adapter card.*
3B0B	Test Mode off	Exchange BOP adapter card.*
3B0C	Wait on (Press Reset/IPL to exit routine)	Exchange BOP adapter card.*

*Location 01B–A1A2

Figure BU204-1. BOP Indicator Test Table

IPL Mode Switch Test – Routine 3C

This test must be selected and requires manual intervention. If the 8100 does not use either DPPX or DPCX, it must be loaded offline from the MD using the Free-Lance Utility. Refer to "How to Run Bringup Tests Using the MD Free-Lance Utility" in Chapter 2, under CP523.

Routine 3C checks for proper system operation of the IPL Mode switch. To invoke the test:

1. IPL the system in Manual mode (see BU201).
2. At successful completion of the basic BU tests (BOP prompt message 0200), enter 33PA and press Enter Data on the BOP, where PA is the system-resident disk physical address.
3. At prompt 0201, enter '003C' and press Enter Function.

The test then loads from disk storage and begins execution with a BOP display value of 3C00. Perform the following actions according to the message displayed:

Display	Action
3C00	Turn the IPL Mode switch to Primary and press Enter Function.
3C01	Turn the IPL Mode switch to Manual and press Enter Function.
3C02	Press any Display/Function pushbutton (0–F) to ensure that the panel is disabled. To exit the routine, press Reset/IPL.

Error	Error Repair Action
3C3A	Perform the IPL Mode switch checkout procedure in BU254.
3C3C	Exchange BOP adapter card 01B–A1A2.

Keylock Switch Test – Routine 3D

This test must be selected and requires manual intervention. If the 8100 does not use either DPPX or DPCX, it must be loaded offline from the MD using the Free-Lance Utility. Refer to "How to Run Bringup Tests Using the MD Free-Lance Utility" in Chapter 2, under CP523.

Routine 3D checks that the system can recognize the keylock feature switch settings. To invoke the test:

1. IPL the system in manual mode with the keylock switch in Enable (see BU201).
2. At successful completion of the basic BU tests (BOP prompt message 0200), enter 33PA and press Enter Data on the BOP, where PA is the system-resident disk physical address.
3. At prompt message 0201, enter '003D' and press Enter Function.

The test then loads from disk storage and executes starting with a BOP display value of 3D00. Perform the following actions according to the message displayed:

Display	Action
3D00	Press Enter Function and turn the keylock switch to Secure. If not done within 5 seconds, an error will occur.
3D01	Turn the keylock switch to Enable and press Enter Function.
3D02	Press Enter Function and turn the keylock switch to Power Only. If not done within 5 seconds, an error occurs.
3D03	Turn the keylock switch to Enable and press Enter Function.
3F00	Test completed successfully.

Error	Repair Action
3D3B	Perform the keylock switch checkout procedure in BU256.

BU205 How to Display IPL Parameters

This test option displays the value of either the PSCF IPL hardware switches or the PSCF programmed IPL register. To invoke this option:

1. IPL the system in manual mode (see BU201).
2. At the completion of the basic BU tests (prompt message 0200), press Clear Display and then Enter Data on the BOP.
3. At prompt message 0201, enter the test options according to the following format, then press Enter Function.

Option	Description
0001	Display IPL hardware switch values. This option places the PSCF hardware IPL switch register value into the BOP display.
0002	Display IPL programmed register contents. This option places the PSCF programmed IPL register value into the BOP display.

The BOP now displays the parameter value according to the option selected. Refer to Chapter 2, CP510, "IPL Parameters" for a description of the IPL parameter meanings.

BU206 How to Invoke the Processor Storage Data Retention Test

This test, which is actually Routine 37 of the extended BUs, completes within 18 to 35 minutes, if manually selected, depending on the processor machine type. When the 8100 does not use either DPPX or DPCX, the routine must be loaded offline from the MD by using the Free-Lance Utility. Refer to "How to Run Bringup Tests Using the MD Free-Lance Utility" in Chapter 2 under CP523.

Routine 37 ensures that processor storage can retain data after not being active for a period of time. The routine stores all one bits in all storage addresses above 4K, delays a specified time without executing a storage access, fetches all data, and then compares it to the values previously stored. It then repeats those steps using all zero-bits. Finally, it uses random bit patterns to check the parity bits.

To invoke the test:

1. IPL the system in manual mode (see BU201).
2. At successful completion of the basic BU tests (BOP prompt message 0200), enter 33PA and press Enter Data on the BOP, where PA is the system-resident disk physical address.
3. At prompt message 0201, enter 0037 and press Enter Function.

The test then loads from disk storage and begins executing with a BOP display value of 3700.

Note: *To abnormally terminate the test press Reset on the 8130/8140 BOP.*

Perform the following action indicated by the error message displayed:

Display	Meaning
3700	Test running
3701	Test running
3702	Test running
3703	Test running
3704	Test running
3705	Test running
3F00	Test completed successfully

Error	Action	Comment
3765 or 37CC	Press Enter Function for extended error code XXYY. The 'XX' value indicates the failing 32K block of storage. (00 to 1F)	Use BU111 to determine the location of the failing card. Exchange with a new card.

BU207 How to Invoke the Storage Scan Test

Note: *Although this test runs on all processor models, its primary purpose is to detect storage problems on 8140 Models A3X, A4X, and A5X.*

The Storage Scan Test checks storage, registers and the translate table for bad parity and resides only on MD Diskette 01.

Note: *Run this test immediately after a system failure if the failure indicates a potential storage problem, and also if a F120 abend occurs.*

To invoke storage scan from the BOP:

1. Insert MD diskette 01 into diskette drive.
2. Press Reset/IPL. The BOP should now display 0200.
3. Enter 0187 and press Enter Data.
4. At prompt message 0201, enter 8039 and press Enter Function.

The test then loads from the diskette and begins with BOP message 3900.

The following table describes BOP messages used and lists the actions required for failure messages:

Message	Description	Action
3900	Scanning R/W storage	
3910	Scanning register storage	
3920	Scanning translation table	
3F00	Scan complete - no bad parity	
3911	Principal register parity error	Replace principal register storage card*.
3912	Adjunct register parity error	Replace adjunct register storage card*.
3913	Address control vector parity error	Replace adjunct register storage card*.
3921	Translation table parity error	Replace translation table card*.
3969	Level switching error	Run extended BUs.
39CX	Storage parity error (512K or less)	X-value indicates failing 32K block of storage*. Press Enter Function on the BOP to display the failing array address within the 32K block.
39DX	Storage parity error (greater than 512K)	X-value indicates failing 32K block of storage*. (0 = block 10, 1 = block 11, etc.) Press Enter Function on the BOP to display the failing array address within the 32K block.
39EX	System check	See BU241 RREX messages for meaning.

*See BU111 for card locations.

BU210 Offline Test Routine Descriptions

Section BU211 discusses the common error message handler subroutine used to process unexpected system check interruptions during BU testing. Sections BU212 and BU213, respectively, list and describe the routines used in basic and extended BU testing, as well as listing all valid error and status messages for each routine.

BU211 Common Error Message Handler Subroutine

This subroutine handles all system check interrupts that occur while running either the basic or extended BU tests. Because system checks can occur at any time, the error message format RREN indicates the routine in which the system check occurred and the error number. This subroutine generates test error messages RRB0 to RRBF, RRC0 to RRCF, and RRE0 to RREF on the BOP display. Refer to section BU241 for the meaning of these test error messages.

BU212 Basic Bringup Test Routine Descriptions

The following lists and describes the routines used for basic BU testing. Note that all basic BU test messages do not correspond to the RREN format.

Routine 01, Condition Value and Jump Test. Begins at storage address 0000, operates on level 0, and ignores any system checks. Errors stop processing with a test error message displayed in the BOP. A KDO instruction first executes to step the display to 0001, indicating the beginning of IPL. Before using any registers, the PSV 0 contents load into processor storage to retain data for the dump utilities. A later routine checks the validity of this save. To permit error analysis for subsequent routines, testing begins for all logical type condition value settings and jumps by performing the LRI, TRI, ORI, XRI, NRI, ARI, and JC register-immediate instructions. During this routine, the System Check indicator should be on and the Test indicator off. The valid error halt numbers are 0000 to 000E.

Routine 02, Control Vector Storage Area Initial Test. Verifies the reset of the registers used to contain the system control vector information, as well as the ability to set values into these areas by performing certain KI instructions. IPL alters primary register set numbers 30 and 31, which become the primary and secondary register sets used throughout the IPL operation. During this routine, the contents of these registers transfer into processor storage.

This routine tests the following KI instructions:

Set Master Mask (KI 14)
Reset Master Mask (KI 0)
Read Master Mask (KI 1)
Write Condition Indicators (KI 26)
Read Condition Indicators (KI 27)
Write Common Mask (KI 2)
Read Common Mask (KI 3)
OR to PIRV (KI 4)
AND to PIRV (KI 6)
Read PIRV (KI 5)
Read Current and Last Levels (KI 15)
Read IOIRV (KI 7)
Write PAV (KI 120)
Read PAV (KI 121)
Read Channel Mask (KI 25)
Write Primary Register Set Number (KI 10)
Read Primary Register Set Number (KI 11)
Write Secondary Register Set Number (KI 12)
Read Secondary Register Set Number (KI 13)
Write System Check/Program Exception (KI 8)
Read System Check/Program Exception (KI 9)

The Test indicator should remain off and the system Check indicator should turn off during this routine. The valid routine error halt numbers are 000F to 001B.

Routine 03, Basic Arithmetic and Compare Test. Checks basic arithmetic instructions for proper results and condition values, as well as using and testing compare instructions. The instructions tested are: AHR, AYR, AHRI, SYR, CR, and CHR. The Test indicator should remain off, and the valid routine error halt numbers are 001C to 001F.

Routine 04, Register-to-Register Instruction Test. Checks instructions that transfer data between registers. The instructions tested are: LR, LHR, RL, RLH, XR, XHR, LHRN, STHRN, and OR. The Test indicator should remain off, and the valid routine error halt numbers are 0020 to 0022.

Routine 05, Branch Instruction Test. Verifies the ability to link and return to a subroutine. It tests the BALR instruction to ensure that (1) a branch to the proper address occurs and that it stores the correct link address, and (2) it stores the correct link address but that no branch occurs on register 0. It also tests the BCR instruction under all branch conditions to ensure a return to the next sequential address. All branches occur to addresses within the ROS area. The Test indicator should remain off, and the valid routine error halt numbers are 0023 and 0024.

Routine 06, Storage-to-Register Instruction Test. Checks the basic instructions that transfer data between processor storage and a register. The instructions tested are: LN, LHN, LH, STN, STHN, and STH. The Test indicator should remain off, and the valid routine error halt numbers are 0025 to 002D.

Routine 07, ROS Parity and Checksum Test. Tests all 4096 ROS bytes for validity. It reads all halfword locations using the LHN instruction, adds them together, and then compares this value to a predetermined checksum value (FFFE). It also tests all ROS locations for correct parity (no system check), except the bad parity location used to generate a system check. The Test indicator should remain off, and the valid routine error halt numbers are 002E to 0034.

Routine 08, Register Logout. Transfers into processor storage primary register sets 30 and 31, channel pointers, adjunct registers, and the primary register set locations used to contain PSV levels 0 and 1. The Test indicator should remain off, and the valid routine error halt numbers are 0035 and 0036.

Routine 09, I/O Instruction Basic Test. Tests I/O instructions while attempting to transfer information with the SCF. It tests initial basic status after system reset, the Set and Reset Basic Status commands, the Reset SCF Control command, and the Read and Write Program IPL Parameter commands. The Test indicator should remain off, and the valid routine error halt numbers are 0037 to 003B.

Routine 10, Basic Operator Panel Adapter Test. Tests the system's ability to transfer information with the BOP by opening the system direct control bus to the BOP adapter and then performing the following commands: Read Basic Status, Read Control Byte, Read Display Register, and Set and Reset Basic Status. It also checks the initial validity of the BOP BSTAT, the control register, and the display register. The Test indicator should remain off, and failures turn on the Panel Check indicator, resulting in valid routine error halt numbers from 003C to 0049.

Routine 11, Basic Operator Panel Test. Tests the ability to use the BOP for output. It performs Write Control Register and Write Display Register commands to the BOP, followed by read and compare operations. Previously, the KDO instruction only set the last two BOP display characters. Successful completion of this routine results in writing four-character progress and error codes to the panel display. This routine turns on the Test indicator, which remains on throughout the rest of IPL testing, and the valid routine error halt numbers are 004A and 004B.

Routine 12, Processing Level Zero and One Interrupt Test. Causes an interrupt from level zero to level one processing, and also determines that a system check will interrupt level one processing. Level zero to level one interrupt occurs by: (1) setting the PIRV for level zero, which specifies an interrupt request on this level, (2) resetting the program interrupt request bit in the EIRV, which deactivates level zero, (3) setting the PIRV for level one, which specifies an interrupt on this level, (4) setting the common mask for levels zero and one to permit interruption, and (5) resetting the PIRV for level zero. The processor now executes on level one, and the level zero interrupt handler routine then controls future processing level zero interruptions. In this routine, the Test indicator either blinks for error halt numbers 0120, 0121, and 01C0 to 01EF, or remains on for progress indicator values of 0100 and 0101.

Routine 13, IPL Mode Determination. Examines the IPL variables that determine if the test exits either to Routine 14, 16, 18, or 19. These variables are:

1. How the IPL was invoked.
2. The parameters specified: (a) the IPL load device, (b) whether to initialize storage, and (c) whether to run extended bringups.
3. The IPL switch position.

The Test indicator remains on for a progress indicator of 0102, and blinks for error halt numbers 0122, 0123, 014C, and 01C0 to 01EF.

Routine 14, Manual IPL Handler. When performing a manual IPL, this routine stops, prompts, and reads the manual IPL parameters entered from the BOP. This routine does the following:

1. Turns on the Operator Attention indicator.
2. Writes a prompt message (0200) to the BOP display.
3. Enables the Data/Function pushbuttons.
4. Waits for an interrupt from either the Enter Data or Enter Function pushbutton.
5. Reads the panel display register value.

If the interrupt was caused by the Enter Data pushbutton, the routine repeats steps 4 and 5.

If the interrupt was caused by the Enter Function pushbutton, the following explains how the entry is interpreted:

- The first four characters are always IPL parameters.
- The first character of the next four defines the rest. If the value is from hex 8 to hex F, it specifies that the control program should receive the entered value. If the value is from hex 0 to hex 7, the value is used for test looping and test run options.

Depending on the pushbutton pressed, the test interprets the variables and then either branches to Routine 13 for the remaining IPL variables, or branches to Routine 15 for test options. Both conditions turn off the Operator Attention indicator and disable the Data/Function pushbuttons.

The Operator Attention indicator remains on when prompting for these parameters. The Test indicator remains on for progress indicator values of 0200 and 0201, and the Test indicator blinks for error halt numbers 0223, 023C, 024C, 0281, 0282, and 02C0 to 02EF.

Routine 15, Basic Operator Panel Manual Tests. This routine is selected only by specifiying the BOP manual test or the display IPL parameter option during manual IPL. According to the option selected, this routine either (1) tests the BOP display and Data/Function pushbuttons, (2) displays the IPL parameter switch settings, or (3) displays the IPL programmed register parameters. IPL must again be performed to exit from this routine. The Test indicator remains on for progress indicator values of 0202 and 0203, and blinks for error halt numbers 023C, 024C, 0282, and 02C0 to 02EF.

Routine 16, Bits 16–31 Principal Register Test. Executes only when initiated by a power-on IPL sequence, or with IPL parameter bit 2 (exended test) on. It checks all principal registers except principal register set numbers 30 and 31.

Note: *Up to this point, the only registers tested were the principal register PSV 0 and 1 save area (half of principal register set 0) and principal register set numbers 30 and 31.*

This test uses several data patterns, which are placed into principal register sets 0–29 and 32–63 by using STHRN instructions, and then read back by using LHRN instructions. These patterns are then compared to previously stored data to ensure validity. The Test indicator remains on for progress indicator value 0300, and blinks for error halt numbers 0325, and 03C0 to 03EF.

Routine 17, Zero to 64K Processor Storage Test. Executes only when initiated by a power-on IPL sequence, or with IPL parameter bit 2 (extended test) on. It should be performed before loading from an IPL device, and if errors occur the system stops processing. It checks the first 64K bytes of processor storage by loading each storage halfword location with its corresponding address and then performing a read-back operation. The whole process then repeats using five more data patterns. The Test indicator remains on for a progress indicator value of 0301, and blinks for error halt numbers 0323, 0324, and 03C0 to 03EF.

Routine 18, Processor Storage and Register Storage Initialization. As a system power-on sequence does not generate correct storage parity, this test must be performed for every IPL initiated by a power-on sequence. It executes only when initiated by a power-on IPL, or with IPL parameter status bit 3 (initialize storage) on. The test initializes all of register storage (except principal register set numbers 30 and 31), the translation table, processor storage areas not used by an IPL operation, and the address control vector area. It uses an STHN instruction to increment through all possible storage locations. After initialization, processor storage locations should contain hex FFFF, register storage should contain hex 0000 or hex 0016, the translation table should contain hex 8000, and the address control vectors should contain real addressing values for a storage size of 512K using 64K byte blocks. An STHRN instruction then increments through all storage locations except principal register set numbers 30 and 31. This routine ensures only that correct parity can be established in these areas. It performs no testing, ignores any incorrect parity conditions, and makes no data comparison. The System Check indicator turns on and off; the Test indicator remains on for progress indicator values of 0302, 0303, and 0304, and blinks for error halt numbers 0321, 034C, and 03C0 to 03EF.

Routine 19, IPL SSCF Configuration.

Note: *This routine is bypassed on an 8130 without the System Expansion feature.*

This routine is selected only if the IPL parameters did not specify the maintenance device. The test examines the IPL device address obtained from the IPL parameters to enable configuration of the SSCF for the correct IPL device. SSCF configuration occurs by issuing a Set I/O SSCF Basic Status command with the enable I/O SSCF (byte 0, bit 3) and the enable I/O unit (byte 0, bit 0) bits on. The test then performs a status check to ensure correct online configuration of the I/O unit with no error bits on. The Test indicator remains on for a progress indicator values of 0400 and 0450, and blinks for error halt numbers 0426, 044C, and 04C0 to 04EF.

Routine 20, Initialize PSCF Interrupt Register and Determine IPL Device Type.

Note: *This routine is bypassed on an 8130 without the System Expansion feature.*

This routine initializes the PSCF interrupt register by using the PIO Write Translate Register command, and sets the proper register value to permit IPL device interrupts on level one. It then examines the IPL device parameters to determine the IPL device type, and transfers control to the appropriate loader routine. This routine is selected only if the IPL parameters do not specify the maintenance device. The Test indicator remains on for progress indicator values of 0402, 0403, and 0404, and blinks for error halt numbers 0430, 0441, and 04C0 to 04EF.

Routine 21. NOT ASSIGNED

Routine 22. NOT ASSIGNED

Routine 23, Diskette IPL Loader. When the IPL parameters specify the diskette as the IPL device, this routine transfers the bootstrap loader from the first four records of diskette storage track zero into processor storage. It then branches to Routine 26 and transfers control. The Test indicator remains on for a progress indicator value of 0600, and blinks for error halt numbers 0632, 0633 to 0635, and 06C0 to 06EF.

Note: *If the diskette storage is not ready, 0632 appears in the BOP for 20 seconds and, if not ready after 20 seconds, 0633 then appears.*

Routine 24, Disk Storage IPL Loader. When the IPL parameters specify the disk storage as the IPL device, this routine transfers the bootstrap loader from disk storage track 0, sector 0, head 1 into processor storage. The test then branches to Routine 26 and transfers control. The Test indicator remains on for a progress indicator value of 0700, and blinks for error halt numbers 0734 and 07C0 to 07EF.

Routine 25, Maintenance Device IPL Loader. When the IPL parameters specify the MD as the IPL device, this routine loads either the extended BU tests or the TCM from the MD into processor storage. The Test indicator remains on for progress indicator values 0F00 to 0F04, and blinks for error halt numbers 0F38, 0F39, 0F3C, and 0FC0 to 0FEF.

Routine 26, Transfer Control. Turns off the IPL and Test indicators on the BOP, transfers program control to the previously loaded program, and then switches processing back to level zero. The Test indicator remains on for progress indicator values of 0E00 and 0EFF, and blinks for error halt numbers 0E21, 0E3C, and 0EC0 to 0EEF.

BU213 Extended Bringup Test Routine Descriptions

All test error messages used for the extended BU tests are in the RREN format, where RR equals the routine number and EN equals the error number. Certain routines use more than four hex characters for an error message. This type 2 format error message contains another four hex characters that further define the error, and which can be displayed by pressing Enter Function on the BOP.

Routine 12, Instruction Test 1. Tests the NR, AR, SR, NHR, OHR, AYHR, SHR, SYHR, and SHRI instructions. It displays a progress indicator value of 1200 and test error message numbers from 1201 to 1209.

Routine 13, Instruction Test 2. Tests the CYHRE, AYHRE, SYHRE, LHRUL, LHRLU, and LHRU instructions. It displays a progress indicator value of 1300 and test error message numbers from 1301 to 1306.

Routine 14, Instruction Test 3. Tests the SLL, SLHL, STNI, LHNI, STHNI, LNI, STND, LHND, STHND, and LND instructions. It displays a progress indicator value of 1400 and test error message numbers from 1401 to 140A.

Routine 15, Instruction Test 4. Tests the STRN, LRN, L, ST, STW, LA, STHQ, LHQ, STHS, and LHS instructions. It displays a progress indicator value of 1500 and test error message numbers from 1501 to 150B.

Routine 16, Instruction Test 5. Tests the KI 28, KI 24, KI 35, KI 37, KI 38, KI 127, JBZ, JCX, BC, JAL, BAL, TS, BCTR, CTLZ, and BNX instructions. It displays a progress indicator value of 1600 and test error message numbers from 1601 to 160F.

Routine 17, Instruction Test 6. Tests the MHR, DHR, MVS, MVHS, CLS, and CLHS instructions. It displays a progress indicator value of 1700 and test error message numbers from 1701 to 1706.

Routine 18, Level Switch Tests. Issues instructions to change the level of processing, checks to ensure that the levels changed, and also tests the ability to swap PSVs within the same level. It displays a progress indicator value of 1800 and test error message numbers from 1801 to 180A.

Routine 19, Invalid Instruction Test. Issues all invalid instructions to ensure they can be detected and that they result in a program exception. It also issues privileged instructions in both I/O and application modes to ensure that process modes operate properly. The routine displays a progress-indicator value of 1900 and test error message numbers from 1901 to 1903.

***Routine 1A, Floating-Point Initialization Test.** Verifies that all floating-point status vectors and registers can be set to zero when performing a reset/IPL function, and tests the WFC, RFC, WFS, and RFS instructions. It displays a progress indicator value of 1A00 and test error message numbers 1A10, 1A11, and 1A12.

***Routine 1B, Floating-Point Mode Test.** Checks the set and reset of the floating-point overflow, underflow, precision, and significance bits, and tests the SFOM, SFUM, SFPM, and SFSM instructions. It displays a progress indicator value of 1B00 and test error message numbers from 1B13 to 1B16.

*Routines 1A through 22 run only on 8140s with floating-point.

***Routine 1C, Floating-Point Basic Instruction Test.** Tests the LF, STF, CF, LFR, and CFR instructions. It displays a progress indicator value of 1C00 and test error message numbers 1C17 and 1C18.

***Routine 1D, Floating-Point Load Instruction Test.** Tests the LTFR, LCFR, LNFR, LPFR, and LRFR instructions. It displays a progress indicator value of 1D00 and test error message numbers from 1D19 to 1D1D.

***Routine 1E, Floating-Point Add Instruction Test.** Tests the AU, AUR, AF, and AFR instructions using both short and long precision formats. It displays a progress indicator value of 1E00 and test error message numbers from 1E20 to 1E27.

***Routine 1F, Floating-Point Subtract Instruction Test.** Tests the SU, SUR, SF, and SFR instructions using both short and long precision formats. It displays a progress indicator value of 1F00 and test error message numbers from 1F20 to 1F27.

***Routine 20, Floating-Point Multiply Instruction Test.** Tests the MF and MFR instructions using both short and long precision formats. It displays a progress indicator value of 2000 and test error message numbers from 2028 to 202B.

***Routine 21, Floating-Point Divide Instruction Test.** Tests the DF and DFR instructions using both short and long precision formats. It displays a progress indicator value of 2100 and test error message numbers from 2128 to 212B.

***Routine 22, Floating-Point Exception Test.** Ensures that floating-point exception conditions cause a floating-point system check. It displays a progress indicator value of 2200 and test error message numbers 2210 through 2212, and 2220 through 2223.

Routine 23. NOT ASSIGNED.

Routine 24, Bits 0–15 General Register Test. Loads various data patterns into all general register bits 0–15, then reads these data patterns and compares them to the expected results. It also attempts to access beyond the upper halfword address boundaries, which should result in a program exception. The routine displays a progress indicator value of 2400 and test error message numbers 2451, 2464, 2465, 2466, 2469, and 24B0 to 24EF.

Routine 25, Adjunct Register Test. Loads various data patterns into all adjunct registers then reads these data patterns and compares them to the expected results. It also attempts to access beyond the adjunct register address boundaries, which should result in a program exception. The routine displays a progress indicator value of 2500 and test error message numbers 2551, 2564, 2565, 2566, 2569, and 25B0 to 25EF.

Routine 26, PSV Instruction Address Error-Checking Test. Checks that valid PSV addresses used during logical addressing can be accepted without generating an error. It also ensures that invalid addresses cause a program exception. The routine displays a progress indicator value of 2600 and test error message numbers 2657, 2664, 2667, 2669, and 26B0 to 26EF.

Routine 27, Adjunct Register Relative Mode Test. Checks that valid adjunct register addresses do not cause a program exception and that program exceptions can be generated from invalid address values. It displays a progress indicator value of 2700 and test error message numbers 2751, 2752, 2769, 2767, 2769, and 27B0 to 27EF.

Routine 28, General Register Error-Checking Test. Checks that valid general register addresses do not cause a program exception and that program exceptions can be generated from invalid address values. It displays a progress indicator value of 2800 and test error message numbers 2851, 2864, 2869, and 28B0 to 28EF.

Routine 29. Unused General Register Access Test. Addresses general registers not used by the 8130/8140, which should generate a program exception. It displays a progress indicator value of 2900 and test error message numbers 2951, 2964, 2969, and 29B0 to 29EF.

Routine 2A. 8130 Register Delay Test. This routine can only be IPL'ed from the MD, and ensures that register space can retain data after not being active for a period of time. This routine displays progress indicator values of 2A00 and 2A01 and test error messages of 2A51, 2A52, 2A53, and 2AB0-2AEF.

Routine 2B, Boundary Violation Test. Ensures that no program exceptions occur when crossing 64K boundaries with PSV I field (instruction address range) and S field (storage-operand address range) values equal to 1. It also attempts to cross 64K boundaries with the I and S fields equal to 0, and ensures that program exceptions occur. The routine displays a progress indicator value of 2B00 and test error message numbers 2B51, 2B52, 2B64, 2B65, 2B69, and 2BB0 to 2BEF.

Routine 2F, Translation Table Addressing Test. Uses the LAT and STAT instructions and loads various combinations of block index values and relocated addresses into the translation table, where they are then verified. It also sets various zero check conditions for operands and ensures that program exceptions occur, and tests for proper control of the translation table. The routine displays a progress indicator value of 2F00 and test error message numbers from 2F51 to 2F58, 2F64, 2F65, 2F69, and 2FB0 to 2FEF.

Routine 31, Address Control Vector Test. Generates all valid address control vector addresses from 32K to 4M, switches processing levels while using each address, and ensures that no program exceptions occur. It displays a progress indicator value of 3100 and test error message numbers 3151, 3169, and 31B0 to 31EF.

Routine 34, 8130 Storage and ECC Control Test. Runs only on machines with ECC and tests that the storage control card can access all storage locations, correct all single bit failures, and detect all double bit failures. The routine also tests all storage locations using multiple read, write, and access tests. It displays progress indicator values of 3400, 3401, and 3440 through 345F and test error message numbers 3420 through 3423, 3430, 3474, and 34B0 through 34EF.

Routine 35. 8140 Storage and ECC Test. Runs only on Models A6X, A7X, and BXX and completes within 5 to 10 seconds, depending on storage size. The routine first stores several bit patterns to initialize the ECC check bits to all ones, fetches each pattern, and reverses one or two bits. With the ECC function turned off it stores these new patterns in the same storage location and again turns on ECC. The routine then fetches this pattern and expects the ECC to generate a bit correction for a single-bit reversal and a storage check for a double bit error. For unchanged patterns, the routine also ensures that the ECC logic does not either correct them or generate a storage check. The routine displays a progress indicator value of 3500 and test error message numbers of 3574 to 3578 and 35B0 to 35EF.

Routine 36, Processor Storage Test. This routine tests the accessing of each storage card and storage address by verifying the ability to access every byte and halfword storage address and to store various data patterns. It also accesses beyond physical storage limits, which should result in a program exception. The routine displays progress indicator values of 3600, 3602 to 361F, 3640, 3641, 3642, and test error message numbers 3651, 3665, 3666, 3669, 3671, 3672, 36AA, 36CC, and 36B0 to 36EF.

Routine 37, 8140 Processor Storage Data Retention Test. Runs only on Models A3X, A4X, and A5X. The routine completes in approximately 1 minute if run as part of the extended tests, approximately 3 minutes if run from the CSU diskette, and approximately 18 minutes if manually selected. It ensures that processor storage can retain data after not being active for a period of time. The routine stores one-bits in all R/W storage locations, delays without executing a storage access, fetches all data, then compares it to the values previously stored. It then repeats these steps using all zero-bits. Finally, it uses random bit patterns to check the parity bits. The routine displays progress indicator values of 3700 to 3705 and test error message numbers 3765 and 37CC.

Routine 38, Move/Compare Storage Test. This routine completes within 4 to 8 minutes, depending on storage size and checks the proper storage execution of the MVHS and CLHS instructions. Both instructions use several varied data patterns in each read/write storage location and the routine checks these data patterns after each operation to ensure that instruction execution did not alter them. The routine displays progress indicator values of 3800, 3802 through 381F, 3841, and 3842 and test error message numbers 3865, 38CC, and 38B0 through 38EF.

Routine 3A, Basic Operator Panel Test. Tests that the BOP logic rejects all invalid commands. It displays a progress indicator value of 3A00 and test error message numbers 3A38, 3A39, 3A3D, 3A3E, and 3AB0 to 3AEF.

***Routine 3B, Basic Operator Panel Indicator Test.** Tests the BOP indicators under system control for both on and off status. It also tests the BOP display register and the system wait state. It displays progress indicator values of 3B01 to 3B0C, and test error message numbers 3BB0 to 3BEF.

***Routine 3C, Basic Operator Panel IPL Mode Switch Test.** Tests the correct operation of the BOP IPL mode switch and the disable panel function under system control. It displays progress indicator values of 3C00 to 3C02 and test error message numbers 3CBA, 3C3C, and 3CB0 to 3CEF.

***Routine 3D, Basic Operator Panel Keylock Switch Test.** Checks the correct operation of the keylock feature switch under system control. It displays progress indicator values of 3D00 to 3D03 and test error message numbers 3D3B and 3DB0 to 3DEF.

*This routine must be selected and requires manual intervention.

BU230 Test Message Formats

The following describes the test messages formats used when running the BU tests. The BOP displays all actual messages relating to these formats.

Format	Test Message	Meaning
1	00EN	Basic BU test message
1	RREN	Extended BU test message
2	RREN XXXX	Extended BU test message with extended error data

Where:

RR = Routine number

EN = Error number

XXXX = Extended error data available for certain error numbers and displayed by pressing the BOP Enter Function pushbutton.

BU240 Test Message and Error Number Descriptions

The following sections describe all test and test error messages generated when performing the BU tests. It also includes in which routines they appear, the error format type, and the meaning of each. These sections are divided into the common BU test messages (BU241), basic BU test messages (BU242), and extended BU test messages (BU243).

To locate any message number, first refer to section BU241. If the number or format is not contained in this section, then refer to either BU242 or BU243 according to the BU test being performed.

BU241 Bringup Test Common Messages and Error Number Descriptions

This section describes those messages generated when a system check occurs while running either the basic or extended BU tests. The error messages generated are either in the Type 1 or Type 2 formats.

- In the Type 1 format (RREN), RR equals the routine number and EN equals the error number.
- In the Type 2 format (RREN XXYY), the XXYY field provides additional error information that displays when pressing the BOP Enter Function pushbutton.

RREN	Format	Meaning
All errors from RRB0 to RRBF indicate that a system check occurred during a data transfer with the SCF.		
RRB0	1	Either an SCF address byte parity error or a timeout occurred while reading SCF status.
RRB1	1	The processor detected a parity error while executing a command to SCF address hex 08.
RRB2	1	The processor detected a parity error while executing a command to SCF address hex 0C.
RRB3	1	An invalid command was issued to SCF address hex 0C.
RRB4	1	A parity error occurred while executing either a command or a write data operation to SCF address hex 0C.
RRB5	1	An invalid command was issued to SCF address hex 08.
RRB6	1	A parity error occurred while executing either a command or a write data operation to SCF address hex 08.
RRB7	1	The SCF detected a parity error while executing either a command or a read data operation to SCF address hex 08.
RRB8	1	The SCF detected a parity error while executing either a command or a read data operation to SCF address hex 0C.
RRB9	1	An address byte parity error occurred while executing a command to the BOP.
RRBA	1	A command byte parity error occurred while executing a command to the BOP.
RRBB	1	An SDC bus parity error occurred while executing a Read command to the BOP.
RRBC	1	The processor detected a parity error while executing a command to the SCF.
RRBD	1	Either an invalid command or a write parity error occurred during a data transfer to the SSCF.
RRBE	1	The SSCF detected a parity error during a Read command to the SSCF.
RRBF	1	Not defined
RRC0	1	A storage check occurred while executing within processor storage addresses zero to 32K (basic BUs only).
RRC1	1	A storage check occurred while executing within processor storage addresses 32K to 64K (basic BUs only).
RRCC	2	A storage check occurred while executing within processor storage. The first two digits of the extended error field indicate the failing 32K block of storage. Refer to BU111 for storage card locations.

RREN	Format	Meaning
All errors from RRE0 to RREF are caused from various sources whose meanings are described below.		
RRE0	1	A system check was caused from an undetermined source.
RRE1	1	A register parity check was caused from an undetermined source.
RRE2	1	A storage check was caused from an undetermined source.
RRE3	1	An SCF system check was caused from an undetermined source.
RRE4	1	An invalid storage address occurred.
RRE5	1	A principal register parity check occurred.
RRE6	1	An adjunct register parity check occurred.
RRE7	1	A translation table parity check occurred.
RRE8	1	A program exception occurred.
RRE9	1	A ROS parity check occurred.
RREA	1	An I/O timeout occurred on an IPL device.
RREB	1	An I/O read parity check occurred during a PIO operation to the IPL device.
RREC	1	The IPL device accessed beyond the channel pointer limits.
RRED	1	An I/O read parity check occurred during a CHIO operation to the IPL device.
RREE	1	A floating-point system check occurred.
RREF	1	A program exception occurred during a PIO data transfer operation.

BU242 Basic Bringup Test Messages and Descriptions

This section describes, in numerical order, those messages generated when running basic BU tests. These tests messages do not correspond to the RREN format.

Routine	Msg No.	Meaning
01	0000	System reset occurred but KDO instruction did not increment display.
01	0001	Initial KDO instruction functioned correctly, but either the PSV readout stopped system processing or a Jump Forward Unconditional instruction failed.
01	0002	Jump Backward Unconditional instruction failed.
01	0003	Jump Forward Unconditional instruction failed.
01	0004	Either an LRI, TRI, or JC instruction failed.
01	0005	Either an ORI or JC instruction failed.
01	0006	Either an XRI or JC instruction failed.
01	0007	Either an ARI or JC instruction failed.
01	0008	Either an XRI or JC instruction failed.
01	0009	Either an ARI or JC instruction failed.
01	000A	Either an NRI or JC instruction failed.
01	000B	Either an ARI or JC instruction failed.
01	000C	Either an LRI, ARI, or JC instruction failed.
01	000D	Either an LRI, TRI, or JC instruction failed.
01	000E	Either an NRI or JC instruction failed.
02	000F	Either a Read Error Interrupt Request Vector instruction failed or EIRV bit 4 is off.
02	0010	Either a Read I/O Interrupt Request Vector instruction failed or IOIRV bit 0 is off.
02	0011	Either a Read Master Mask instruction failed or the master mask bit is off.
02	0012	Either a Reset or a Read Master Mask instruction failed.
02	0013	Either a Read I/O Interrupt Request Vector instruction failed or IOIRV bit zero is on. EIRV bit 4 should be reset and the System Check indicator should be off.
02	0014	Either a Read Condition Indicators, Write Condition Indicators, or a Read Program Interrupt Request Vector instruction failed.
02	0015	Either a Read Current Levels, Read Primary Register Set Number, or Read Secondary Register Set Number instruction failed, or the common mask was not set to hex 80.
02	0016	Either a Read Channel Mask instruction failed, or the channel mask is invalid.
02	0017	Either an OR, AND, or Read Program Interrupt Request Vector instruction failed.
02	0018	Either a Read Common Mask or Write Common Mask instruction failed.
02	0019	Either a Read or Write Primary or Secondary Register Set instruction failed.
02	001A	Either EIRV bit 5 is on or a ROS parity check occurred.
02	001B	Either EIRV bit 3 is off or the PC instruction failed.
03	001C	The AYR instruction failed.
03	001D	Either an SYR or AYR instruction failed.
03	001E	The SYR instruction failed.
03	001F	Either an AHRI, AHR, CR, CHR, SYR, or AYR instruction failed.
04	0020	Either an XR, XHR, RL, or RLH instruction failed.
04	0021	Either an STHRN or LHR instruction failed.
04	0022	Either an LHRN, LR, or OR instruction failed.
05	0023	The BALR instruction failed.
05	0024	The BCR instruction failed.
06	0025	The LN instruction failed.
06	*0026	The LHN instruction failed.
06	*0027	The LH instruction failed.
06	0028	Either an STN, STHN, or STH instruction failed.

Note: *This is the first execution and testing of a store operation into a read/write storage area.*

06	0029	A register parity failure occurred. (EIRV value hex 24)
06	002A	A processor storage read data error occurred. (EIRV value hex 20)
06	002B	A ROS parity error occurred. (EIRV value hex 04)
06	002C	A program exception occurred. (EIRV value hex 10)
06	002D	A system check occurred for reasons other than what was previously tested.
07	002E	Storage check did not occur when using data with bad parity.
07	002F	Either a ROS data storage check or a checksum error occurred.
07	0030	A register parity error occurred. (EIRV value hex 24)
07	0031	A storage read data parity occurred. (EIRV value hex 20)
07	0032	A ROS parity error occurred. (EIRV value hex 04)
07	0033	A program exception occurred. (EIRV value hex 10)
07	0034	A system check occurred for reasons other than what was previously tested.
08	0035	Processor instruction execution stopped during a readout operation.
08	0036	Processor instruction execution stopped during a readout operation.
09	0037	Either a Read SCF Basic Status instruction failed or SCF basic status bits 13, 14, or 15 are on.

*In 8130s with ROS PN 5864711, these error message numbers can have the same meaning as 0326 and 0327 if the BOP displayed 0200 just before the error occurred.

Routine	Msg No.	Meaning
09	0038	Either an IOI or an IO instruction failed.
09	0039	Either a Read SCF Basic Status Register instruction failed or BSTAT bits 13, 14, or 15 are on.
09	003A	Either a read, write, or reset basic status, or a reset device operation failed.
09	003B	Either a read or write operation to the IPL programmable register failed.
10	003C	A read BOP basic status register operation failed.
10	003D	Either an invalid command occurred or a command parity error was detected. (BOP BSTAT bit 0 on.)
10	003E	A maintenance device signal bus check occurred. (BOP BSTAT bit 1 on.)
10	003F	An SCF signal bus check occurred. (BOP BSTAT bit 2 on.)
10	0040	A BOP adapter check occurred. (BOP BSTAT bit 3 on.)
10	0041	Either a MD transfer complete, device check, or interrupt enable condition occurred or the IPL indicator is off. (BOP BSTAT bits 10, 12, 13, or 14 on.)
10	0042	Either a read control byte operation failed or the control byte is invalid.
10	0043	A read BOP display character operation failed.
10	0044	Either a read or set BOP BSTAT operation failed.
10	0045	Either an invalid command occurred or a command parity error was detected. (BOP BSTAT bit 0 on.)
10	0046	An MD signal bus check occurred. (BOP BSTAT bit 1 on.)
10	0047	An SCF signal bus check occurred. (BOP BSTAT bit 2 on.)
10	0048	A BOP adapter check occurred. (BOP BSTAT bit 3 on.)
10	0049	Either an MD transfer complete, device check, or interrupt enable operation failed or the IPL indicator is off. (BOP BSTAT bits 10, 12, 13 or 14 on.)
11	004A	Either a read or write BOP control register operation failed or the control register is invalid.
11	004B	A write BOP display character operation failed.
12	0100	The routine is performing a switch from processing level 0 to 1.
12	0101	The routine is performing a switch to processing level 0.
13	0102	The routine is performing a test of the IPL parameters and SCF status to determine the IPL path.
12	0120	Incorrect address stored in a PSV on a PSV switch operation.
12	0121	The processor failed to switch from processing level 0 or 1 as expected.
13	0122	An automatic IPL should have occurred because power was restored after a utility outage, but was not permitted by the IPL parameter switches.
13	0123	Valid test and initialize parameters were not specified on a primary or programmed IPL operation.
13	013C	A condition indicator error occurred on an I/O to BOP operation.
13	014C	A condition indicator error occurred on an I/O to SCF operation.
13	01BX 01CX 01EX	With an X value of 0—F, a system check occurred. Refer to the common error messages in BU241 for further explanation.
14	0200	Basic BU tests ran successfully. The routine expects an input specifying the IPL parameters. After entering the 4-character IPL parameter, either press Enter Function to continue IPL, or press Enter Data if you want to enter the IPL options. Refer to the Chapter 2, CP500, for IPL parameter bit values and description.
14	0201	The routine expects a four-character input specifying an IPL option. Press Enter Function to resume IPL. Refer to sections BU204 and BU205 for valid IPL options.
15	0202	Enter any four characters in the BOP data/function push-buttons and press Enter Data.
15	0203	Press Enter Data to display the four characters entered at prompt message 0202.
14	0223	Valid test and initialize parameters were not specified during a manual IPL operation.
14, 15	023C	A condition indicator error occurred on an I/O operation to the BOP.
14, 15	024C	A condition indicator error occurred on an I/O operation to the SCF.
14	0281	The first two characters of the IPL option selection are invalid.
14	0282	The second two characters of the IPL option selection are invalid.
15	02BX 02CX 02EX	With an X value of 0—F, a system check occurred. Refer to the common error messages in BU241 for further explanation.
16	0300	The routine is performing a register test.
17	0301	The routine is performing a test of processor storage from 0 to 64K.
18	0302	The routine is performing register initialization.
18	0303	The routine is performing translation table initialization.
18	0304	The routine is performing processor storage initialization. Normal operation of this routine turns the System Check indicator on.
18	0321	The processor failed to switch from processing level 0 to 1.
17	0323	A failure occurred within processor storage addresses zero to 32K.
17	0324	A failure occurred within processor storage addresses 32K to 64K.
16	0325	A register compare error occurred.

Routine	Msg No.	Meaning
16	*0326	A storage failure occurred within 0 to 64K.
16	*0327	A storage refresh failure occurred within 0 to 64K.
18	034C	A condition indicator error occurred on an I/O to PSCF operation.
16, 17	03BX 03CX 03EX	With an X value of 0–F, a system check occurred. Refer to the common error messages in BU241 for further explanation.
19	0400	The routine is performing an IPL SSCF configuration.
20	0402	The routine is performing a write to the SCF interrupt register.
20	0403	The routine is performing a read to the SCF interrupt register.
20	0404	The routine is performing a control transfer to the IPL loader routine.
19	0426	The routine could not configure the IPL SSCF.
20	0430	The SCF register data read did not equal the data written.
19	043C	A condition value error occurred on an I/O to BOP operation.
20	0441	The first two characters of the IPL parameter specified an invalid device.
19	044C	A condition indicator error occurred on an I/O to SSCF operation.
19	0450	Disk storage power on delay (approximately 15 seconds).
19,20	04BX 04CX 04EX	With an X value of 0–F, a system check occurred. Refer to the common error messages in BU241 for further explanation.
23	0600	The routine is attempting to load from the diskette.
23	0632	The diskette drive is not ready. (Ensure door is closed.)
23	0633	The diskette drive did not become ready within 20 seconds. (Re-IPL the test.)
23	0634	A diskette error occurred during a seek operation.
23	0635	A diskette error occurred during a read operation.
23	06BX 06CX 06EX	With an X value of 0–F, a system check occurred while loading from the diskette. Refer to the common error messages in BU241 for further explanation.
24	0700	The routine is attempting to load from disk storage.
24	0734	A disk storage error occurred during IPL.
24	07BX 07CX 07EX	With an X value of 0–F, a system check occurred while loading from disk storage. Refer to the common error messages in BU241 for further explanation.
26	0E00	The routine is preparing to transfer control to the loaded program.
26	0E21	The processor failed to switch to processing level 0.
26	0E3C	A condition indicator error occurred during an I/O operation.
26	0EEX	With an X value of 0–F, a system check occurred. Refer to the common error messages in BU241 for further explanation.
26	0EFF	The processor is transferring control to the loaded program.
25	0F00	Performing a test of the MD data register.
25	0F01	The MD is not enabled.
25	0F02	Performing a load from the MD without an initial free condition.
25	0F03	Performing a load from the MD after an initial free condition on entry.
25	0F04	Performing a load from the MD after receiving a 'Status In' condition.
25	0F38	An MD data register error occurred.
25	0F39	A BOP adapter status error occurred.
23	0F3C	A condition indicator error occurred on an I/O to BOP operation.
25	0FEX	With an X value of 0–F, a system check occurred. Refer to the common error messages in BU241 for further explanation.
25	1000	Disk storage loader has received control from ROS.
25	1001	Disk storage loader is transferring control to the extended tests.
25	1002	Disk storage I/O error occurred after ROS has transferred control to the disk storage loader.
25	10CX	With an X value from 0 to F, a storage check occurred while executing in processor storage. Refer to BU241 for further explanation.
25	10EX	With an X value of from 0 to F, a system check occurred. Refer to BU241 for further explanation.
25	10FF	Disk storage loader has transferred control to the system loader.

*8130's only.

BU243 Extended Bringup Test Messages and Descriptions

This section describes those messages generated when running extended BU tests. These error messages are either in the type 1, 2, or 3 formats, where RR equals the routine number and EN equals the error number. Type-2 format messages provide additional error information by using 4-character field (XXXX) that displays when pressing the BOP Enter Function pushbutton; type-3 formats provide another 4-character field (YYYY) that displays when pressing the Enter Function pushbutton a second time.

Refer to BU230 for a description of the common test messages and formats.

RREN	Format	Meaning
1100	1	Extended tests have received control from loader.
1137	2	A disk storage error occurred. The error extension data contains disk storage basic status.
1139	2	A BOP basic status error occurred. The error extension data contains the BOP basic status.
1200	1	Routine 12 entered.
1201	1	And (byte, register) instruction failed. (NR)
1202	1	Add (byte, register) instruction failed. (AR)
1203	1	Subtract (byte, register) instruction failed. (SR)
1204	1	AND (halfword, register) instruction failed. (SR)
1205	1	OR (halfword, register) instruction failed. (OHR)
1206	1	Add with Carry (halfword, register) instruction failed. (AYHR)
1207	1	Subtract (halfword, register) instruction failed. (SHR)
1208	1	Subtract with Carry (halfword, register) instruction failed. (SYHR)
1209	1	Subtract (halfword, register-immediate) instruction failed. (SHRI)
1300	1	Routine 13 entered.
1301	1	Compare with Carry (halfword, register-extended) instruction failed. (CYHRE)
1302	1	Add with Carry (halfword, register-extended) instruction failed. (AYHRE)
1303	1	Subtract with Carry (halfword, register-extended) instruction failed. (SYHRE)
1304	1	Load (halfword, register, upper half from lower) instruction failed. (LHRUL)
1305	1	Load (halfword, register, lower half from upper instruction failed. (LHRLU)
1306	1	Load (halfword, register, upper half) instruction failed. (LHRU)
1400	1	Routine 14 entered.
1401	1	Shift Left (byte, logical) instruction failed. (SLL)
1402	1	Shift Left (halfword, logical) instruction failed. (SLHL)
1403	1	Store (byte, with index incremented) instruction failed. (STNI)
1404	1	Load (halfword, with index incremented) instruction failed. (LHNI)
1405	1	Store (halfword, with index incremented) instruction failed. (STHNI)
1406	1	Load (byte, with index incremented) instruction failed. (LNI)
1407	1	Store (byte, with index decremented) instruction failed. (STND)
1408	1	Load (halfword, with index decremented) instruction failed. (LHND)
1409	1	Store (halfword, with index decremented) instruction failed. (STHND)
140A	1	Load (byte, with index decremented) instruction failed. (LND)
1500	1	Routine entered.
1501	1	Store (byte, register-indirect) instruction failed. (STRN)
1502	1	Load (byte, register-indirect) instruction failed. (LRN)
1503	1	Load (byte) instruction failed. (L)
1504	1	Store (byte) instruction failed. (ST)
1505	1	Load (word) instruction failed. (LW)
1506	1	Store (word) instruction failed. (STW)
1507	1	Load Address instruction failed. (LA)
1508	1	Store (halfwords, quadrant) instruction failed. (STHQ)
1509	1	Load (halfwords, quadrant) instruction failed. (LHQ)
150A	1	Store (halfwords, short form) instruction failed. (STHS)
150B	1	Load (halfwords, short form) instruction failed. (LHS)
1600	1	Routine 16 entered.
1601	1	Dispatch New Level instruction failed. (KI 28)
1602	1	Reset Channel Mask instruction failed. (KI 24)
1603	1	OR Current PIRV Level instruction failed. (KI 35)
1604	1	AND Current PIRV Level instruction failed. (KI 37)
1605	1	Set Channel Mask instruction failed. (KI 38)
1606	1	Swap PSV instruction failed. (KI 127)
1607	1	Jump on Bit Zero (halfword) instruction failed. (JBZ)
1608	1	Jump on Condition instruction failed. (JCX)
1609	1	Branch on Condition instruction failed. (BC)
160A	1	Jump and Link instruction failed. (JAL)
160B	1	Branch and Link instruction failed. (BAL)
160C	1	Test and Set (byte) instruction failed. (TS)
160D	1	Branch on Count (byte, register) instruction failed. (BCTR)

RREN	Format	Meaning
160E	1	Count Leading Zeros (halfword) instruction failed. (CTLZ)
160F	1	Branch on Index (byte) instruction failed. (BNX)
1700	1	Routine 17 entered.
1701	1	Multiply (halfword, register) instruction failed. (MHR)
1702	1	Divide (halfword, register) instruction failed. (DHR)
1703	1	Move (bytes, storage) instruction failed. (MVS)
1704	1	Move (halfwords, storage) instruction failed. (MVHS)
1705	1	Compare Logical (bytes, storage) instruction failed. (CLS)
1706	1	Compare Logical (halfwords, storage) instruction failed. (CLHS)
1800	1	Routine 18 entered.
1801	1	Either the Z, H, C, or V fields (condition indicators), primary register set number, or secondary register set number do not equal the expected value.
1802	1	Current level does not equal the expected value.
1803	1	Program mode does not equal the expected value.
1804	1	PIRV does not equal expected value.
1805	1	Common mask does not equal expected value.
1806	1	Last level does not equal expected value.
1807	1	Last level I field (instruction address range) does not equal expected value.
1808	1	Either the last level Z, H, C, or V fields (condition indicators), the primary register set number, or the secondary register set number did not equal the expected value.
1809	1	The error interrupt request vector does not equal the expected value when processing switched to level zero.
180A	1	The program information code (PIC) does not equal the expected value.
1900	1	Routine 19 entered.
1901	1	An invalid instruction did not cause a program exception. This error occurs only on 8140 Models with floating-point when the extended tests are not configured for floating-point.
1902	1	A privileged instruction in application mode did not cause a program exception.
1903	1	A privileged instruction in I/O mode did not cause a program exception.
*1A00	1	Routine 1A entered.
*1A10	1	Floating-point (FP) register reset to zero operation failed.
*1A11	1	A read or write FP status operation failed.
*1A12	1	A read or write FP control operation failed.
*1B00	1	Routine 1B entered.
*1B13	1	An FP set overflow mask operation failed.
*1B14	1	An FP set precision mode operation failed.
*1B15	1	An FP set significance mask operation failed.
*1B16	1	An FP set underflow mask operation failed.
*1C00	1	Routine 1C entered.
*1C17	1	A Load, Store, or Compare FP instruction failed. (LF, STF, or CF using register-to-storage format.)
*1C18	1	A Load (register) or compare (register) FP instruction failed. (LFR or CFR using register-to-register format.)
*1D00	1	Routine 1D entered.
*1D19	1	A Load and Test (register) FP instruction failed. (LTFR)
*1D1A	1	A Load Complement (register) FP instruction failed. (LCFR)
*1D1C	1	A Load Positive (register) FP instruction failed. (LPFR)
*1D1D	1	A Load Rounded (register) FP instruction failed. (LRFR)
*1E00	1	Routine 1E entered.
*1E20	1	An Add Unnormalized (register) FP instruction with long precision failed. (AUR using register-to-register format.)
*1E21	1	An Add Unnormalized FP instruction with long precision failed. (AU using register-to-storage format.)
*1E22	1	An Add Normalized (register) FP instruction with long precision failed. (AFR using register-to-register format.)
*1E23	1	An Add Normalized FP instruction with long precision failed. (AF using register-to-storage format.)
*1E24	1	An Add Unnormalized (register) FP instruction with short precision failed. (AUR using register-to-register format.)
*1E25	1	An Add Unnormalized FP instruction with long precision failed. (AU using register-to-storage format.)
*1E26	1	An Add Normalized (register) FP instruction with short precision failed. (AFR using register-to-register format.)
*1E27	1	An Add Normalized FP instruction with short precision failed. (AF using register-to-storage format.)
*1F00	1	Routine 1F entered.
*1F20	1	A Subtract Unnormalized (register) FP instruction with long precision failed. (SUR using register-to-storage format.)
*1F21	1	A Subtract Unnormalized FP instruction with long precision failed. (SU using register-to-storage format.)
*1F22	1	A Subtract Normalized (register) FP instruction with long precision failed. (SFR using register-to-register format.)
*1F23	1	A Subtract Normalized FP instruction with long precision failed. (SF using register-to-storage format.)
*1F24	1	A Subtract Unnormalized (register) FP instruction with short precision failed. (SUR using register-to-register format.)
*1F25	1	A Subtract Unnormalized FP instruction with short precision failed. (SU using register-to-storage format.)

*Occurs only on 8140s with floating-point.

RREN	Format	Meaning
*1F26	1	A Subtract Normalized (register) FP instruction with short precision failed. (SFR using register-to-register format.)
*1F27	1	A Subtract Normalized FP instruction with short precision failed. (SF using register-to-storage format.)
*2000	1	Routine 20 entered.
*2028	1	A Multiply (register) FP instruction with long precision failed. (MFR using register-to-register format.)
*2029	1	A Multiply FP instruction with long precision failed. (MF using register-to-storage format.)
*202A	1	A Multiply (register) FP instruction with short precision failed. (MFR using register-to-register format.)
*202B	1	A Multiply FP instruction with long precision failed. (MF using register-to-storage format.)
*2100	1	Routine 21 entered.
*2128	1	A Divide (register) FP instruction with long precision failed. (DFR using register-to-register format.)
*2129	1	A Divide FP instruction with long precision failed. (DF using register-to-storage format.)
*212A	1	A Divide (register) FP instruction with short precision failed. (DFR using register-to-register format.)
*212B	1	A Divide FP instruction with short precision failed. (DF using register-to-storage format.)
*2200	1	Routine 22 entered.
*2210	1	An FP operation exception failed.
*2211	1	An FP privileged operation exception failed.
*2212	1	An FP specification exception failed.
*2220	1	An FP significance exception failed.
*2221	1	An FP exponent underflow exception failed.
*2222	1	An FP exponent overflow exception failed.
*2223	1	An FP divide exception failed.
2400	1	Routine 24 entered.
2451	1	An invalid upper halfword register access operation did not cause a program exception.
2464	2	The PIC was set incorrectly. The error extension value equals PIC received/PIC expected.
2465	2	An upper halfword register data compare operation failed. The error extension equals the address of the failing register.
2466	2	The value of an address read operation to an upper halfword register did not compare to the address stored. The error extension equals the address of the failing register.
2469	1	The processor failed to switch processing levels correctly.
2500	1	Routine 25 entered.
2551	1	An invalid adjunct register access operation did not cause a program exception.
2564	2	The PIC was set incorrectly. The error extension value equals PIC received/PIC expected.
2565	2	An adjunct register data compare operation failed. The error extension equals the address of the failing register.
2566	2	The value of an address read operation to an adjunct register did not compare to the address stored. The error extension equals the address of the failing register.
2569	1	The processor failed to switch processing levels correctly.
2600	1	Routine 26 entered.
2657	1	No program exception occurred when the PSV instruction address bits 9–11 were not zero.
2664	2	The PIC was set incorrectly. The error extension value equals PIC received/PIC expected.
2667	1	No program exception occurred when the PSV instruction address bits 0–7 were not zero.
2669	1	The processor failed to switch processing levels correctly.
2700	1	Routine 27 entered.
2751	2	A program exception occurred using a valid adjunct register value. The error extension value equals the failing adjunct register contents.
2752	1	A store operation executed beyond the address limit specified by an adjunct register.
2764	2	The PIC was set incorrectly. The error extension value equals PIC received/PIC expected.
2767	1	A program exception did not occur with an invalid adjunct register value.
2769	1	The processor failed to switch processing levels correctly.
2800	1	Routine 28 entered.
2851	1	A program exception did not occur during a store operation when using an invalid value in the upper halfword register.
2864	2	The PIC was set incorrectly. The error extension value equals PIC received/PIC expected.
2869	1	The processor failed to switch processing levels correctly.
2900	1	Routine 29 entered.
2951	1	A program exception did not occur when storing to quadrant 3.
2964	2	The PIC was set incorrectly. The error extension value equals PIC received/PIC expected.
2969	1	The processor failed to switch processing levels correctly.
**2A00	1	Routine 2A entered.
**2A51	1	Principal register data failure.
**2A52	1	Adjunct register data failure.
**2A53	1	Translate table data failure.

*Occurs only on 8140s with floating-point.

**Only occurs on 8130s.

RREN	Format	Meaning
2B00	1	Routine 2B entered.
2B51	1	A program exception did not occur when crossing a 64K boundary with a PSV S-field value of zero.
2B52	1	A program exception did not occur when crossing a 64K boundary with a PSV I-field value of zero.
2B64	2	The PIC was set incorrectly. The error extension value equals PIC received/PIC expected.
2B65	1	A data compare error occurred between a processor storage address contained within 64K to 128K addresses and the one supplied by the translation table.
2B69	1	The processor failed to switch processing levels correctly.
2F00	1	Routine 2F entered.
2F51	1	A program exception did not occur with an invalid W1 field in the STAT instruction.
2F52	1	The translation table address incremented when using invalid data.
2F53	1	A program exception did not occur when using an invalid access control value in a STAT instruction.
2F54	1	A program exception did not occur when using an invalid block index value.
2F55	1	A program exception did not occur when using an invalid translation table address in the STAT instruction.
2F56	1	A program exception did not occur when using an invalid translation table address in a LAT instruction.
2F57	1	A program exception occurred when using a valid access control value.
2F58	1	A program exception did not occur when the access control value was set to not permit access.
2F64	2	The PIC was set incorrectly. The error extension data equals the value received/value expected.
2F65	2	A data compare error occurred while performing a STAT or LAT instruction. The error extension equals the address of the data compare error.
2F69	1	The processor failed to switch processing levels correctly.
3100	1	Routine 31 entered.
3151	2	A program exception occurred when using a valid adjunct register value. The error extension equals the contents of the adjunct register in error.
3169	1	The processor failed to switch processing levels correctly.
*3400	1	Routine 34 entered.
*3401	1	Address testing begun.
*3420	1	A data compare error occurred within 0 to 256K.
*3421	1	A data compare error occurred within 256K to 512K.
*3422	1	A data compare error occurred within 512K to 768K.
*3423	1	A data compare error occurred within 768K to 1024K.
*3430	1	A data compare error occurred within 0 to 8K.
*3440	1	Testing storage address locations 0 to 32K.
*3441	1	Testing storage address locations 32K to 64K.
*3442	1	Testing storage address locations 64K to 96K.
*3443	1	Testing storage address locations 96K to 128K.
*3444	1	Testing storage address locations 128K to 160K.
*3445	1	Testing storage address locations 160K to 192K.
*3446	1	Testing storage address locations 192K to 224K.
*3447	1	Testing storage address locations 224K to 256K.
*3448	1	Testing storage address locations 256K to 288K.
*3449	1	Testing storage address locations 288K to 320K.
*344A	1	Testing storage address locations 320K to 352K.
*344B	1	Testing storage address locations 352K to 384K.
*344C	1	Testing storage address locations 384K to 416K.
*344D	1	Testing storage address locations 416K to 448K.
*344E	1	Testing storage address locations 448K to 480K.
*344F	1	Testing storage address locations 480K to 512K.
*3450	1	Testing storage address locations 512K to 544K.
*3451	1	Testing storage address locations 544K to 576K.
*3452	1	Testing storage address locations 576K to 608K.
*3453	1	Testing storage address locations 608K to 640K.
*3454	1	Testing storage address locations 640K to 672K.
*3455	1	Testing storage address locations 672K to 704K.
*3456	1	Testing storage address locations 704K to 736K.
*3457	1	Testing storage address locations 736K to 768K.
*3458	1	Testing storage address locations 768K to 800K.
*3459	1	Testing storage address locations 800K to 832K.
*345A	1	Testing storage address locations 832K to 864K.
*345B	1	Testing storage address locations 864K to 896K.
*345C	1	Testing storage address locations 896K to 928K.
*345D	1	Testing storage address locations 928K to 960K.
*345E	1	Testing storage address locations 960K to 992K.
*345F	1	Testing storage address locations 992K to 1024K.
*3474	1	A storage correction failure occurred.
*34CC	2	A storage check occurred during storage access. The first two digits of the error extension field indicate the failing storage card. (See BU111 for storage card locations.)

*Occurs only on 8130s.

*Occurs only on 8130s.

RREN	Format	Meaning
**3500	1	Routine 35 entered.
**3569	1	The processor failed to switch processing levels correctly.
**3574	2	ECC corrected data which should not have been corrected.
**3575	2	A storage check occurred when fetching a correct data pattern.
**3576	2	A storage check occurred when fetching a data pattern containing a single bit error.
**3577	2	A single bit error was improperly corrected.
**3578	2	A double bit error did not cause an expected storage check.
3600	1	Routine 36 (Storage Test) entered. This routine completes within 12 to 65 seconds on an 8140 and within 2 to 5 minutes on an 8130, depending on processor storage size.
3602	1	Testing storage address locations 64K to 96K.
3603	1	Testing storage address locations 96K to 128K.
3604	1	Testing storage address locations 128K to 160K.
3605	1	Testing storage address locations 160K to 192K.
3606	1	Testing storage address locations 192K to 224K.
3607	1	Testing storage address locations 224K to 256K.
3608	1	Testing storage address locations 256K to 288K.
3609	1	Testing storage address locations 288K to 320K.
360A	1	Testing storage address locations 320K to 352K.
360B	1	Testing storage address locations 352K to 384K.
360C	1	Testing storage address locations 384K to 416K.
360D	1	Testing storage address locations 416K to 448K.
360E	1	Testing storage address locations 448K to 480K.
360F	1	Testing storage address locations 480K to 512K.
3610	1	Testing storage address locations 512K to 544K.
3611	1	Testing storage address locations 544K to 576K.
3612	1	Testing storage address locations 576K to 608K.
3613	1	Testing storage address locations 608K to 640K.
3614	1	Testing storage address locations 640K to 672K.
3615	1	Testing storage address locations 672K to 704K.
3616	1	Testing storage address locations 704K to 736K.
3617	1	Testing storage address locations 736K to 768K.
3618	1	Testing storage address locations 768K to 800K.
3619	1	Testing storage address locations 800K to 832K.
361A	1	Testing storage address locations 832K to 864K.
361B	1	Testing storage address locations 864K to 896K.
361C	1	Testing storage address locations 896K to 928K.
361D	1	Testing storage address locations 928K to 960K.
361E	1	Testing storage address locations 960K to 992K.
361F	1	Testing storage address locations 992K to 1024K.

**Occurs only on 8140 models A6X, A7X, and BXX.

RREN	Format	Meaning
3640	1	Testing storage addressing.
3641	1	Testing storage address locations 4K to 32K.
3642	1	Testing storage address locations 32K to 64K.
3651	1	Program exception did not occur when accessing an invalid storage address.
3665	2	A processor storage data compare error occurred. The first two digits of the error extension field indicate the 32K storage block in which the error occurred.*
3666	2	A processor storage address compare error occurred. The error extension equals the address of the 32K block in error /address of the 32K block received.*
3669	1	The processor failed to switch processing levels correctly.
3671	1	The EIRV value was incorrect after an access was attempted beyond processor storage physical limits.
3672	1	An instruction in storage above 64K failed to execute properly.
36AA	2	A program exception occurred during processor storage access. The first two digits of the error extension field indicate the failing 32K storage block.*
36CC	2	A storage check occurred during processor storage access. The first two digits of the error extension field indicate the failing 32K storage block.*
3700	1	Routine 37 (Storage Data Retention) entered. Testing all storage address above 64K with all one-bits. This display remains active for approximately 3 minutes (8140) to 6 minutes (8130) if the test was manually selected, or about 10 seconds if run as part of the extended tests.
3701	1	Testing all storage addresses above 64K with all zero-bits. This display remains active for approximately 3 minutes (8140) to 6 minutes (8130) if the test was manually selected, or about 10 seconds if run as part of the extended tests.
3702	1	Testing all storage addresses above 64K with random bit patterns to check zero parity retention. This display remains active for approximately 3 minutes (8140) to 6 minutes (8130) if the test was manually selected, or about 10 seconds if run as part of the extended tests.
3703	1	Testing all storage addresses between 4K and 64K with one-bits. This display remains active for approximately 3 minutes (8140) to 6 minutes (8130) if the test was manually selected, or about 10 seconds if run as part of the extended tests.
3704	1	Testing all storage addresses between 4K and 64K with all zero bits. This display remains active for approximately 3 minutes (8140) to 6 minutes (8130) if the test was manually selected or about 10 seconds if run as part of the extended tests.
3705	1	Testing all storage addresses between 4K and 64K with random bit patterns to check zero parity retention. This display remains active for approximately 3 minutes (8140) to 6 minutes (8130) if the test was manually selected, or about 10 seconds if run as part of the extended tests.
3765	2	A processor storage data compare error occurred. The first two digits of the error extension field indicate the 32K storage block in which the error occurred.*
37CC	2	A storage check occurred during processor storage access. The first two digits of the error extension field indicate the failing 32K storage block.*

*Refer to BU111 for storage card locations.

RREN	Format	Meaning
3800	1	Routine 38 entered. This routine completes within 4 to 8 minutes. Depending on storage size.
3802	1	Testing storage address locations 64K to 96K.
3803	1	Testing storage address locations 96K to 128K.
3804	1	Testing storage address locations 128K to 160K.
3805	1	Testing storage address locations 160K to 192K.
3806	1	Testing storage address locations 192K to 224K.
3807	1	Testing storage address locations 224K to 256K.
3808	1	Testing storage address locations 256K to 288K.
3809	1	Testing storage address locations 288K to 320K.
380A	1	Testing storage address locations 320K to 352K.
380B	1	Testing storage address locations 352K to 384K.
380C	1	Testing storage address locations 384K to 416K.
380D	1	Testing storage address locations 416K to 448K.
380E	1	Testing storage address locations 448K to 480K.
380F	1	Testing storage address locations 480K to 512K.
3810	1	Testing storage address locations 512K to 544K.
3811	1	Testing storage address locations 544K to 576K.
3812	1	Testing storage address locations 576K to 608K.
3813	1	Testing storage address locations 608K to 640K.
3814	1	Testing storage address locations 640K to 672K.
3815	1	Testing storage address locations 672K to 704K.
3816	1	Testing storage address locations 704K to 736K.
3817	1	Testing storage address locations 736K to 768K.
3818	1	Testing storage address locations 768K to 800K.
3819	1	Testing storage address locations 800K to 832K.
381A	1	Testing storage address locations 832K to 864K.
381B	1	Testing storage address locations 864K to 896K.
381C	1	Testing storage address locations 896K to 928K.
381D	1	Testing storage address locations 928K to 960K.
381E	1	Testing storage address locations 960K to 992K.
381F	1	Testing storage address locations 992K to 1024K.
3841	1	Testing storage address locations 4K to 32K.
3842	1	Testing storage address locations 32K to 64K.
3865	3	A processor storage data compare error occurred. The first two digits of the first error extension field indicate the 32K storage block in which the error occurred.* The second error extension field contains the failing array address within the 32K block.
38CC	3	A storage check occurred during processor storage access. The first two digits of the first error extension field indicate the 32K storage block in which the error occurred.* The second error extension field contains the failing array address within the 32K block.

*Refer to BU111 for storage card locations.

RREN	Format	Meaning
3A00	1	Routine 3A entered.
3A38	2	BOP basic status register Bit 0 (invalid command/command parity) did not turn on. The error extension data contains the BOP basic status register value.
3A39	2	A BOP basic status error occurred. The error extension data contains the BOP basic status register value.
3A3D	2	A BOP invalid command was accepted. The error extension data contains the invalid command issued.
3A3E	2	An incorrect address was stored on an invalid command to the BOP. The error extension data contains the address stored.
3F00	1	Extended BU tests ran successfully.
3F01	1	Offline TCM program load started.
3F02	1	Offline TCM program load now occurring.
3F03	1	Offline TCM program load retry operation.
3F39	2	A BOP basic status error occurred. The error extension data contains the BOP basic status register value.
3FFF	1	Offline TCM program loaded.

BU249 How to Interpret the Processor Test Pushbutton Display Values

The Processor Test pushbutton, when pressed, indicates if a parity error occurred within any of four processor cards. Each of these cards has an error latch that remains set until a system reset occurs. You can determine the latch status at any time by observing the BOP hex display value while pressing the processor test pushbutton. The following lists the display parity error values and the card that most likely caused the failure.

Display	8130	8140 AXX Model	8140 BXX Model	Card Function
XXX1	L2	G2	K2	Principal Register Storage
XXX2	Q2	C2	F2	Pico ROS
XXX4	H2	J2	M2	Adjunct Register Storage
XXX8	J2	L2	P2	Storage Addressing

Any combination of the above hex values indicates multiple card failures.

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BU250 Possible Causes of BOP Failure—Action Plans

The following sections describe how to perform certain checks and procedures relating to possible BOP failure causes. You were referred here by the BU MAP to perform these procedures; after any repair action, you should run verification tests to ensure proper system operation. The following table summarizes the action plans by section:

BOP Checkout Procedure	Section
Keypad	**BU251**
Indicator	**BU252**
Hexadecimal Display	**BU253**
Cable Interlock	**BU254**
IPL Mode Switch	**BU255**
Keylock Switch	**BU256**
MD Signal Bus	**BU257**

As these action plans refer to the BOP and adapter card, this section includes Figure BU250-1 to explain the BOP adapter card pin numbering scheme. Notice that the pins do not always correspond by number. This is because the cables and BOP adapter card do not plug directly into each other, but instead use connector blocks.

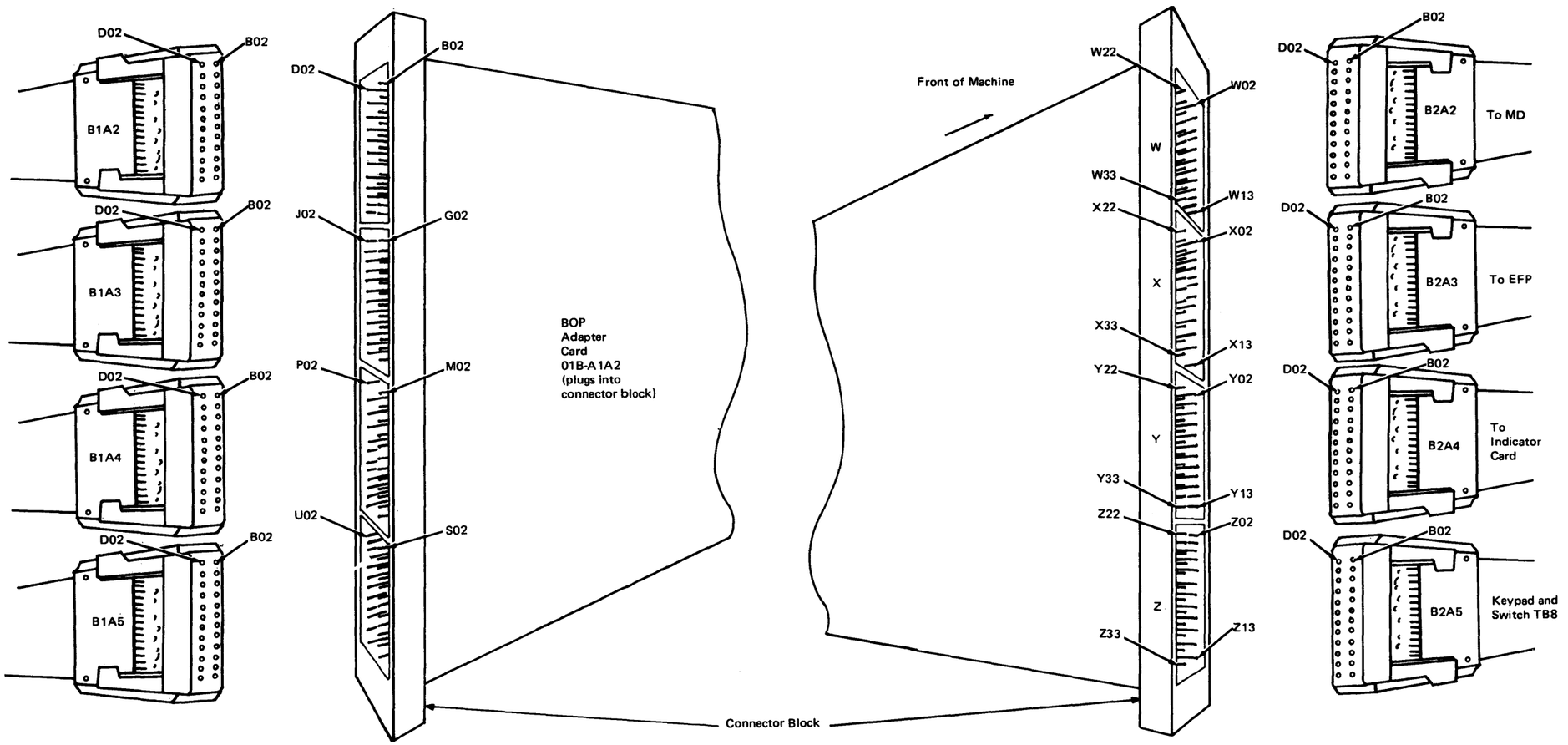


Figure BU250-1. BOP Adapter Card and Cable Pin Numbering

BU251 BOP Data/Function Pushbutton Checkout Procedure

Use this action plan if the BU MAP directs you here because it determined that the failing component is either the Data/Function pushbutton keypad, BOP adapter card, or associated wiring. Perform the actions in the following table to determine the cause of failure.

Caution: Turn power off when removing or exchanging cards or cables.

Cause	Action	Comments
Loose or damaged cable or connector.	Visually check cable and connectors for damaged pins or wiring, and ensure that the connectors are seated securely at the keypad (P1) and BOP adapter card (01B—B2A5).	Refer to Notes 1, 2, and 4 in BU260.
Defective Data/ Function push-button keypad or cable wiring	1. Disconnect cable 01B—B2A5 from the BOP adapter card (see Figure BU251-1). 2. Connect an ohmmeter to the B2A5 pins according to the failing Data/Function pushbutton using the table in Figure BU251-2. 3. The circuit for each pushbutton should show continuity when pressing the pushbutton, and open when releasing it.	Refer to Notes 1, 2, and 4 in BU260. If the keypad circuit does not show continuity, use Figure BU251-3 to determine if the cable or the keypad caused the failure. Repair or replace as necessary.
Defective BOP adapter card	Exchange BOP adapter card (01B—A1A2).	Refer to Notes 2, 3, and 4 in BU260.
Defective SC1 card	Exchange card. 8130 = 01A—A2G2 8140 (Models AXX) = 01A—A1A2 8140 (Models BXX) = 01A—A1D2 Before exchanging, set the switches on the new card to the same positions as the original card.	Refer to Note 5 in BU260.

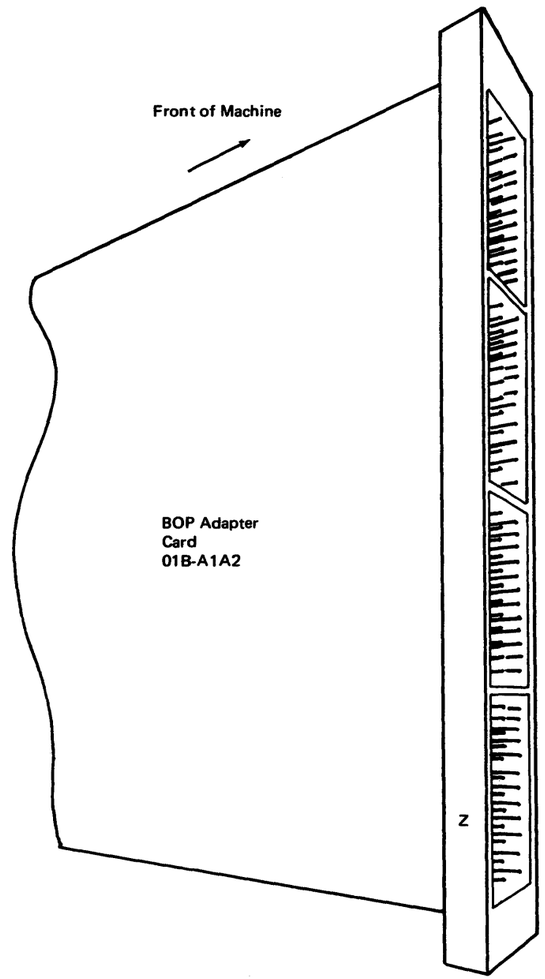
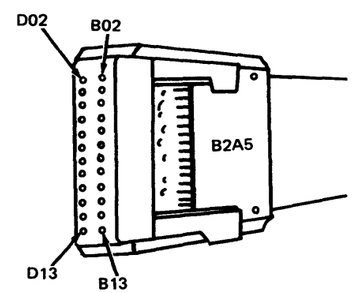


Figure BU251-1. BOP Adapter Card and Keypad Cable

Pushbutton	A5 Cable Pin	
Clear Display	D10	B02
Enter Data	D10	B06
Enter Function	D10	B09
Reset/IPL	D10	B10
0	D02	B02
1	D02	B04
2	D02	B06
3	D02	B09
4	D04	B02
5	D04	B04
6	D04	B06
7	D04	B09
8	D06	B02
9	D06	B04
A	D06	B06
B	D06	B09
Processor Test	D06	B10
C	D09	B02
D	D09	B04
E	D09	B06
F	D09	B09
Lamp Test	D09	B10

Figure BU251-2. BOP Keypad Continuity Check Table



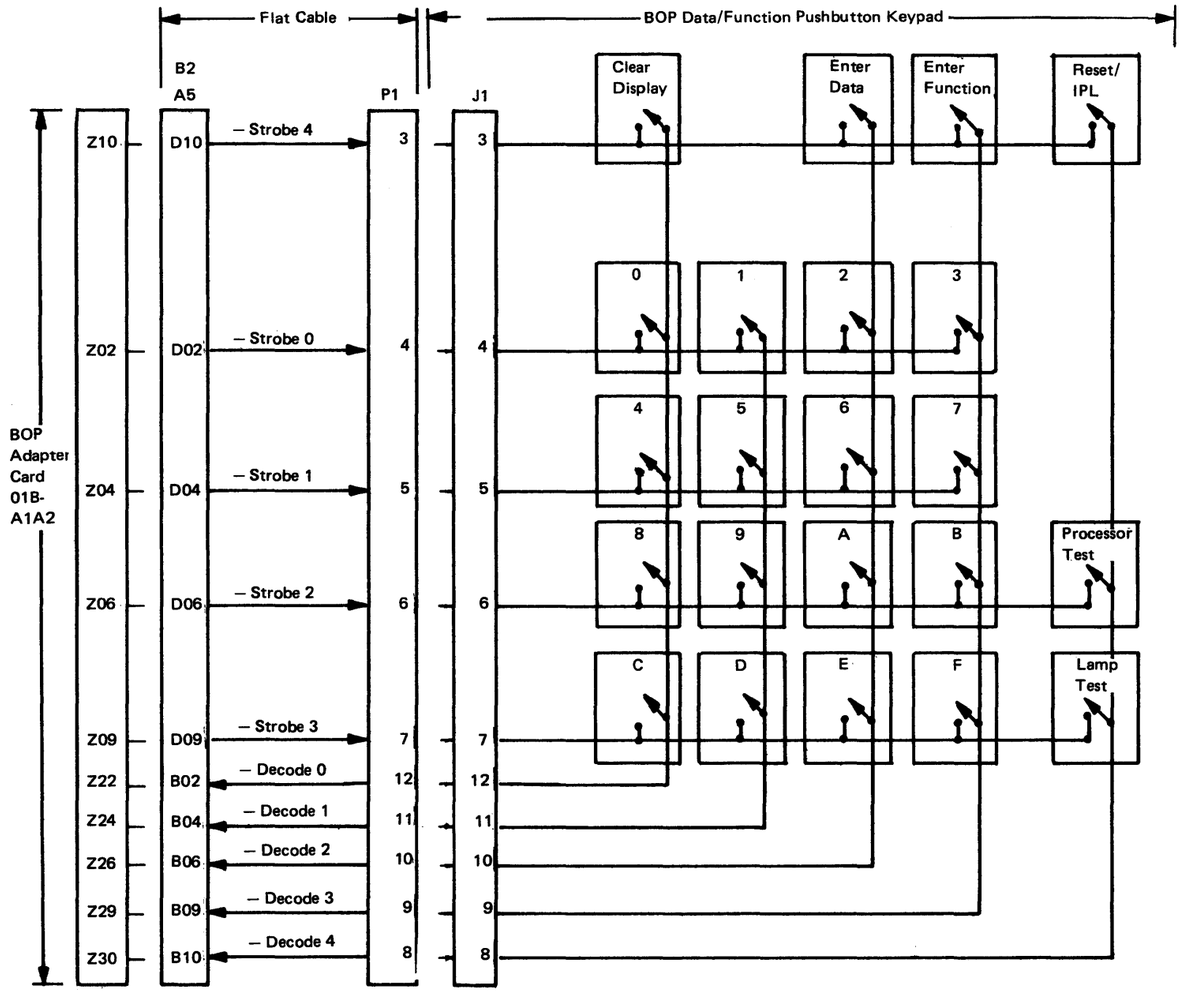


Figure BU251-3. BOP Keypad to Adapter Card Cable Continuity

BU252 BOP Indicator Checkout Procedure

When pressing the Lamp Test pushbutton, the BOP adapter card supplies a ground (OV) level to each indicator to turn them on. If an individual indicator fails to light with the Lamp Test pushbutton, perform the actions in the following table to determine the cause of failure.

Caution: Turn power off when removing or exchanging cards or cables.

Cause	Action	Comments
Loose or damaged cable or connector	Visually check cable and connectors for damaged pins or wiring, and ensure that the following are seated securely: • Indicator card P2 connector • BOP adapter card 01B–B2A4 cable	Refer to Notes 1, 2, and 4 in BU260.
Defective BOP indicator card or cable wiring	1. Disconnect cable 01B–B2A4 from the BOP adapter card (see Figure BU252-1). 2. Connect a jumper from ground to the pin of the failing indicator on the A4 cable. Refer to the table in Figure BU252-2. 3. Turn power on and observe the indicator.	Refer to Notes 1, 2, and 4 in BU260. If indicator fails to light with the jumper installed, refer to Figure BU252-3 to determine if the cable or the indicator card caused the failure. Repair or replace as necessary.
Defective BOP adapter card	Exchange BOP adapter card (01B–A1A2).	Refer to Notes 2, 3, and 5 in BU260.

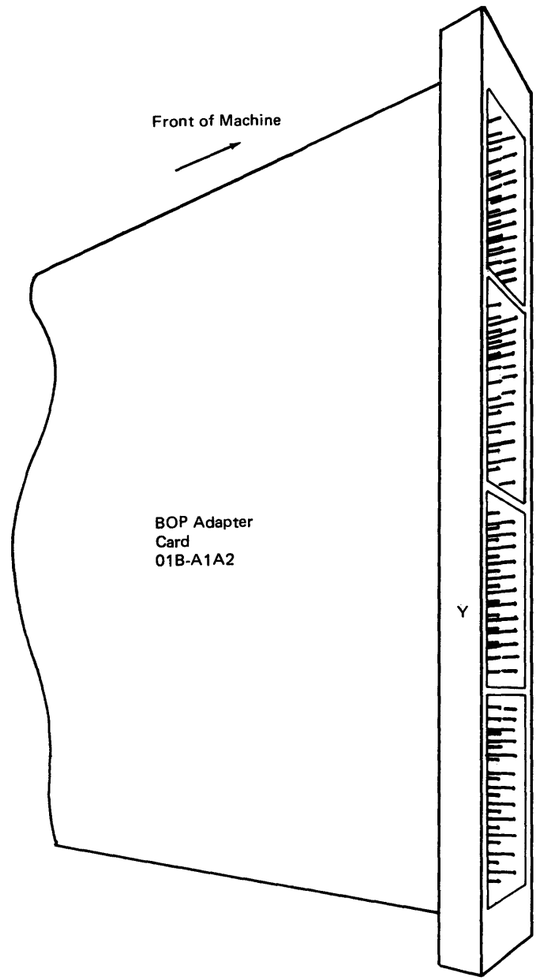
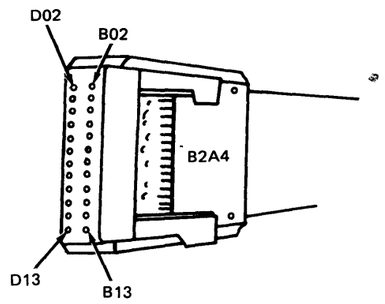


Figure BU252-1. BOP Adapter Card and Indicator Cable



BOP Indicator	Cable Pin
Operator Attention	A4D06
System Check	A4B06
I/O Interface Check	A4B07
Panel Check	A4D10
Wait	A4D08
IPL	A4B11
Test Mode	A4B09
Power On	A5B07
Power On Disabled	A5B07
Power/Thermal Check	A5B07

Figure BU252-2. BOP Indicator Continuity Check

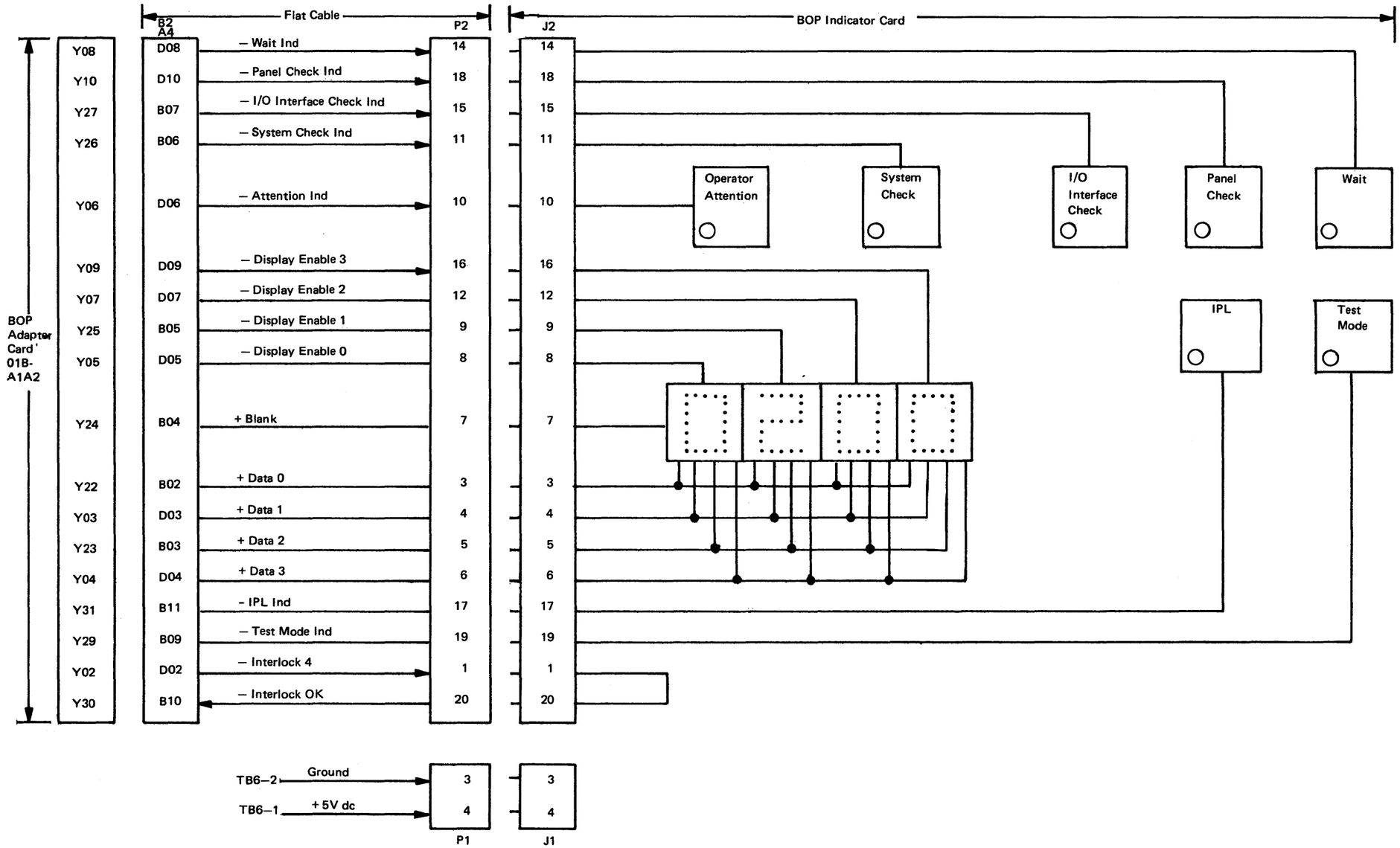


Figure BU252-3. BOP Adapter Card-to-Indicator Card Continuity

BU253 BOP Hexadecimal Display Checkout Procedure

Use this action plan if the BU MAP directs you here because it determined that the failing component is either the hexadecimal display, BOP adapter card, or associated wiring. See Figures BU253-1 through BU253-3. Perform the actions in the following table to determine the cause of failure.

Caution: Turn power off when removing or exchanging cards or cables.

Cause	Action	Comments
Loose or damaged cable or connector	Visually check cable and connectors for damaged pins or wiring, and ensure that the BOP indicator card P2 connector and BOP adapter card 01B–B2A4 cable are seated securely.	Refer to Notes 1, 2, and 4 in BU260.
Defective BOP adapter card	1. Obtain the General Logic Probe. 2. Turn 8130/8140 power on and allow 90 seconds for power-on delay. 3. With the IPL Mode switch in Manual, press Reset/IPL. 4. Enter FFFF in the Data/ Function pushbuttons. 5. Leave power on and disconnect cable in position 01B–B2A4 from the BOP adapter card. 6. Using the General Logic Probe, check for pulses on the BOP adapter card at all pins listed in Figure BU253-2.	Refer to Notes 2, 3, and 4 in BU260. If any of the eight signals are not pulsing, exchange the BOP adapter card (01B–A1A2).
Defective BOP indicator card or cable wiring	1. Turn power off and check continuity of the B2A4 cable to the indicator card 20 pin connector. Refer to Figure BU253-3 and check the continuity of the 'disp enable 0–3' and 'data 0–3' signal lines. 2. If cable continuity is correct, exchange the BOP indicator card.	Refer to Notes 1, 2, and 5 in BU260. If any of the lines indicate bad continuity, repair or replace as necessary.

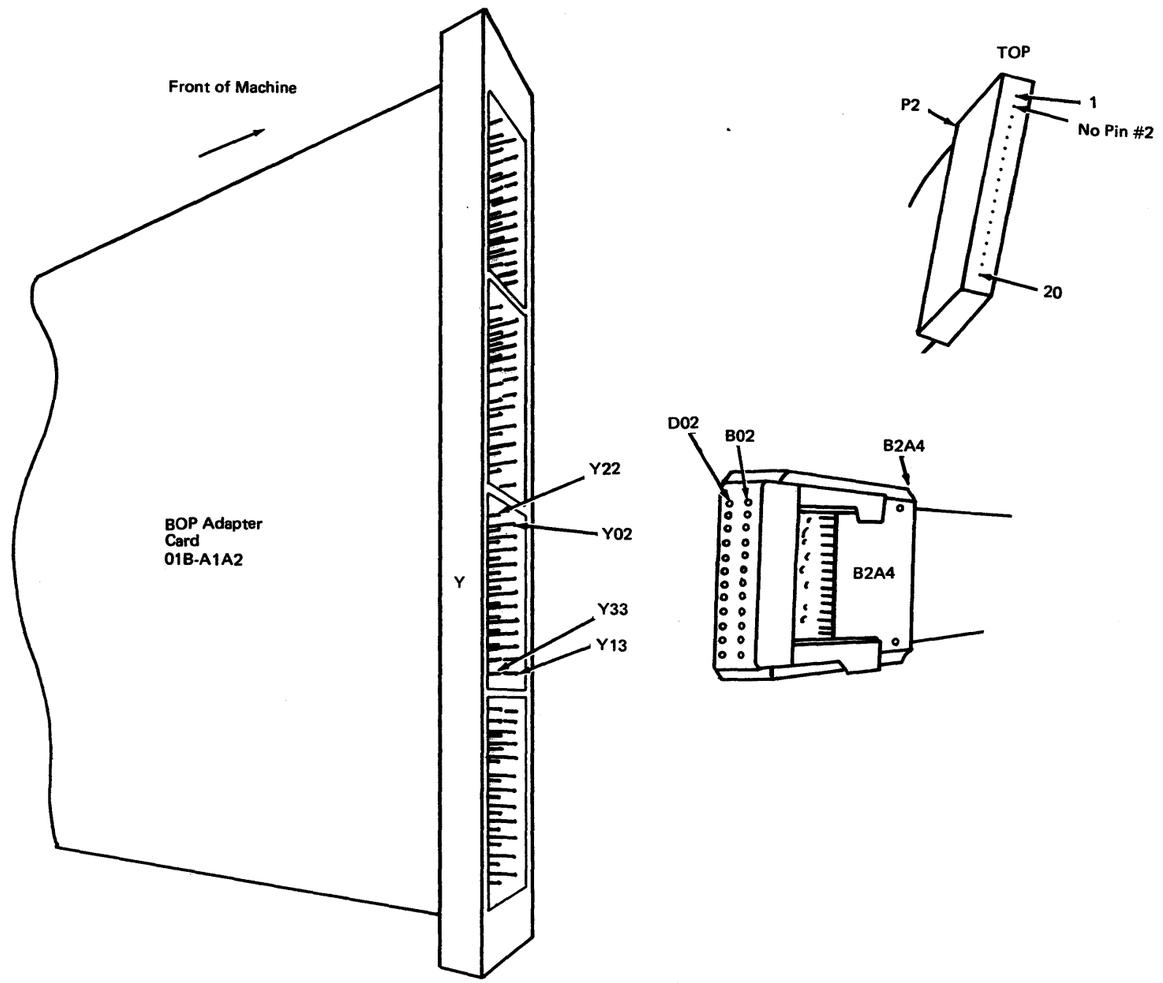


Figure BU253-1. BOP Adapter Card to Hex Display Cable Pin Numbering

Line Name	A4 Cable Pin
Display Enable 3	Y09
Display Enable 2	Y07
Display Enable 1	Y25
Display Enable 0	Y05
Data 0	Y22
Data 1	Y03
Data 2	Y23
Data 3	Y04

Figure BU253-2. BOP Adapter Card Hexadecimal Display Signals

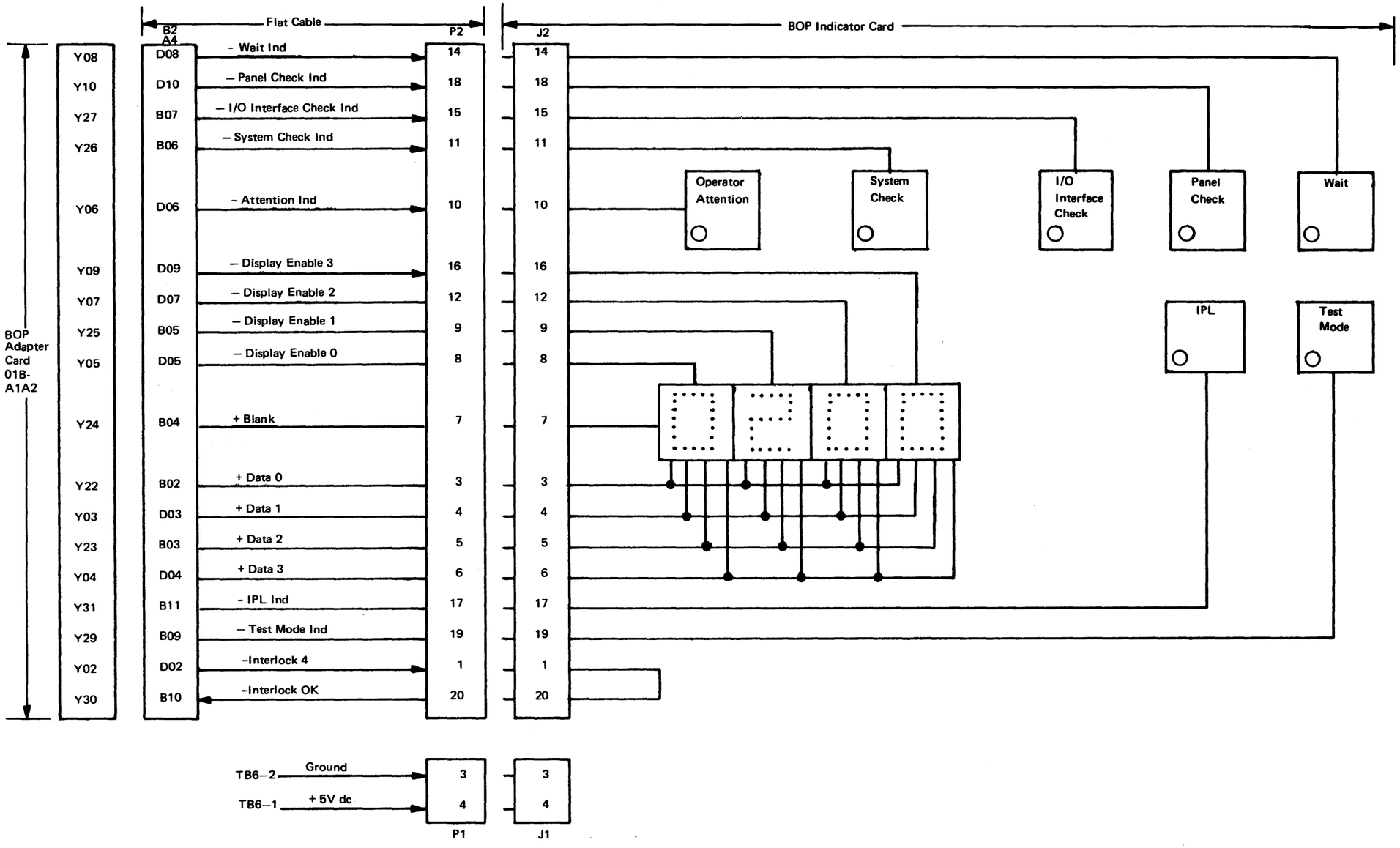


Figure BU253-3. BOP Adapter Card-to-Hexadecimal Display Continuity

BU254 BOP Cable Interlock Checkout Procedure

Three cables from the BOP adapter card, two of which go to the 01A–A1 board in 8140s and to the 01A–A2 board in 8130s and the other to the BOP indicator card, use a cable interlock circuit to detect if they are loose or unplugged. When the circuit loses continuity, the Panel Check indicator turns on and cannot be reset by either a system reset or programming. When the BU MAP directs you to use this procedure, perform the actions in the following table to determine the cause of failure.

Caution: Turn power off when removing or exchanging cards or cables.

Cause	Action	Comments
Loose or damaged cable or connector	Visually check cable and connectors for damaged pins or wiring, and ensure that the following are seated securely: • BOP adapter card 01B–B1A2 cable • BOP adapter card 01B–B1A5 cable • BOP adapter card 01B–B2A4 cable • 01A–A2 board 01A-A2A5 cable (8130) • 01A–A1 board 01A-A1Y1 cable (8140) • 01A–A2 board 01A-A2Z1 cable (8130) • 01A–A1 board 01A–A1Y2 cable (8140) • BOP indicator card P2 connector	Refer to Notes 1, 2, and 4 in BU260.
Open cable interlock circuit	Check the cable interlock circuit continuity using Figure BU254-1 (8130s) or Figure BU254-2 (8140s).	Refer to Notes 1, 2, and 4 in BU260. If the interlock circuit indicates bad continuity, repair or replace as necessary.
Defective BOP adapter card	Exchange BOP adapter card (01B–A1A2).	Refer to Notes 2, 3, and 5 in BU260.

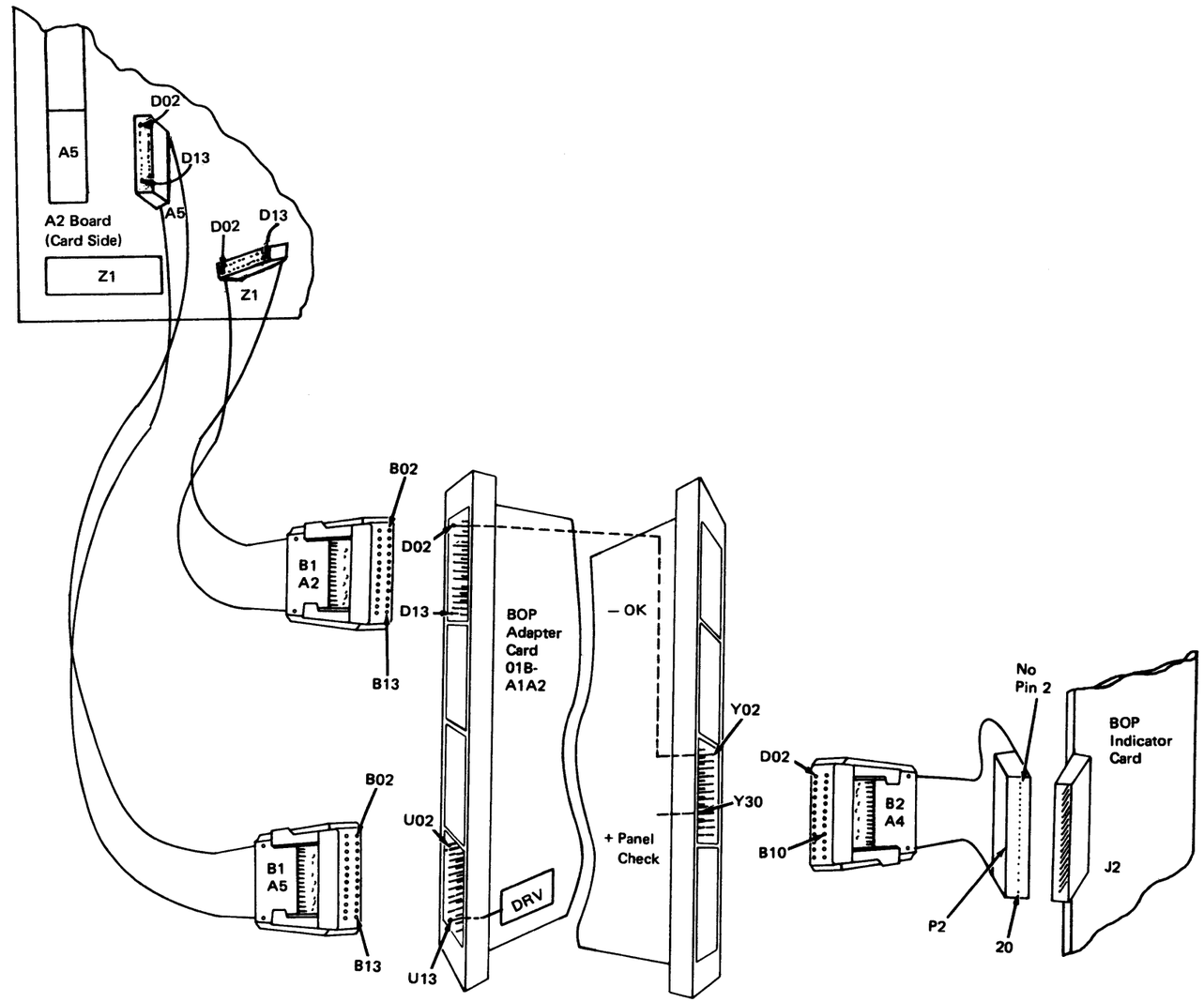


Figure BU254-1. 8130 Panel Check Interlock Circuit Cable Continuity

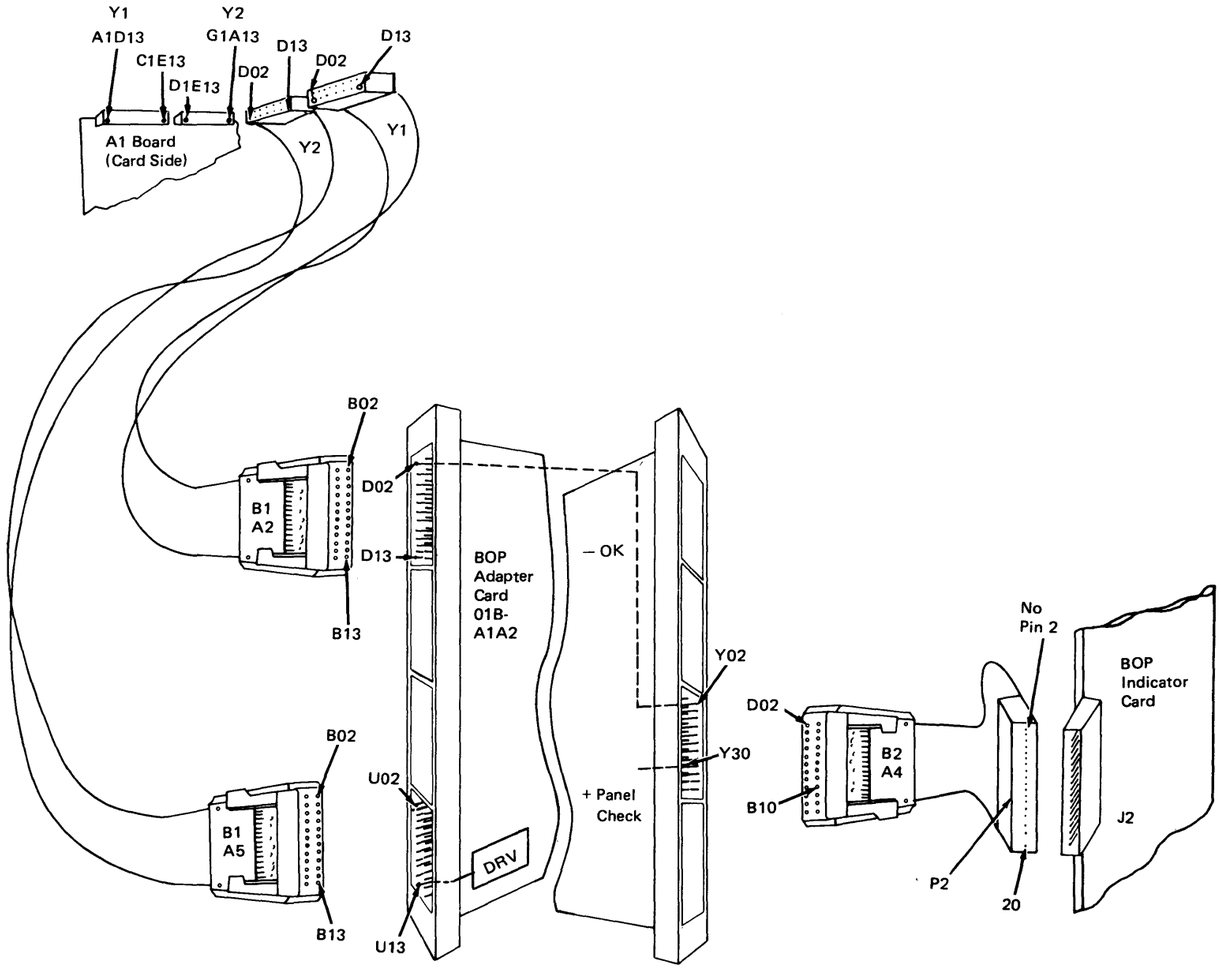


Figure BU254-2. 8140 Panel Check Interlock Circuit Cable Continuity

BU255 IPL Mode Switch Checkout Procedure

The IPL mode switch position determines if the IPL parameters must be entered manually or are obtained under system control. When in the Manual position, the IPL sequence stops at prompt message 0200 and permits you to manually enter IPL parameters. When in the Primary position, the parameters are retrieved from either the PSCF IPL switches or programmed IPL register.

If routine 3C of the extended BUs (IPL Mode Switch Test) fails, or it appears that the switch does not function correctly, perform the actions in the following table to determine the cause of failure.

Caution: Turn power off when removing or exchanging cards or cables.

Cause	Action	Comments
Loose or damaged cable or connector	Visually check cable and connectors for damaged pins or wiring, and ensure that the IPL Mode switch P1 connector and BOP adapter card 01B–B2A5 cable are seated securely.	Refer to Notes 1, 2, and 4 in BU260.
Defective IPL Mode switch	Disconnect the IPL Mode switch cable (P1) and check the continuity of the switch in both positions. Refer to Figure BU255-1.	Refer to Notes 1, 2, and 4 in BU260.
Defective or incorrect cable wiring	Measure the continuity of the cable to the IPL mode switch using Figure BU255-1.	Refer to Notes 1, 2, and 4 in BU260.
Defective BOP adapter card	Exchange BOP adapter card (01B–A1A2).	Refer to Notes 2, 3, and 4 in BU260.

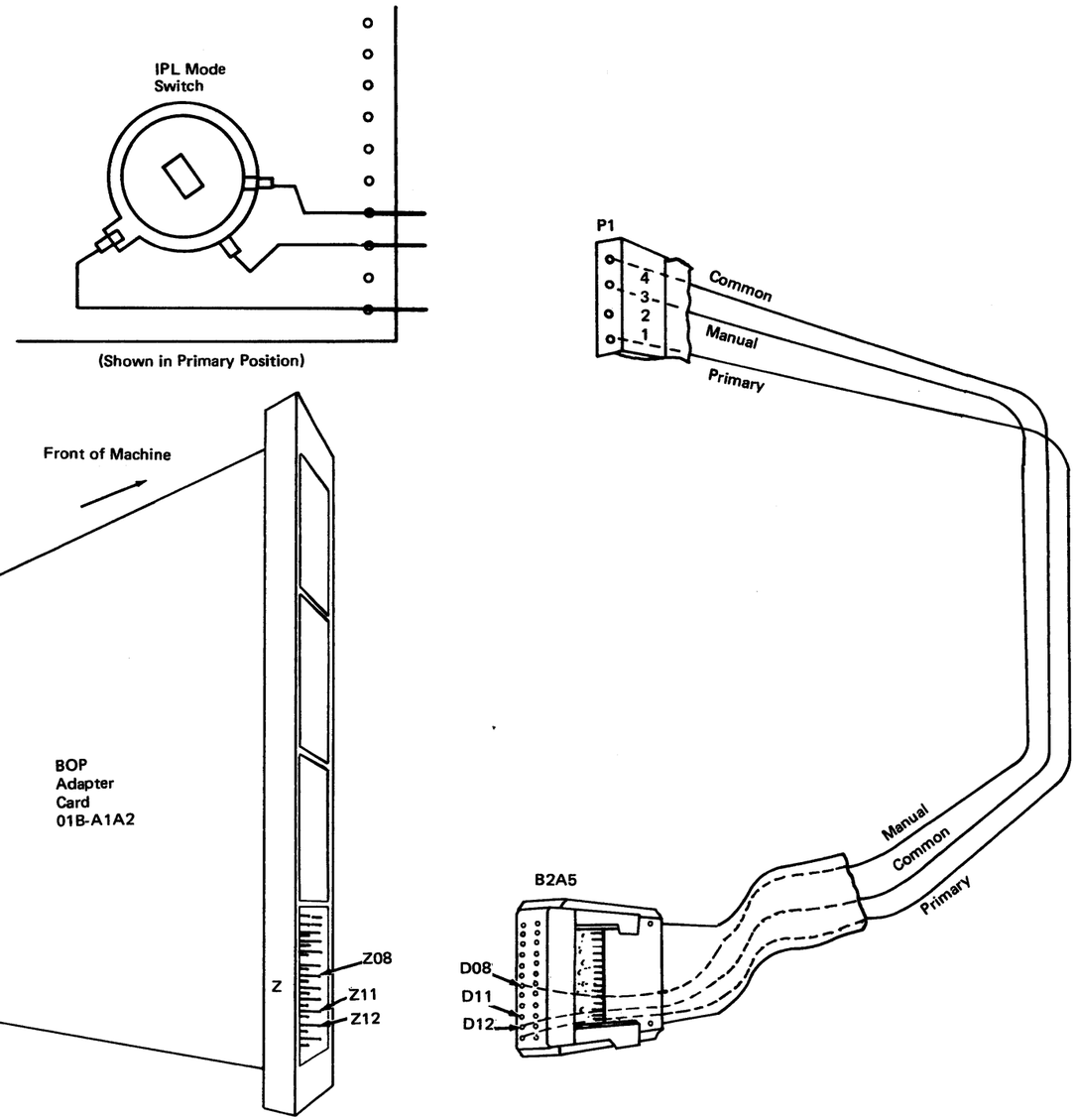


Figure BU255-1. IPL Mode Switch-to-BOP Adapter Card Continuity

BU256 Keylock Switch Checkout Procedure

Refer to BU122 for an explanation of proper keylock switch operation if necessary. If extended BU test routine 3D (Keylock Switch Test) fails or it appears that the keylock switch does not function correctly, perform the actions in the following table to determine the cause of failure.

Caution: Turn power off when removing or exchanging cards or cables.

Cause	Action	Comments
Loose or damaged cable or connector	Visually check cable and connector for damaged pins or wiring, and ensure that the BOP adapter card 01B–B2A5 cable is seated securely.	Refer to Notes 1, 2, and 4 in BU260.
Defective keylock switch or cable wiring	1. Disconnect cable 01B–B2A5 from the BOP adapter card (see Figure BU256-2). 2. Measure the continuity from the B2A5 connector to the keylock switch in all three positions using Figures BU256-1 and BU256-2.	Refer to Notes 1, 2, and 4 in BU260. If the keylock switch shows bad continuity, use Figure BU256-1 to determine if the wiring or the switch caused the failure. Repair or replace as necessary.
Defective BOP adapter card	Exchange BOP adapter card (01B–A1A2).	Refer to Notes 2, 3, and 5 in BU260.

Switch Position	Edge Connector Number	BOP Cable Pin No.	BOP Card Pin No.	Line Name	BOP BSTAT Register Bits 6, 7
Enable	EC2–f	B2–A5B08	A1–A2Z28	k/l com	00
Secure	EC1–g	B2–A5B11	A1–A2Z31	k/l pos 1	11
Power Only	EC1–h	B2–A5B12	A1–A2Z32	k/l pos 2	10

Figure BU256-1. Keylock Switch-to-BOP Adapter Card Continuity

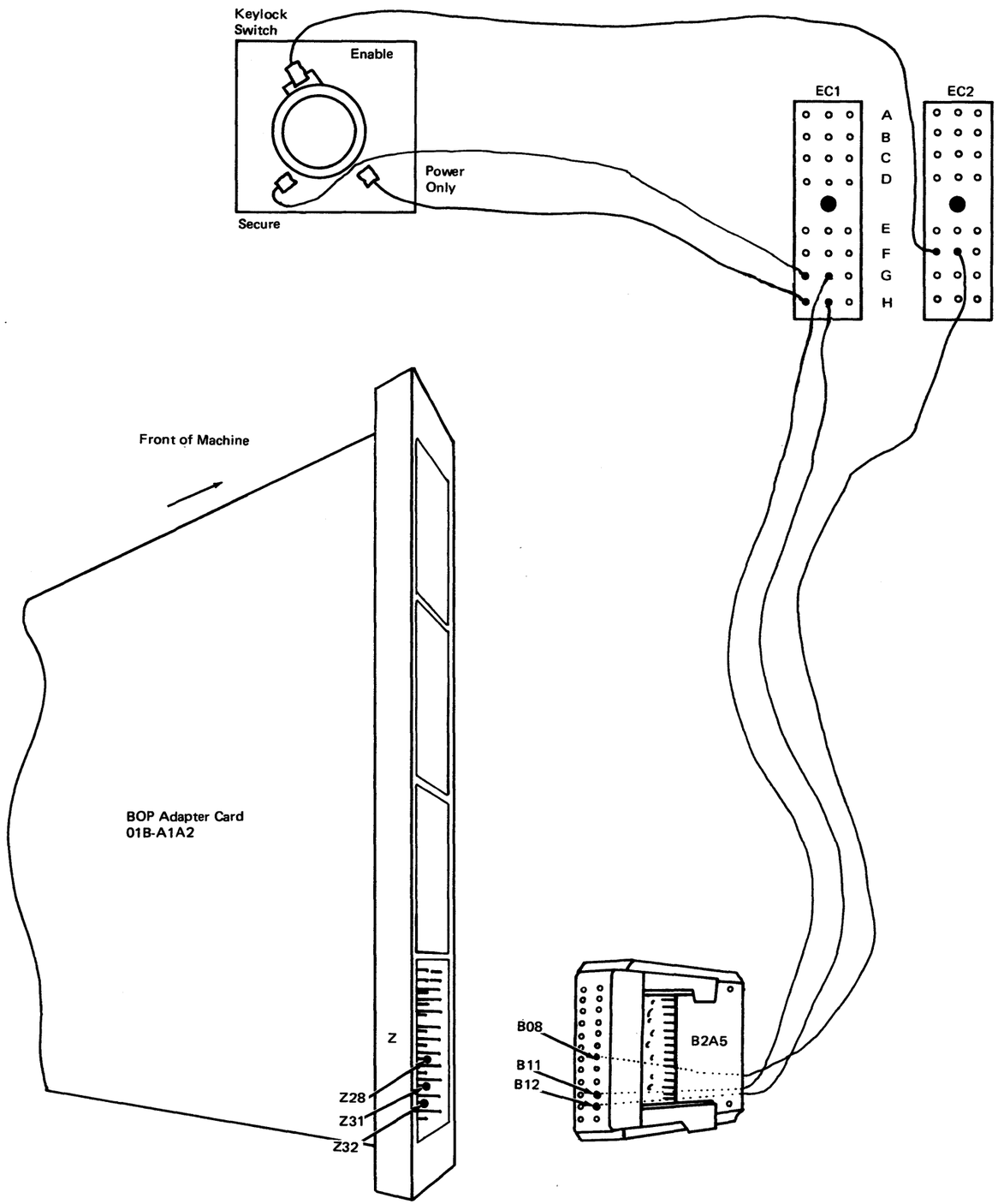


Figure BU256-2. Keylock Switch-to-BOP Adapter Card Wiring

BU257 Maintenance Device (MD) Signal Bus Checkout Procedure

The BU MAP checks the MD signal bus automatically whenever the IPL parameters specify the loading of extended tests from the MD. When the BU MAP detects a failure in this area, it directs you to exchange probable FRUs or perform a signal bus checkout according to the test results. To determine the cause of failure when directed to this procedure by the BU MAP, perform the actions in the following table that you have not previously done.

Caution: Turn power off when removing or exchanging cards or cables.

Cause	Action	Comments
Loose or damaged cable or connector	Visually check cable and connector for damaged pins or wiring, and ensure that the following are seated securely: • BOP adapter card 01B–B2A2 cable • MD connector 01H–J1 connector • MD plug on maintenance device	Refer to Notes 1, 2, and 4 in BU260.
Defective or incorrect cable wiring	1. Disconnect cable 01B–B2A2 from the BOP adapter card (see Figure BU257-1). 2. Measure the continuity from the B2A2 connector to the MD connector socket pins using Figures BU257-1 and BU257-2.	Refer to Notes 1, 2, and 4 in BU260.
Defective BOP adapter card	Exchange BOP adapter card (01B–A1A2).	Refer to Notes 2, 3, and 4 in BU260.
Defective MD	Exchange MD	Refer to Note 5 in BU260.

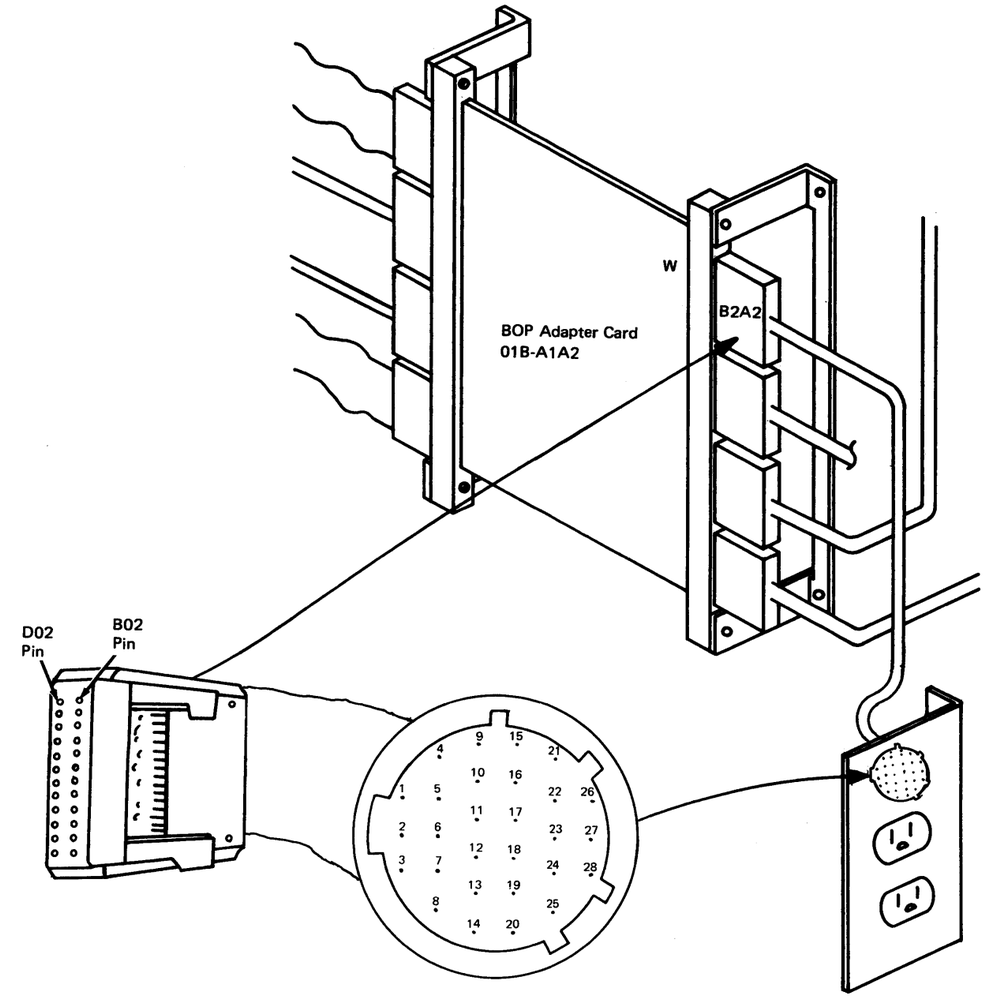


Figure BU257-1. BOP Adapter Card Cable-to-MD Socket

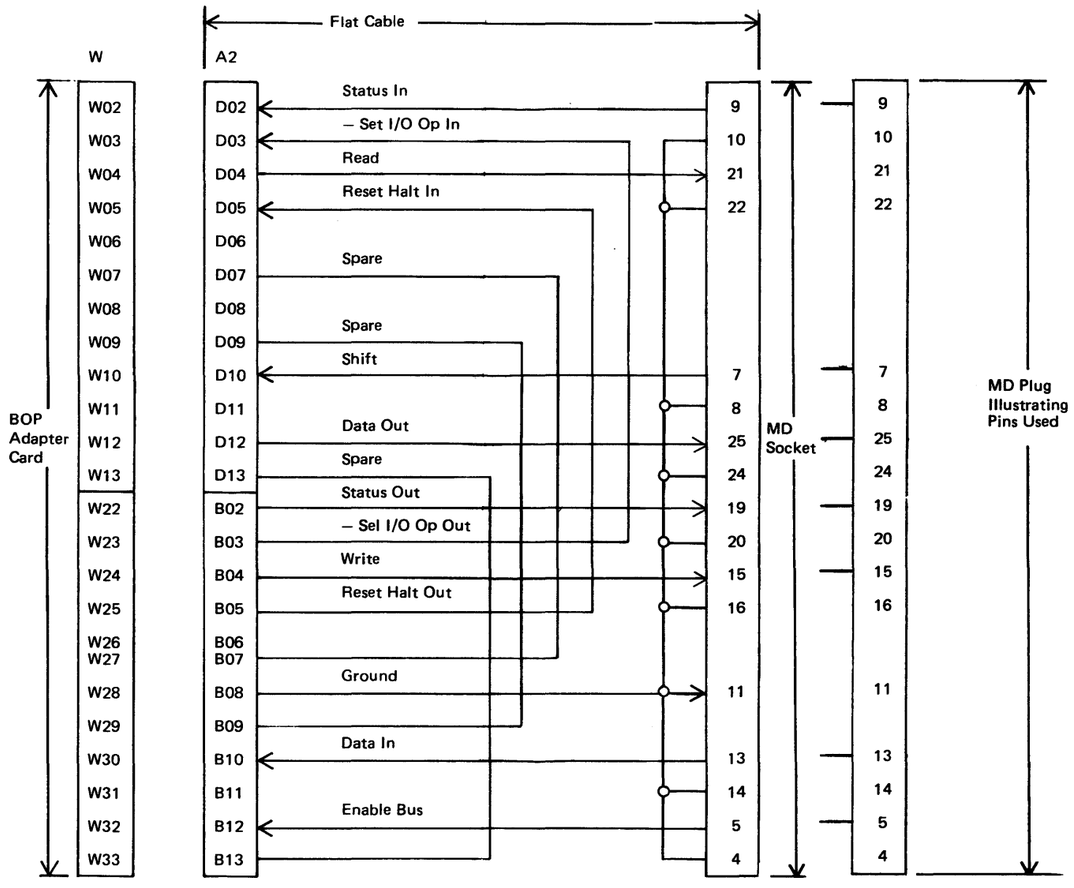


Figure BU257-2. BOP Adapter Card-to-MD Socket Signal Pins

BU260 Common Action Plan Notes

Note 1: *Refer to section BU520 to gain access to BOP components and for removal/replacement procedures.*

Note 2: *Refer to BU111 for BOP cable locations.*

Note 3: *Refer to BU510 for BOP adapter card removal/replacement procedures.*

Note 4: *To verify the repair, run the BU tests using the BU MAP menu selection A, offline checkout. If the same failure occurs, go to the next step in the table.*

Note 5: *If the same failure occurs after completing the last step in the table, reinstall the original FRUs if any were exchanged and go to section BU350.*

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BU300 Intermittent or Random Failure Repair Strategy

Certain errors make the BU MAP ineffective. For example, random errors can occur during different test routines and generate different test error message numbers. Also, the MAP might not detect errors if they occur infrequently.

When intermittent failures occur, you can attempt fault isolation by looping the tests for an extended period while under MAP control, or using the free-lance looping option to selectively loop the tests. Sections BU311 and 312 explain these repair strategies.

When random or hard to analyze failures occur, refer to section BU350, which lists the action plans you can take to help determine the cause of failures.

BU310 Unique Intermittent Repair Strategy

Other than the action plans contained in BU350, you can use the following two options for determining the cause of an intermittent failure:

1. You can loop the tests under BU MAP control for a specified period. Ten to twenty minutes is usually sufficient to detect the failing condition, but this depends on the frequency of failure.
2. You can loop the tests selectively by using the free-lance option. In this manner, you can select a routine or group of routines and specify certain run options.

The following sections explain how to use these options.

BU311 Looping Extended BU Tests Using the BU MAP

The extended BU tests can be looped offline under control of the BU MAP. If answering "yes" to the prompt message "DO YOU WANT TO CHECK FOR INTERMITTENT FAILURES BY LOOPING THE EXTENDED TESTS", the tests loop continuously. The MD display indicates the following three status messages:

TEST STARTED – ERROR INDICATED BY ..... OP. PANEL TEST MODE LIGHT BLINKING. *FWD	IF NO ERROR AFTER 10 MINUTES, RESET/IPL 8100 TO END LOOP. *FWD	ENTER C AT MD ON AN ERROR OR MD RESET TO TERMINATE.

If the BOP displays an error message, enter C at the MD. The MAP then checks the failure as if it were detected while running the BU tests without looping.

After performing a repair action, loop the BU tests to verify the repair. If an error does not occur after looping the tests for 10 minutes, press Reset/IPL on the BOP to terminate looping and end the repair action.

BU312 Free-Lance Operation

The extended BU tests can be looped using the Free-Lance Utility. Refer to CP462 "Free-Lance Utility" in Chapter 2 for further explanation.

You should use option A, which specifies offline tests, and then select the proper options at the 80BC and 81BC prompt messages to run the extended BUs. The tests then loop continuously until either detecting an error or being terminated by pressing the BOP Reset/IPL pushbutton.

If an error occurs during free-lance operation, the BOP displays the error message. Record this error message. If the error message is 0F00–0FFF, select BU MAP menu option A. For any other failure, select BU MAP menu option B. The BU MAP then prompts you to enter the error message, and uses this message for fault isolation.

After performing a repair action, loop the BU tests for at least 5 minutes to verify the repair.

BU350 Repair Strategy for Random or Hard to Analyze Failures

Note: *Use this strategy only after the MAP failed to locate the failing FRU. Perform only those actions not previously performed.*

The MAP uses a step-by-step approach to isolate BU test failures to a particular FRU, and might be ineffective for failures that occur intermittently, randomly, or infrequently.

To perform fault isolation on failures of this type, perform the following actions according to the probable cause, and then run the BU MAP menu selection A offline checkout. As an aid in determining the area of failure, look up the error message in section BU240 and also refer to the failing routine description in section BU210. If the failure is not found after performing all actions listed, reinstall all cards into their original positions and request aid.

Caution: Unless otherwise specified, turn power off when loosening, removing, or replacing cards or cables.

Probable Cause	Action	Comments
Missing or out of tolerance voltage	Perform voltage checks using the procedures in the BU530 section.	
Missing voltage or power signal (8140 only)	1. Verify that cables in the following locations are correctly seated: Models A3X, A4X, 01A-A2Z3 Models A5X, A6X, A7X 01A-A2Z1 Models BXX 01A-A1Z1 2. If cables were properly seated and problem remains, perform continuity check between the following points: Models A3X, A4X 01A-A2H6A04 to PC-1 J8A12 01A-A2H6B04 to PC-1 J8A15 Models A5X, A6X, A7X 01A-A2A6D04 to PC-1 J8A12 01A-A2A6E04 to PC-1 J8A15 Models BXX 01A-A1A6D04 to PC-1 J8A12 01A-A1B6B04 to PC-1 J8A15	Can be caused by defective or loose cable. Possible symptoms are BOP messages 04EA, 06EA or if BOP message 0200 appears immediately after power up.
Loose or damaged processor card or top card connector	1. Remove the top card connectors from the processor cards BU1—BU9. (See BU111 for locations.) 2. Remove processor cards BU1—BU9 and inspect the board for foreign material and bent or broken pins. 3. Examine each card for damaged pins or shrouds and verify that the part numbers are correct for each location. (See Card Part Number Listing.) 4. Reinstall the cards in the correct board locations and ensure that they are seated securely. When inserting the cards, be sure that you face the component side of the card to the right and that you line up the card shrouds with the board sockets. 5. Carefully examine the top card connectors for bent or broken pins. Use a pin straightener if needed. 6. Reinstall the top card connectors and ensure that they are seated securely. See BU111 for correct part numbers and locations.	

Probable Cause	Action	Comments
Hardware failure on the I/O bus external to the processor instruction/ execution unit and PSCF (SC1) card	1. With power on, loosen the three cables at locations W, X, and Y on the 01A–A1A2 card (8140 Models AXX), on the 01A-A1D2 card (8140 Models BXX), or on the 01A–A2G2 card (8130). If power has just been turned on, allow 90 seconds for the system to complete the power on sequence before loosening the cables. 2. If the basic and extended BU tests now load and run correctly from the MD, the failure is external to the processor instruction/ execution unit. Power down, reseat the cables, and go to the SC MAP and select menu option 6, IPL failure.	If the same failure occurs with the cables loosened, reseat the cables and go to the next step.
Defective R/W storage card above 64K (8140 Models A3X, A4X, and A5X only)	1. Loosen the R/W storage cards having a hex address of 10000 and above. (See BU111 for locations.) 2. If the basic BU tests now run correctly (message 0200) and the first extended test failure is in Routine 2B (Routine 36 on an 8130), one of the loosened cards caused the original failure. Reseat the cards one at a time and run the BU tests after reseating each one to isolate the failing card.	If the same failure occurs with the cards loosened, reseat the cards and go to the next step.
Defective R/W storage card 32–64K (8140 Models A3X, A4X, and A5X only)	1. Remove R/W storage card having hex address 8000 and replace it with the card having hex address 10000. (See BU111 for locations.) 2. If the basic BU tests now run correctly (message 0200), and the first extended test failure is in Routine 2B, the original card used for hex address 8000 caused the failure.	If the same failure occurs with the card removed, restore cards to their original locations and go to the next step.

Probable Cause	Action	Comments
Defective R/W storage (8140 only)	1. Verify that all storage cards are seated securely. 2. Verify that cables at the following locations are seated securely according to 8140 model number: • 8140 Models A3X, A4X, and A5X 01A–A1Z4 to 01A–A2Y4 01A–A1Z5 to 01A–A2Y5 01A–A1Z6 to 01A–A2Y6 • 8140 Models A6X and A7X 01A–A1Z3 to 01A–A2Y3 01A–A1Z4 to 01A–A2Y4 01A–A1Z5 to 01A–A2Y5 01A–A1Z6 to 01A–A2Y6 • 8140 Models BXX 01A–A1V2W to 01A–C1Y2 01A–A1V2X to 01A–C1Y1 01A–A1V2Y to 01A–C1Z1 01A–A1V2Z to 01A–C1Z2 3. If cables are seated securely and the error persists, perform continuity check to determine if cables are defective. 4. Examine the storage cards and storage boards for bent or broken pins and shrouds.	If the same failure still occurs, go to the next step.

Probable Cause	Action	Comments
Defective R/W storage (8140 Models A3X, A4X, and A5X only)	If all other methods fail to isolate a possible R/W storage failure, use the following procedure: 1. Loosen all but the first four storage cards (storage block numbers 00-03). See BU111 for card locations. 2. Using the Configuration Utility on MD diskette 01 (see CP466 for description and instructions), record the original YY value for future use and change the first configuration table entry From: 0C990F00XXYYXXXX To: 0C990F00XX04XXXX **Note:** *Do not change any XX values.* 3. Using the Free-Lance Utility (see CP462 for description and instructions), run the extended bring-up tests. 4. If no failure occurs, remove the two rightmost storage cards still in use, and swap them for two of the loosened cards. 5. Repeat steps 3 and 4 until all the storage cards have been tested or a failure occurs. • If a failure occurs, isolate the failing card and replace it. After verifying the fix, return the first configuration table entry to its original value and reseat any loosened cards. • If no failures occur, return the first configuration table entry to its original value and reseat any loosened cards.	

Probable Cause	Action	Comments
Defective ECC. (8140 Models A6X, A7X, and BXX only.)	1. Exchange ECC card 1 at location 01A-A2M2 in 8140 Models A6X and A7X or at location 01A-C1B2 in 8140 Models BXX with a new card. 2. Run basic and extended BU tests. If tests now run correctly, ECC card 1 was failing. 3. If tests still do not run correctly, exchange ECC card 2 at location 01A-A2L2 in 8140 Models A6X and A7X or at location 01A-C1A2 in 8140 Models BXX with a new card. Reseat original ECC card 1. 4. Run basic and extended BU tests. If tests now run correctly, ECC card 2 was failing.	
Defective floating-point card (8140 models with floating point).	1. Remove the top card connectors and loosen the cards at locations 01A—A1M2 and 01A—A1N2 in 8140 Models A4X, A6X, or A7X or at locations 01A—A1Q2 and 01A—A1R2 in 8140 Models BXX. 2. If the basic BU tests now run correctly (message 0200) and the first extended test failure is in Routine 19, one of the loosened cards caused the original failure. Exchange the cards one at a time and run the BU tests to determine the failing card.	If the same failure occurs with the cards loosened, reseat the cards, reinstall the top card connectors, and go to the next step.
Defective expanded function panel adapter (8140 only feature)	1. Loosen the EFP adapter card: Models A3X = 01A—A1M2 Models A4X, A6X and A7X = 01A—A1P2 Models BXX = 01A—A1S2 2. Loosen the EFP cable on the BOP adapter card at 01B—B2A3. 3. If all basic and extended BU tests now run correctly with the card and cable loosened, exchange the EFP card with a new card. 4. If the same failure occurs with a new EFP card, go to the SP MAP and use the IPL FAILURE menu selection.	If the same failure occurs with the card and cable loosened, reseat the card and cable and go to the next step.
Defective BOP adapter card.	Exchange the BOP adapter card (01B—A1A2) with a new card if not previously done. See BU510 for removal/replacement procedures.	
Defective SC1 card	Exchange card: 8130 = 01A—A2G2 8140 Models AXX = 01A—A1A2 8140 Models BXX = 01A—A1D2 Before exchanging, set the switches on the new card to the same positions as the original card.	
Defective ROS card (8140 only)	Exchange the storage card that contains read-only storage. **Model** — **Location** A31—34 — 01A—A1P2 A41—44 — 01A—A1R2 A51—54 — 01A—A1N2 A6X, A7X — 01A—A2K2 BXX — 01A—A1U2	
Defective processor card	1. Determine the processor card locations (BU1—BU9) for your machine type (see BU111). 2. Exchange all cards (BU1—BU9) not previously exchanged with new cards. 3. If basic and extended BU tests now run correctly with the new cards, reinstall the original cards one at a time and run the BU tests to determine the failing card.	If the same failure occurs with the new cards, reinstall all original cards removed in this and all previous steps and request aid. While waiting, do a continuity check of the board wiring using the BU400 section.

BU400 Signal Paths and Detailed Operational Description

This section contains information not necessarily needed for fault isolation, but which can be useful to determine certain possible areas of processor, operator panel, and BOP adapter failures. It shows point-to-point logic card signal lines, data flow diagrams, and provides detailed descriptions of processor instruction/execution unit and BOP functions.

BU410 Board Signal Paths

The following sections show the processor instruction/execution unit point-to-point signal path to the BOP, EFP, storage, PSCF, and floating-point functions.

BU411 8130 Processor Instruction/Execution Unit

Figure BU411-1 shows the interconnection of logic signals in the 8130 processor instruction/execution unit. The signals are listed alphabetically by signal name. For further information see the BU420, BU450, and BU460 sections.

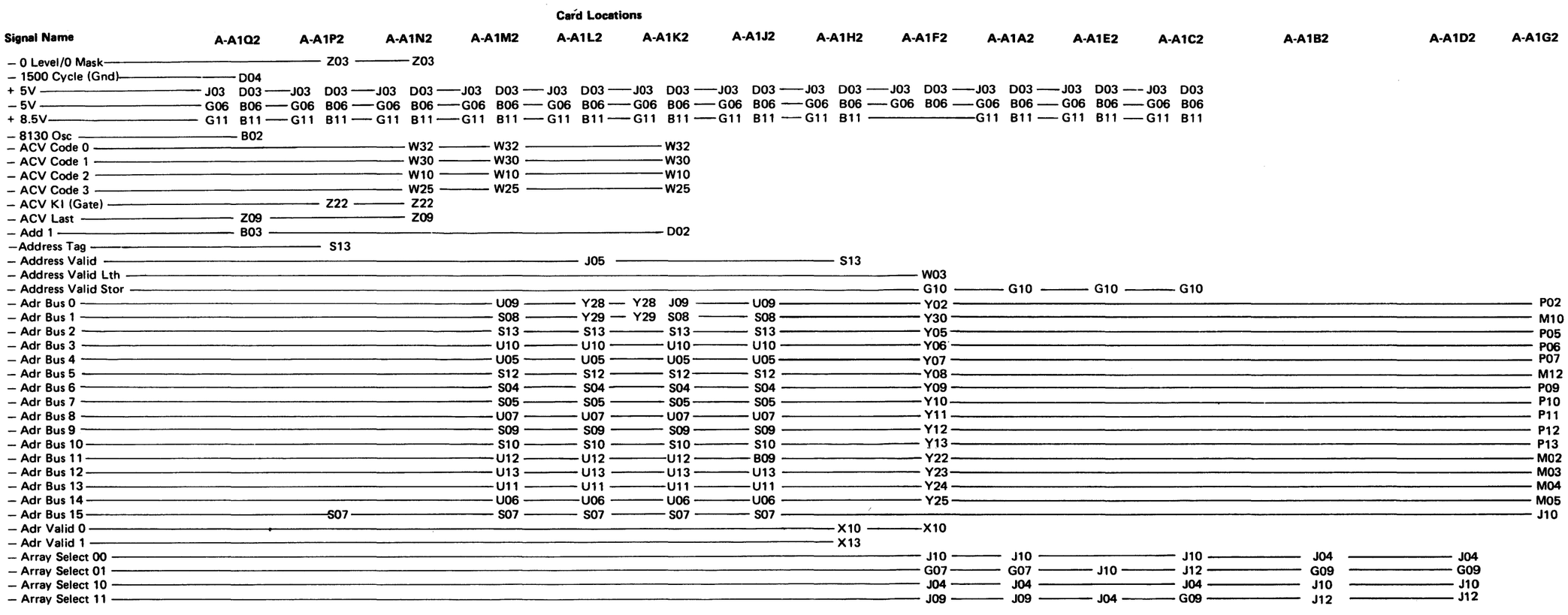

Figure BU411-1 (Part 1 of 9). 8130 Processor Instruction/Execution Unit Point-to-Point Signal Path

Signal Name	Card Locations														
	A-A1Q2	A-A1P2	A-A1N2	A-A1M2	A-A1L2	A-A1K2	A-A1J2	A-A1H2	A-A1F2	A-A1A2	A-A1E2	A-A1C2	A-A1B2	A-A1D2	A-A1G2
– B							Y13	Y13							
– BAR C0						Z26 M05		P06							
– BAR To Source				P12		P12									
– BAR-1 Bit 0						X28	X28								
– BAR-1 Bit 1						X29	X29								
– BAR-1 Bit 2						X30	X30								
– BAR-1 Bit 3						X32	X32								
– BAR-1 Bit 4						X33	X33								
– BAR-A		J06			Y13 J13	Y13									
– Branch Taken	S07		S07												
– Byte	B04			B13		B13									
Byte Select 0									X29	J05		J05	J05	J05	G09
Byte Select 1									X28	J11		J11	J11	J11	G08
– Byte Tag		P02													
– C To ADC			P05	B08											
– C0		Y12	Y12	Y12											
– C0 High				J09				G13							
+ C0 HW Latch	Y05			Y05											
– C1			P06	P06											
– Card Select 0									G04	G04					
– Card Select 1									G03				G04		
– Card Select 2									G05			G04			
– Card Select 3									G09					G04	
– Chk 5 0 Or S/L	B13				D12										
– CIN			S08												
– CLA To Source (Gate)		Z13	Z13												
+ Clear Channel	W02	W02													
– Cnt Not = 0	Z12		Z12												
– Cntl Sys Rst															
Command A									G12	G12		G12	G12	G12	
Command B,C									J06	J06 G07		J06 G07	J06 G07	J06 G07	
– Command Tag		U13													
+ Common	P02														
– Compare Inst		D04				B02									
+ Count = 1	M12						M10								
+ CHIO In Progress	W11	W11	S05				S02	S05							
+ CHIO Or PSV Sw Req	W03	W03													
– CHIO Req	Z08	Z08	Z08	U09											
– CHIO Request Latch	W30	W30													
– CHIO Request Tag			B13												
– CHIO Gate Tag		U12													
– D							Y22	Y22							
+ Data Gate 1									P13	P13		P13	P13	P13	
+ Data Gate 2									P06	P06		P06	P06	P06	
+ Data Gate 3									B12	B12		B12	B12	B12	
+ Data Gate 4									P07	P07		P07	P07	P07	
+ Data Gate 5									M09	M09		M09	M09	M09	
+ Data Gate 6									M05	M05		M05	M05	M05	
+ Data Gate 7									M03	M03		M03	M03	M03	
+ Data Gate 8									P04	P04		P04	P04	P04	
– Data Not Valid	X02														
– Data Parity Chk Lth 0									Y26						
– Data Parity Chk Lth 1									Y08						
– Data Tag		P09													
– Dest Bus 0			J11 Z06		J11 Z06			J10							
– Dest Bus 1			D04 Z07		D04 Z07			J11							
– Dest Bus 2			B02 Z02		B02 Z02			G03							
– Dest Bus 3			B03 Z03		B03 Z03			G07							
– Dest Bus 4			D05 Z24		D05 Z24			G04							
– Dest Bus 5			D02 Z10		D02 Z10			J07							
– Dest Bus 6			B05 Z05		B05 Z05			J09							
– Dest Bus 7			P02 Z28		P02 Z28			J05							
– Dest Bus 8			M12 Z09		M12 Z09		Z09	D02							
– Dest Bus 9			D13 Z13		D13 Z13		Z13	B02							
– Dest Bus 10			P07 Z12		P07 Z12		Z12	B10							
– Dest Bus 11			U02 Z11		U02 Z11		Z11	D04							
– Dest Bus 12			J12 Z29		J12 Z29		Z29	B12							

Figure BU411-1 (Part 2 of 9). 8130 Processor Instruction/Execution Unit Point-to-Point Signal Path

Signal Name	Card Locations													
	A-A1Q2	A-A1P2	A-A1N2	A-A1M2	A-A1L2	A-A1K2	A-A1J2	A-A1H2	A-A1F2	A-A1A2	A-A1E2	A-A1C2	A-A1B2	A-A1D2	A-A1G2
– Dest Bus 13			P10	Z30 P10	Z30	Z30		B13							
– Dest Bus 14			P11	Z22 P11	Z22	Z22		D05							
– Dest Bus 15	J09		J05	Z23 J05	Z23	Z23		J04							
– Dest Bus PH			G12		G12			G12							
– Dest Bus PL			M02		M02			M02							
+ Dest Bus = 0	Y02		Y02	Y02											
– Dest Field 0 ROS	Y13		Y13	Y13											
– Dest Field 1 ROS	Y32		Y32	Y32											
– Dest Field 2 ROS	Y30		Y30	Y30											
– Dest Field 3 ROS	Y33		Y33	Y33											
– Dir/Ind Chaining	D11				D11										
– Div/Ovf				D10	D05										
– Div/CLC	B09					D09									
– E							Y25	M07 Y25							
– EOC Latch	W05	W05													
– EOC Tag		M12													
– ESA 1							B08								
– ESA 2							B05								
– ESA 3							B04								
– ESA 4							D02								
– ESA Stack Op															
– ESA Stack Sel					D04										
+ Exit		D11	P09			X03 D11		D09							
– Exit	W06	W06													
+ Exit Allow I-Fetch		X30			X30										
– Ext Stk Error		D09													
– Ext Stk Op					G13			U05							
– Ext Stk Out Bus 0							W06	W06							
– Ext Stk Out Bus 1							W07	W07							
– Ext Stk Out Bus 2							W08	W08							
– Ext Stk Out Bus 3							W09	W09							
– Ext Stk Out Bus 4							W10	W10							
– Ext Stk Out Bus 5							W11	W11							
– Ext Stk Out Bus 6							W12	W12							
– Ext Stk Out Bus 7							W13	W13							
– Ext Stk Out Bus 8							W22	W22							
– Ext Stk Out Bus 9							W23	W23							
– Ext Stk Out Bus 10							W24	W24							
– Ext Stk Out Bus 11							W25	W25							
– Ext Stk Out Bus 12							W26	W26							
– Ext Stk Out Bus 13							W27	W27							
– Ext Stk Out Bus 14							W28	W28							
– Ext Stk Out Bus 15							W29	W29							
– Ext Stk Out Bus PH							W30	W30							
– Ext Stk Out Bus PL							W32	W32							
– Ext Stk Sel					D10			P07							
– F0			U10												
– F1			U11												
– F2			S05												
– F3			B08												
– FA I/O		Y08	Y08												
– FA Logic 0 ROS	W07	W07													
– FA Logic 1 ROS	Y25	Y25		Y25											
– FB Logic 0	Y29	Y29		Y29											
– FB Logic 1	Y11	Y11		Y11											
– FB-A				U04	U04										
+ First Half	Z25 B05	Z25	Z25				P05	U06							
+ Force Dec = 15			D12	D12											
– Force PSV Swap		X02	X02												
– FP Inst	P04			G04		B04	B02								
– FP PC					G07										
– FP Req 0	G13														
– FP Req 1	S04														
– FPT02	J13														
– FPT02 Delta	U10														

Figure BU411-1 (Part 3 of 9). 8130 Processor Instruction/Execution Unit Point-to-Point Signal Path

Signal Name	A-A1Q2	A-A1P2	A-A1N2	A-A1M2	A-A1L2	A-A1K2	A-A1J2	A-A1H2	A-A1F2	A-A1A2	A-A1E2	A-A1C2	A-A1B2	A-A1D2	A-A1G2
					Card Locations										
– Gate Ext Stk To Source							Y10	Y10							
– Gate I Field				M04		P13									
– Gate Initial Adr					J09			M08							
– Gate MOR HL		X12			X12										
– Gate MOR HW		X26			X26										
– Gate MS HL					Y02	Y02									
– Gate MS HW					Y22	Y22									
– Gate Pages to Source		X24			X24										
– Gate Pty Err							Y11	Y11							
+ Gate Set ROS Output	Y27	Y27													
– Gate Stk HL					G10		G10								
– Gate Stk HW					J07										
Gnd	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08
– Halt Tag Ext		B05				B08									
– Hi Stor								W05	J07						
– I Fetch		X10 G07			X10										
– I Reg 4			U04			J11									
– I Reg 5			S02			G08									
– I Reg 6			M09			J12									
– I Reg 7			P13			G07									
– Imm FD Bit 8						Z27 G10		G10							
+ Inc/Dec				J13				J13							
– Inh Val/Wrt							Y32	Y32							
– Inhibit CHIO Reg		X03	X03												
– Initial Rel							Y26	Y26							
– Interrupt KI		Z23	Z23												
– Interrupt Sys Reset		Z29	Z29												
+ Invalid Access Code					J11			B09							
– Invalid ALV					J04		J02	J06							
– Invalid Op		G13				B03									
– Invalid VS Lth									W26						
– IPL ROS									X25						G05
– IRP Tag		U10													
+ I-F NLI		X25			X25										
– I/O							Y23 M09	Y23							
– I/O Bus 0			B07												
– I/O Bus 1			D06												
– I/O Bus 2			B10												
– I/O Bus 3			B09												
– I/O Bus 4			J04												
– I/O Bus 5			B04												
– I/O Bus 6			G08												
– I/O Bus 7			J07												
– I/O Bus 8			G02		G02										
– I/O Bus 9			J02												
– I/O Bus 10			B12												
– I/O Bus 11			J09												
– I/O Bus 12			D10												
– I/O Bus 13			D07												
– I/O Bus 14			D09												
– I/O Bus 15			G05												
– I/O Bus PH			G09												
– I/O Bus PL			M03												
– I/O Data Out Gate			M04	D09											
– I/O Exception		Z06 M03	Z06												
– I/O PH Error		Z07	Z07												
– I/O Int Bus Bit 8			W27		W27										
– I/O PL Error		Z02	Z02												
– I/O Sample Interrupt		Z05	Z05												
– I/O Tag (Gate)		M04													
– I/O to Source Bus		Z33	Z33												
– Jump to Adder			D11			G03									
– KI Inst		M09				B10									
+ Last Phase	D05	X11 J10	G03		X11		J10	D11							
– LD Acc Out							G07	S07							
– LD SS Pty Err							Y29	Y29							

Figure BU411-1 (Part 4 of 9). 8130 Processor Instruction/Execution Unit Point-to-Point Signal Path

Signal Name	Card Locations														
	A-A1Q2	A-A1P2	A-A1N2	A-A1M2	A-A1L2	A-A1K2	A-A1J2	A-A1H2	A-A1F2	A-A1A2	A-A1E2	A-A1C2	A-A1B2	A-A1D2	A-A1G2
+ Load Dec			W08	W08		W08									
– Load FA Hi		Y03		Y03											
– Load FA Lo		Y23		Y23											
– Load FB Pulse		S03		S03											
+ Load Interrupt		Z30	Z30												
+ Load R1/R2	D07				G08										
– Load UCW Gate	D09	X13			X13	B10									
+ Logical Stor Installed						D13									
– Long Inst		P04				M09									
– Loop on ROS	X28														
– Low 3 Cnt = 0	Z11		Z11												
– Modifier	U07														
– Monitor		G10													
– N							W02	P10	W02						
Not Strg Prtk															
– NSE Pty							P07								
– Osc	J04			M02											
+ Osc	J05			M03											
+ Osc Out Ext				J07					X22						G02
– Parity Valid		U07													
– PC CP14	U12	G09			Y10	Y10	J09								
– PC Err		X07 J11			X07		J05	U04							
– PC I-F Dly Err		X05			X05										
– PC No Response						B07									
– PIC Bit 0		D12						B08							
+ PM 0						G04	Y30	Y30	M07						
+ PM 1						D07	D07	P02							
– Proc Stk Error		B10													
– Proc Stk PH Err		U05			G03										
– Proc Stk PL Err		U06			G04										
– Prog Loaded	W10	J06	W10												
– PSV		X06	X06												
– PSV 2 to Source (Gate)		Z27	Z27												
– PSV Switch Ext			S09												
– PSV Switch Gate	Z32		Z32												
– PSV Switch Req	Z24		Z24												
– PSV-1			U12												
– PSV-2			S12				J06	S12							
– PSV-A		X27	X27		X27										
– Pwr On Reset									Y28						M08
+ R-Reg Out 9							Y02	Y02							
+ R-Reg Out 10							Y03	Y03							
+ R-Reg Out 11							Y05	Y05							
+ R-Reg Out 12							Y06	Y06							
+ R-Reg Out 13							Y07	Y07							
+ R-Reg Out 14							Y08	Y08							
+ R-Reg Out 15							Y09	Y09							
+ R1 Bit 0	Z28	Z28	X29		X29										
+ R1 Bit 1	M13				G09										
– R1/R3 Bit 0					Y07	Y07									
– R1/R3 Bit 1					Y06	Y06									
– R1/R3 Bit 2					Y33	Y33									
– R1/R3 Bit 3					Y12	Y12									
+ R1/R3 Sp					Y05	Y05									
– R2 Bit 0					Y23	Y23									
– R2 Bit 1					Y09	Y09									
– R2 Bit 2					Y11	Y11									
– R2 Bit 3					Y32	Y32									
+ R2 Sp					Y25	Y25									
– R2 = 0		X09D10			X09										
– Range Check Jpr 1									Y29						M09
– Range Check Jpr 2									Z33						S13
– Range Check Jpr 4									Z13						U13
+ Rd Adr Inv		X23			X23										
– Regen Request	J11								X24						G04

Figure BU411-1 (Part 5 of 9). 8130 Processor Instruction/Execution Unit Point-to-Point Signal Path

Signal Name	Card Locations													
	A-A1Q2	A-A1P2	A-A1N2	A-A1M2	A-A1L2	A-A1K2	A-A1J2	A-A1H2	A-A1F2	A-A1A2	A-A1E2	A-A1C2	A-A1B2	A-A1D2	A-A1G2
– Register Select 00									G08	G08		G08	J13	J13	
– Register Select 01									J05	J07		J07	G05	G05	
– Register Select 10									J13	J13		J13	G08	G08	
– Register Select 11									G13	G05		G05	J07	J07	
– Reset C Reg		D05				B09									
– Reset Pic		P05			S08										
– Restart		G12			P10										
– Restart Latch	W08	W08													
– System Restart A							Z32		Z32						S12
– Restart To Proc															
– ROAR Bit 0	X05														
– ROAR Bit 1	X06														
– ROAR Bit 2	X07														
– ROAR Bit 3	X08														
– ROAR Bit 4	X09														
– ROAR Bit 5	X10														
– ROAR Bit 6	X11														
– ROAR Bit 7	X12														
– ROAR Bit 8	X13														
– ROAR Bit 9	X33	D10	B03												
– ROS Adder Ctrl 0	Y22			Y22											
– ROS Adder Ctrl 1	Y06			Y06											
– ROS Adder Ctrl 2	Y09			Y09											
– ROS Adder Ctrl 3	Y10			Y10											
– ROS Adder Ctrl 4	Y07			Y07											
– ROS Branch 0	X23														
– ROS Branch 1	X24														
– ROS Branch 2	X25														
– ROS Branch 3	X26														
– ROS Branch 4	X27														
– ROS Extension Reg	M07				D09										
– ROS Ctrl 0	D12						D12		D12						
– ROS Ctrl 1	D13						D11		D13						
– ROS Ctrl 2	G02						G02		G02						
– ROS Ctrl 3	G05						G05		G05						
– ROS Ctrl 4	G08						G08		G08						
– ROS Ctrl 5	G09						G09		G09						
– ROS Ctrl 6	G10								P05						
– ROS Ctrl 7	G12								P10						
– ROS Stor Adr 0	M03				S02										
– ROS Stor Adr 1	M04				S03										
– ROS Stor Adr 2	M05				U02										
– ROS Stor Ctrl 0	M08				M08										
– ROS Stor Ctrl 1	M09				J06										
– ROS Stor Ctrl 2	P07				J12										
– ROS Order 0	W12	W12													
– ROS Order 1	W13	W13													
– ROS Order 2	W22	W22													
– ROS Order 3	W23	W23													
– ROS PC Bit	W29	W29													
– ROS Pty Err	U11	U09													
– ROS Pty Err Lth	U13														
– ROS Source 0	W24	W24													
– ROS Source 1	W25	W25													
– ROS Source 2	W26	W26													
– ROS Source 3	W27	W27													
– R/V							W03	B10	W03						
– R/W Stor Err		M10							Y33						M13
– S							Y24	M13	Y24						
– S Adr Bus 0							P13		Y02						P02
– S Adr Bus 1							P12		Y30						M10
– S Adr Bus 2							M08		Y05						P05
– S Adr Bus 3							P06		Y06						P06
– S Adr Bus 4							M03		Y07						P07
– S Adr Bus 5									Y32						M12
– S Adr Bus 6									Y09						P09
– S Adr Bus 7									Y10						P10

Figure BU411-1 (Part 6 of 9). 8130 Processor Instruction/Execution Unit Point-to-Point Signal Path

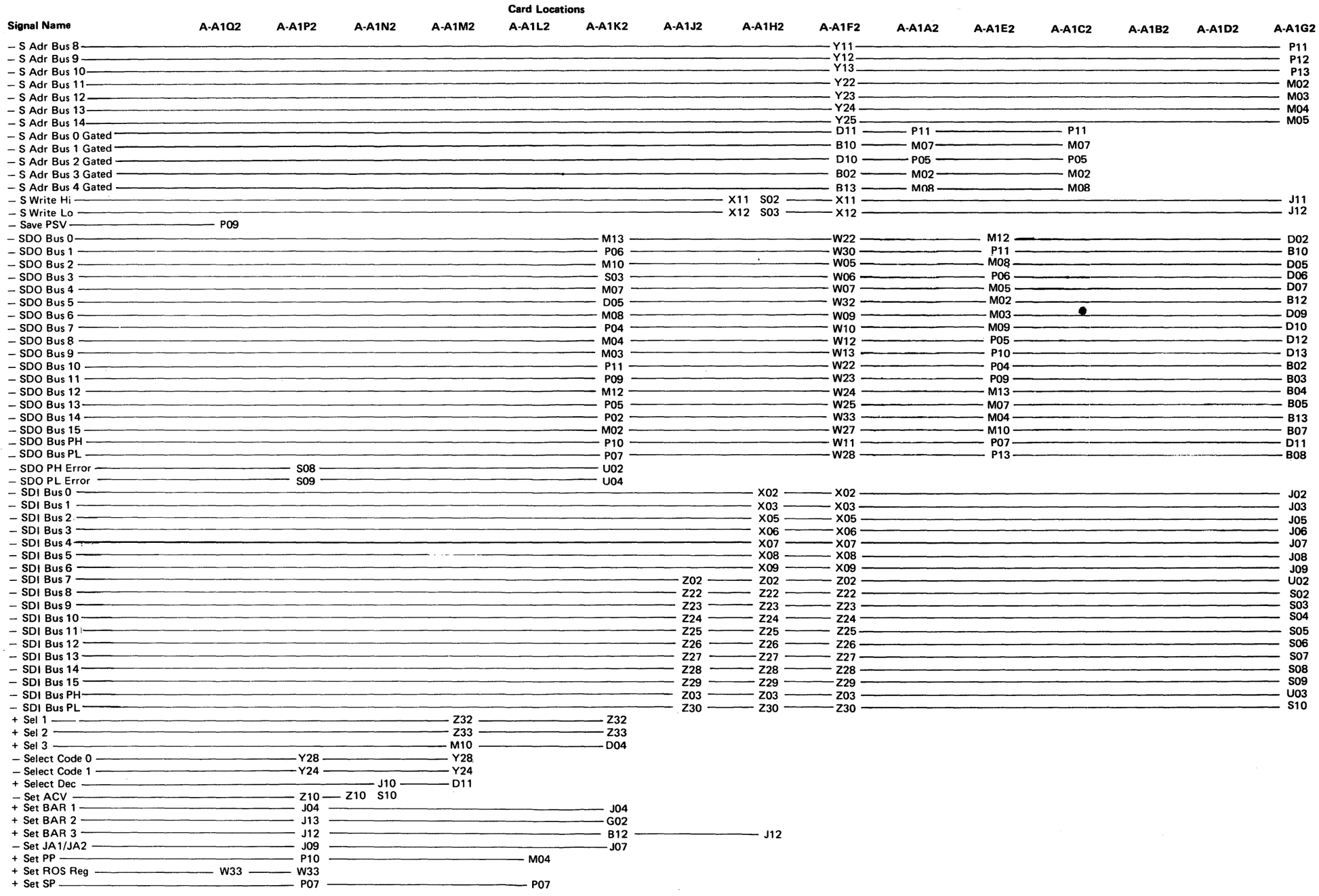

Figure BU411-1 (Part 7 of 9). 8130 Processor Instruction/Execution Unit Point-to-Point Signal Path

Signal Name	Card Locations														
	A-A1Q2	A-A1P2	A-A1N2	A-A1M2	A-A1L2	A-A1K2	A-A1J2	A-A1H2	A-A1F2	A-A1A2	A-A1E2	A-A1C2	A-A1B2	A-A1D2	A-A1G2
– Single Cycle	X29														
– Single Inst	X03														
– Source Bus 0			W13	W13 G07	W13	X02 W13	X02								
– Source Bus 1			W24	W24 G08	W24	X05 W24	X05								
– Source Bus 2			W11	W11 G09	W11	X06 W11	X06								
– Source Bus 3			W23	W23 G10	W23	X07 W23	X07								
– Source Bus 4			W05	W05 G12	W05	X08 W05	X08								
– Source Bus 5			W22	W22 G13	W22	X09 W22	X09								
– Source Bus 6			W33	W33 J04	W33	X10 W33	X10								
–Source Bus 7	S13		W29	W29 J06	W29	X11 W29	X11								
–Source Bus 8	B07	B07	W26	W26 B07	W26	X12 W26	X12								
–Source Bus 9	P05	B04	W09	W09 B04	W09	X13 W09	X13								
–Source Bus 10	B12	B12	W06	W06 B12	W06	X22 W06	X22								
–Source Bus 11	G03	G03	W12	W12 G03	W12	X23 W12	X23								
–Source Bus 12	D06	D06	W28	W28 D06	W28	X24 W28	X24								
–Source Bus 13	B10	G02	W03	W03 B10	W03	X25 W03	X25								
–Source Bus 14	U05	D07	W02	W02 D07	W02	X26 W02	X26								
–Source Bus 15	U06		W07	W07 G02	W07	X27 W07	X27								
–Source Bus PH					Y26	Y26 G12	G12								
–Source Bus PL					Y27	Y27 J13	J07								
–SS FRU							P09								
–SS Pty Err		B13					D13								
–SS Reset							P04								
–SS Sel							D04								
–SS Stk in 0							B12								
–SS Stk in 1							D05								
–SS Stk in 2							D09								
–SS Stk in 4							D10								
–SS Stk in PH							M12								
–SS Tst Clk							P02								
+SS Wrt Hi							J09								
+SS Wrt Lo							J11								
+SS Start Inst	M10	D13		J10	M07	J10									
–Start Inst	Z26		Z26												
–Step ACV		Y26	Y26												
–Step Cycle/Inst Off	X22														
–Step Cycle/Inst On	X30														
–Step Dec			J13	M08											
–Stk Adr Bus 6					P12		P12								
–Stk Adr Bus 7					M12		M12								
–Stk Adr Bus 8					P11		P11								
–Stk Adr Bus 9			G13		P13		P13								
–Stk Adr Bus 10					M13		M13								
–Stk Adr Bus 11			U13		M10		M10								
–Stk Adr Bus 12			U07		P04		P04								
–Stk Adr Bus 13			S03		M09		M09								
–Stk Adr Bus 14		X32		X32	B07		B07								
–Stk Adr Bus 15		X33			X33										
+Stk CSRL		X28		X28	X28										
–Stk RST					M08		S09								
–Stk Sel					Y30										
–Stop Ack	S02	S02		S02	Y03 B04	Y03	W33	W33 B04							
–Stop Clock	J10														
–Stop Clock 1					P05										
–Stop Request	P10														
– Stor Busy	J07						J12								
+ Stor Cntl Installed						B05									
– Stor Cntl Stk PH Err		J02					G03								
– Stor Cntl Stk PL Err		G04					G04								
– Stor Not Ready					D13										
– Stor Res (+ 5)							B03								
– Stor Reset					B13										
– Stor Select	J12	S10			D09		J04	S10	B13						

Figure BU411-1 (Part 8 of 9). 8130 Processor Instruction/Execution Unit Point-to-Point Signal Path

Card Locations

Signal Name	A-A1Q2	A-A1P2	A-A1N2	A-A1M2	A-A1L2	A-A1K2	A-A1J2	A-A1H2	A-A1F2	A-A1A2	A-A1E2	A-A1C2	A-A1B2	A-A1D2	A-A1G2
– Stor Sel (Gnd)							M04								
– Sys Ck Inh Stor		X22			X22										
– Sys Ck Not 0		J07			D02										
– Sys Ck Stop Delayed	J02	D02													
– Sys Reset		B08					Y12	B07	Y12						
– Sys Restart	W32	W32 M02					G13	J02							
– T0	G07	G08													
+ T0	S05				M05		M05	M05							
– T0 Delta	M02						M02	M03							
+ T0 Delta	W09	W09													
+ T1	S12	S12													
– T1	P12	M05		M05											
+ T1 Delta	S10	S04													
– T1 Delta	G04		M13	M13	P02										
+ T1 Delta M	S08						S03	S04							
+ T2	P11	P11	M05												
– T2	U09	G05		G05	G05	G05									
+ T2 Delta	U02	U02					U02	U02							
– T2 Delta	U04	U04	P04	J02	J02										
– T3	P13	M07		M07											
+ T3	S09	M08	S04												
+ T3 Delta	S03	P13		P09	P09										
– T3 Delta	B08	B09	G04	B09	B09		U12								
– Test 1									Y03						P03
– Test 2									W08						D08
+ Tie Up Stor Protect								B03 D03							
+ T.O. = 0		X08			X08										
– VB Latch	W28	W28													
– VB Tag		P12													
– VH Tag		U11			P06										
– Vol Release								U13							
– Volume Sel 0							Z05	Z05 U11	Z05						U05
– Volume Sel 1							Z06	Z06 U10	Z06						U06
– Volume Sel 2							Z07	Z07 U09	Z07						U07
– Volume Sel 3							Z08	Z08 U07	Z08						U08
– Volume Sel 4							Z09	Z09 U12	Z09						U09
– Volume Sel 5							Z10	Z10 P09	Z10						U10
– Volume Sel 6						Z11	J13		Z11						U11
– Volume Sel 7						Z12	P11		Z12						U12
+ Wait or PSV	P06	P06						M04							
– Wait State Gate	D02		M10												
Word SAR 0									P02	P02	P02	P02			
Word SAR 1									P10	P10	P10	P10			
Word SAR 2									M04	M04	M04	M04			
Word SAR 3									P12	P12	P12	P12			
Word SAR 4									M10	M10	M10	M10			
Word SAR 5									M12	M12	M12	M12			
Word SAR 6									P09	P09	P09	P09			
– Write Hi					B05			B05	X11						J11
– Write Low					D06			D06	X12						J12
– WSE Zero Chk							Y33	Y33							
– Xlate Table Adr Bit					B12			S08							
– Xlate Table Op							D06								
– Xlate Table Op Proc						D06									

Figure BU411-1 (Part 9 of 9). 8130 Processor Instruction/Execution Unit Point-to-Point Signal Path

BU412 8140 Processor Instruction/Execution Unit

Figure BU412-1 shows the interconnection of logic signals in the 8140 Processor Instruction/Execution unit. The signals are listed alphabetically by signal name. For further information, see BU420, BU450, and BU460.

			Card Locations								
	MODELS	BXX	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2	A1M2	A1N2	A1P2
Signal Name	MODELS	AXX	A1C2	A1D2	A1E2	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2
–0 Level/0 Mask				Z03	Z03						
+5V			J03 D03	J03 D03	J03 D03	J03 D03	J03 D03	J03 D03	J03 D03	J03 D03	J03 D03
–5V			G06 B06	G06 B06	G06 B06	G06 B06	G06 B06	G06 B06	G06 B06	G06 B06	G06 B06
+8.5V			G11 B11	G11 B11	G11 B11	G11 B11	G11 B11	G11 B11	G11 B11	G11 B11	G11 B11
+32K Stor											
–8140 Stor Err				M10							
–ACV Code 0					W32	W32		W32			
–ACV Code 1					W30	W30		W30			
–ACV Code 2					W10	W10		W10			
–ACV Code 3					W25	W25		W25			
–ACV KI (Gate)				Z22	Z22						
–ACV Last			Z09		Z09						
–Add 1			B03					D02			
–Address Tag				S13							
–Address Valid							J05			S13	
–Adr Bus 0						U09	Y28	Y28 U09			U09
–Adr Bus 1						S08	Y29	Y29 S08			S08
–Adr Bus 2						S13	S13	S13			S13
–Adr Bus 3						U10	U10	U10			U10
–Adr Bus 4						U05	U05	U05			U05
–Adr Bus 5						S12	S12	S12			S12
–Adr Bus 6						S04	S04	S04			S04
–Adr Bus 7						S05	S05	S05			S05
–Adr Bus 8						U07	U07	U07			U07
–Adr Bus 9						S09	S09	S09			S09
–Adr Bus 10						S10	S10	S10			S10
–Adr Bus 11						U12	U12	U12			B09
–Adr Bus 12						U13	U13	U13			U13
–Adr Bus 13						U11	U11	U11			U11
–Adr Bus 14						U06	U06	U06			U06
–Adr Bus 15				S07		S07	S07	S07			S07
–Adr Valid 0										P06	
–Adr Valid 1										P07	
–B										Y13	Y13
–BAR C0								Z26 M05		Z26	
–BAR to Source						P12		P12			
–BAR-1 Bit 0								X28			X28
–BAR-1 Bit 1								X29			X29
–BAR-1 Bit 2								X30			X30
–BAR-1 Bit 3								X32			X32
–BAR-1 Bit 4								X33			X33
–BAR-A				J06			Y13J13	Y13			
–Branch Taken			S07		S07						
–Byte			B04			B13		B13			
–Byte Tag				P02							
–C to ADC					P05	B08					
–C0				Y12	Y12	Y12					
–C0 High						J09				G13	
+C0 HW Latch			Y05			Y05					
–C1					P06	P06					
–Chk 5 0 or S/L			B13				D12				
–Cin					S08						
–CLA to Source (Gate)				Z13	Z13						
+Clear Channel			W02	W02							
–Cnt Not = 0			Z12		Z12						
–Cntl Sys Rst											
–Compare Inst				D04				B02			
+CHIO in Progress			W11	W11 S05						S05	S02

Figure BU412-1 (Part 1 of 8). 8140 Processor Instruction/Execution Unit Point-to-Point Signal Path

Card Locations

Signal Name	MODELS	BXX	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2	A1M2	A1N2	A1P2
	MODELS	AXX	A1C2	A1D2	A1E2	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2
–CHIO or PSV Sw Req			W03	W03							
–CHIO Req			Z08	Z08	Z08 U09						
–CHIO Request Latch			W30	W30							
–CHIO Request Tag					B13						
–Channel Grant				U12							
–Command Tag				U13							
–D									Y22	Y22	
–Data Not Valid			J07								
–Data Tag				P09							
–Dest Bus 0					J11	Z06 J11	Z06		Z06		
–Dest Bus 1					D04	Z07 D04	Z07		Z07		
–Dest Bus 2					B02	Z02 B02	Z02		Z02		
–Dest Bus 3					B03	Z03 B03	Z03		Z03		
–Dest Bus 4					D05	Z24 D05	Z24		Z24		
–Dest Bus 5					D02	Z10 D02	Z10		Z10		
–Dest Bus 6					B05	Z05 B05	Z05		Z05		
–Dest Bus 7					P02	Z28 P02	Z28		Z28		P02
–Dest Bus 8					M12	Z09 M12	Z09	Z09	Z09		M12
–Dest Bus 9					D13	Z13 D13	Z13	Z13	Z13		D13
–Dest Bus 10					P07	Z12 P07	Z12	Z12	Z12		P07
–Dest Bus 11					U02	Z11 U02	Z11	Z11	Z11		U02
–Dest Bus 12					J12	Z29 J12	Z29	Z29	Z29		J12
–Dest Bus 13					P10	Z30 P10	Z30	Z30	Z30		P10
–Dest Bus 14					P11	Z22 P11	Z22	Z22	Z22		P11
–Dest Bus 15			J09		J05	Z23 J05	Z23	Z23	Z23		J05
–Dest Bus PH					G12		G12		G12		G12
–Dest Bus PL					M02		M02		M02		M02
+ Dest Bus = 0			Y02		Y02	Y02					
–Dest Field 0 ROS			Y13		Y13	Y13					
–Dest Field 1 ROS			Y32		Y32	Y32					
–Dest Field 2 ROS			Y30		Y30	Y30					
–Dest Field 3 ROS			Y33		Y33	Y33					
–Dir/Ind Chaining			D11				D11				
–Div Ovf						D10	D05				
–Div/CLC			B09				D09				
–E									Y25	Y25	M09
–EOC Latch			W05	W05							
–EOC Tag				M12							
–ESA 1										B08	
–ESA 2										B05	
–ESA 3										B04	
–ESA 4										B03	
–ESA Stack Clock							D04				
–ESA Stk Op											
+ Exit				D11	P09			X03 D11	X03		
–Exit			W06	W06							
+ Exit Allow I-Fetch				X30			X30				
–Ext Reg Sel							B03		B03		
–Ext Stk Error				D09							
–Ext Stk Out Bus 0									W06	W06	W06
–Ext Stk Out Bus 1									W07	W07	W07
–Ext Stk Out Bus 2									W08	W08	W08
–Ext Stk Out Bus 3									W09	W09	
–Ext Stk Out Bus 4									W10	W10	W10
–Ext Stk Out Bus 5									W11	W11	
–Ext Stk Out Bus 6									W12	W12	
–Ext Stk Out Bus 7									W13	W13	
–Ext Stk Out Bus 8									W22	W22	
–Ext Stk Out Bus 9									W23	W23	
–Ext Stk Out Bus 10									W24	W24	
–Ext Stk Out Bus 11									W25	W25	
–Ext Stk Out Bus 12									W26	W26	
–Ext Stk Out Bus 13									W27	W27	
–Ext Stk Out Bus 14									W28	W28	
–Ext Stk Out Bus 15									W29	W29	
–Ext Stk Out Bus PH									W30	W30	W30
–Ext Stk Out Bus PL									W32	W32	

Figure BU412-1 (Part 2 of 8). 8140 Processor Instruction/Execution Unit Point-to-Point Signal Path

	Card Locations									
	MODELS	BXX	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2	A1M2	A1N2	A1P2
Signal Name	MODELS	AXX	A1C2	A1D2	A1E2	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2
–F0					U10						
–F1					U11						
–F2					S05						
–F3					B08						
–FA I/O				Y08	Y08						
–FA Logic 0 ROS			W07	W07							
–FA Logic 1 ROS			Y25	Y25		Y25					
–FB Logic 0			Y29	Y29		Y29					
–FB Logic 1			Y11	Y11		Y11					
–FB-A						U04	U04				
+ First Half			Z25	Z25	Z25						
+ Force Dec=15					D12	D12					
–Force PSV Swap				X02	X02						
–FP											B02
–FP Inst			D04			G04		B04			
–FP PC							G07				
–FP Req 0			G13								
–FP Req 1			S04								
–FPT02			J13								
–FPT02 Delta			U10								
–Gate Ext Stk to Source									Y10		Y10
–Gate I Field						M04		P13			
–Gate Initial Adr							J09		M08		
–Gate MOR HL				X12			X12				
–Gate MOR HW				X26			X26				
–Gate MS HL							Y02	Y02			
–Gate MS HW							Y22	Y22			
–Gate Pages to Source				X24			X24				
–Gate Pty Err									Y11		Y11
+ Gate Set ROS Output			Y27		Y27						
–Gate Stk HL							G10				G10
–Gate Stk HL or HW							Z08				Z08
–Gate Stk HW							J07				
Gnd			J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08	J08 D08
–Halt Tag Ext				B05				B08			
–I Fetch			X10 G07				X10				
–I Reg 4					U04			J11			
–I Reg 5					S02			G08			
–I Reg 6					M09			J12			
–I Reg 7					P13			G07			
–Imm Fd Bit 8							Z27 G10		Z27		
+ Inc/Dec						J13			J13		
–Inh Val/Wrt									Y32		Y32
–Inhibit CHIO Req				X03	X03						
–Initial Rel									Y26		Y26
–Interrupt K1				Z23	Z23						
–Interrupt Sys Reset				Z29	Z29						
+ Invalid Access Code							J11		B09		
–Invalid Alv							U09		J06		J02
–Invalid Op				G13				B03			
–Irp Tag				U10							
+ I-F NLI				X25			X25				
–I/O									Y23		Y23 P06
–I/O Bus 0					B07						
–I/O Bus 1					D06						
–I/O Bus 2					B10						
–I/O Bus 3					B09						
–I/O Bus 4					J04						
–I/O Bus 5					B04						
–I/O Bus 6					G08						
–I/O Bus 7					J07						
–I/O Bus 8					G02		G02				
–I/O Bus 9					J02						
–I/O Bus 10					B12						
–I/O Bus 11					J09						
–I/O Bus 12					D10						
–I/O Bus 13					D07						
–I/O Bus 14					D09						

Figure BU412-1 (Part 3 of 8). 8140 Processor Instruction/Execution Unit Point-to-Point Signal Path

		Card Locations								
	MODELS	BXX	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2	A1M2	A1N2	A1P2
Signal Name	MODELS	AXX	A1C2	A1D2	A1E2	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2
–I/O Bus 15				G05							
–I/O Bus PH				G09							
–I/O Bus PL				M03							
–I/O Data Out Gate				M04	D09						
–I/O Exception			Z06 M03	Z06							
–I/O PH Error			Z07	Z07							
–I/O Int Bus Bit 8				W27		W27					
–I/O PL Error			Z02	Z02							
–I/O Sample Interrupt			Z05	Z05							
–I/O Tag (Gate)			M04								
–I/O to Source Bus			Z33	Z33							
–Jump to Adder				D11			G03				
+ KI Inst			M09				B10				
+ Last Phase		D05	X11 J10	G03		X11		D11	J10		
–Ld Acc In									Z33	Z33	
–Ld Acc Out								S07	G07		
–Ld SS Pty Err								Y29		Y29	
+ Load Dec				W08	W08		W08				
–Load FA Hi			Y03		Y03						
–Load FA Lo			Y23		Y23						
–Load FB Pulse			S03		S03						
+ Load Interrupt			Z30	Z30							
+ Load R1/R2		D07				G08					
–Load UCW Gate		D09	X13			X13	B10				
+ Logical Stor Installed							D13				
–Long Inst			P04				M09				
–Loop on ROS		X28									
–Low 3 Cnt = 0		Z11		Z11							
–Modifier		U07									
–Monitor			G10								
–N								S08		S07	
–Not S/P									D09		
–Not SAB Bit 14						B07		B07			
Not Strg Pty											
–NSE Pty										M10	
–Osc		J04			M02						
+ Osc		J05			M03						
+ Osc Out Ext					J07						
–Parity Valid			U07								
–PC CP14		U12	G09			Y10	Y10 J09				
–PC Err		X07 J11				X07		U04	J05		
–PC I-F Dly Err			X05			X05					
–PC No Response							B07				
–PIC Bit 0			D12					B08			
+ PM 0							G04	Y30 M07		Y30	
+ PM 1							D07	P02		D07	
–Proc Stk Error			B10								
–Proc Stk PH Err			U05			G03					
–Proc Stk PL Err			U06			G04					
–Proc Stk Sel						Y24					
–Prog Loaded		W10 J06	W10								
–PSV 2 to Source (Gate)			Z27	Z27							
–PSV Switch Ext				S09							
–PSV Switch Gate		Z32		Z32							
–PSV Switch Req		Z24		Z24							
–PSV-1				U12							
–PSV-2				S12				S12	J06		
–PSV-A			X27	X27		X27					
+R-Reg Out 9								Y02		Y02	
+R-Reg Out 10								Y03		Y03	
+R-Reg Out 11								Y05		Y05	
+R-Reg Out 12								Y06		Y06	
+R-Reg Out 13								Y07		Y07	
+R-Reg Out 14								Y08		Y08	
+R-Reg Out 15								Y09		Y09	
+R1 Bit 0		Z28	Z28 X29			X29					
+R1 Bit 1		M13				G09					
–R1/R3 Bit 0						Y07	Y07				

Figure BU412-1 (Part 4 of 8). 8140 Processor Instruction/Execution Unit Point-to-Point Signal Path

Signal Name	MODELS	BXX AXX	Card Locations A1F2 A1C2	A1G2 A1D2	A1H2 A1E2	A1J2 A1F2	A1K2 A1G2	A1L2 A1H2	A1M2 A1J2	A1N2 A1K2	A1P2 A1L2
–R1/R3 Bit 1							Y06	Y06			
–R1/R3 Bit 2							Y33	Y33			
–R1/R3 Bit 3							Y12	Y12			
+R1/R3 Sp							Y05	Y05			
–R2 Bit 0							Y23	Y23			
–R2 Bit 1							Y09	Y09			
–R2 Bit 2							Y11	Y11			
–R2 Bit 3							Y32	Y32			
+R2 SP							Y25	Y25			
–R2 = 0				X09 D10			X09				
+RD Adr Inv				X23			X23				
–RD Stk											
–Refresh Allow			J11								
–Reset C Reg				D05				B09			
–Reset PIC				P05			S08				
–Restart				G12			P10		P09	G13	P09
–Restart Latch			W08	W08							
–ROAR Bit 0			X05								
–ROAR Bit 1			X06								
–ROAR Bit 2			X07								
–ROAR Bit 3			X08								
–ROAR Bit 4			X09								
–ROAR Bit 5			X10								
–ROAR Bit 6			X11								
–ROAR Bit 7			X12								
–ROAR Bit 8			X13								
–ROAR Bit 9			X33 D10	B03							
–ROS Adder Ctrl 0			Y22			Y22					
–ROS Adder Ctrl 1			Y06			Y06					
–ROS Adder Ctrl 2			Y09			Y09					
–ROS Adder Ctrl 3			Y10			Y10					
–ROS Adder Ctrl 4			Y07			Y07					
–ROS Branch 0			X23								
–ROS Branch 1			X24								
–ROS Branch 2			X25								
–ROS Branch 3			X26								
–ROS Branch 4			X27								
–ROS Extension Reg			M07				D09				
–ROS Inh Upd Bar 3			M12								
–ROS Ctrl 0			D12					D12			D12
–ROS Ctrl 1			D13					D13			D11
–ROS Ctrl 2			G02					G02			G02
–ROS Ctrl 3			G05					G05			G05
–ROS Ctrl 4			G08					G08			G08
–ROS Ctrl 5			G09					G09			G09
–ROS Ctrl 6			G10					P05			
–ROS Ctrl 7			G12					P10			
–ROS STOR Adr 0			M03				S02				
–ROS STOR Adr 1			M04				S03				
–ROS STOR Adr 2			M05				U02				
–ROS STOR Ctrl 0			M08				M08				
–ROS STOR Ctrl 1			M09				J06				
–ROS STOR Ctrl 2			P07				J12				
–ROS Order 0			W12	W12							
–ROS Order 1			W13	W13							
–ROS Order 2			W22	W22							
–ROS Order 3			W23	W23							
–ROS PC Bit			W29	W29							
–ROS Pty Err			U11	U09							
–ROS Pty Err Ltch			U13								
–ROS Source 0			W24	W24							
–ROS Source 1			W25	W25							
–ROS Source 2			W26	W26							
–ROS Source 3			W27	W27							
–ROS Spare 1			X32								
–R/V								W03	W03 B10		
–S								Y24			Y24 M08

Figure BU412-1 (Part 5 of 8). 8140 Processor Instruction/Execution Unit Point-to-Point Signal Path

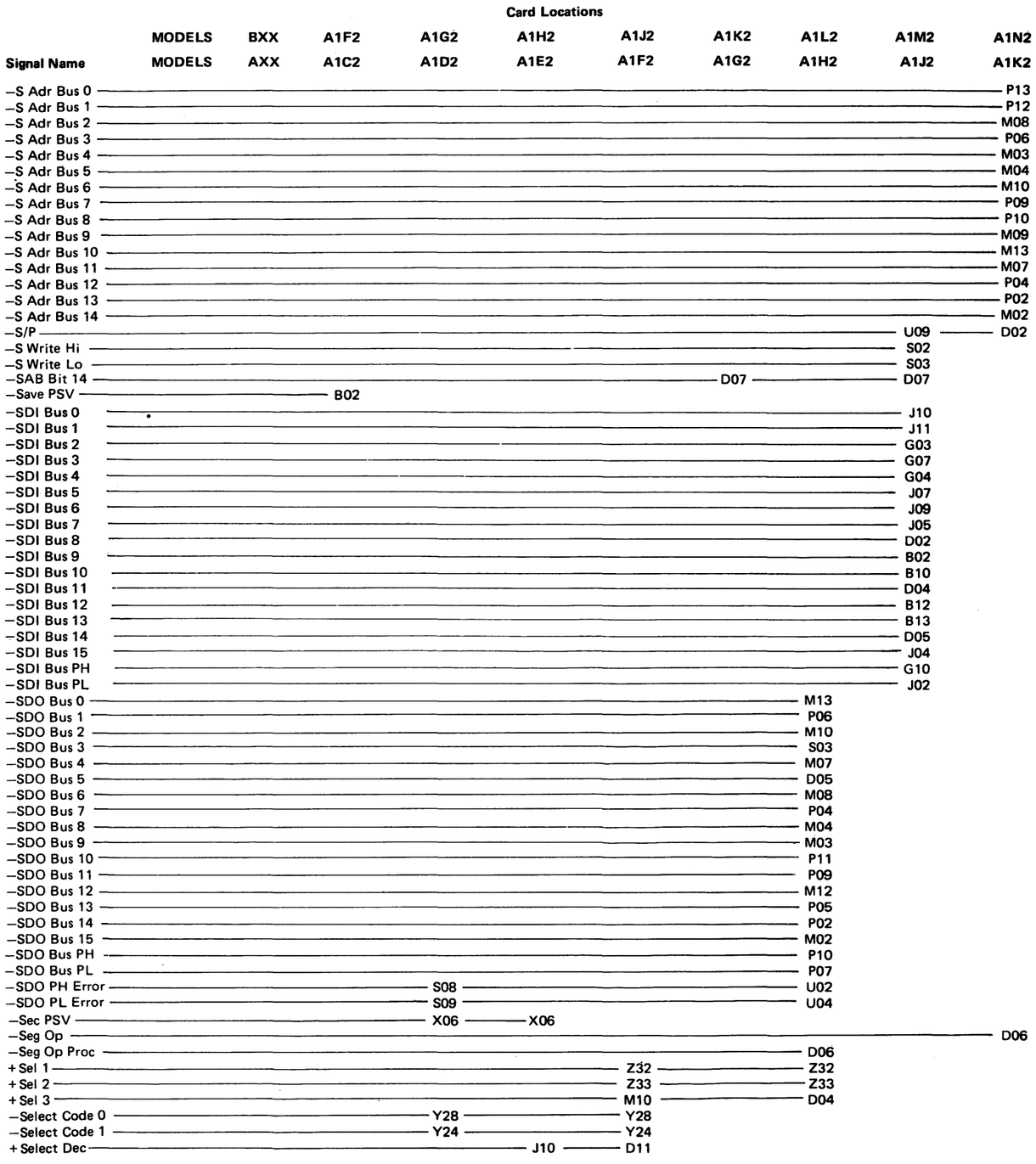

Figure BU412-1 (Part 6 of 8). 8140 Processor Instruction/Execution Unit Point-to-Point Signal Path

			Card Locations								
	MODELS	BXX	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2	A1M2	A1N2	A1P2
Signal Name	MODELS	AXX	A1C2	A1D2	A1E2	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2
–Set ACV				Z10	Z10 S10						
+Set BAR 1				J04				J04			
+Set BAR 2				J13				G02			
+Set BAR 3				J12				B12	J12		
–Set JA1/JA2				J09				J07			
+Set PP				P10			M04				
+Set ROS Reg			W33	W33							
+Set SP				P07			P07				
–Single Cycle			X29								
–Single Inst			P04								
–Source Bus 0					W13	W13 G07	W13	X02 W13			X02
–Source Bus 1					W24	W24 G08	W24	X05 W24			X05
–Source Bus 2					W11	W11 G09	W11	X06 W11			X06
–Source Bus 3					W23	W23 G10	W23	X07 W23			X07
–Source Bus 4					W05	W05 G12	W05	X08 W05			X08
–Source Bus 5					W22	W22 G13	W22	X09 W22			X09
–Source Bus 6					W33	W33 J04	W33	X10 W33			X10
–Source Bus 7			S13		W29	W29 J06	W29	X11 W29			X11
–Source Bus 8			B07	B07	W26	W26 B07	W26	X12 W26			X12
–Source Bus 9			P05	B04	W09	W09 B04	W09	X13 W09			X13
–Source Bus 10			B12	B12	W06	W06 B12	W06	X22 W06			X22
–Source Bus 11			G03	G03	W12	W12 G03	W12	X23 W12			X23
–Source Bus 12			D06	D06	W28	W28 D06	W28	X24 W28			X24
–Source Bus 13			B10	G02	W03	W03 B10	W03	X25 W03			X25
–Source Bus 14			U05	D07	W02	W02 D07	W02	X26 W02			X26
–Source Bus 15			U06		W07	W07 G02	W07	X27 W07			X27
–Source Bus Hi Byte Pty							Y26	Y26 G12			G12
–Source Bus Low Byte Pty							Y27	Y27 J13			J07
–SS Clk 1									Y27		Y27
–SS Clk 2									Y28		Y28
–SS FRU											M07
–SS Pty Err				B13						D13	M05
–SS Pty Err Lth										M12	P12
–SS Sel										D05	D05
–SS Stk in 0											B04
–SS Stk in 1											B07
–SS Stk in 2											B08
–SS Stk in 4											B10
–SS Stk in Pty Hi											B09
–SS Tst Clk									U07		
–SS Wrt 1									U10		B05
–SS Wrt 2									U11		B13
–Stack Clock 1							Y30				
–Stack Clock 2							Z25		Z25		
+Start Inst			M10	D13		J10	M07	J10			
–Start Inst			Z26	Z26							
+STCL Installed							M03	B05			
–STCL Stk PH Err				J02							G03
–STCL Stk PL Err				G04							G04
–Step ACV				Y26	Y26						
–Step Cycle/Inst Off			P02								
–Step Cycle/Inst On			P09								
–Step Dec					J13	M08					
–Stk Adr Bus 6							P12		P12		
–Stk Adr Bus 7							M12		M12		
–Stk Adr Bus 8							P11		P11		
–Stk Adr Bus 9					G13		P13		P13		
–Stk Adr Bus 10							M13		M13		
–Stk Adr Bus 11					U13		M10		M10		
–Stk Adr Bus 12					U07		P04		P04		
–Stk Adr Bus 13					S03		M09		M09		
–Stk Adr Bus 14				X32			X32				
–Stk Adr Bus 15				X33			X33				
+Stk CSRL				X28		X28		X28			
–Stop ACK			S02	S02		S02	Y03	B04 Y03	W33	B04 W33	W33
–Stop Clock			J10				P05				
–Stop Request			P10								

Figure BU412-1 (Part 7 of 8). 8140 Processor Instruction/Execution Unit Point-to-Point Signal Path

			Card Locations								
	MODELS	BXX	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2	A1M2	A1N2	A1P2
Signal Name	MODELS	AXX	A1C2	A1D2	A1E2	A1F2	A1G2	A1H2	A1J2	A1K2	A1L2
–Stor Not Ready							D13				
–Stor Reset							B13				B13
–Stor Select				S10			J04		S10		J04
–Stor Sel 0											J09
–Stor Sel 1											J11
–Stor Sel 2											J12
–Stor Sel 3											J13
–Stor Sel 4											P05
–Stor Sel 5											P07
–Stor Sel 6											U04
–Stor Sel 7											P11
–Sys Ck Inh Stor				X22			X22				
–Sys Ck Not 0				J07			D02				
–Sys Ck Stop Delayed			J02	D02							
–Sys Reset				B08					Y12	Y12	B07
–Sys Restart			W32	W32 M02							
–T0			G07	G08							
+T0			S05				M05		M05		M05
–T0 Delta			M02						M03		
+T0 Delta			W09	W09							
+T1			S12	S12							
–T1			P12	M05		M05					
+T1 Delta			S10	S04							
–T1 Delta			G04		M13	M13	P02				
+T1 Delta M			S08						S04		S03
+T2			P11	P11	M05						
–T2			U09	G05		G05	G05	G05			
+T2 Delta			U02	U02					U02		U02
–T2 Delta			U04	U04	P04	J02	J02	J02			
–T3			P13	M07		M07					
+T3			S09	M08	S04						
+T3 Delta			S03	P13			P09				
–T3 Delta			B08	B09	G04	B09	B09		U12		U12
–Test (+5V)			X02								
+T.O. = 0				X08			X08				
–TTE 7									Z22	Z22	P05
–TTE 8									Z23	Z23	P13
–TTE 9									Z24	Z24	S04
–TTE 10									Z25	Z25	S05
–TTE 11									Z26	Z26	P04
–TTE 12									Z27	Z27	S08
–TTE 13									Z28	Z28	S09
–TTE 14									Z29	Z29	S10
–TTE 15									Z30	Z30	S12
–TTE PH									W05	W05	M13
–TTE PL									W02	W02	S13
–TTEA 0									Z02		Z02
–TTEA 1									Z03		Z03
–TTEA 2									Z05		Z05
–TTEA 3									Z06		Z06
–TTEA 4									Z07		Z07
–TTEA 5									Z08		Z08
–TTEA 6									Z09		Z09
–TTEA 7									Z10		Z10
–TTEA 8									Z11		Z11
–TTEA 9									Z12		Z12
–TTEA 10									Z13		Z13
–VB Latch			W28	W28							
–VB Tag				P12							
–VH Tag				U11			P06				
–Vol Release									U13		
+Wait or PSV			P06	P06					M04		
–Wait State Gate			D02		M10						
–Write Hi							B05		B05		
–Write Low							D06		D06		
–WSE Zero Chk									Y33		Y33
–Xlate Table Stk Sel							D10		D10		

Figure BU412-1 (Part 8 of 8). 8140 Processor Instruction/Execution Unit Point-to-Point Signal Path

BU413 8130 Signal Path: Processor, SC1, and BOP Adapter Cards

Figure BU413-1 shows the logic signal interconnection between the 8130 Processor instruction/execution unit and the SC1 card and BOP adapter card.

	A1 BOARD		A2 BOARD		
Signal Name	**Proc**	**Crossover Cable**	**Crossover Cable**	**SC1**	**BOP Cable**
– Save PSV	Q2P09	C6D02	C1D11	G2D12	
– Address Tag	P2S13	F6C04	F1C13	G2G10	
– Command Tag	P2U13	F6C02	F1C11	G2J10	
– Data Tag	P2P09	D6E04	D1E13	G2G02	
– Byte Tag	P2P02	F6D02	F1D11	G2J11	
– Halt Tag	P2B05	F6B02	F1B11	G2J09	
– I/O Tag	P2M04	E6C02	E1C11	G2J05	
– Wait State	N2M10	E6E04	E1E13	G2G07	
– Channel Grant	P2U12	F6E02	F1E11	G2J12	
– Proc Stk Err	P2B10	F6A04	F1A13		A5D12
– System Check Not 0	P2J07	G6A04	G1A13		A5B09
– Dest Bus 12	M2J12	H6A04	H1A13	G2M02	
– Dest Bus 13	M2P10	H6A02	H1A11	G2P02	
– Dest Bus 14	M2P11	H6B04	H1B13	G2M03	
– Dest Bus 15	M2J05	H6C04	H1C13	G2M04	
+ PM 0	H2M07	H6D02	H1D11	G2P05	
– Monitor	P2G10	H6E02	H1E11	G2P06	
+ 50/60 Hz	P6C02	J6E02	J1E11	G2P11	
+ 60 Hz Control	P6B05	J6D02	J1D11	G2P10	
+ VE (–POR)	S6D02	J6A04	J1A13	H2M02	
+ Osc Out Ext	M2J07	K6B04	K1B13	G2U02	
– Valid Byte 0		F6E04	F1E13	G2G12	
– Valid Byte 1	P1P12	E6E02	E1E11	G2J07	
– Valid HW	L2P06/P2U11	E6D02	E1D11	G2J06	
– Par Valid	P2U07	E6C04	E1C13	G2G05	
– IRR	P2U10	F6B04	F1B13	G2G09	
– Exception	P2M03	E6A04	E1A13	G2G03	
– Modifier	Q2U07	E6B04	E1B13	G2G04	
– CH IO Request Tag	N2B13	G6A02	G1A11	G2J13	
– EOC	P2M12	E6B02	E1B11	G2J04	
– Restart	L2P10/P2G12	H6C02	H1C11	G2P04	
– System Reset	J2B07/P2B08	J6A02	J1A11	G2U04	C6A02
– Pwr Off to Pwr Supply	S6C05	J6D04	J1D13	G2U12	
+ RAM Accessible	G2G05	J6C04	J1C13	G2M09	
– ROS Pty Err Latch	Q2U13	H6D04	H1D13		A5D11
– SS FRU	J2P09	J6B04	J1B13		A5D09
– PIC Bit 0	H2B08/P2D12	J6C02	J1C11		A5B11
– Ext Stk Error	P2D09	K6A04	K1A13		A5D10
– Data 0, 0	N2B07	A6D04	A1D13	G2B02	
0, 1	N2D06	B6E04	B1E13	G2B08	
0, 2	N2B10	C6C02	C1C11	G2D11	
0, 3	N2B09	B6A04	B1A13	G2B04	
0, 4	N2J04	B6A02	B1A11	G2D04	
0, 5	N2B04	B6B04	B1B13	G2B05	
0, 6	N2G08	B6D02	B1D11	G2D07	
0, 7	N2J07	B6C02	B1C11	G2D06	
0, P	N2G09	B6D04	B1D13	G2B07	

	A1 BOARD		A2 BOARD		
Signal Name	**Proc**	**Crossover Cable**	**Crossover Cable**	**SC1**	**BOP Cable**
– Data 1, 0	L2G02/N2G02	B6B02	B1B11	G2D05	
1, 1	N2J02	C6B04	C1B13	G2B10	
1, 2	N2B12	C6E02	C1E11	G2D13	
1, 3	N2J09	C6A02	C1A11	G2D09	
1, 4	N2D10	C6A04	C1A13	G2B09	
1, 5	N2D07	C6B02	C1B11	G2D10	
1, 6	N2D09	A6E04	A1E13	G2B03	
1, 7	N2G05	C6D04	C1D13	G2B12	
1, P	N2M03	C6E04	C1E13	G2B13	
– PB Reset Req				G2S04	C6B02
– BOP Interrupt Request				G2P12	A5D06
– SDC Selected				G2P07	A5B10
– IO OP				G2S03	B6A02
– Wait State Out				G2G13	A5B12
– BOP Adapter Check				G2P09	A5D03
– BOP Check				G2M10	A5D04
– SDC Halt				G2M08	A5D07
– SDC Sync (100 NS)				G2U13	B6C02
– SDC Bus 0				G2U09	A6E04
– SDC Bus 1				G2S09	B6A04
– SDC Bus 2				G2S05	B6B04
– SDC Bus 3				G2U07	B6C04
– SDC Bus 4				G2S08	B6E04
– SDC Bus 5				G2S10	C6A04
– SDC Bus 6				U06	C6B04
– SDC Bus 7				U05	C6C04
– SDC Bus P				S12	C6D04
– 1 m-Hz				M05	B6B02
+ 500 ms				P13	A6E02
+ 1.024 ms				M13	A6D02
– Interlock					A5B02
					A5B13
					A6D04
					C6E04
Ground					B6D04
					B6E02
					A5B07
					A5D08

Figure BU413-1. 8130 Logic Signals Between the Processor, SC1 and BOP Adapter Cards

BU414 8140 Models A3X, A4X, and A5X Signal Path: SC1, Storage, EFP, and Floating–Point Cards

Figure BU414-1 shows the logic signal interconnection between the 8140 Models A3X, A4X, and A5X Processor I/E Unit and the SC1, EFP (feature only), floating-point (A4X only), and processor storage cards.

	A1 BOARD						A2 BOARD	
Signal Name	**Proc**	**Stor***	**SC1**	**FP**	**EFP****	**Conn**	**Conn**	**Stor***
– I/O Bus 0	E2B07		A2B02					
– I/O Bus 1	E2D06		A2B08					
– I/O Bus 2	E2B10		A2D11					
– I/O Bus 3	E2B09		A2B04					
– I/O Bus 4	E2J04		A2D04					
– I/O Bus 5	E2B04		A2B05					
– I/O Bus 6	E2G08		A2D07					
– I/O Bus 7	E2J07		A2D06					
– I/O Bus PH	E2G09		A2B07					
– I/O Bus 8	G2G02		A2D05					
	E2G02							
–I/O Bus 9	E2J02		A2B10					
– I/O Bus 10	E2B12		A2D13					
– I/O Bus 11	E2J09		A2D09					
			A2J02					
– I/O Bus 12	E2D10		A2B09					
– I/O Bus 13	E2D07		A2D10					
– I/O Bus 14	E2D09		A2B03					
– I/O Bus 15	E2G05		A2B12					
– I/O Bus PL	E2M03		A2B13					
– Address Tag	D2S13		A2G10					
– Command Tag	D2U13		A2J10					
– Data Tag	D2P09		A2G02					
– I/O Tag	D2M04		A2J05					
– Interrupt Tag	D2U10		A2G09					
– Byte Tag	D2P02		A2J11					
– Halt Tag Ext	D2B05		A2J09					
	H2B08							
– Valid Byte 1	D2P12		A2J07					
			A2P07					
– Valid Halfword	D2U11		A2J06					
	G2P06							
– Parity Valid	D2U07		A2G05					
– Monitor	D2G10		A2P06					
– End of Chain Tag	D2M12		A2J04					
– I/O Exception	D2M03		A2G03					
– CHIO Request Tag	E2B13		A2J13					
– Channel Grant	D2U12		A2J12					
– Wait State Gate	C2D02		A2G07		XXD02			
	E2M10							
– SAB Bit 14	C2B02		A2D12					
– Restart	K2G13			A2P04				
	L2P09							
	J2P09							
	G2P10							
	D2G12							
– Modifier	C2U07		A2G04					
– Oscillator Out Ext	F2J07		A2U02					
+ PM 0	J2M07		A2P05	M2G04	XXD09			
	H2G04							
– System Reset	K2B07		A2U04	M2B07	XXG08	C1A11		
	D2B08							
– Wait State Out			A2G13			F1E13		
– EFP Interrupt Request			A2S07		XXD04			
– SDC Bus 0			A2U09		XXU09	A1E13		
– SDC Bus 1			A2S09		XXS09	B1A13		
– SDC Bus 2			A2S05		XXU10	B1B13		
– SDC Bus 3			A2U07		XXB02	B1C13		
– SDC Bus 4			A2S08		XXB03	B1E13		
– SDC Bus 5			A2S10		XXB04	C1A13		
– SDC Bus 6			A2U06		XXB05	C1B13		
– SDC Bus 7			A2U05		XXB07	C1C13		
– SDC Bus P			A2S12		XXB08	C1D13		
– SDC Selected			A2P07		XXS12	F1C13		
– SDC Sync			A2U13		XXM05	B1C11		
– SDC Halt			A2M08		XXS04	E1E11		
– I/O Operation			A2S03		XXD06	B1A11		
– 1-MHz Oscillator			A2M05		XXU04	B1B11		
					XXS05			
– 500 ms Rate			A2M12		XXU07	A1E11		
			A2P13					
– 1.024 ms Rate			A2M13		XXS07	A1D11		
			A2S02					
– Pushbutton Reset Req			A2S04			C1B11		
– BOP Interrupt Request			A2P12			E1D11		
– BOP Adapter Check			A2P09			E1A11		
– BOP Check			A2M10			E1B11		
– System Check Not 0	D2J07				XXJ07	F1B13		
	G2D02							
– SS FRU	L2M07					F1B11		
– Ext Stk Error	D2D09					F1C11		
– ROS Pty Error Lth	C2U13					F1D11		
– Proc Stk Error	D2B10					F1E11		
– PIC Bit 0	J2B08				XXD12			
	D2D12							
+ PM 1	K2D07				XXD07			
	J2P02							
	H2D07							
– R/V	K2B10				XXB10			
– ROS Control 1	K2D11				XXD13			
	J2D13							
	C2D13							
+ T2	E2M05				XXJ06			
	D2P11							
	C2P11							
– I Fetch	D2G07			M2G08	XXG07			
+ Exit	H2D11				XXD05			
	E2P09							
	D2D11							
– Long Instruction	H2M09				XXG09			
	D2P04							
– PSV Switch Ext	E2S09				XXD10			
– Stack Address Bus 9	J2P13				XXM12			
	G2P13							
	E2G13							
– Stack Address Bus 11	J2M10			M2J10	XXP11			
	G2M10							
	E2U13							
– Stack Address Bus 12	J2P04			M2G02	XXP05			
	G2P04							
	E2U07							
– Stack Address Bus 13	J2M09			M2G05	XXP07			
	G2M09							
	E2S03							

*See BU111 for card locations. **See SP111 for card locations.

Figure BU414-1 (Part 1 of 3). 8140 Model A3X, A4X, and A5X Logic Signals Between the Processor, Storage, SC1, Floating Point, and EFP Cards.

Signal Name	A1 BOARD						A2 BOARD	
	Proc	Stor*	SC1	FP	EFP**	Conn	Conn	Stor*
– PSV 2	K2J06 J2S12 E2S12			M2J06	XXU02			
– Stor Adr Bus 0								
Model A3X	K2P13	P2U13 Q2S12 R2U13 S2S12 T2U13 U2S12 V2U13			M2P13	Q6A04	R1E13	V2S12 U2U13 T2S12 S2U13 R2S12
Model A4X	K2P13	R2U13 S2S12 T2U13 U2S12 V2U13			P2P13	Q6A04	R1E13	V2S12 U2U13 T2S12 S2U13 R2S12
Model A5X	K2P13	N2U13 P2S12 Q2U13 R2S12 S2U13 T2S12 U2U13 V2S12				Q6A04	R1E13	V2U13 U2S12 T2U13 S2S12 R2U13 Q2S12 P2U13 N2S12
– Stor Adr Bus 1	K2P12	XXU12			XXP12	Q6B04	R1D13	XXU12
– Stor Adr Bus 2	K2M08	XXS07			XXM08	Q6C04	R1C13	XXS07
– Stor Adr Bus 3	K2P06	XXU05			XXP06	Q6D04	R1B13	XXU05
– Stor Adr Bus 4	K2M03	XXS03			XXM03	R6A04	Q1E13	XXS03
– Stor Adr Bus 5	K2M04	XXS04			XXM04	R6B04	Q1D13	XXS04
– Stor Adr Bus 6	K2M10	XXS09			XXM10	R6C04	Q1C13	XXS09
– Stor Adr Bus 7	K2P09	XXU09			XXP09	R6D04	Q1B13	XXU09
– Stor Adr Bus 8	K2P10	XXU10			XXP10	R6E04	Q1A13	XXU10
– Stor Adr Bus 9	K2M09	XXS08			XXM09	Q6A02	R1E11	XXS08
– Stor Adr Bus 10	K2M13	XXS10			XXM13	P6E04	S1A13	XXS10
– Stor Adr Bus 11	K2M07	XXS05			XXM07	Q6B02	R1D11	XXS05
– Stor Adr Bus 12	K2P04	XXU04			XXP04	Q6C02	R1C11	XXU04
– Stor Adr Bus 13	K2P02	XXU02			XXP02	Q6D02	R1B11	XXU02
– Stor Adr Bus 14	K2M02	XXS02			XXM02	R6B02	Q1D11	XXS02
– Stor Select	J2S02	XXB13			XXS02	R6D02	Q1B11	XXB13
– Stor Write Lo	J2S03	XXD13			XXS03	R6C02	Q1C11	XXD13
– Stor Select 0					M2J09			
Model A3X	K2J09	P2U11 Q2U11						
Model A4X	K2J09	R2U11 S2U11			P2J09			
Model A5X	K2J09	N2U11 P2U11						
– Stor Select 1								
Model A3X	K2J11	R2U11 S2U11			M2J11			
Model A4X	K2J11	T2U11 U2U11			P2J11			
Model A5X	K2J11	Q2U11 R2U11						

*See BU111 for card locations. **See SP111 for card locations.

Figure BU414-1 (Part 2 of 3). 8140 Model A3X, A4X, and A5X Logic Signals Between the Processor, Storage, SC1, Floating Point, and EFP Cards.

Signal Name	A1 BOARD						A2 BOARD	
	Proc	Stor*	SC1	FP	EFP**	Conn	Conn	Stor*
– Stor Select 2								
Model A3X	K2J12	T2U12 U2U11			M2J12			
Model A4X	K2J12	V2U11			P2J12	L6D04	N1E13	V2U11
Model A5X	K2J12	S2U11 T2U11						
– Stor Select 3								
Model A3X	K2J13	V2U11			M2J13	N6E02	L1D11	V2U11
Model A4X	K2J13				P2J13	N6E02	L1D11	U2U11 T2U11
Model A5X	K2J13	U2U11 V2U11						
– Stor Select 4								
Model A3X (f)	K2P05				M2G12	M6E04	M1D13	U2U11 T2U11
Model A4X	K2P05				P2G12	M6E04	M1D13	S2U11 R2U11
Model A5X	K2P05					M6E04	M1D13	V2U11 U2U11
– Stor Select 5								
Model A3X (f)	K2P07				M2G10	L6D04	N1E13	S2U11 R2U11
Model A5X	K2P07					L6D04	N1E13	T2U11 S2U11
– Stor Select 6								
Model A5X	K2U04					N6E02	L1D11	R2U11 Q2U11
– Stor Select 7								
Model A5X	K2P11					T6A04	V1B13	P2U11 N2U11
– Stor Reset	G2B13 K2B13	XXP12				N6D02	L1E11	XXP12
– SDI Bus 0	J2J10	XXD11				T6C04	U1E13	XXD11
– SDI Bus 1	J2J11	XXD12				T6D04	U1D13	XXD12
– SDI Bus 2	J2G03	XXB07				T6E04	U1C13	XXB07
– SDI Bus 3	J2G07	XXB09				U6B04	U1A13	XXB09
– SDI Bus 4	J2G04	XXB08				U6C04	T1E13	XXB08
– SDI Bus 5	J2J07	XXD09				U6D04	T1D13	XXD09
– SDI Bus 6	J2J09	XXD10				U6E04	T1C13	XXD10
– SDI Bus 7	J2J05	XXB10				V6A04	T1B13	XXB10
– SDI Bus PH	J2G10	XXB12				T6B04	V1A13	XXB12
– SDI Bus 8	J2D02	XXD02				V6A02	T1B11	XXD02
– SDI Bus 9	J2B02	XXB02				T6B02	V1A11	XXB02
– SDI Bus 10	J2B10	XXB03				T6C02	U1E11	XXB03
– SDI Bus 11	J2D04	XXD04				T6D02	U1D11	XXD04
– SDI Bus 12	J2B12	XXB04				T6E02	U1C11	XXB04
– SDI Bus 13	J2B13	XXB05				V6B02	T1A11	XXB05
– SDI Bus 14	J2D05	XXD05				U6C02	T1E11	XXD05
– SDI Bus 15	J2J04	XXD07				U6D02	T1D11	XXD07
– SDI Bus PL	J2J02	XXD06				U6E02	T1C11	XXD06

(F) = Feature

Signal Name	A1 BOARD						A2 BOARD	
	Proc	Stor*	SC1	FP	EFP**	Conn	Conn	Stor*
– Addr Valid 0								
Model A3X	J2P06	P2P02						
		Q2P02						
		R2P02						
		S2P02						
		T2P02						
		U2P02						
Model A4X	J2P06	R2P02						
		S2P02						
		T2P02						
		U2P02						
Model A5X	J2P06	XXP02						
– Addr Valid 1								
Model A3X, A4X	J2P07	V2P02				S6A02	P1E11	XXP02
Model A5X	J2P07					S6A02	P1E11	XXP02
– SDO Bus 0	H2M13	XXM12		M2M13		L6E04	N1D13	XXM12
– SDO Bus 1	H2P06	XXP11		M2P06		M6A04	N1C13	XXP11
– SDO Bus 2	H2M10	XXM08		M2M10		M6B04	N1B13	XXM08
– SDO Bus 3	H2S03	XXP06		M2S03		M6C04	N1A13	XXP06
– SDO Bus 4	H2M07	XXM05		M2M05		M6D04	M1E13	XXM05
– SDO Bus 5	H2D05	XXM02		M2D05		N6A04	M1C13	XXM02
– SDO Bus 6	H2M08	XXM03		M2M08		N6B04	M1B13	XXM03
– SDO Bus 7	H2P04	XXM09		M2P04		N6C04	M1A13	XXM09
– SDO Bus PH	H2P10	XXP07		M2J07		N6D04	L1E13	XXP07
– SDO Bus 8	H2M04	XXP05		M2M04		N6E04	L1D13	XXP05
– SDO Bus 9	H2M03	XXP10		M2M03		L6E02	N1D11	XXP10
– SDO Bus 10	H2P11	XXP04		M2P05		M6A02	N1C11	XXP04
– SDO Bus 11	H2P09	XXP09		M2P09		M6B02	N1B11	XXP09
– SDO Bus 12	H2M12	XXM13		M2G10		M6C02	N1A11	XXM13
– SDO Bus 13	H2P05	XXM07		M2M07		L6D02	N1E11	XXM07
– SDO Bus 14	H2P02	XXM04		M2B12		N6A02	M1C11	XXM04
– SDO Bus 15	H2M02	XXM10		M2B13		N6B02	M1B11	XXM10
– SDO Bus PL	H2P07	XXP13		M2G03		N6C02	M1A11	XXP13
– Dest Bus 0	F2J11			M2J11				
	E2J11							
– Dest Bus 1	F2D04			M2D04				
	E2D04							
– Dest Bus 2	F2B02			M2B02				
	E2B02							
– Dest Bus 3	F2B03			M2B03				
	E2B03							
– Dest Bus 4	F2D05			M2D06				
	E2D05							
– Dest Bus 5	F2D02			M2D02				
	E2D02							
– Dest Bus 6	F2B05			M2B05				
	E2B05							
– Dest Bus 7	F2P02			M2P02				
	E2P02							
	L2P02							
– Dest Bus PH	L2G12			M2G12				
	J2G12							
	G2G12							
	E2G12							
– Dest Bus 8	L2M12			M2M12				
	F2M12							
	E2M12							

Signal Name	A1 BOARD						A2 BOARD	
	Proc	Stor*	SC1	FP	EFP**	Conn	Conn	Stor*
– Dest Bus 9	L2D13			M2D13				
	F2D13							
	E2D13							
– Dest Bus 10	L2P07			M2P07				
	F2P07							
	E2P07							
– Dest Bus 11	L2U02			M2U02				
	F2U02							
	E2U02							
– Dest Bus 12	L2J12		A2M02	M2J12				
	F2J12							
	E2J12							
– Dest Bus 13	L2P10		A2P02	M2P10				
	F2P10							
	E2P10							
– Dest Bus 14	L2P11		A2M03	M2P11				
	F2P11							
	E2P11							
– Dest Bus 15	L2J05		A2M04	M2J05				
	F2J05							
	E2J05							
– Dest Bus PL	L2M02			M2M02				
	J2M02							
	G2M02							
	E2M02							
– FP Inst	H2B04			M2D04				
	F2G04							
	C2D04							
– FP CHIO Reg	E2U09			M2U09				
– FP Req 0	C2G13			M2S04				
– FP Req 1	C2S04			M2S05				
– FPT02	C2J13			M2U13				
– FPT02 Delta	C2U10			M2U10				
– Set ACV	E2S10			M2S10				
– Stor Sel	K2J04			M2J04				
	J2S10							
	G2J04							
	D2S10							
– ROS Extended Register	G2D09			M2D09				
	C2M07							
– FP PC	G2G07			M2G07				
– ROS Pty Error	D2U09			M2J09				
	C2U11							
– Sys Ck Stop Delayed	C2J02			M2J02				
	D2D02							
– Stop Acknowledge	J2B04			M2D07				
	G2B04							
	F2S02							
	D2S02							
	C2S02							

* See BU111 for card locations.
** See SP111 for card locations.

Figure BU414-1 (Part 3 of 3). 8140 Model A3X, A4X, and A5X Logic Signals Between the Processor, Storage, SC1, Floating Point, and EFP Cards

BU415 8140 Models A6X and A7X Signal Path: SC1, Storage, EFP, and Floating—Point Cards

Figure BU415-1 shows the logic signal interconnection between the 8140 models A6X and A7X Processor I/E Unit and the SC1, EFP (RPQ only), floating-point (RPQ only), and processor storage cards.

	A1 BOARD					A2 BOARD		
Signal Name	Proc	SC1	FP	EFP**	Conn	Conn	Stor*	ECC
– I/O Bus 0	E2B07	A2B02						
– I/O Bus 1	E2D06	A2B08						
– I/O Bus 2	E2B10	A2D11						
– I/O Bus 3	E2B09	A2B04						
– I/O Bus 4	E2J04	A2D04						
– I/O Bus 5	E2B04	A2B05						
– I/O Bus 6	E2G08	A2D07						
– I/O Bus 7	E2J07	A2D06						
– I/O Bus PH	E2G09	A2B07						
– I/O Bus 8	G2G02	A2D05						
	E2G02							
– I/O Bus 9	E2J02	A2B10						
– I/O Bus 10	E2B12	A2D13						
– I/O Bus 11	E2J09	A2D09						
		A2J02						
– I/O Bus 12	E2D10	A2B09						
– I/O Bus 13	E2D07	A2D10						
– I/O Bus 14	E2D09	A2B03						
– I/O Bus 15	E2G05	A2B12						
– I/O Bus PL	E2M03	A2B13						
– Address Tag	D2S13	A2G10						
– Command Tag	D2U13	A2J10						
– Data Tag	D2P09	A2G02						
– I/O Tag	D2M04	A2J05						
– Interrupt Tag	D2U10	A2J11						
– Byte Tag	D2P02	A2J11						
– Halt Tag Ext	D2B05	A2J09						
	H2B08							
– Valid Byte 1	D2P12	A2J07						
		A2P07						
– Valid Halfword	D2U11	A2J06						
	G2P06							
– Parity Valid	D2U07	A2G05						
– Monitor	D2G10	A2P06			Q6B02	Q1B11		L2S13
– End of Chain Tag	D2M12	A2J04						
– I/O Exception	D2M03	A2G03						
– CHIO Request Tag	E2B13	A2J13						
– Channel Grant	D2U12	A2J12						
– Wait State Gate	C2D02	A2G07		XXD02				
	E2M10							
– SAB Bit 14	C2B02	A2D12						
– Restart	K2G13		A2P04					
	L2P09							
	J2P09							
	G2P10							
	D2G12							
– Modifier	C2U07	A2G04						
– Oscillator Out Ext	F2J07	A2U02						
+ PM 0	J2M07	A2P05	M2G04	XXD09	Q6B04	Q1B13		L2S10
	H2G04							
– System Reset	K2B07	A2U04	M2B07	XXG08	Q6A04	Q1A13		L2U09
	D2B08							

*See BU111 for card locations. **See SP111 for card locations.

Figure BU415-1 (Part 1 of 3). 8140 Models A6X and A7X Logic Signals Between the Processor, Storage, SC1, Floating Point, and EFP Cards

	A1 BOARD					A2 BOARD		
Signal Name	Proc	SC1	FP	EFP**	Conn	Conn	Stor*	ECC
– Wait State Out		A2G13			F1E13			
– EFP Interrupt Request		A2S07		XXD04				
– SDC Bus 0		A2U09		XXU09	A1E13			
– SDC Bus 1		A2S09		XXS09	B1A13			
– SDC Bus 2		A2S05		XXU10	B1B13			
– SDC Bus 3		A2U07		XXB02	B1C13			
– SDC Bus 4		A2S08		XXB03	B1E13			
– SDC Bus 5		A2S10		XXB04	C1A13			
– SDC Bus 6		A2U06		XXB05	C1B13			
– SDC Bus 7		A2U05		XXB07	C1C13			
– SDC Bus P		A2S12		XXB08	C1D13			
– SDC Selected		A2P07		XXS12	F1C13			
– SDC Sync		A2U13		XXM05	B1C11			
– SDC Halt		A2M08		XXS04	E1E11			
– I/O Operation		A2S03		XXD06	B1A11			
– 1-MHz Oscillator		A2M05		XXU04	B1B11			
				XXS05				
– 500 ms Rate		A2M12		XXU07	A1E11			
		A2P13						
– 1.024 ms Rate		A2M13		XXS07	A1D11			
		A2S02						
– Pushbutton Reset Req		A2S04			C1B11			
– BOP Interrupt Request		A2P12			E1D11			
– BOP Adapter Check		A2P09			E1A11			
– BOP Check		A2M10			E1B11			
– System Check Not 0	D2J07			XXJ07	F1B13			
	G2D02							
– SS FRU	L2M07				F1B11			
– Ext Stk Error	D2D09				F1C11			
– ROS Pty Error Lth	C2U13				F1D11			
– Proc Stk Error	D2B10				F1E11			
– PIC Bit 0	J2B08			XXD12				
	D2D12							
+ PM 1	K2D07			XXD07				
	J2P02							
	H2D07							
– R/V	K2B10			XXB10				
– ROS Control 1	K2D11			XXD13				
	J2D13							
	C2D13							
+ T2	E2M05			XXJ06				
	D2P11							
	C2P11							
– I Fetch	D2G07		M2G08	XXG07				
+ Exit	H2D11			XXD05				
	E2P09							
	D2D11							
– Long Instruction	H2M09			XXG09				
	D2P04							
– PSV Switch Ext	E2S09			XXD10				
– Stack Address Bus 9	J2P13			XXM12				
	G2P13							
	E2G13							
– Stack Address Bus 11	J2M10		M2J10	XXP11				
	G2M10							
	E2U13							
– Stack Address Bus 12	J2P04		M2G02	XXP05				
	G2P04							
	E2U07							
– Stack Address Bus 13	J2M09		M2G05	XXP07				
	G2M09							
	E2S03							

Signal Name	A1 BOARD Proc	SC1	FP	EFP**	Conn	A2 BOARD Conn	Stor*	ECC
– PSV 2	K2J06		M2J06	XXU02				
	J2S12							
	E2S12							
– Stor Adr Bus 0	K2P13			M2P13	T6A02	T1A11	XXU12	
– Stor Adr Bus 1	K2P12			XXP12	T6C04	T1C13	XXS07	
– Stor Adr Bus 2	K2M08			XXM08	T6D04	T1D13	XXU05	
– Stor Adr Bus 3	K2P06			XXP06	T6E02	T1E11	XXS03	
– Stor Adr Bus 4	K2M03			XXM03	U6A02	U1A11	XXS04	
– Stor Adr Bus 5	K2M04			XXM04	U6B04	U1B13	XXS09	
– Stor Adr Bus 6	K2M10			XXM10	U6C02	U1C11	XXU09	
– Stor Adr Bus 7	K2P09			XXP09	U6D02	U1D11	XXU10	
– Stor Adr Bus 8	K2P10			XXP10	V6A04	V1A13	XXS08	
– Stor Adr Bus 9	K2M09			XXM09	T6B04	T1B13	XXS10	
– Stor Adr Bus 10	K2M13			XXM13	T6A04	T1A13	XXS05	
– Stor Adr Bus 11	K2M07			XXM07	T6C02	T1C11	XXU04	
– Stor Adr Bus 12	K2P04			XXP04	T6D02	T1D11	XXU02	
– Stor Adr Bus 13	K2P02			XXP02	U6A04	U1A13	XXS02	
– Stor Adr Bus 14	K2M02			XXM02	U6C04	U1C13		L2S08
– Stor Write Hi	J2S02			XXS02	U6E02	U1E11		L2S07
– Stor Write Lo	J2S03			XXS03	U6D04	U1D13		L2U07
– Stor Select 0	K2J09			S2J09	R6B02	R1B11	V2U11	
							U2U11	
							R2U11	
							Q2U11	
–Stor Select 1	K2J11			S2J11	R6C04	R1C13	V2S13	
							U2S13	
							R2S13	
							Q2S13	
–Stor Select 2	K2J12			S2J12	R6C02	R1C11	V2U06	
							U2U06	
							R2U06	
							Q2U06	
– Stor Select 3	K2J13			S2J13	R6D02	R1D11	V2U07	
							U2U07	
							R2U07	
							Q2U07	
– Stor Select 4								
Model A6X	K2P05			S2G12	R6E04	R1E13	T2U11	
							S2U11	
Model A7X	K2P05			S2G12	R6E04	R1E13	T2U11	
							S2U11	
							P2U11	
							N2U11	

*See BU111 for card locations. **See SP111 for card locations.

Figure BU415-1 (Part 2 of 3). 8140 Model A6X and A7X Logic Signals Between the Processor, Storage, SC1, Floating Point, and EFP Cards

Signal Name	A1 BOARD Proc	SC1	FP	EFP**	Conn	A2 BOARD Conn	Stor*	ECC
– Stor Select 5								
Model A6X	K2P07			S2G10	R6E02	R1E11	T2S13	
							S2S13	
Model A7X	K2P07			S2G10	R6E02	R1E11	T2S13	
							S2S13	
							P2S13	
							N2S13	
– Stor Select 6								
Model A6X	K2U04				S6A04	S1A13	T2U06	
							S2U06	
Model A7X	K2U04				S6A04	S1A13	T2U06	
							S2U06	
							P2U06	
							N2U06	
– Stor Select 7								
Model A6X	K2P11				S6A02	S1A11	T2U07	
							S2U07	
Model A7X	K2P11				S6A02	S1A11	T2U07	
							S2U07	
							P2U07	
							N2U07	
– Not M S/P	K2D09				P6E02	P1E13	V2G03	
							U2G03	
							T2G03	
							S2G03	
– M S/P								
Model A6X	K2D02				P6E04	P1E11	R2G03	
							Q2G03	
Model A7X	K2D02				P6E04	P1E11	R2G03	
							Q2G03	
							P2G03	
							N2G03	
– Stor Reset	G2B13				K6A02	K1A11		
	K2B13							
– SDI Bus 0	J2J10				L6E04	L1E13		L2M02
– SDI Bus 1	J2J11				M6A02	M1A11		L2P02
– SDI Bus 2	J2G03				M6B02	M1B11		L2M03
– SDI Bus 3	J2G07				M6D04	M1D13		L2P04
– SDI Bus 4	J2G04				M6D02	M1D11		L2M04
– SDI Bus 5	J2J07				N6A04	N1A13		L2P05
– SDI Bus 6	J2J09				N6B09	N1B13		L2M05
– SDI Bus 7	J2J05				N6C02	N1C11		L2P06
– SDI Bus PH	J2G10				L6D04	L1D13		L2M12
– SDI Bus 8	J2D02				N6D04	N1D13		L2M07
– SDI Bus 9	J2B02				L6D02	L1D11		L2P07
– SDI Bus 10	J2B10				M6A04	M1A13		L2M08
– SDI Bus 11	J2D04				M6B04	M1B13		L2P09
– SDI Bus 12	J2B12				M6C02	M1C11		L2M09
– SDI Bus 13	J2B13				N6D02	N1D11		L2P10
– SDI Bus 14	J2D05				M6E04	M1E13		L2M10
– SDI Bus 15	J2J04				N6A02	N1A11		L2P11
– SDI Bus PL	J2J02				N6B02	N1B11		L2P12

Signal Name	A1 BOARD					A2 BOARD		
	Proc	SC1	FP	EFP**	Conn	Conn	Stor*	ECC
– Addr Valid 0	J2P06				V6A02	V1A11		
– Addr Valid 1	J2P07							
– SDO Bus 0	H2M13		M2M13		H6A02	H1A11		M2G02
– SDO Bus 1	H2P06		M2P06		H6C04	H1C13		M2J02
– SDO Bus 2	H2M10		M2M10		H6D04	H1D13		M2G03
– SDO Bus 3	H2S03		M2S03		H6E02	H1E11		M2J04
– SDO Bus 4	H2M07		M2M05		J6A02	J1A11		M2G04
– SDO Bus 5	H2D05		M2D05		J6B04	J1B13		M2J05
– SDO Bus 6	H2M08		M2M08		J6C02	J1C11		M2G05
– SDO Bus 7	H2P04		M2P04		J6D02	J1D11		M2J06
– SDO Bus PH	H2P10		M2J07		K6A04	K1A13		M2G12
– SDO Bus 8	H2M04		M2M04		K6B04	K1B13		M2G07
– SDO Bus 9	H2M03		M2M03		H6B04	H1B13		M2J07
– SDO Bus 10	H2P11		M2P05		H6C02	H1C13		M2G08
– SDO Bus 11	H2P09		M2P09		H6D02	H1D11		M2J09
– SDO Bus 12	H2M12		M2G10		J6A04	J1A13		M2G09
– SDO Bus 13	H2P05		M2M07		H6A04	H1A13		M2J10
– SDO Bus 14	H2P02		M2B12		J6C04	J1C13		M2G10
– SDO Bus 15	H2M02		M2B13		J6D04	J1D13		M2J11
– SDO Bus PL	H2P07		M2G03		J6E02	J1E11		M2J12
– Dest Bus 0	F2J11		M2J11					
	E2J11							
– Dest Bus 1	F2D04		M2D04					
	E2D04							
– Dest Bus 2	F2B02		M2B02					
	E2B02							
– Dest Bus 3	F2B03		M2B03					
	E2B03							
– Dest Bus 4	F2D05		M2D06					
	E2D05							
– Dest Bus 5	F2D02		M2D02					
	E2D02							
– Dest Bus 6	F2B05		M2B05					
	E2B05							
– Dest Bus 7	F2P02		M2P02					
	E2P02							
	L2P02							
– Dest Bus PH	L2G12		M2G12					
	J2G12							
	G2G12							
	E2G12							
– Dest Bus 8	L2M12		M2M12					
	F2M12							
	E2M12							
– Dest Bus 9	L2D13		M2D13					
	F2D13							
	E2D13							
– Dest Bus 10	L2P07		M2P07					
	F2P07							
	E2P07							
– Dest Bus 11	L2U02		M2U02					
	F2U02							
	E2U02							
– Dest Bus 12	L2J12	A2M02	M2J12					
	F2J12							
	E2J12							
– Dest Bus 13	L2P10	A2P02	M2P10					
	F2P10							
	E2P10							

*See BU111 for card locations. **See SP111 for card locations.

Figure BU415-1 (Part 3 of 3). 8140 Model A6X and A7X Logic Signals Between the Processor, Storage, SC1, Floating Point, and EFP Cards

Signal Name	A1 BOARD					A2 BOARD		
	Proc	SC1	FP	EFP**	Conn	Conn	Stor*	ECC
– Dest Bus 14	L2P11	A2M03	M2P11					
	F2P11							
	E2P11							
– Dest Bus 15	L2J05	A2M04	M2J05					
	F2J05							
	E2J05							
– Dest Bus PL	L2M02		M2M02					
	J2M02							
	G2M02							
	E2M02							
– FP Inst	H2B04		M2D04					
	F2G04							
	C2D04							
– FP CHIO Reg	E2U09		M2U09					
– FP Req 0	C2G13		M2S04					
– FP Req 1	C2S04		M2S05					
– FPT02	C2J13		M2U13					
– FPT02 Delta	C2U10		M2U10					
– Set ACV	E2S10		M2S10					
– Stor Sel	K2J04		M2J04		Q6C02	Q1C11		M2B07
	J2S10							
	G2J04							
	D2S10							
– ROS Extended Register	G2D09		M2D09					
	C2M07							
– FP PC	G2G07		M2G07					
– ROS Pty Error	D2U09		M2J09					
	C2U11							
– Sys Ck Stop Delayed	C2J02		M2J02					
	D2D02							
– Stop Acknowledge	J2B04		M2D07		V6B04	V1B13		L2U06
	G2B04							
	F2S02							
	D2S02							
	C2S02							
– ECC Clock	E2M08				Q6D02	Q1D11		
– Refresh Allow	C2J11				Q6E04	Q1E13		
– First Half Store Op	G2P05				Q6E02	Q1E11		M2D05
– RMC 0	E2U05				R6A04	R1A13		L2U13
– Storage Busy					R6B04	R1B13		M2D09
– Wrt Pty Chk Pulse	D2M10				V6B02	V1B11		L2S12
– ROS Select	01A-A2K2J13				K6B02	K1B11		
– Stor Op	K2J04				N6E04	N1E13	XXG10	M2D07 L2U11
– Stop Clock	C2J10				N6E02	N1E11		M2D10
	G2P05							

BU416 8140 Models BXX Signal Path: SC1, Storage, EFP, and Floating–Point Cards

Figure BU416-1 shows the logic signal interconnection between the 8140 Model BXX Processor I/E Unit and the SC1, EFP (feature only), floating-point (feature only), and processor storage cards.

Signal Name	A1 BOARD					C1 BOARD		
	Proc	SC1	FP	EFP**	Conn	Conn	Stor*	ECC
– I/O Bus 0	H2B07	D2B02						
– I/O Bus 1	H2D06	D2B08						
– I/O Bus 2	H2B10	D2D11						
– I/O Bus 3	H2B09	D2B04						
– I/O Bus 4	H2J04	D2D04						
– I/O Bus 5	H2B04	D2B05						
– I/O Bus 6	H2G08	D2D07						
– I/O Bus 7	H2J07	D2D06						
– I/O Bus PH	H2G09	D2B07						
– I/O Bus 8	K2G02	D2D05						
	H2G02							
– I/O Bus 9	H2J02	D2B10						
– I/O Bus 10	H2B12	D2D13						
– I/O Bus 11	H2J09	D2D09						
		D2J02						
– I/O Bus 12	H2D10	D2B09						
– I/O Bus 13	H2D07	D2D10						
– I/O Bus 14	H2D09	D2B03						
– I/O Bus 15	H2G05	D2B12						
– I/O Bus PL	H2M03	D2B13						
– Address Tag	G2S13	D2G10						
– Command Tag	G2U13	D2J10						
– Data Tag	G2P09	D2G02						
– I/O Tag	G2M04	D2J05						
– Interrupt Tag	G2U10	D2G09						
– Byte Tag	G2P02	D2J11						
– Halt Tag Ext	G2B05	D2J09						
	L2B08							
– Valid Byte 1	G2P12	D2J07						
		D2P07						
– Valid Halfword	G2U11	D2J06						
	K2P06							
– Parity Valid	G2U07	D2G05						
– Monitor	G2G10	D2P06			V2D04	F1B11		A2S13
– End of Chain Tag	G2M12	D2J04						
– I/O Exception	G2M03	D2G03						
– CHIO Request Tag	H2B13	D2J13						
– Channel Grant	G2U12	D2J12						
– Wait State Gate	F2D02	D2G07		XXD02				
	H2M10							
– SAB Bit 14	F2B02	D2D12						
– Restart	N2G13							
	P2P09							
	M2P09							
	K2P10							
	G2G12							
– Modifier	F2U07	D2G04						
– Oscillator Out Ext	J2J07	D2U02						
+ PM 0	M2M07	D2P05	Q2G04	XXD09	V2B04	F1B13		A2S10
	L2G04							
– System Reset	M2B07	D2U04	Q2B07	XXG08	V2B03	F1A13	XXS12	A2U09
	G2B08							

*See BU111 for card locations. **See SP111 for card locations.

Figure BU416-1 (Part 1 of 3). 8140 Model BXX Logic Signals Between the Processor, Storage, SC1, Floating Point, and EFP Cards

Signal Name	A1 BOARD					C1 BOARD		
	Proc	SC1	FP	EFP**	Conn	Conn	Stor*	ECC
– Wait State Out		D2G13			F1E13			
– EFP Interrupt Request		D2S07		XXD04				
– SDC Bus 0		D2U09		XXU09	A1E13			
– SDC Bus 1		D2S09		XXS09	B1A13			
– SDC Bus 2		D2S05		XXU10	B1B13			
– SDC Bus 3		D2U07		XXB02	B1C13			
– SDC Bus 4		D2S08		XXB03	B1E13			
– SDC Bus 5		D2S10		XXB04	C1A13			
– SDC Bus 6		D2U06		XXB05	C1B13			
– SDC Bus 7		D2U05		XXB07	C1C13			
– SDC Bus P		D2S12		XXB08	C1D13			
– SDC Selected		D2P07		XXS12	F1C13			
– SDC Sync		D2U13		XXM05	B1C11			
– SDC Halt		D2M08		XXS04	E1E11			
– I/O Operation		D2S03		XXD06	B1A11			
– 1-MHz Oscillator		D2M05		XXU04	B1B11			
				XXS05				
– 500 ms Rate		D2M12		XXU07	A1E11			
		D2P13						
– 1.024 ms Rate		D2M13		XXS07	A1D11			
		D2S02						
– Pushbutton Reset Req		D2S04			C1B11			
– BOP Interrupt Request		D2P12			E1D11			
– BOP Adapter Check		D2P09			E1A11			
– BOP Check		D2M10			E1B11			
– System Check Not 0	G2J07			XXJ07	F1B13			
	K2D02							
– SS FRU	P2M07				F1B11			
– Ext Stk Error	G2D09				F1C11			
– Ros Pty Error Lth	F2U13				F1D11			
– Proc Stk Error	G2B10				F1E11			
– PIC Bit 0	M2B08			XXD12				
	G2D12							
+ PM 1	N2D07			XXD07				
	M2P02							
	L2D07							
– R/V	N2B10			XXB10				
– ROS Control 1	N2D11			XXD13				
	M2D13							
	F2D13							
+ T2	H2M05			XXJ06				
	G2P11							
	F2P11							
– 1 Fetch	G2G07		Q2G08	XXG07				
+ Exit	L2D11			XXD05				
	H2P09							
	G2D11							
– Long Instruction	L2M09			XXG09				
	G2P04							
– PSV Switch Ext	H2S09			XXD10				
– Stack Address Bus 9	M2P13			XXM12				
	K2P13							
	H2G13							
– Stack Address Bus 11	M2M10		Q2J10	XXP11				
	K2M10							
	H2U13							
– Stack Address Bus 12	M2P04		Q2G02	XXP05				
	K2P04							
	H2U07							
– Stack Address Bus 13	M2M09		Q2G05	XXP07				
	K2M09							
	H2S03							

Signal Name	A1 BOARD					C1 BOARD		
	Proc	SC1	FP	EFP**	Conn	Conn	Stor*	ECC
– PSV 2	N2J06		Q2J06	XXU02				
	M2S12							
	H2S12							
– Stor Adr Bus 0	N2P13			XXP13	V2U02	D6F02	XXU12	
– Stor Adr Bus 1	N2P12			XXP12	V2S04	F6B04	XXS07	
– Stor Adr Bus 2	N2M08			XXM08	V2S05	F6C04	XXU05	
– Stor Adr Bus 3	N2P06			XXP06	V2U06	F6D02	XXS03	
– Stor Adr Bus 4	N2M03			XXM03	V2U07	F6F02	XXS04	
– Stor Adr Bus 5	N2M04			XXM04	V2S08	F6A04	XXS09	
– Stor Adr Bus 6	N2M10			XXM10	V2U09	F6B02	XXU09	
– Stor Adr Bus 7	N2P09			XXP09	V2U10	F6C02	XXU10	
– Stor Adr Bus 8	N2P10			XXP10	V2S12	F6F04	XXS08	
– Stor Adr Bus 9	N2M09			XXM09	V2S03	F6A04	XXS10	
– Stor Adr Bus 10	N2M13			XXM13	V2S12	D6F04	XXS05	
– Stor Adr Bus 11	N2M07			XXM07	V2U04	F6B02	XXU04	
– Stor Adr Bus 12	N2P04			XXP04	V2U05	F6C02	XXU02	
– Stor Adr Bus 13	N2P02			XXP02	V2S07	F6F04	XXS02	
– Stor Adr Bus 14	N2M02			XXM02	V2S09	F6B04		A2S08
– Stor Write Hi	M2S02			XXS02	V2U11	F6D02		A2S07
– Stor Write Lo	M2S03			XXS03	V2S10	F6C04		A2U07
– Stor Select 0								
Model B5X	N2J09			XXJ09	V2D09	F1B11	F2U11	
							K2U11	
Models B6X, B7X	N2J09			XXJ09	V2D09	F1B11	D2U11	
							F2U11	
							H2U11	
							K2U11	
– Stor Select 1								
Model B5X	N2J11			XXJ11	V2B10	F1C13	F2S13	
							K2S13	
Models B6X, B7X	N2J11			XXJ11	V2B10	F1C13	D2S13	
							F2S13	
							H2S13	
							K2S13	
–Stor Select 2								
Model B5X	N2J12			XXJ12	V2D10	F1C11	F2U06	
							K2U06	
Models B6X, B7X	N2J12			XXJ12	V2D10	F1C11	D2U06	
							F2U06	
							H2U06	
							K2U06	
– Stor Select 3								
Model B5X	N2J13			XXJ13	V2D11	F1D11	F2U07	
							K2U07	
Models B6X, B7X	N2J13			XXJ13	V2D11	F1D11	D2U07	
							F2U07	
							H2U07	
							K2U07	
– Stor Select 4								
Models B5X, B6X	N2P05			XXG12	V2B12	F1E13	E2U11	
							J2U11	
Model B7X	N2P05			XXG12	V2B12	F1E13	C2U11	
							E1U11	
							G2U11	
							J2U11	
– Stor Select 5								
Models B5X, B6X	N2P07			XXG10	V2D12	F1E11	E2S13	
							J2S13	
Model B7X	N2P07				V2D12	F1E11	C3S13	
							E2S13	
							G2S13	
							J2S13	
– Stor Select 6								
Models B5X, B6X	N2U04				V2B13	G1A13	E2U06	
							J2U06	
Model B7X	N2U04				V2B13	G1A13	C2U06	
							E2U06	
							G2U06	
							J2U06	
– Stor Select 7								
Models B5X, B6X	N2P11				V2D13	G1A11	E2U07	
							J2U07	
Model B7X	N2P11				V2D13	G1A11	C2U07	
							E2U07	
							G2U07	
							J2U07	
– M S/P								
Model B6X	N2D02				V2B02	D1E13	D2G03	
							H2G03	
Model B7X	N2D02				V2B02	D1E13	D2G03	
							H2G03	
							C2G03	
							G2G03	
– Not M S/P								
Models BXX	N2D09				V2D02	D1E11	F2G03	
							K2G03	
							E2G03	
							J2G03	
– Stor Reset	K2B13				V2P12	C6D02		
	N2B13							
– SDI Bus 0	M2J10				V2G03	A1F13		A2M02
– SDI Bus 1	M2J11				V2J04	B1A11		A2P02
– SDI Bus 2	M2G03				V2J05	B1B11		A2M03
– SDI Bus 3	M2G07				V2G07	B1D13		A2P04
– SDI Bus 4	M2G04				V2J07	B1D11		A2M04
– SDI Bus 5	M2J07				V2G09	C1A13		A2P05
– SDI Bus 6	M2J09				V2G10	C1B13		A2M05
– SDI Bus 7	M2J05				V2J11	C1C11		A2P06
– SDI Bus PH	M2G10				V2G02	A1D13		A2M12
– SDI Bus 8	M2D02				V2G12	C1D13		A2M07
– SDI Bus 9	M2B02				V2J02	A1D11		A2P07
– SDI Bus 10	M2B10				V2G04	B1A13		A2M08

*See BU111 for card locations. **See SP111 for card locations.

Figure BU416-1 (Part 2 of 3). 8140 Model BXX Logic Signals Between the Processor, Storage, SC1, Floating Point, and EFP Cards

Signal Name	A1 BOARD					C1 BOARD		
	Proc	SC1	FP	EFP**	Conn	Conn	Stor*	ECC
– SDI Bus 11	M2D04				V2G05	B1B13		A2P09
– SDI Bus 12	M2B12				V2J06	B1C11		A2M09
– SDI Bus 13	M2B13				V2J12	C1D11		A2P10
– SDI Bus 14	M2D05				V2G08	B1F13		A2M10
– SDI Bus 15	M2J04				V2J09	C1A11		A2P11
– SDI Bus PL	M2J02				V2J10	C1B11		A2P12
– Addr Valid 0	M2P06				V2U12	F6F02	XXP02	
– Addr Valid 1	M2P07							
– SDO Bus 0	L2M13		Q2M13		V2P02	A6D02		B2G02
– SDO Bus 1	L2P06		Q2P06		V2M04	B6A04		B2J02
– SDO Bus 2	L2M10		Q2M10		V2M05	B6B04		B2G03
– SDO Bus 3	L2S03		Q2S03		V2P06	B6C02		B2J04
– SDO Bus 4	L2M07		Q2M05		V2P07	B6D02		B2G04
– SDO Bus 5	L2D05		Q2D05		V2M08	B6F04		B2J05
– SDO Bus 6	L2M08		Q2M08		V2P09	C6A02		B2G05
– SDO Bus 7	L2P04		Q2P04		V2P10	C6B02		B2J06
– SDO Bus PH	L2P10		Q2J07		V2M12	C6D04		B2G12
– SDO Bus 8	L2M04		Q2M04		V2M13	C6F04		B2G07
– SDO Bus 9	L2M03		Q2M03		V2M03	A6F04		B2J07
– SDO Bus 10	L2P11		Q2P05		V2P04	B6A02		B2G08
– SDO Bus 11	L2P09		Q2P09		V2P05	B6B02		B2J09
– SDO Bus 12	L2M12		Q2G10		V2M07	B6D04		B2G09
– SDO Bus 13	L2P05		Q2M07		V2M02	A6D04		B2J10
– SDO Bus 14	L2P02		Q2B12		V2M09	C6A04		B2G10
– SDO Bus 15	L2M02		Q2B13		V2M10	C6B04		B2J11
– SDO Bus PL	L2P07		Q2G03		V2P11	C6C02		B2J12
– Dest Bus 0	J2J11		Q2J11					
	H2J11							
– Dest Bus 1	J2D04		Q2D04					
	H2D04							
– Dest Bus 2	J2B02		Q2B02					
	H2B02							
– Dest Bus 3	J2B03		Q2B03					
	H2B03							
– Dest Bus 4	J2D05		Q2D06					
	H2D05							
– Dest Bus 5	J2D02		Q2D02					
	H2D02							
– Dest Bus 6	J2B05		Q2B05					
	H2B05							
– Dest Bus 7	J2P02		Q2P02					
	H2P02							
	P2P02							
– Dest Bus PH	P2G12		Q2G12					
	M2G12							
	K2G12							
	H2G12							
– Dest Bus 8	P2M12		Q2M12					
	J2M12							
	H2M12							
– Dest Bus 9	P2D13		Q2D13					
	H2D13							
	J2D13							
– Dest Bus 10	P2D07		Q2P07					
	J2P07							
	H2P07							
– Dest Bus 11	P2U02		Q2U02					
	J2U02							
	H2U02							
– Dest Bus 12	P2J12	D2M02	Q2J12					
	J2J12							
	H2J12							
– Dest Bus 13	P2P10	D2P02	Q2P10					
	J2P10							
	H2P10							
– Dest Bus 14	P2P11	D2M03	Q2P11					
	J2P11							
	H2P11							
– Dest Bus 15	P2J05	D2M04	Q2J05					
	J2J05							
	H2J05							
– Dest Bus PL	P2M02		Q2M02					
	M2M02							
	K2M02							
	H2M02							
– FP Inst	L2B04		Q2D04					
	J2G04							
	F2D04							
– FP CHIO Req	H2U09		Q2U09					
– FP Req 0	F2G13		Q2S04					
– FP Req 1	F2S04		Q2S05					
– FPT02	F2J13		Q2U13					
– FPT02 Delta	F2U10		Q2U10					
– Set ACV	H2S10		Q2S10					
– Stor Sel	N2J04		Q2J04		V2D05	F1C11		B2B07
	M2S10							
	K2J04							
	G2S10							
– ROS Extended Register	K2D09		Q2D09					
	F2M07							
– FP PC	K2G07		Q2G07					
– ROS Pty Error	G2U09		Q2J09					
	F2U11							
– Sys Ck Stop Delayed	F2J02		Q2J02					
	G2D02							
– Stop Acknowledge	M2B04		Q2D07		V2S13	G6A04		B2U06
	K2B04							
	J2S02							
	G2S02							
	F2S02							
– Stop Clock	F2J10				V2P13	C6F02		B2D10
	K2P05							
– First Half Store Op	K2P05				V2U13	G6A02		B2D05
– Write Pty Check Pulse	G2M10				V2B09	F1B13		A2S12
– RMC0	H2U06				V2B08	F1A13		A2U13
– Store Op	N2J04				V2G13	C1F13	XXG10	B2D07
								A2U11
– ROS Select	U2J13				V2J13	C1F11	F2J05	
							K2J05	
– ECC Clock	H2M08				V2D06	E1D11		A2S02
– Refresh Allow	F2J11				V2B07	E1E13	XXJ06	

*See BU111 for card locations. **See SP111 for card locations. (f) Available as a feature only.

Figure BU416-1 (Part 3 of 3). 8140 Model BXX Logic Signals Between the Processor, Storage, SC1, Floating Point, and EFP Cards

BU417 8140 BOP Adapter Card to 01A–A1 Board

Figure BU417-1 shows the logic signal interconnection from the 8140 basic operator panel adapter card to the 01A–A1 board. When these logic signals continue to the EFP card (if installed) SC1 card, and processor I/E unit, they are so indicated.

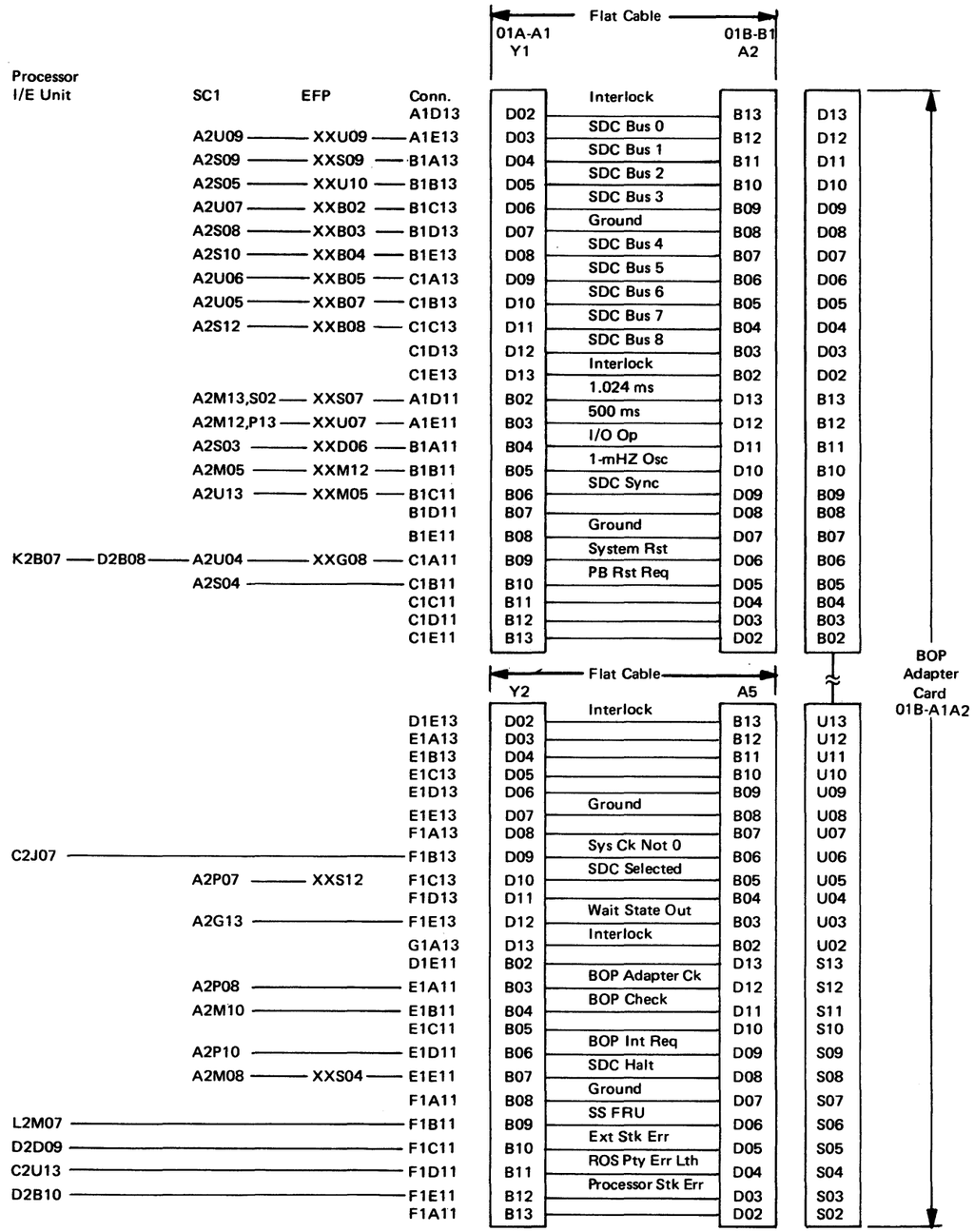

Figure BU417-1. 8140 BOP Adapter Card to 01A-A1 Board Signal Path

BU420 Processor I/E Unit and BOP Card and Card Connector Logic Signals

The figures in BU421 through BU424 show the 8130/8140 instruction/execution, storage addressing, storage control, storage, floating-point, and BOP card and card connector logic signals for use in continuity checking and in-depth problem analysis.

BU421 8130/8140 Processor and Storage Control Card Logic Signals

Refer to Figures BU421-1 through BU421-15 for the logic signal interconnection of the 8130/8140 processor and storage control cards.

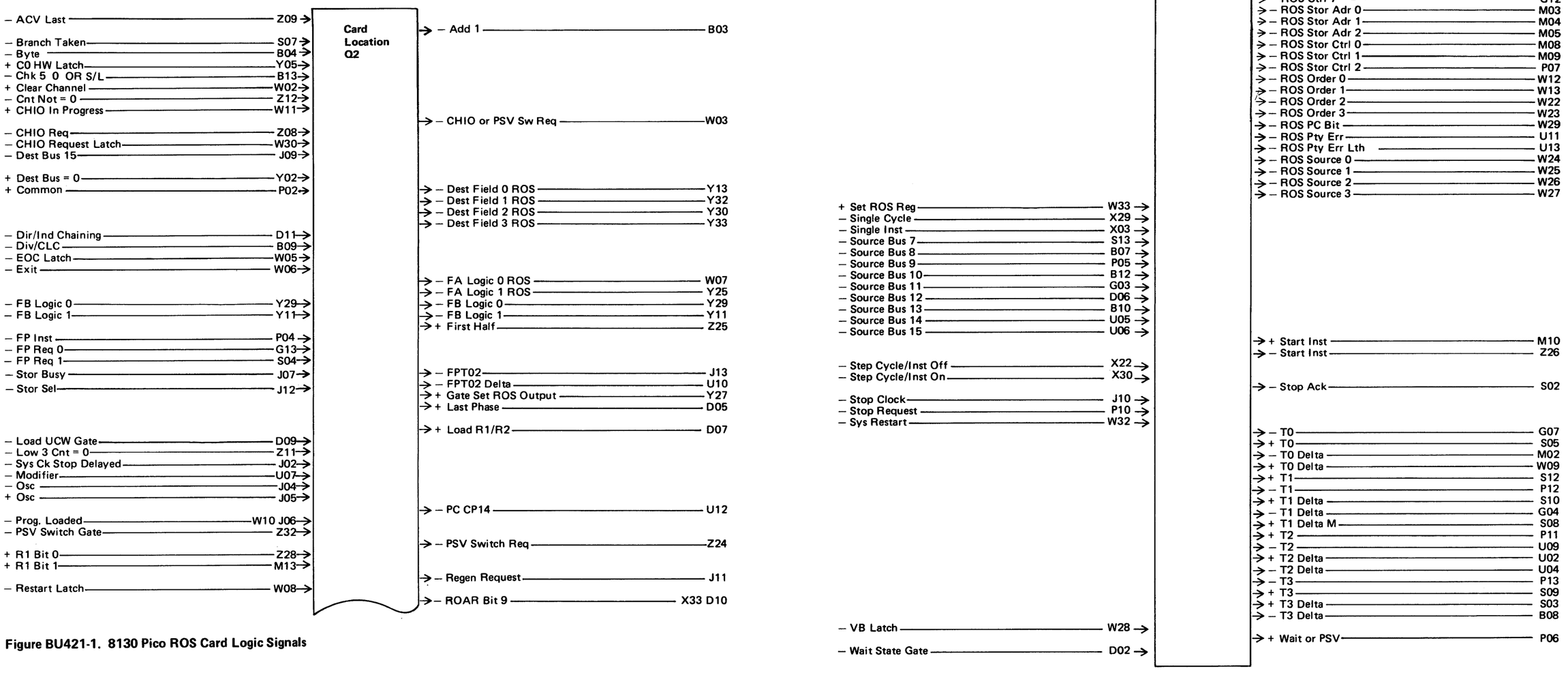

Figure BU421-1. 8130 Pico ROS Card Logic Signals

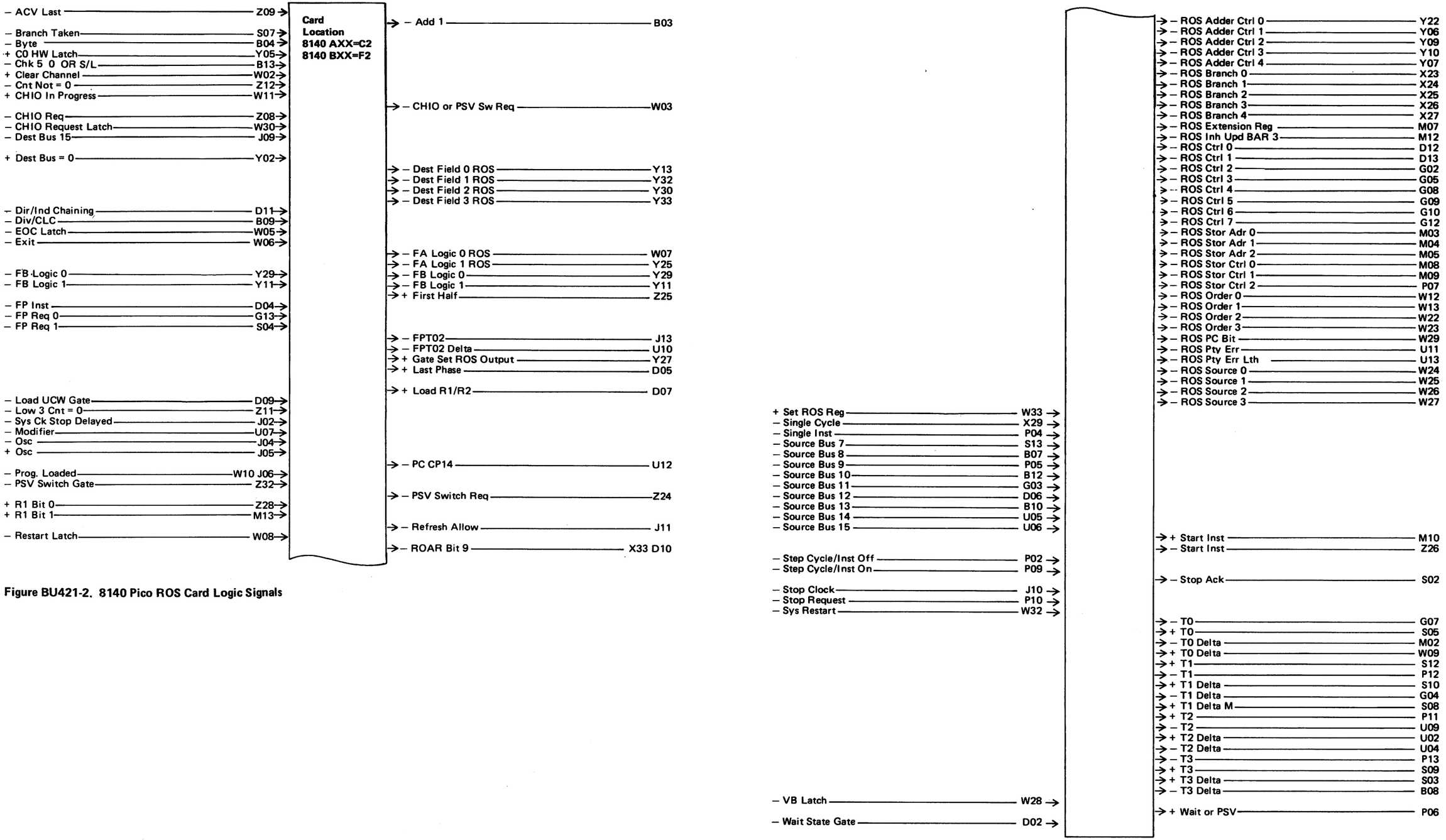

Figure BU421-2. 8140 Pico ROS Card Logic Signals

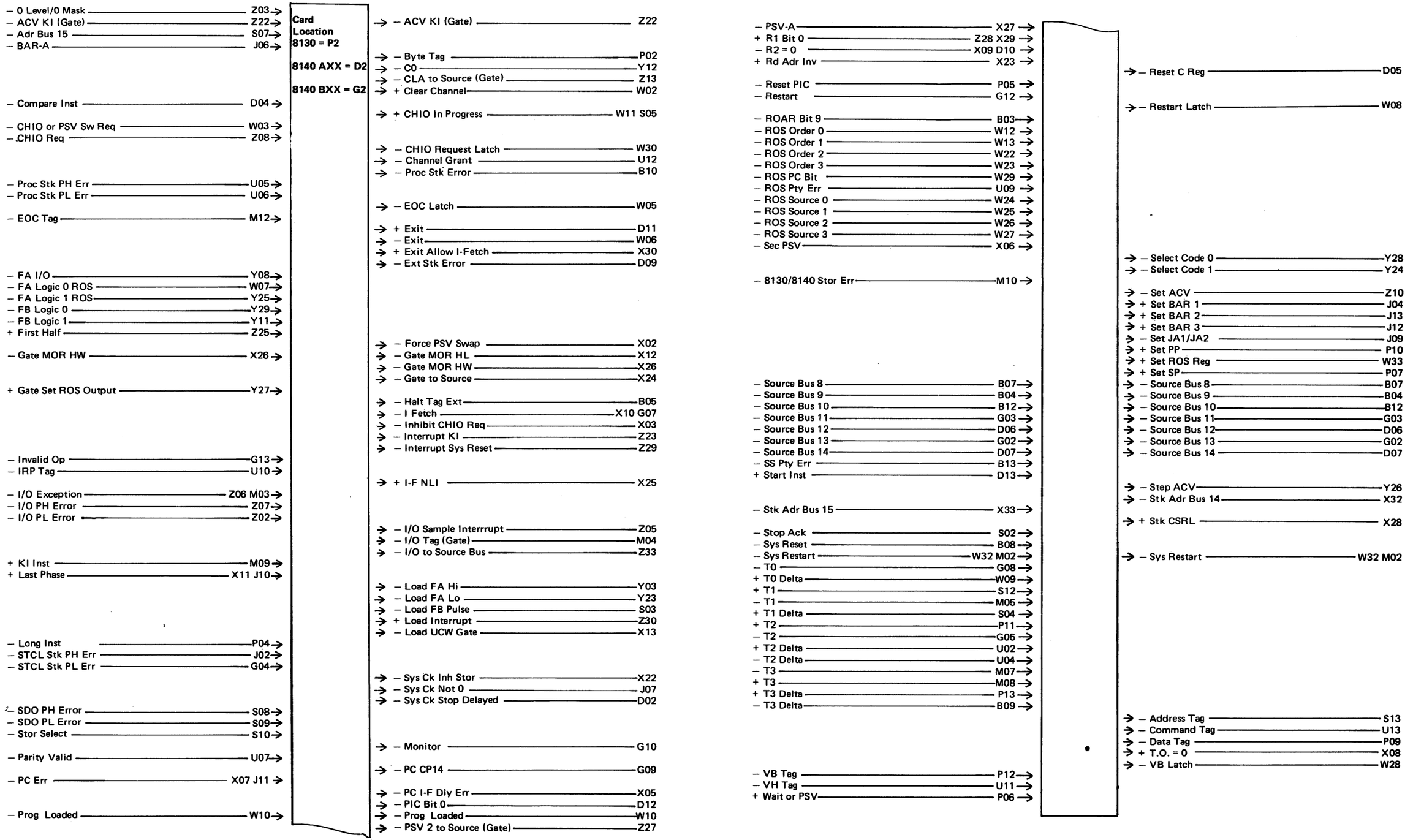

Figure BU421-3. 8130/8140 Pico ROS Decode and EIRV Card Logic Signals

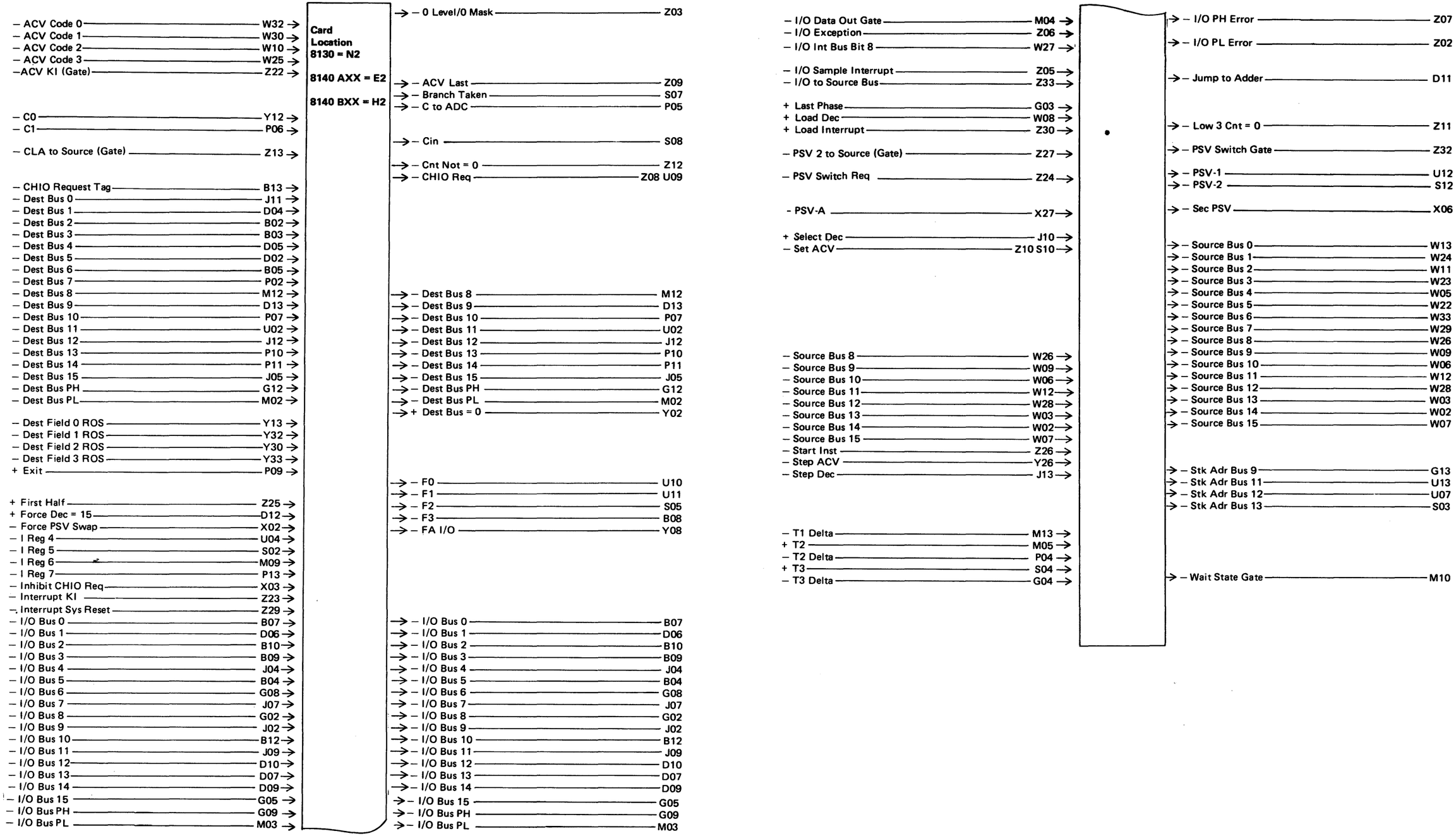

Figure BU421-4. 8130/8140 I/O Handling and Interrupt Card Logic Signals

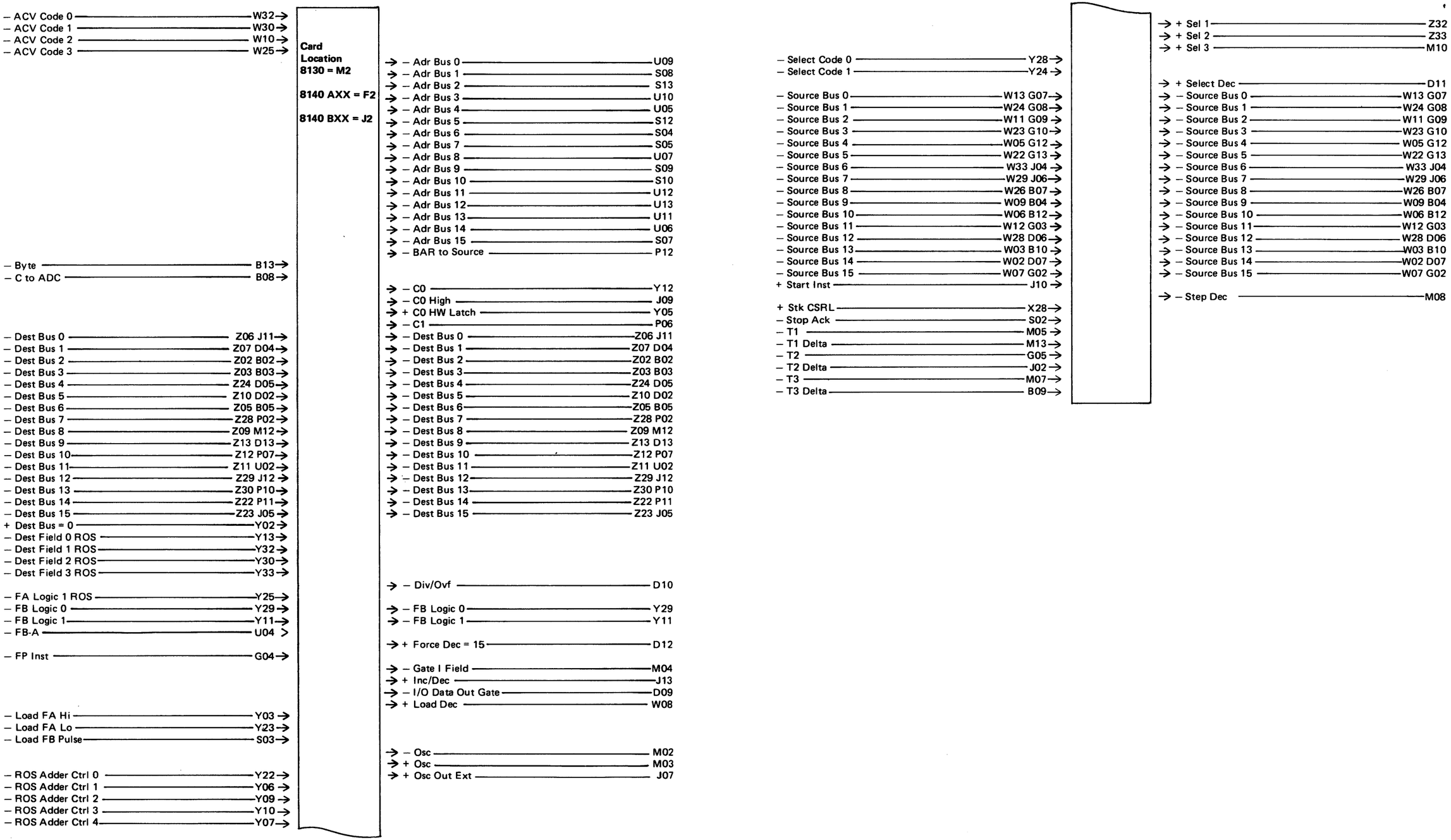

Figure BU421-5. 8130/8140 Arithmetic and Oscillator Card Logic Signals

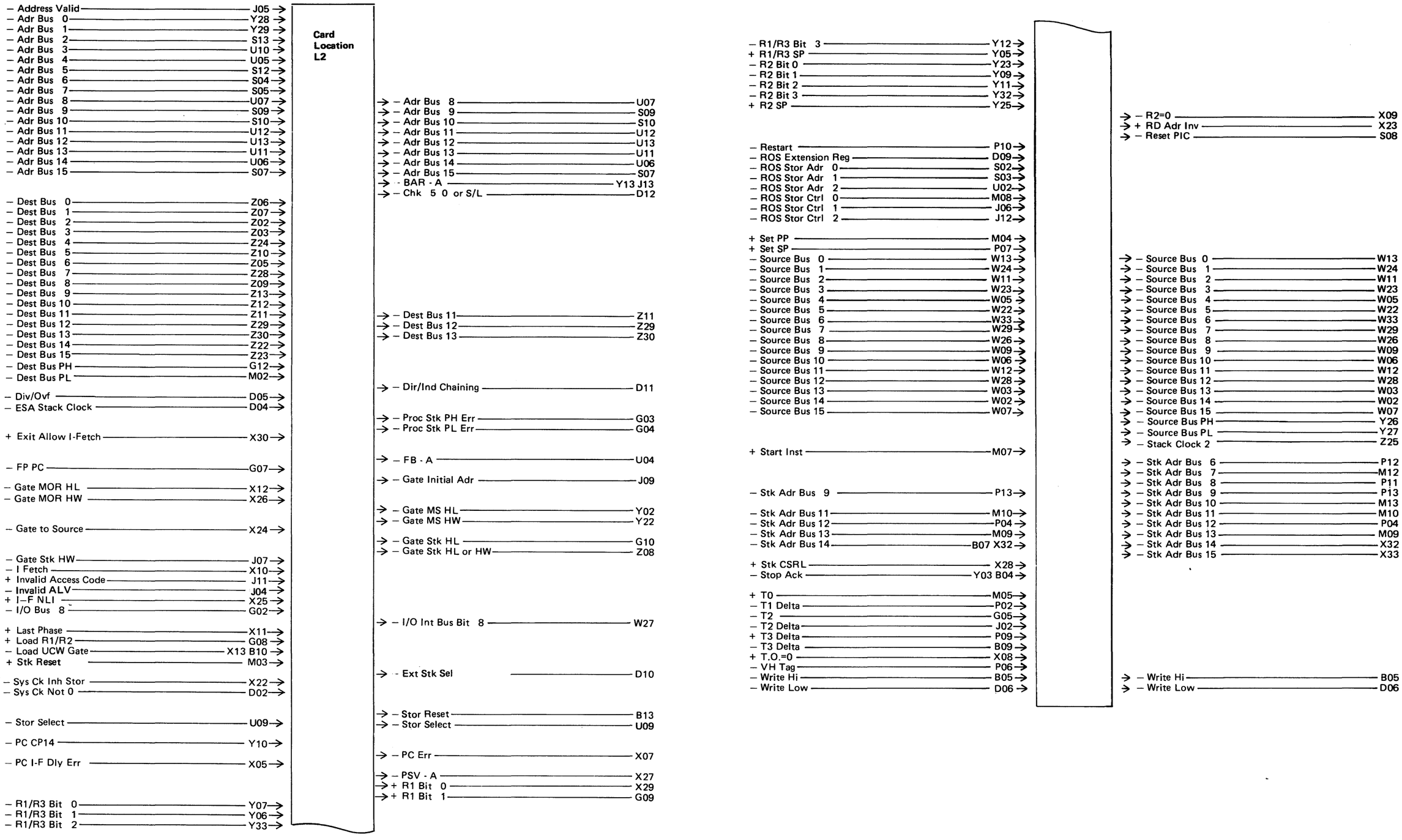

Figure BU421-6. 8130 Principal Register Storage Card Logic Signals

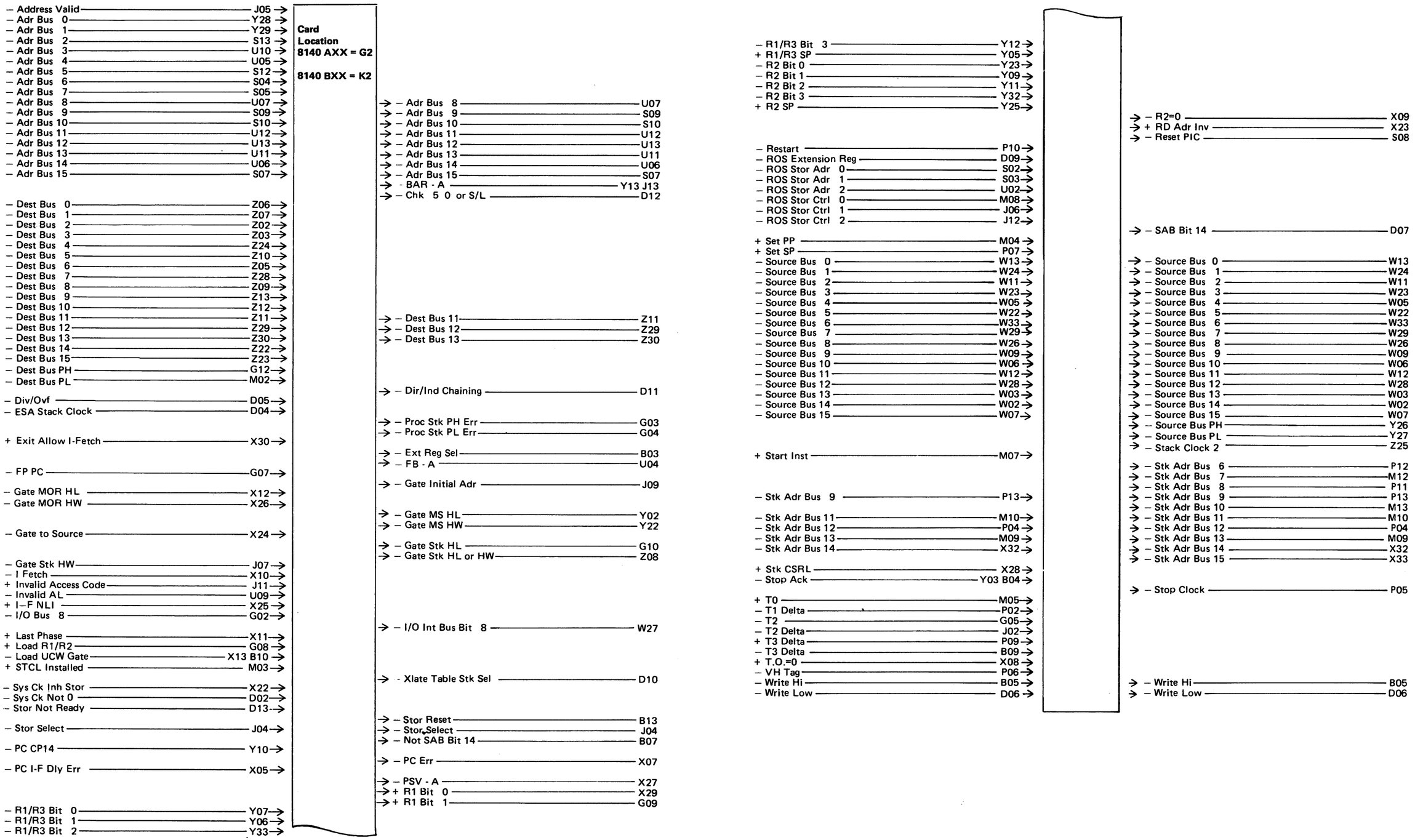

Figure BU421-7. 8140 Principal Register Storage Card Logic Signals

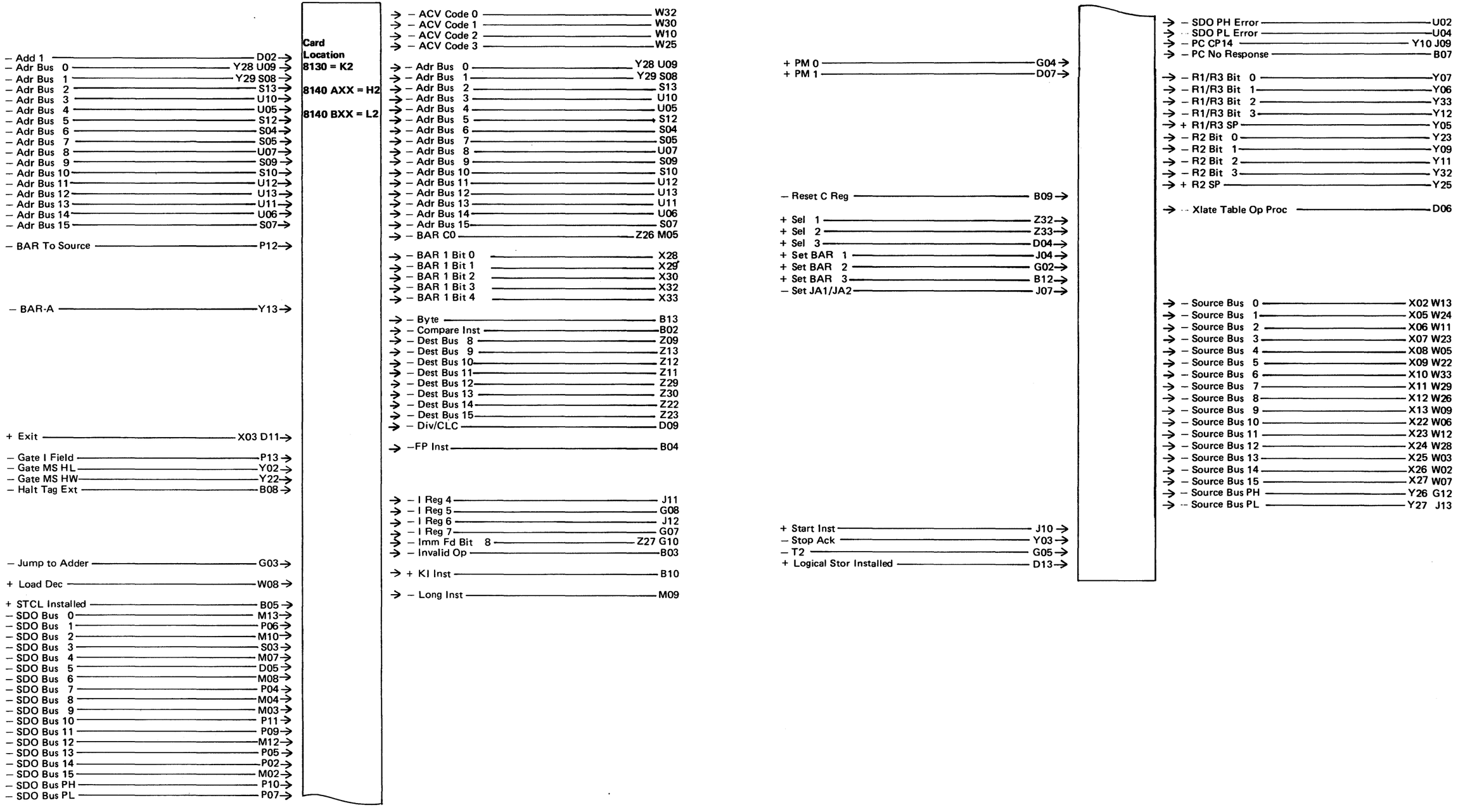

Figure BU421-8. 8130/8140 Instruction Decode Card Logic Signals

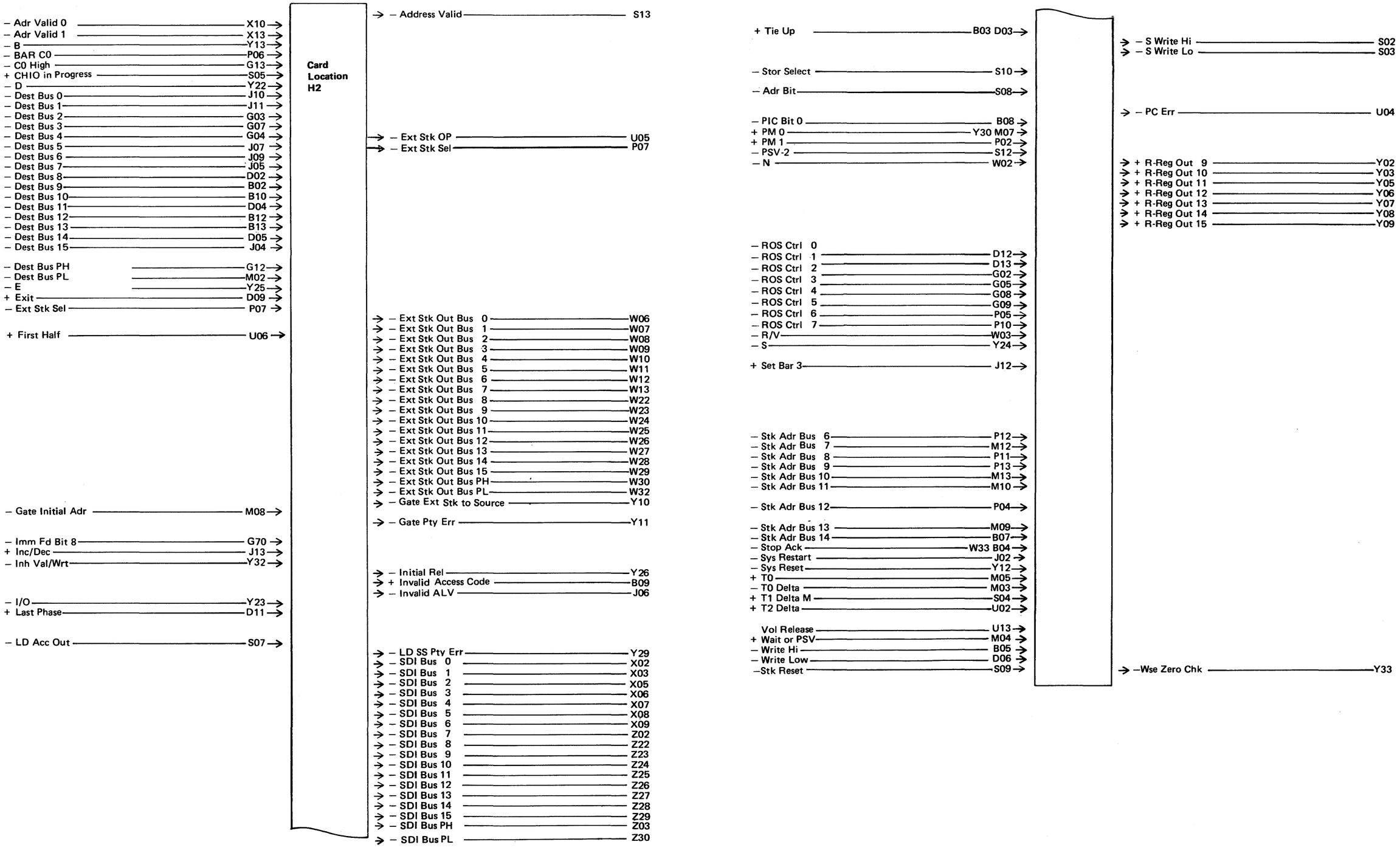

Figure BU421-9. 8130 Adjunct Register Storage Card Logic Signals

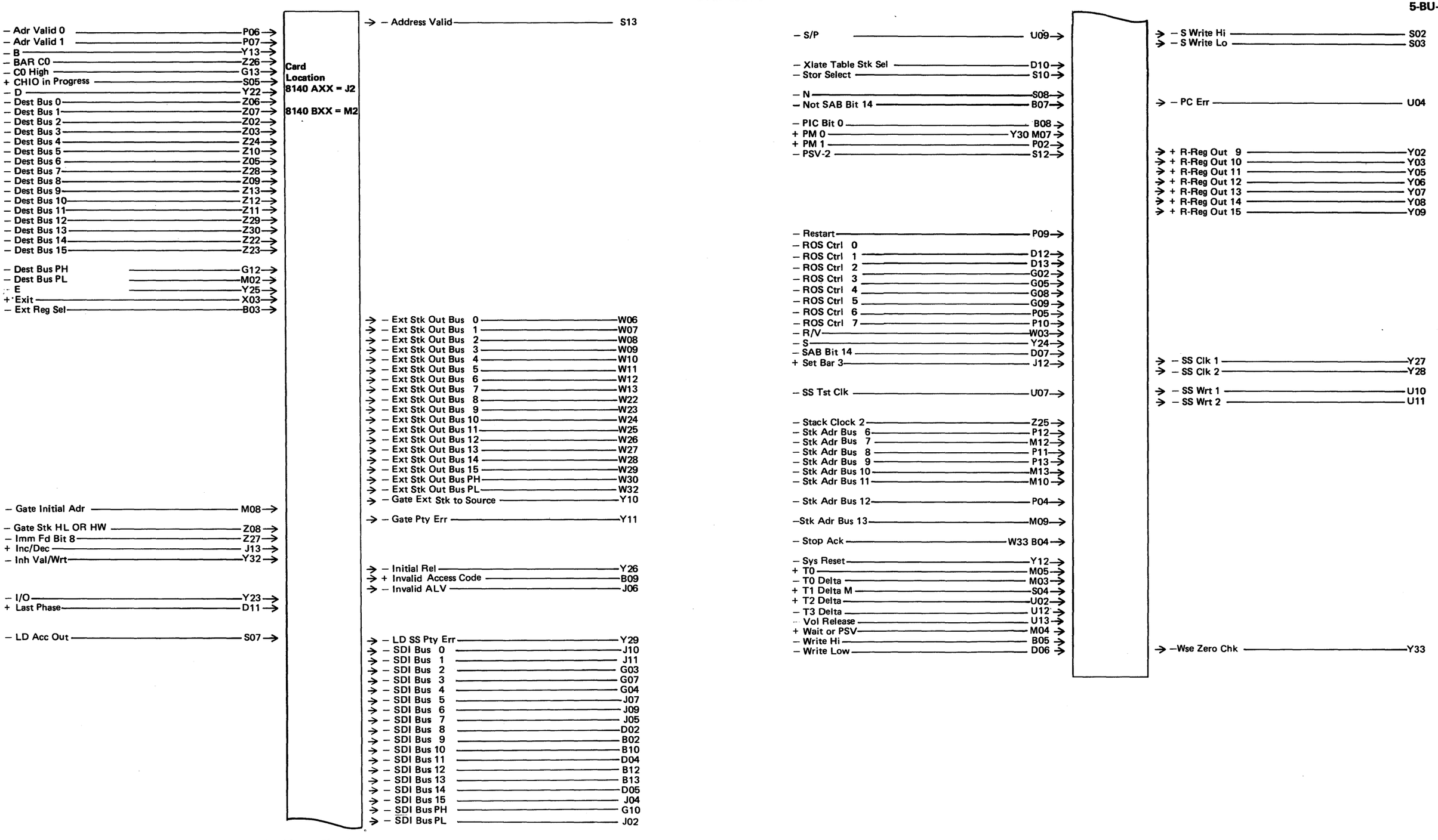

Figure BU421-10. 8140 Adjunct Register Storage Card Logic Signals

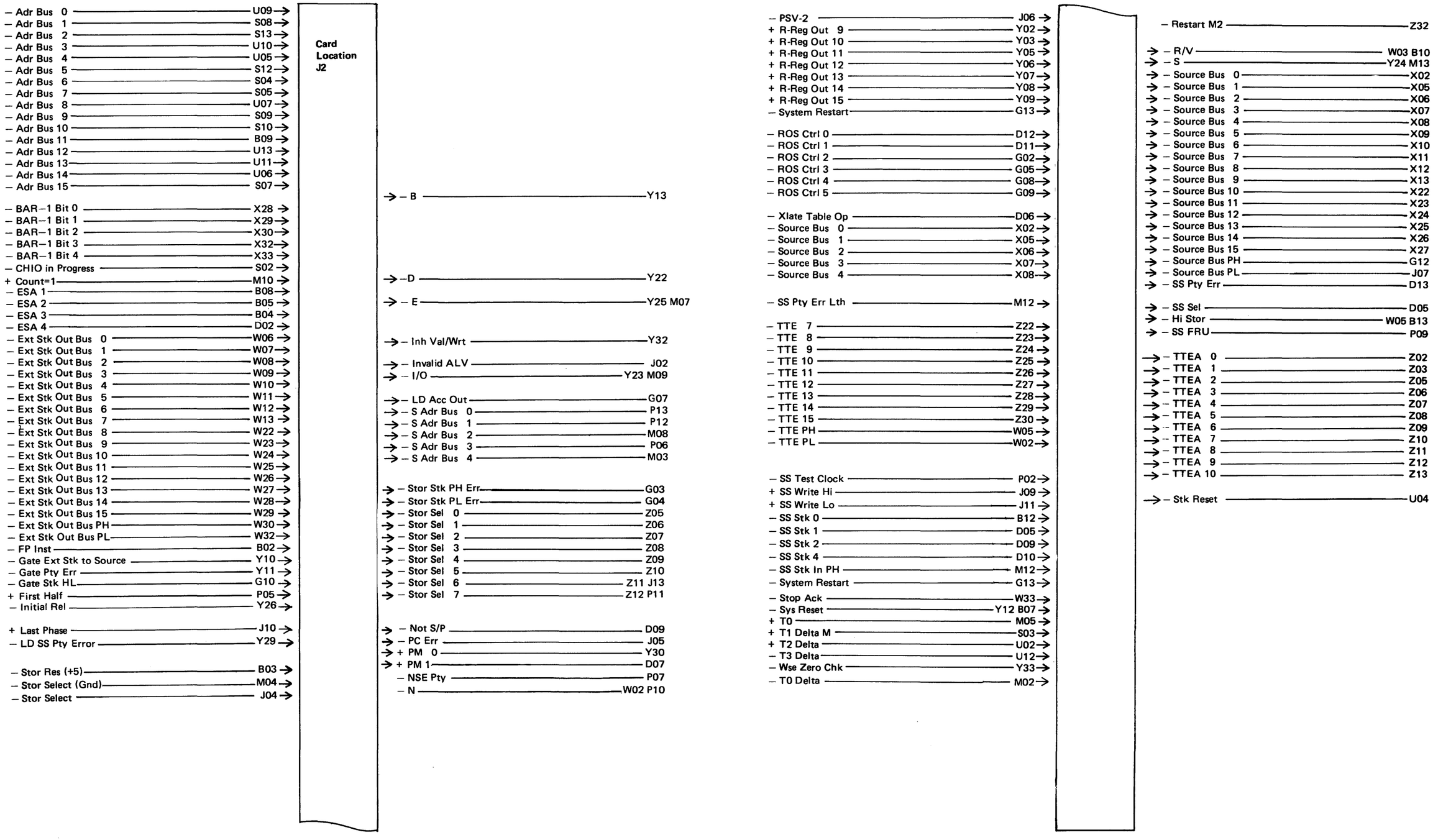

Figure BU421-11. 8130 Storage Addressing Card Logic Signals

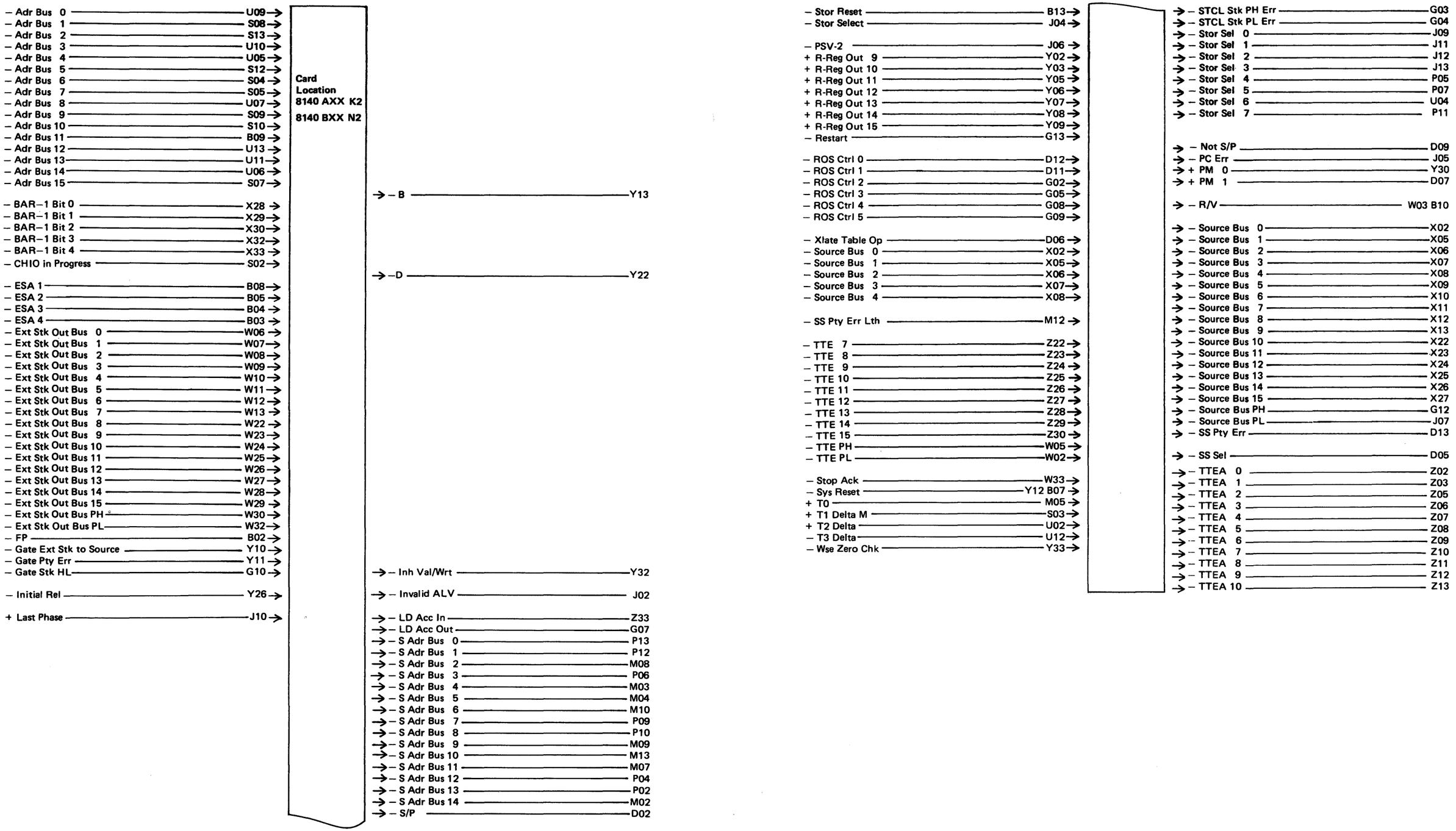

Figure BU421-12. 8140 Storage Addressing Card Logic Signals

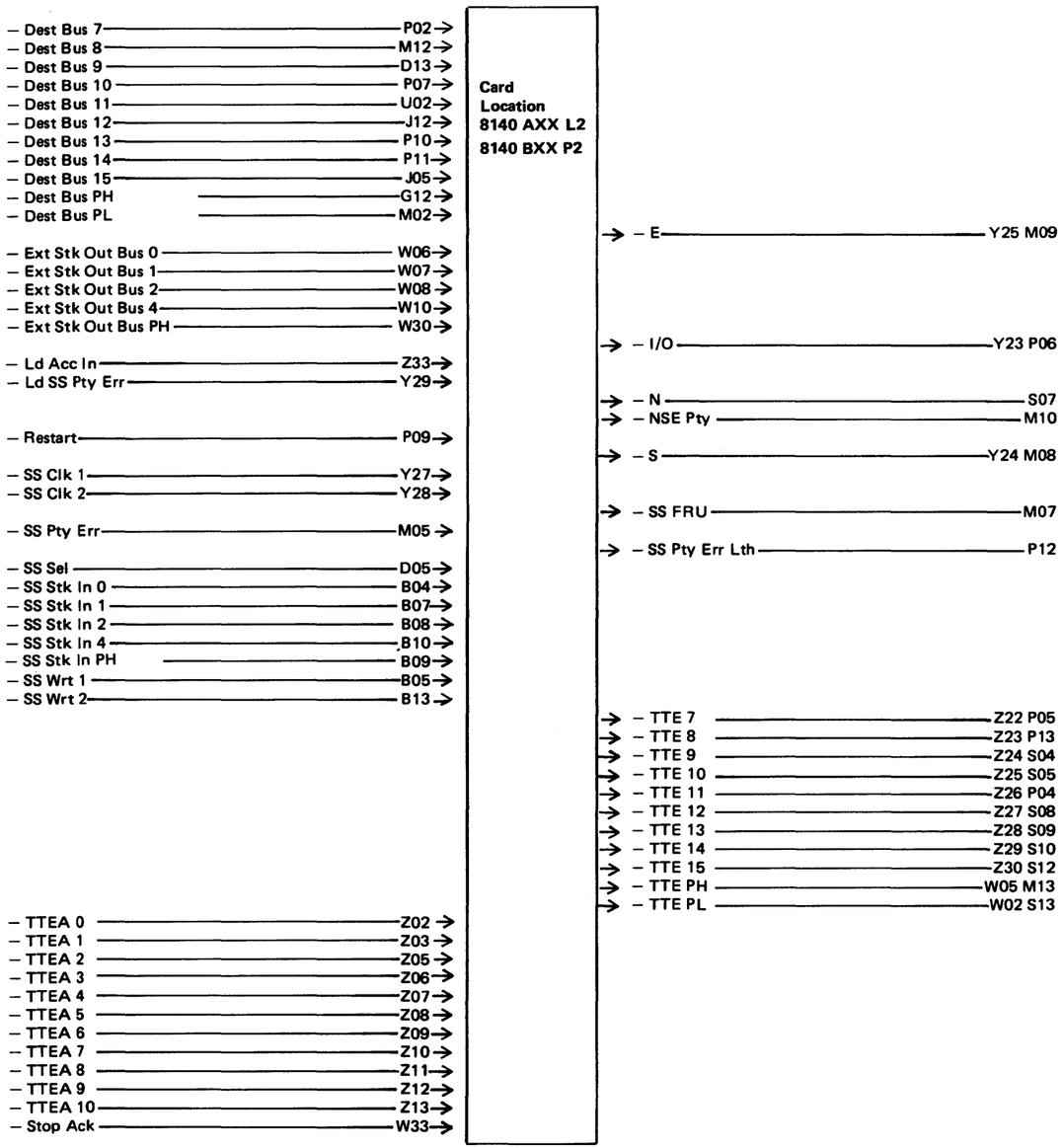

Figure BU421-13. 8140 Translation Table Card Logic Signals

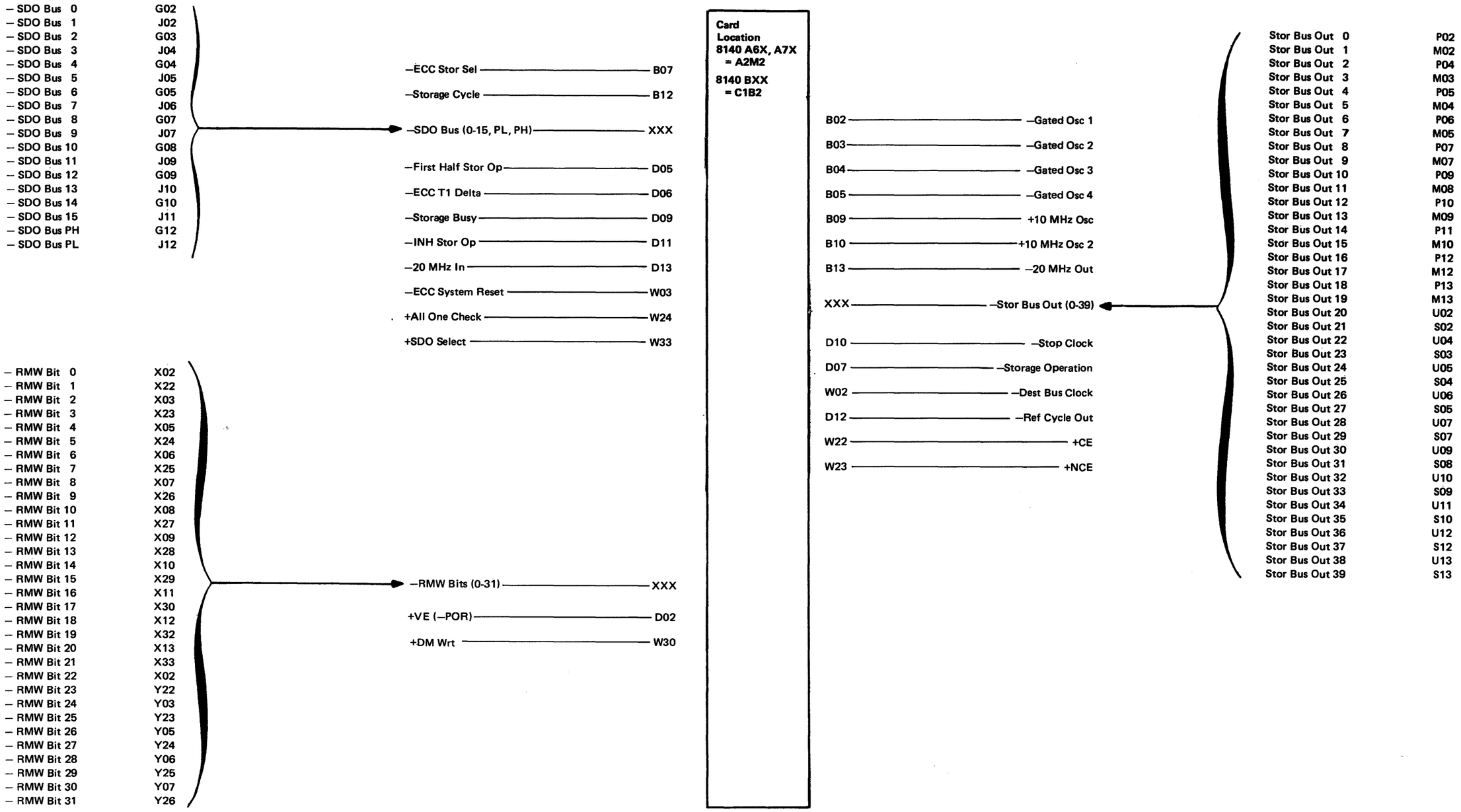

Figure BU421-14. 8140 Models A6X, A7X, and BXX ECC Card 1 Logic Signals

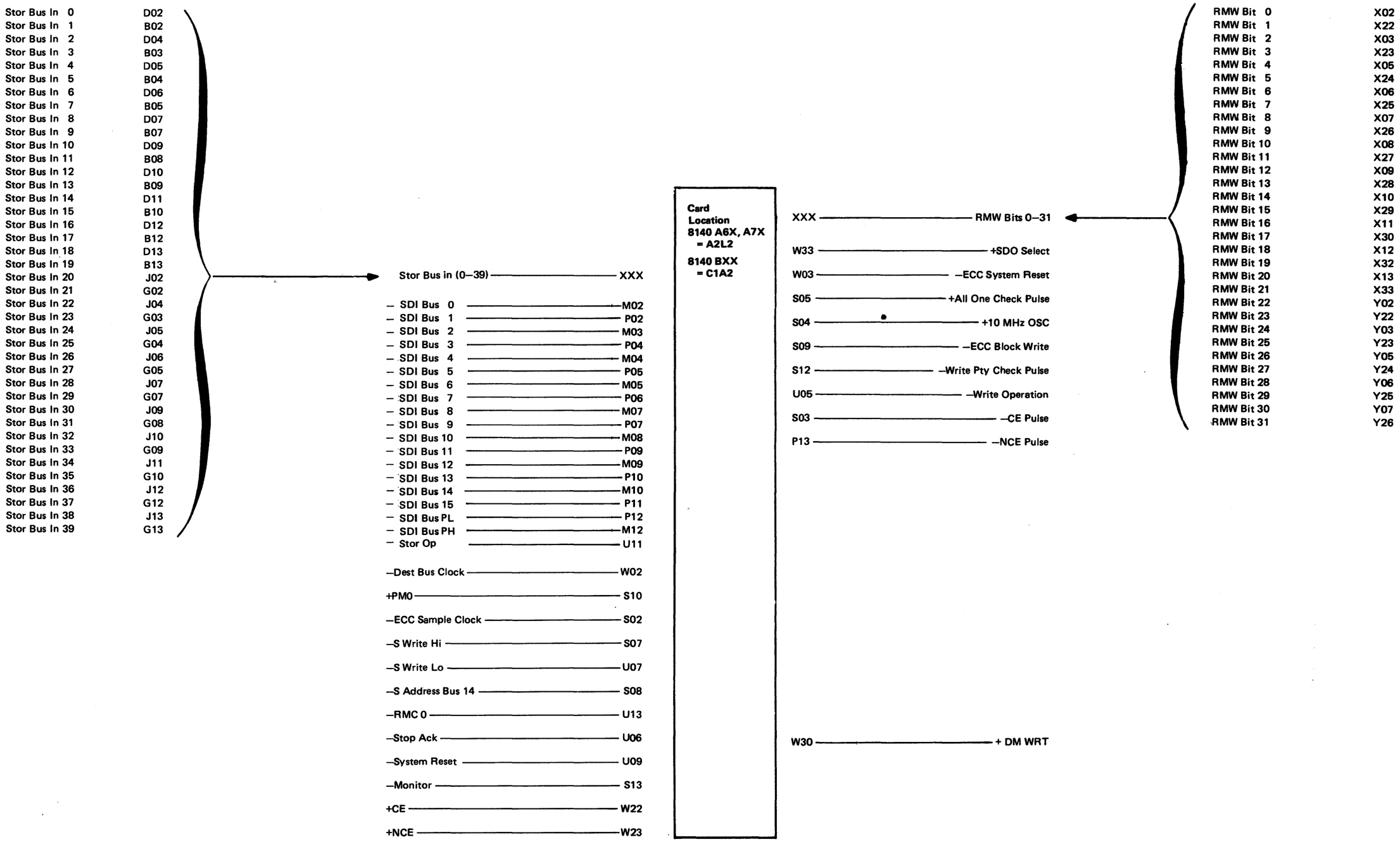

Figure BU421-15. 8140 Models A6X, A7X, and BXX ECC Card 2 Logic Signals

BU422 Storage Card Logic Signals

Refer to Figures BU422-1, BU422-2, and BU422-3 for the 8130/8140 storage card logic signals. See BU111 for card locations.

– Array Select 00	J10	>			
– Array Select 01	J04	>			
– Array Select 10	J12	>			
– Array Select 11	G09	>		> G10	– Address Valid
– Register Select 00	G08	>			
– Register Select 01	J13	>			
– Register Select 10	J07	>			
– Register Select 11	G05	>			
– Card Select	G04	>		> S04	– Array 000
				> U07	– Array 001
– S Adr Bus 0	P11	>		> U06	– Array 002
– S Adr Bus 1	M07	>		> S05	– Array 003
– S Adr Bus 2	P05	>		> S08	– Array 004
– S Adr Bus 3	M02	>		> S07	– Array 005
– S Adr Bus 4	M08	>		> S03	– Array 006
– Word SAR 0	P02	>		> U05	– Array 007
– Word SAR 1	P10	>		> U04	– Array 008
– Word SAR 2	M04	>		> U02	– Array 009
– Word SAR 3	P12	>		> S02	– Array 00A
– Word SAR 4	M10	>		> D12	– Array 010
– Word SAR 5	M12	>		> D11	– Array 011
– Word SAR 6	P09	>		> D13	– Array 012
– Data Gate 1	P13	>		> D10	– Array 013
– Data Gate 2	P06	>		> B09	– Array 014
– Data Gate 3	B12	>		> D09	– Array 015
– Data Gate 4	P07	>		> D07	– Array 016
– Data Gate 5	M09	>		> B10	– Array 017
– Data Gate 6	M05	>		> B08	– Array 018
– Data Gate 7	M03	>		> G02	– Array 019
– Data Gate 8	P04	>		> J02	– Array 01A
– Command A	G12	>		> U09	– Array 100
– Command B, C	J06	>		> U13	– Array 101
– Byte Select 0	J11	>		> U10	– Array 102
– Byte Select 1	J05	>		> S09	– Array 103
				> S13	– Array 104
				> U11	– Array 105
				> S10	– Array 106
				> S12	– Array 107
				> U12	– Array 108
				> B04	– Array 110
				> D02	– Array 111
				> B07	– Array 112
				> D06	– Array 113
				> B05	– Array 114
				> B02	– Array 115
				> B03	– Array 116
				> D05	– Array 117
				> D04	– Array 118

Figure BU422-1. 8130 Read/Write Storage Card Logic Signals

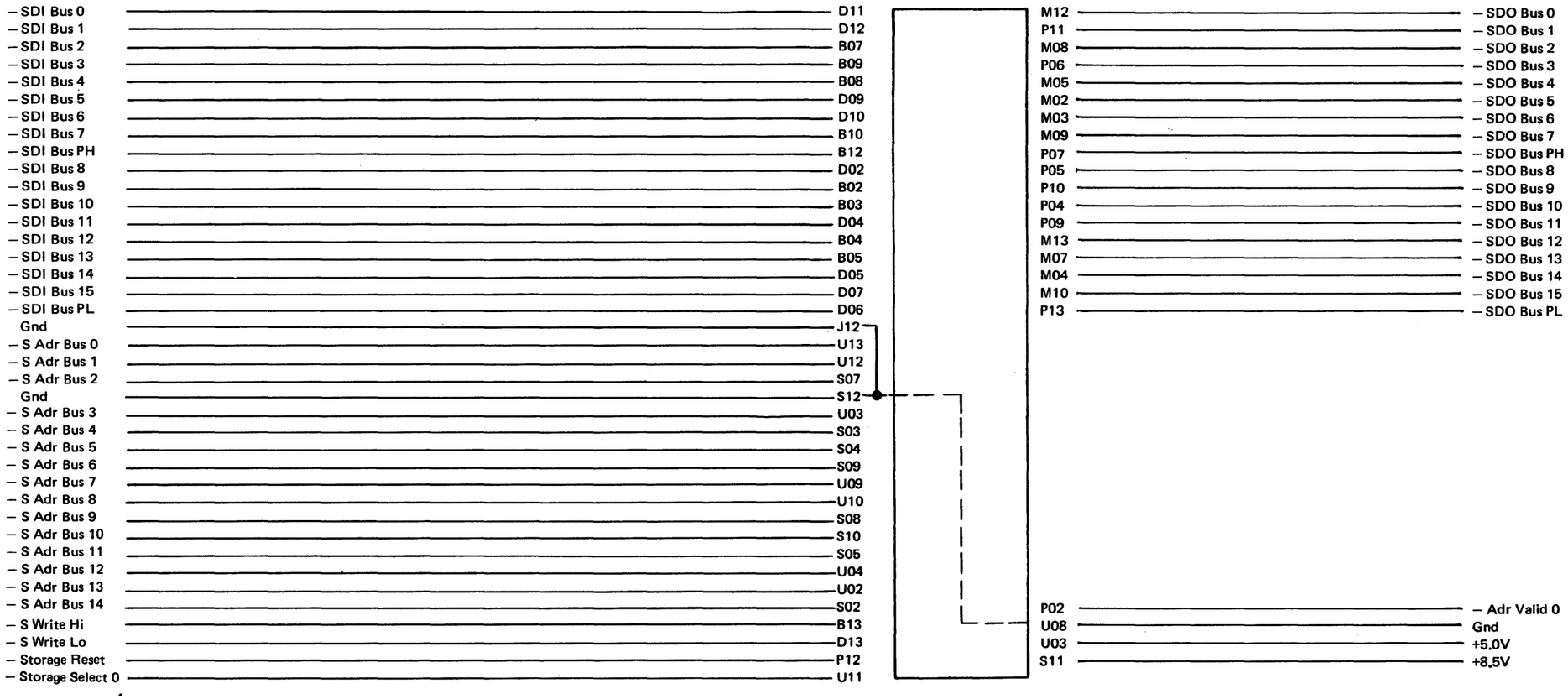

Figure BU422-2. 8140 Models A3X, A4X, and A5X Read/Write Storage Card Logic Signals

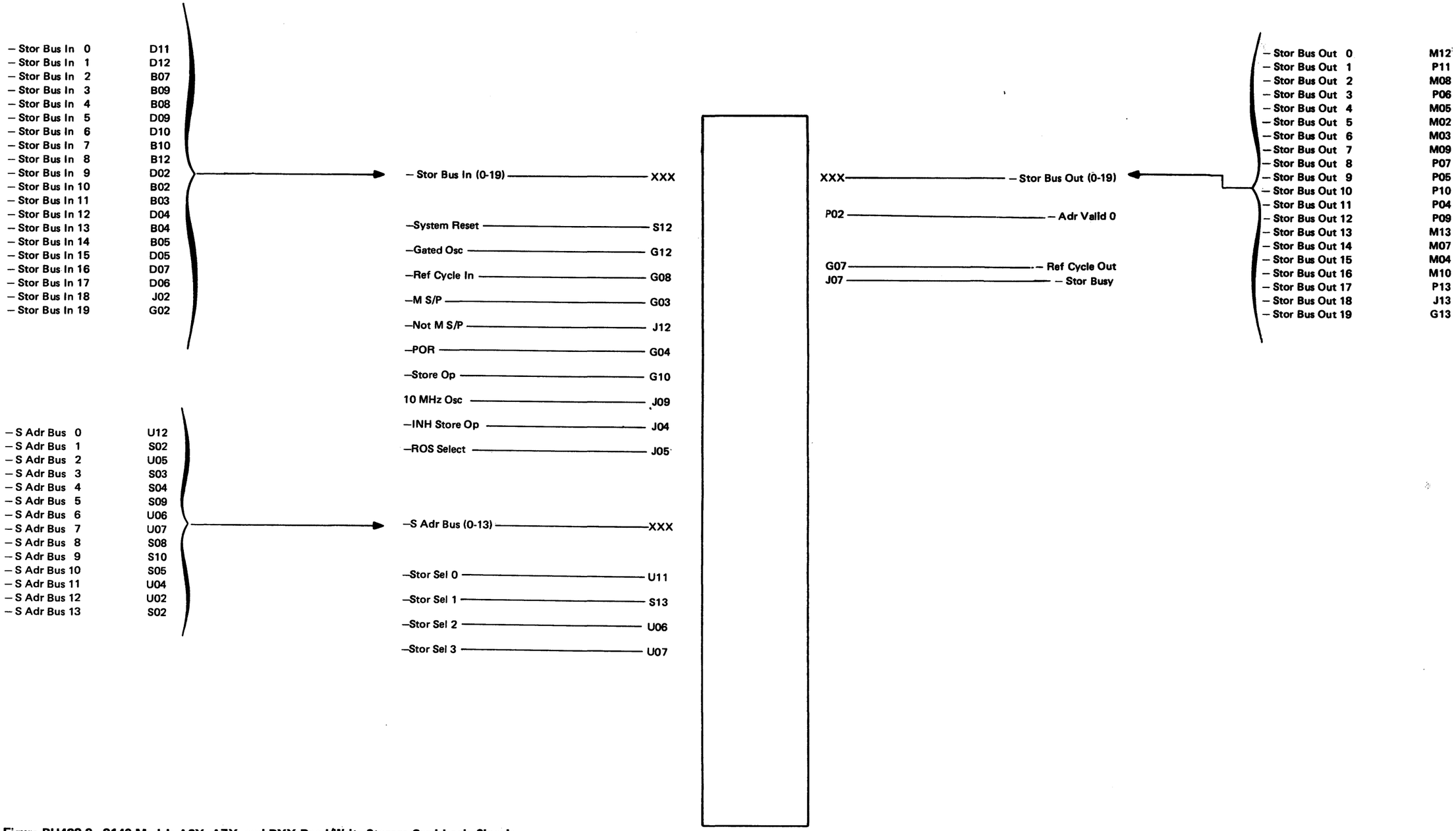

Figure BU422-3. 8140 Models A6X, A7X, and BXX Read/Write Storage Card Logic Signals

BU423 8140 Floating-Point Card Logic Signals

Refer to Figures BU423-1 and BU423-2 for the floating-point control and floating-point fraction logic signals. These cards are present only on 8140 Models A41—A44, 8140 Models A6X and A7X as an RPQ, and 8140 Model BXX as a feature. See BU111 for card locations.

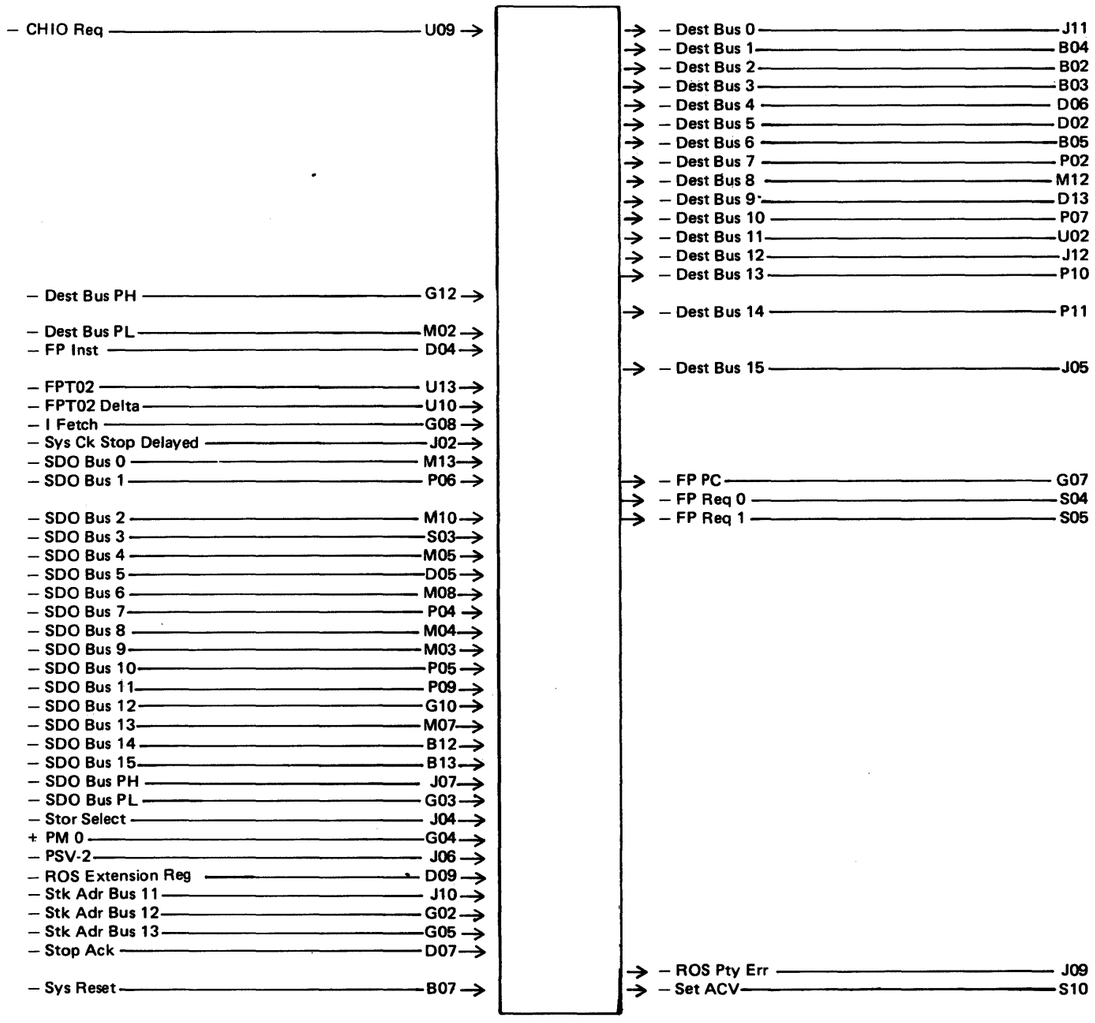

Figure BU423-1. 8140 Floating-Point Control Card Logic Signals

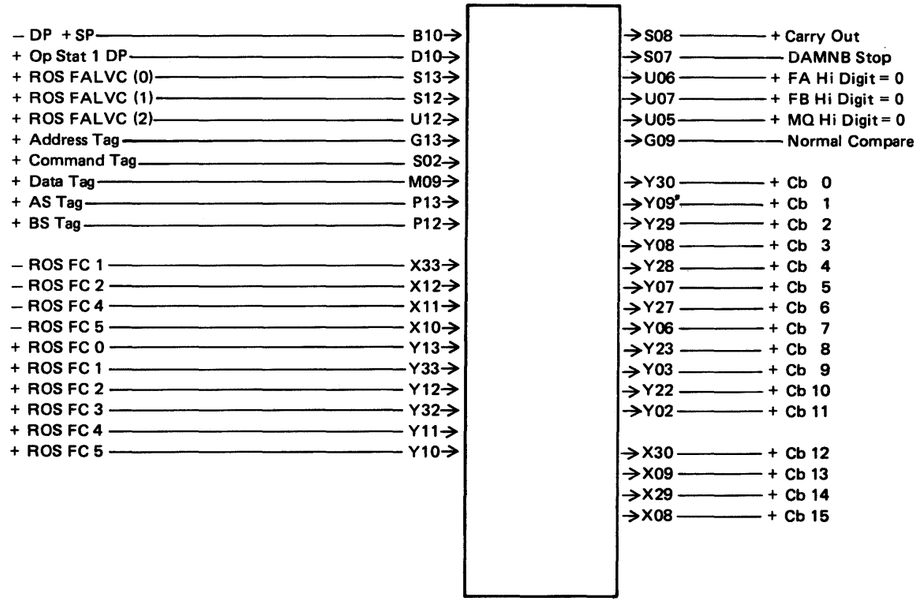

Figure BU423-2. 8140 Floating-Point Fraction Card Logic Signals

BU424 BOP Adapter Card Logic Signals

Figure BU424-1 shows the BOP adapter card and all connected points.

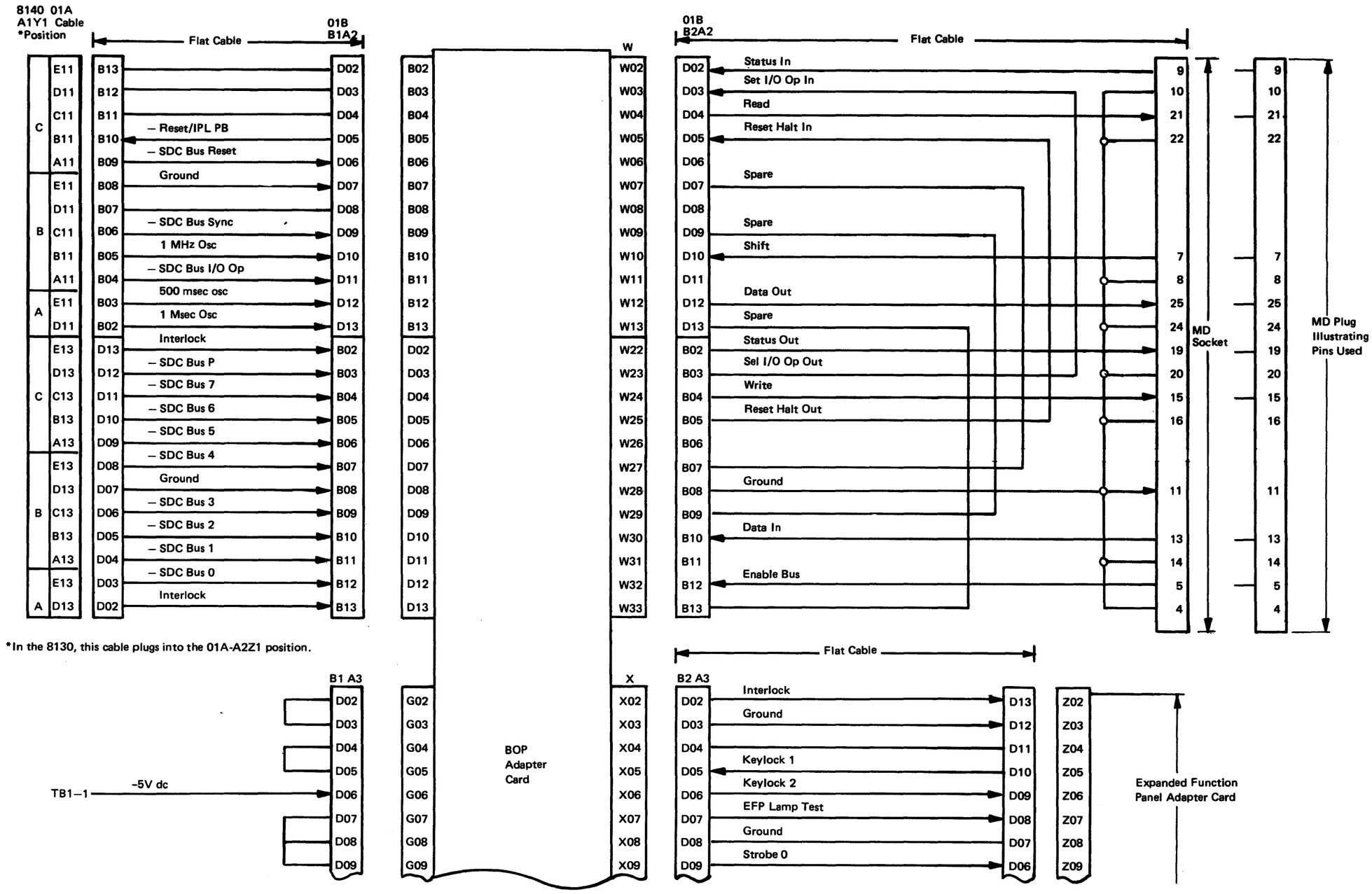

Figure BU424-1 (Part 1 of 3). BOP Adapter Card Point-to-Point Logic Signals

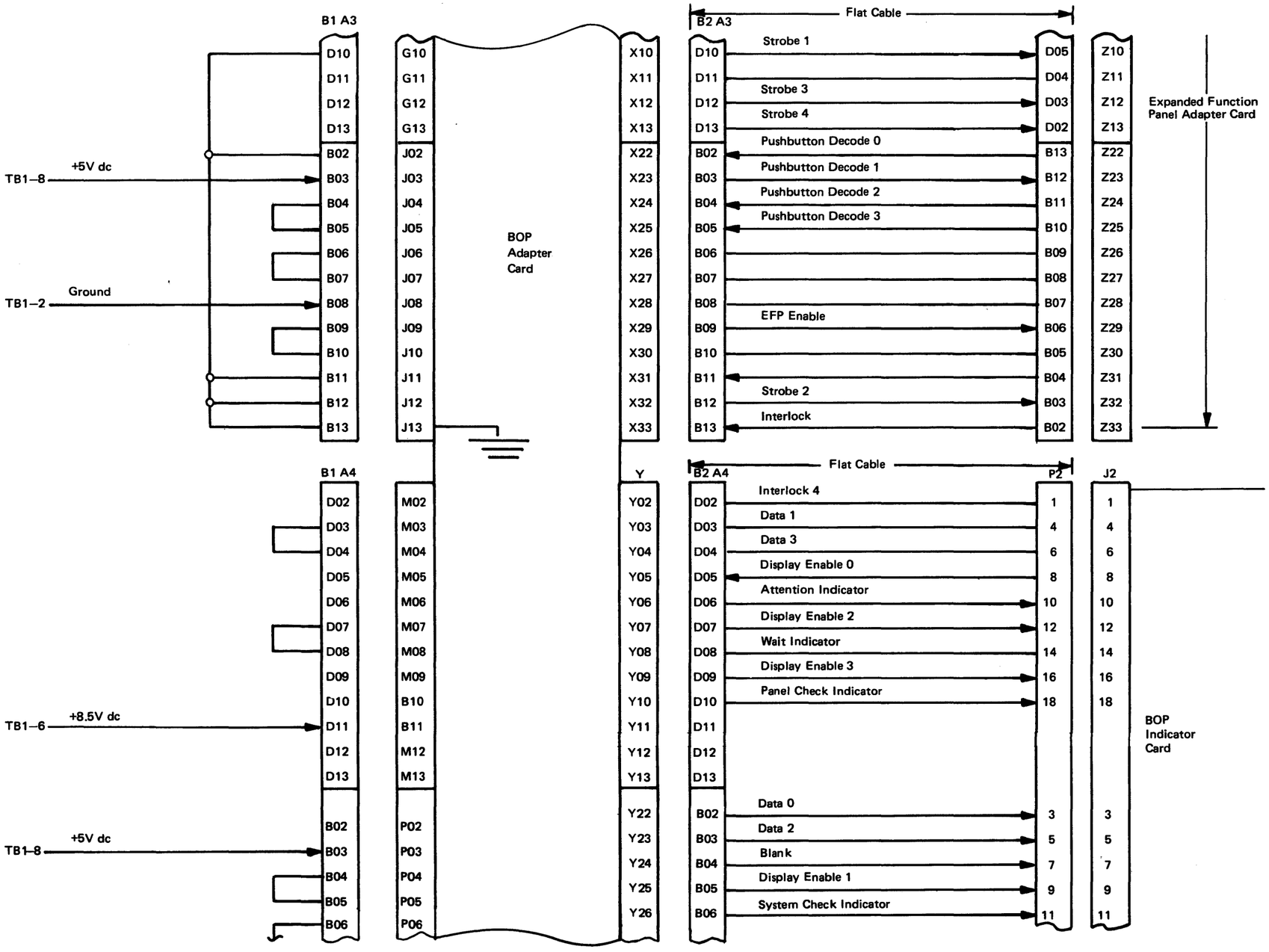

Figure BU424-1 (Part 2 of 3). BOP Adapter Card Point-to-Point Logic Signals

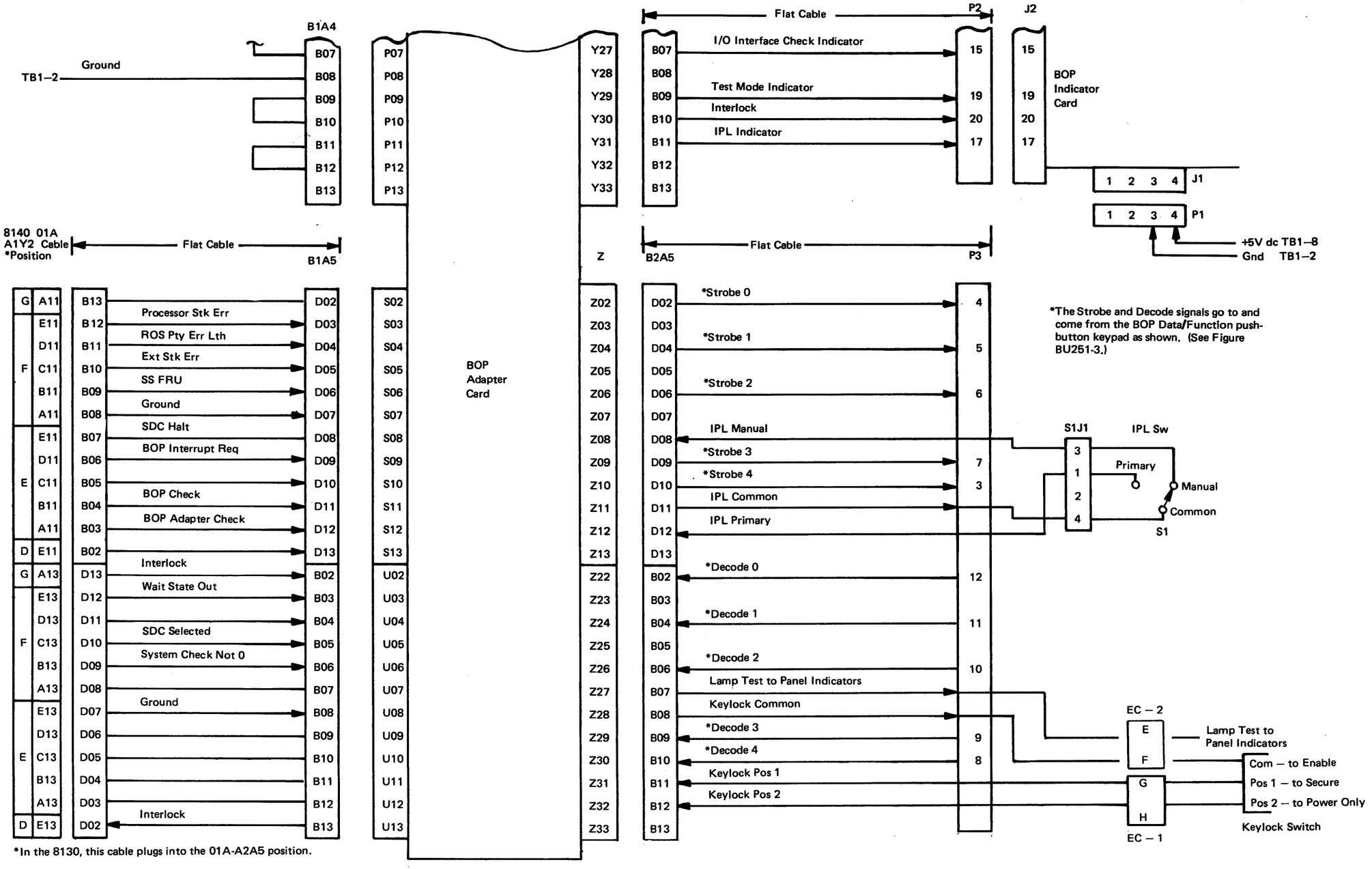

Figure BU424-1 (Part 3 of 3). BOP Adapter Card Point-to-Point Logic Signals

BU450 Processor I/E Unit Card Detailed Description and Data Flow

Sections BU450 to BU480 describe and show information not directly related to fault isolation, but which can aid in further understanding how the processor instruction, execution unit, BOP, and BOP adapter operate. Refer to Figures BU450-1 and BU450-2 for basic processor I/E unit data flow.

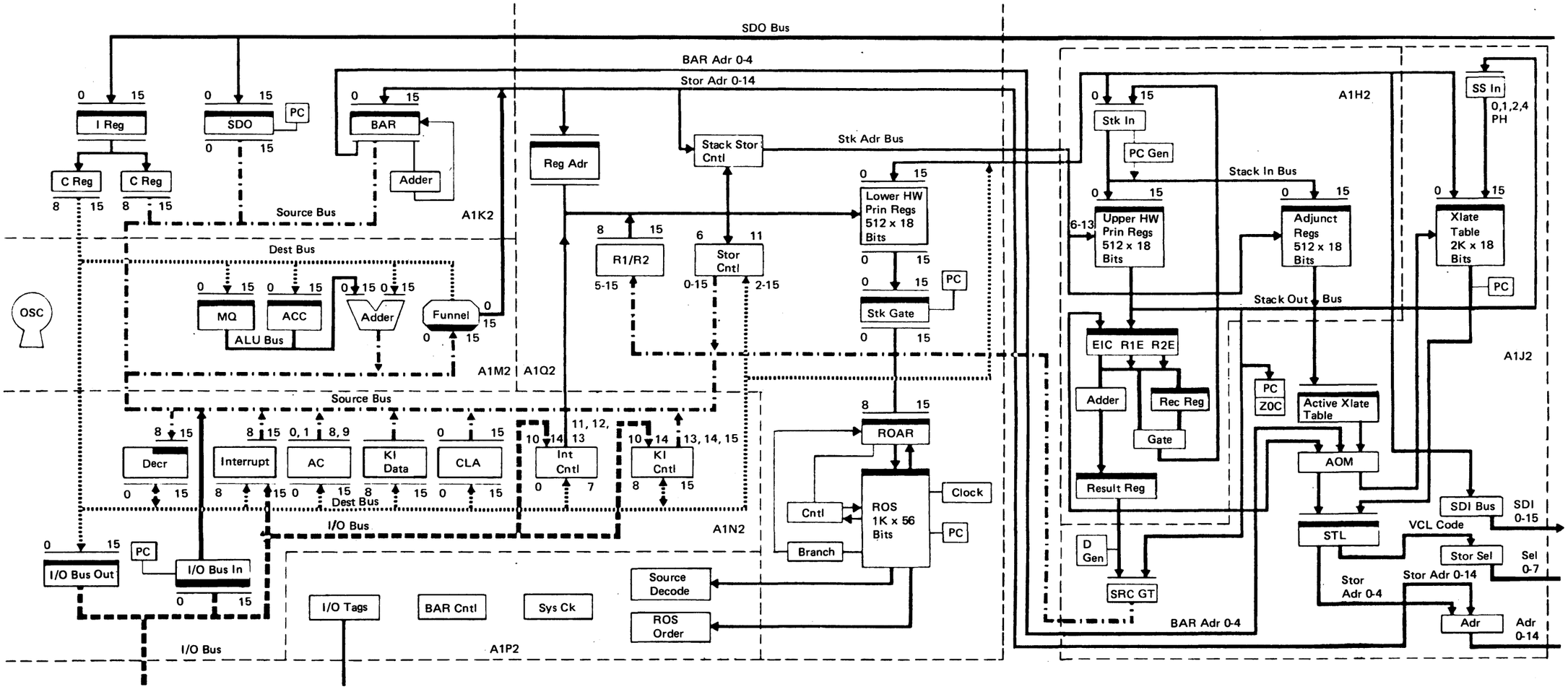

Figure BU450-1. 8130 Processor I/E Unit Detailed Data Flow

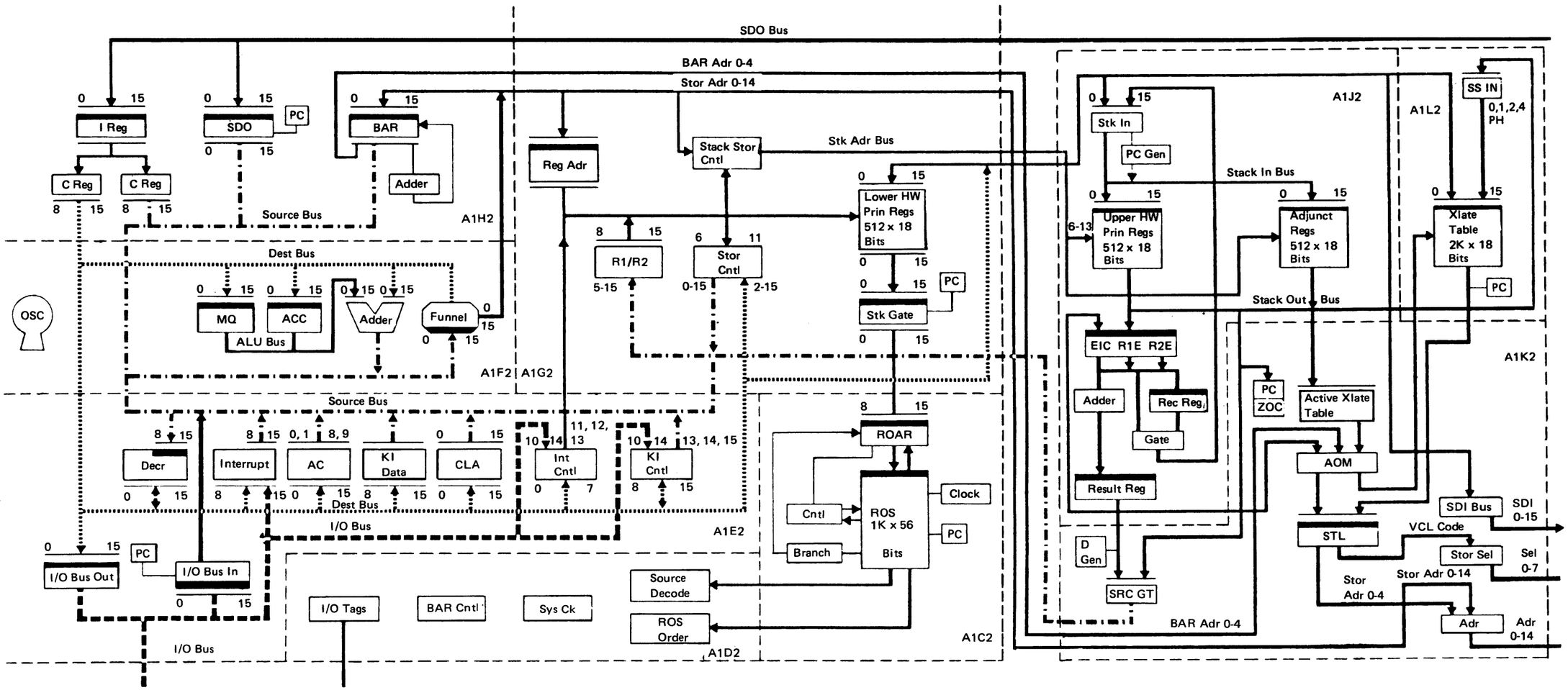

Figure BU450-2. 8140 Processor I/E Unit Detailed Data Flow

BU451 8130/8140 Pico ROS Card

- 8130 Card Location = A1Q2
- 8140 Models AXX Card Location = A1C2
- 8140 Models BXX Card Location = A1F2

This card contains the following major functions:

- 56 bit x 1K ROS — This as well as other processor I/E unit cards decode the bit values of the various ROS fields used to control all processor operations.
- Clock generation — Generates four 100-ns pulses (T0, T1, T2, and T3), and also generates four other 100-ns pulses (T0—T3 delta) by delaying the T0—T3 pulses by 50 ns. These are used as the basic processor clocking pulses.
- ROS address register (ROAR) — The 1024 ROS patterns containing the information necessary to execute processor functions and to generally control processor operation.
- Clock extension (8130 ONLY) — Refer to Figure BU451-1 for the following explanation. Due to the nature of the regenerative storage used in the 8130, storage access time can be delayed if access is requested during a refresh cycle. For this reason, and because of the different access times between processor storage and register storage, it is sometimes necessary to extend the clock pulse duration. This is done by a decode of the 3-bit clock control field in each ROS pattern. Using this decode, the clock pulses can be selectively extended so that the clock sequence remains the same, but the overall machine cycle is increased.

Refer to Figures BU451-2 and BU451-3 for pico ROS card data flow.

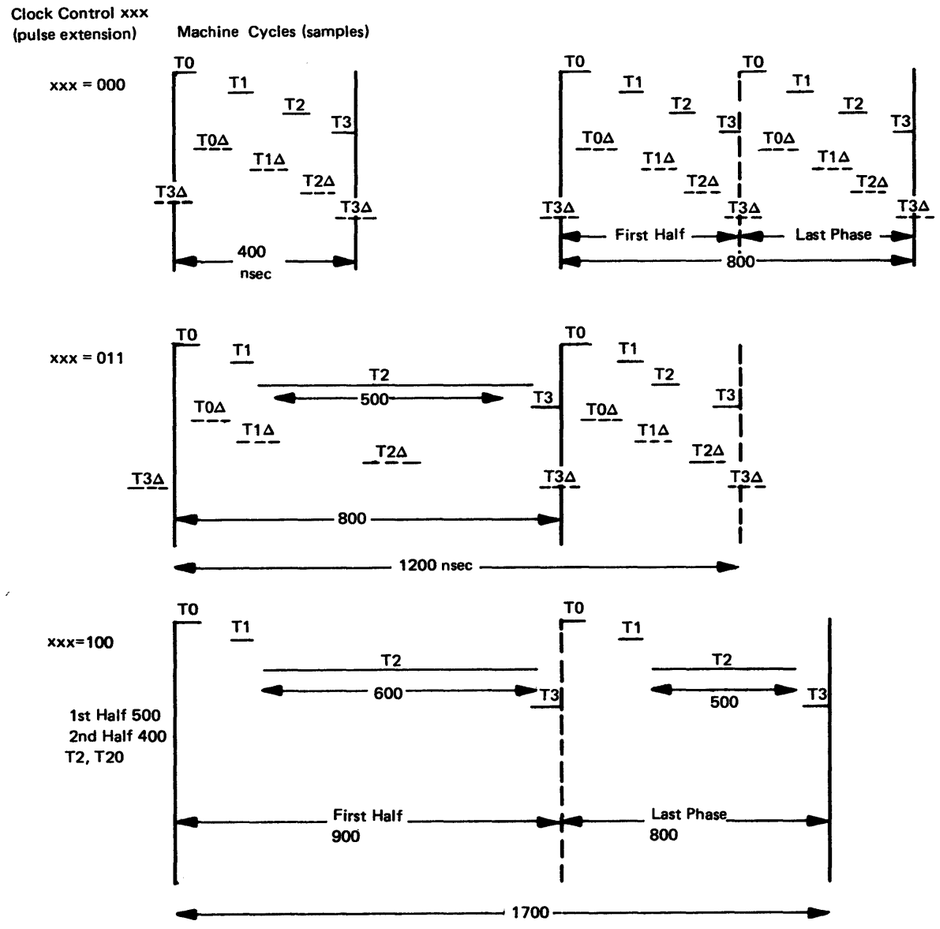

Figure BU451-1. 8130 Storage Delay Clock Pulse Timing

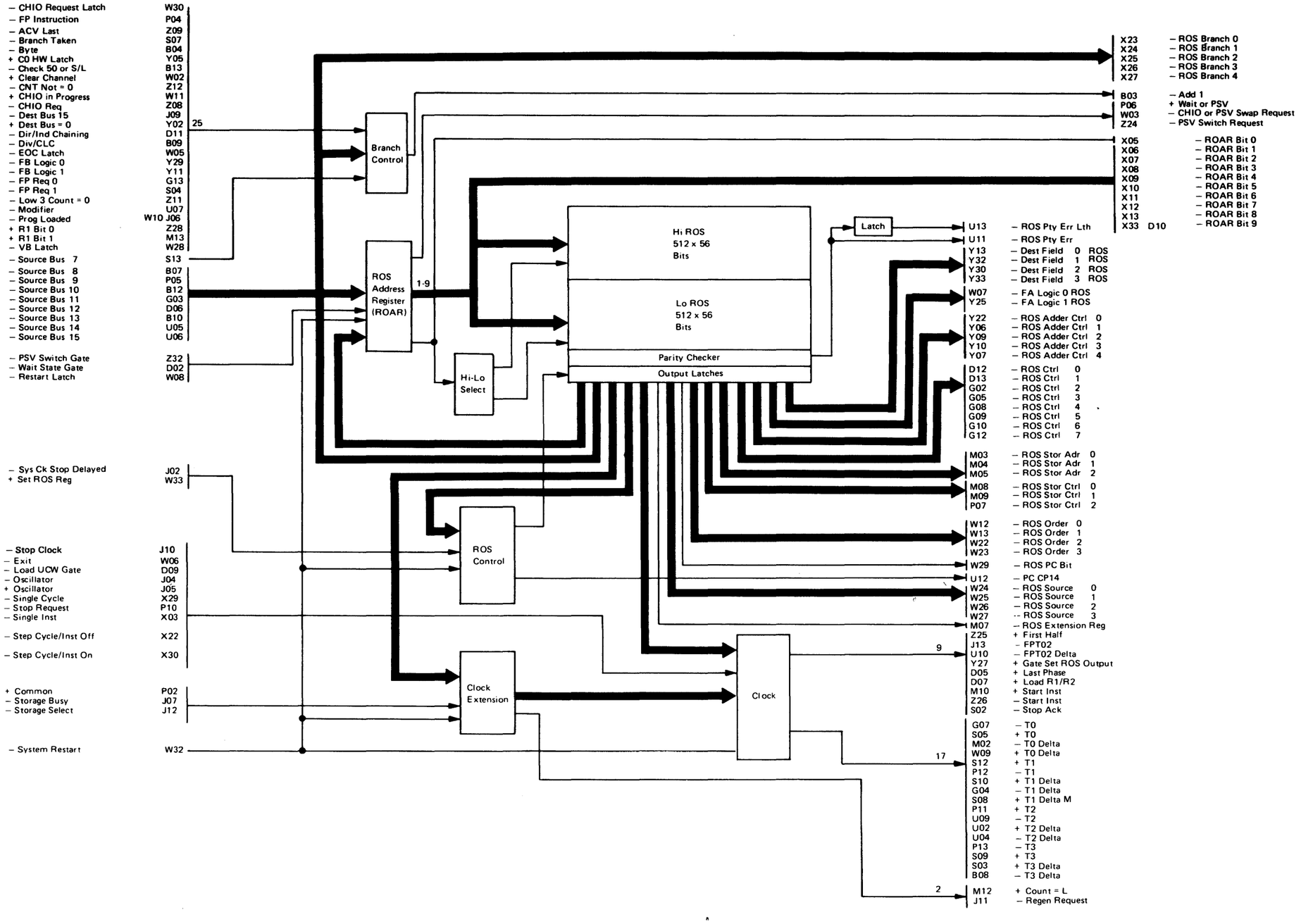

Figure BU451-2. 8130 Pico ROS Card Data Flow

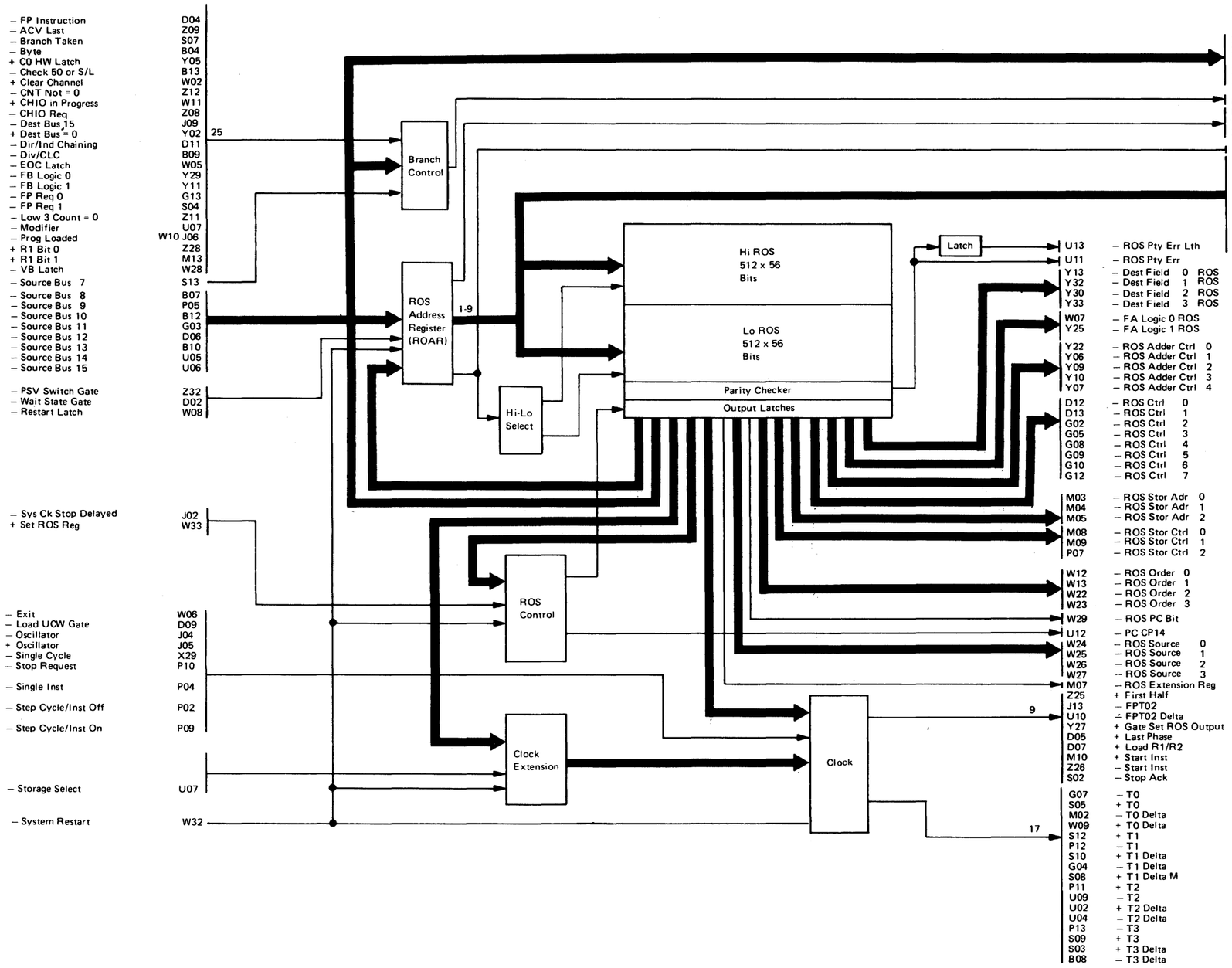

Figure BU451-3. 8140 Pico ROS Card Data Flow

BU452 8130/8140 Pico ROS Decode and EIRV Card

- 8130 Card Location = A1P2
- 8140 Models AXX Card Location = A1D2
- 8140 Models BXX Card Location = A1G2

This card contains the following major functions:

- Buffer address register (BAR) controls
- I/O tag controls
- System check logic
- Program information code (PIC) bits
- ROS order decode and source decode logic that perform decoding operations on four ROS bits.

Refer to Figure BU452-1 for pico ROS decode and EIRV card data flow.

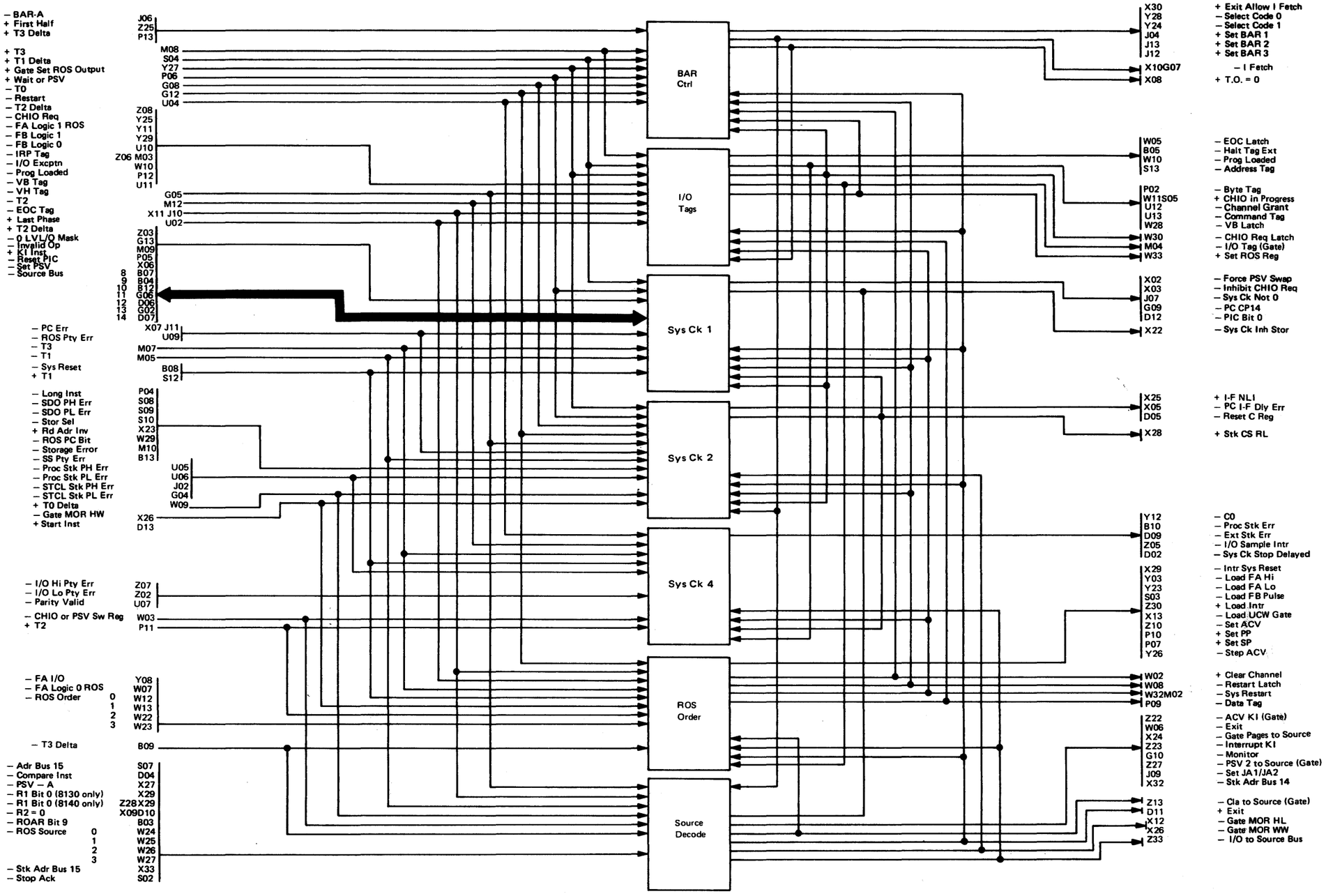

Figure BU452-1. 8130/8140 Pico ROS Decode and EIRV Card Data Flow

BU453 8130/8140 I/O and Interrupt Card

- 8130 Card Location = A1N2
- 8140 Models AXX Card Location = A1E2
- 8140 Models BXX Card Location = A1H2

This card contains the following major functions:

- Interrupt logic registers
- Condition code setting and gating of the I/O bus
- Carry lookahead (CLA) adder used in shift and rotate instructions
- 8-bit count register (DECR) used in move instructions
- CHCV bits of the PSV. Bits 4–7 of the I register (mask field for branches and jumps) are decoded to determine if a branch should occur.
- U21–U24 logic that primarily converts logic levels. U24 is also used to load the I/O bus from the destination bus.
- MEG logic that gates the I/O bus to the source bus.

The interrrupt and interrupt control logic uses the programmed interrupt request vector (PIRV), I/O interrupt request vector (IOIRV), and common mask to determine when an interrupt should occur.

The control immediate (KI) instruction logic contains most of register storage. The KI logic decodes the 8 low-order bits of the destination bus during a KI instruction, and activates the appropriate control lines. The KI data logic contains a register that has a bit for each interrupt level, which determines whether the primary or secondary program status vector should be used.

Refer to Figure BU453-1 for I/O and interrupt card data flow.

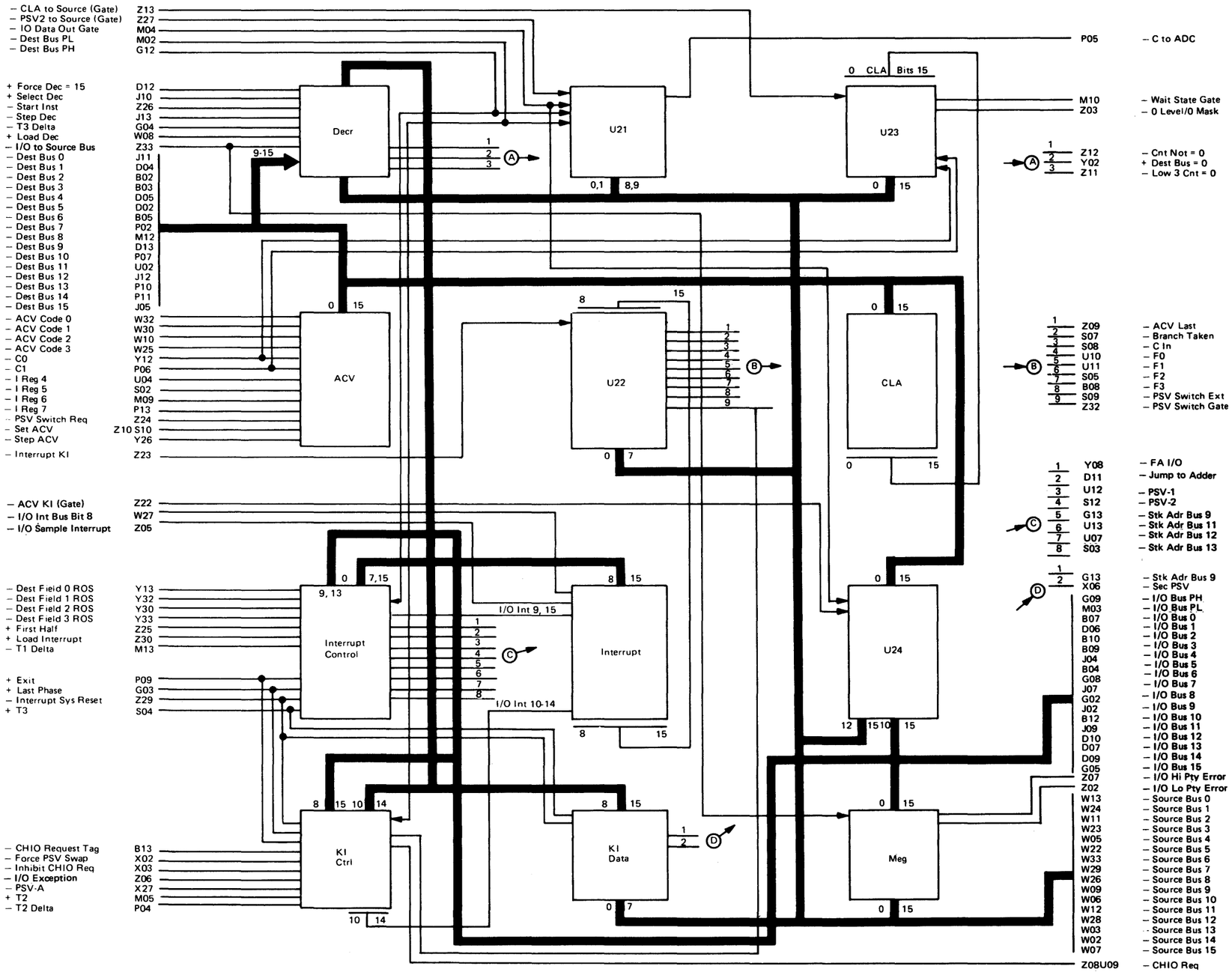

Figure BU453-1. 8130/8140 I/O and Interrupt Card Data Flow

BU454 8130/8140 Arithmetic and Oscillator Card

- 8130 Card Location = A1M2
- 8140 Models AXX Card Location = A1F2
- 8140 Models BXX Card Location = A1J2

This card performs most of the arithmetic and logical functions of the processor instruction/execution unit. It contains the funnel, parallel adder, and their associated controls.

- Funnel – Two 16-bit halfwords (FA and FB), either of which can be loaded from the source bus. The contents can then be AND'ed, OR'ed, or exclusive OR'ed with the source bus, and the results then gated to the destination bus. The low-order eight bits of the FA halfword can be gated to the high-order eight bits of the FB halfword, and the low-order eight bits of the FB halfword can be gated to the high-order eight bits of the FA halfword. The funnel control logic regulates funnel operation, which decodes four ROS bits, as well as other signals.
- Adder – Two 16-bit halfwords (adder A and adder B) used for inputs. Adder B can be loaded from either the funnel outputs or the destination bus in either true or complement form. Adder A can be loaded from the MQ and accumulator registers in true form only.
- Accumulator and MQ registers – Loaded from either the funnel or the destination bus. MQ is used mainly for multiply and divide operations. The accumulator can also hold an intermediate result initially sent from the adder to the funnel.

The adder control logic regulates accumulator and MQ register gating. This logic also decodes five ROS bits, the address control vector (ACV), and other signals.

Refer to Figure BU454-1 for arithmetic and oscillator card data flow.

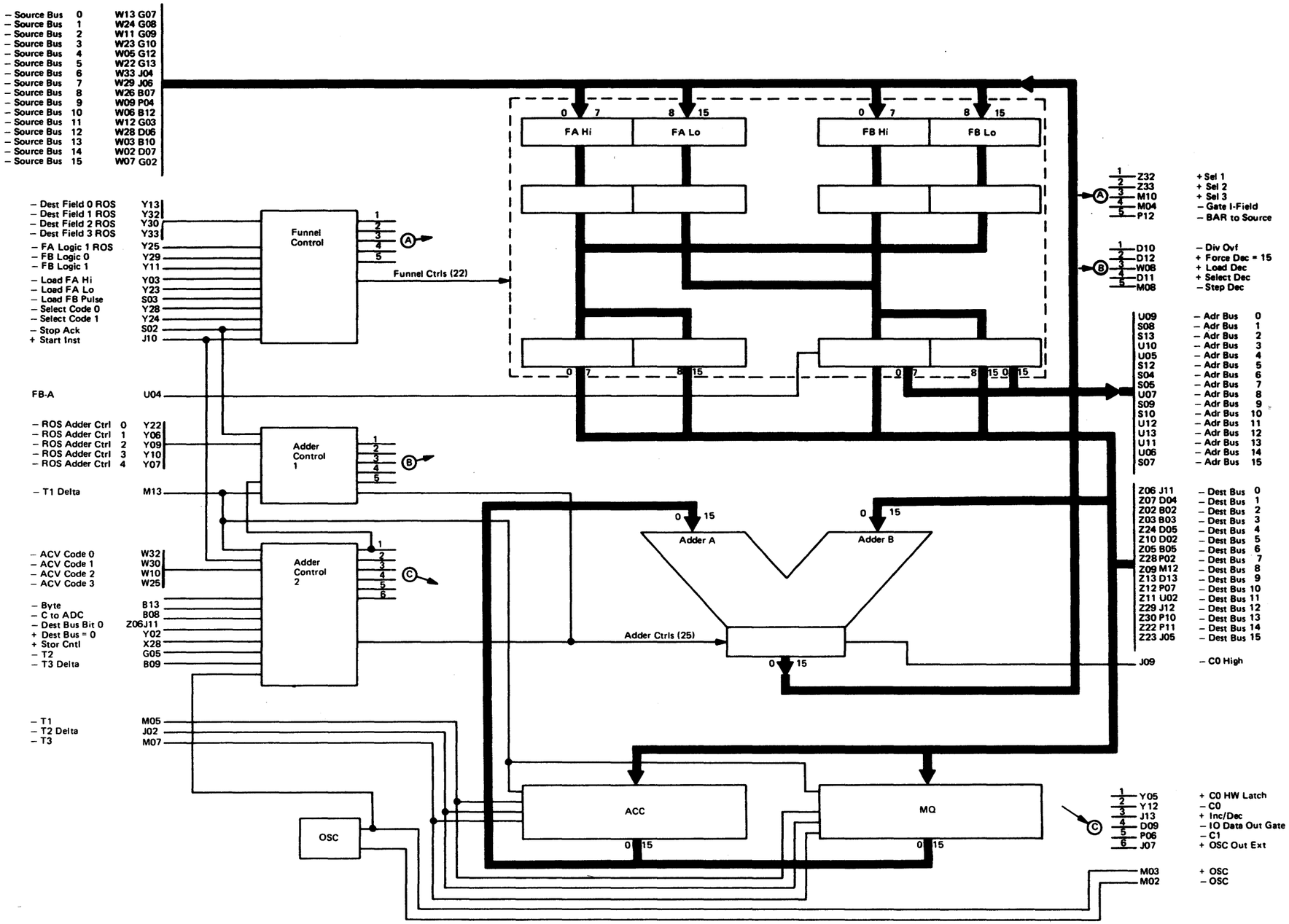

Figure BU454-1. 8130/8140 Arithmetic and Oscillator Card Data Flow

BU455 8130/8140 Register Storage Card

- 8130 Card Location = A1L2
- 8140 Models AXX Card Location = A1G2
- 8140 Models BXX Card Location = A1K2

This card contains the following major functions:

- Principal register storage (512 x 18).
- Program interrupt request vector (PIRV) used to determine the primary or secondary program status vector (PSV).
- R1, R2, and R3 registers.
- Control logic used to gate the source of both the stack address bus (SAB) and the storage address bus.
- Encode logic and registers used for the program exception code (PEC) bits of the PSV.

The R1 and R2 registers hold either the R1 and R2 operands of an instruction, or the address of the channel control vector (bits 8—15) that specifies which register contains the channel pointer used for a channel I/O (CHIO) data transfer.

Combining the low-order bits of the logical address with the address base field of the address control vector (ACV) forms the actual address of the register used as part of the instruction. The address base field actually specifies the register number within the register set, and has no significance during a CHIO operation. Instead, the R1 and R2 register contents combine to form the register address used during a CHIO operation. The I/O bus loads the source bus, which is contained on the I/O and interrupt card (8130 = A1N2, 8140 Models AXX = A1E2, 8140 Models BXX = A1H2). The source bus then loads the R1 and R2 registers used during a CHIO operation.

Decoding the three ROS storage address bits determines the gating of both the stack address bus and the address bus used for this and other processor instruction/execution cards. Decoding the three ROS storage control bits determines the operation to be performed, such as a write to processor storage or a read to the principal registers.

The program exception code (PEC) bits represent the binary value for conditions that cause a program exception, such as an invalid operation or an address exception condition. These bits are gated to destination bus bits 11—13 during a PSV swap, which occurred as the result of program exception, and are saved in primary PSV bits 43—45 respectively.

Refer to Figures BU455-1 and BU455-2 for register storage card data flow.

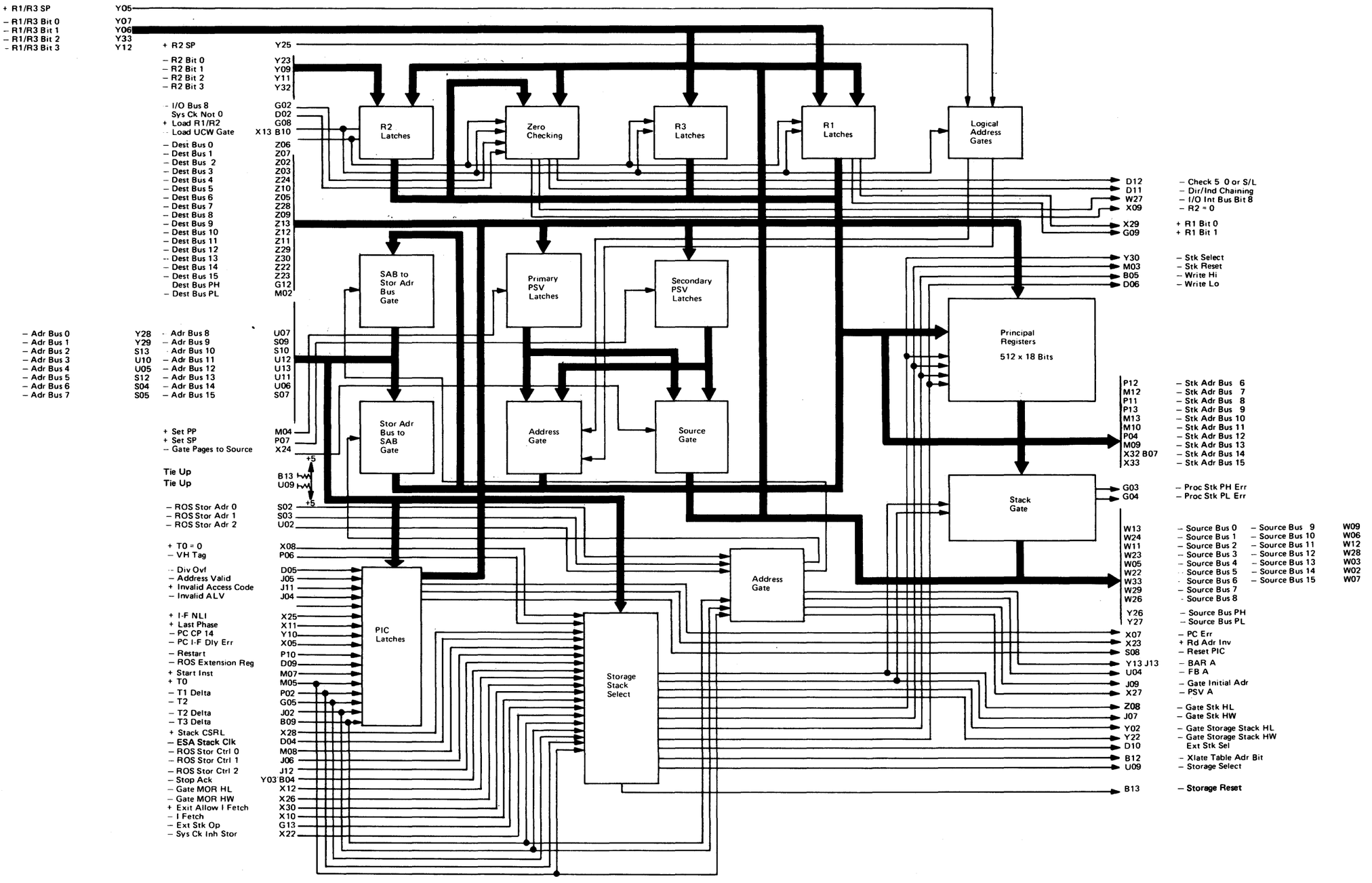

Figure BU455-1. 8130 Register Storage Card Data Flow

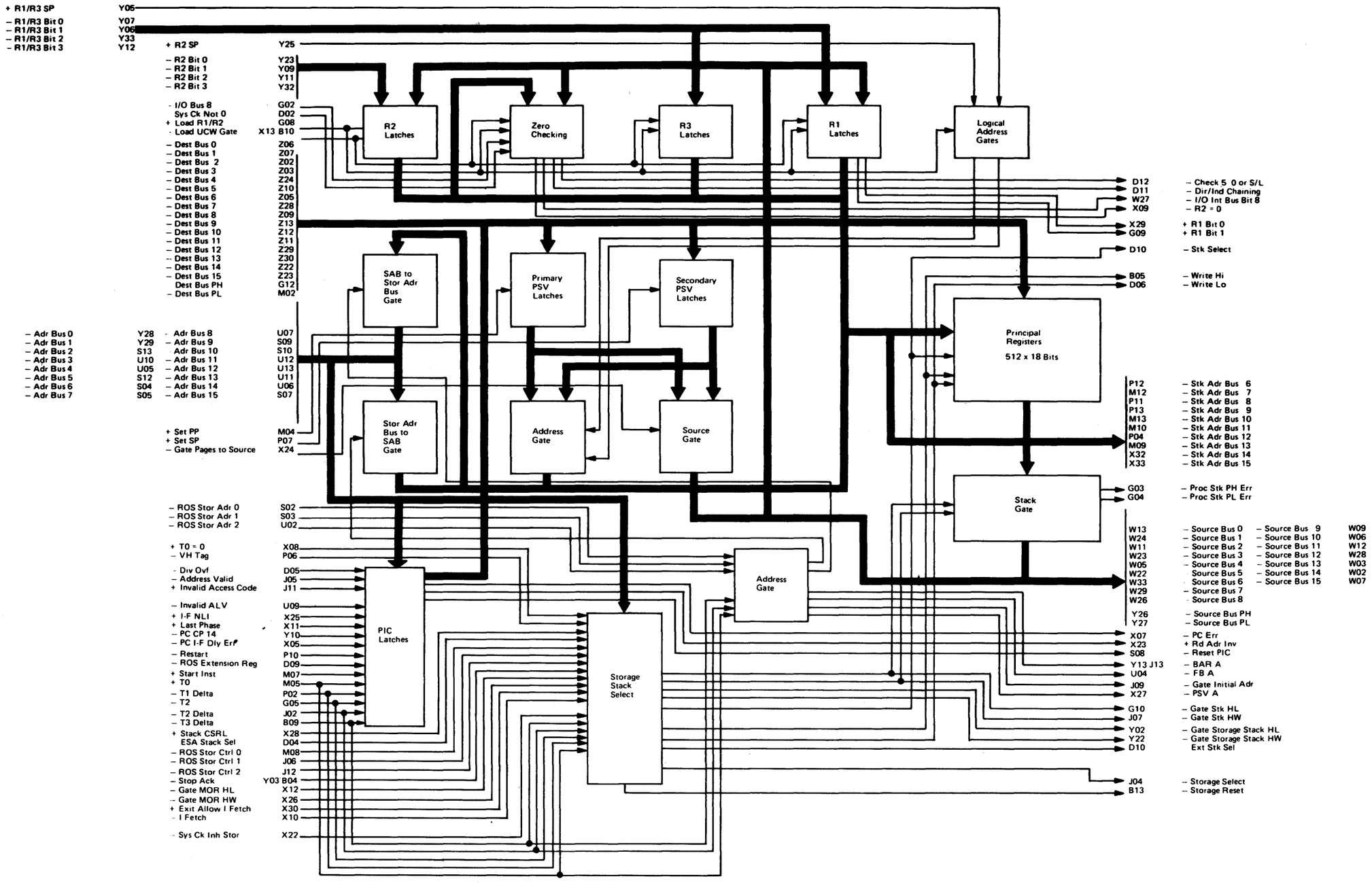

Figure BU455-2. 8140 Register Storage Card Data Flow

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BU456 8130/8140 Instruction Decode Card

- 8130 Card Location = A1K2
- 8140 Models AXX Card Location = A1H2
- 8140 Models BXX Card Location = A1L2

This card contains the following major functions:

- Instruction address registers and their associated adder, instruction register, and instruction decode registers.
- Checks the storage data out bus for correct (odd) parity, which can then be gated to either the I register or the source bus.

There are three instruction address registers: BAR 1, 2, and 3.

- BAR 1 can be loaded from either the address bus, BAR 3, or the updated address from the adder. Bits 4–7 of this register are gated to the storage addressing card (see BU457) to determine the actual address used.
- BAR 2 loads from BAR 1, and the BAR 2 output then gates to the address bus, BAR 3, and the adder for updating.
- BAR 3 contains an address that is not updated, and which is used for error recovery. The adder either increases the address to a value that is one or two locations higher than the original value, or adds the immediate field from a jump instruction.

When BARs 1–3 are used during channel I/O (CHIO) operations, BAR 3 contains the current instruction address. Single byte CHIO operations use the +1 function of the adder.

The adjunct register storage card (BU458) receives a carryout from the adder, which is also added to the extended instruction address register value.

Storage data out bus bits 0–15 load into the instruction register, and are gated by the '–set JA1/JA2' signal. The instruction register contents then transfer to the five C registers for instruction decode:

- C-register A generates the ROS starting address for instructions with ROS starting address 256. These addresses are sent to the pico ROS card (BU451) on source bus bits 10–15.
- C-register B generates a ROS starting address for instructions with ROS starting address 256. It also decodes the PM0 and PM1 bits from PSV bits 32–63 to determine which instructions are allowed.
- C-register C decodes the second half of extended instructions.
- C-register D generates the immediate, R1/R3, and R2 fields.
- C-register E generates the value used to determine whether the primary or secondary PSV should be used for the R1/R3 and R2 fields. It also generates the address control vector (ACV) value used by the arithmetic and oscillator card (BU454) to control adder functions and the setting of condition values.

Refer to Figure BU456-1 for instruction decode card data flow.

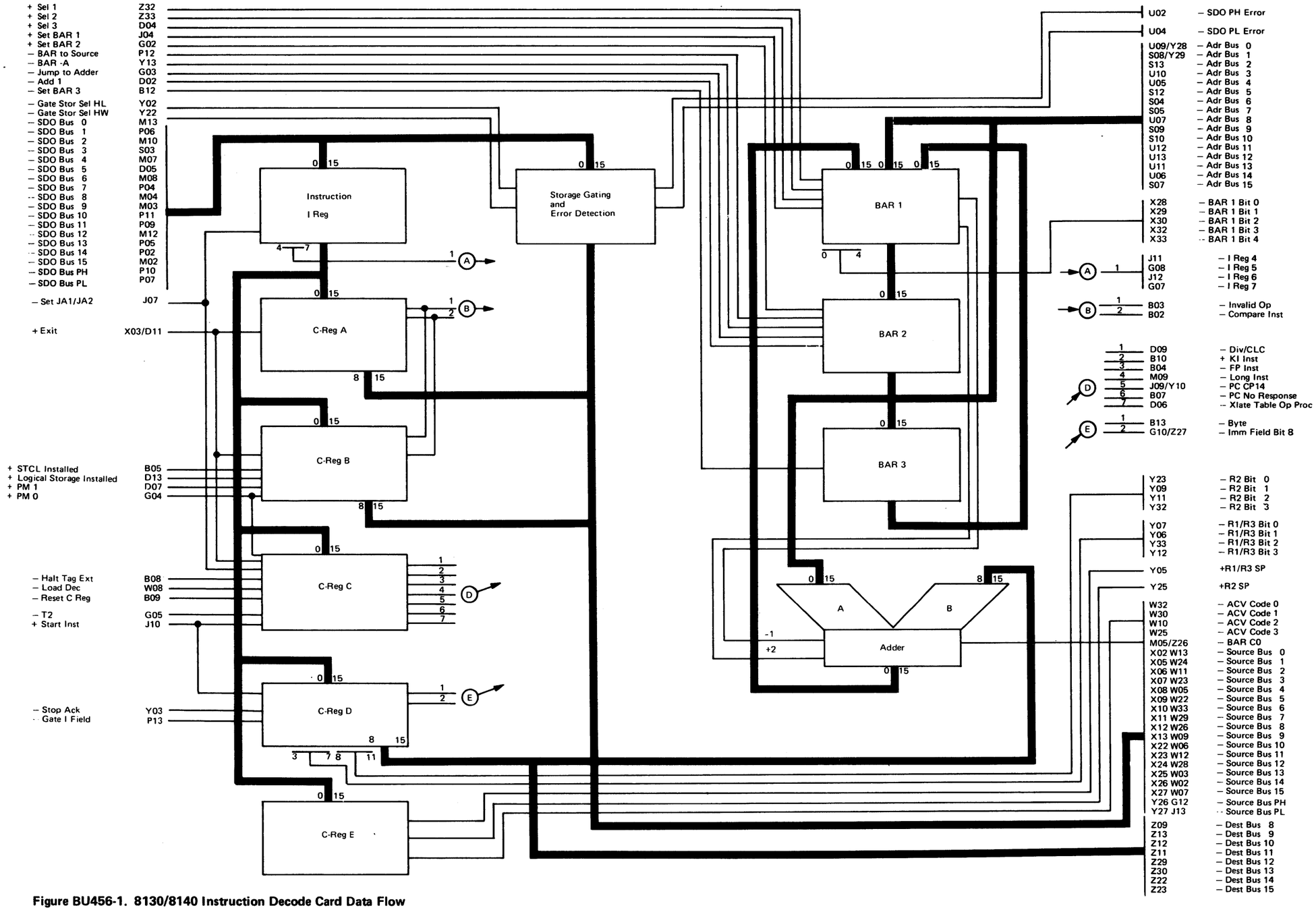


Figure BU456-1. 8130/8140 Instruction Decode Card Data Flow

BU457 8130/8140 Storage Addressing and Translation Table Cards

The logical functions performed during 8130 and 8140 storage addressing and translation are identical, but the processor I/E units do not use the same card logic.

- The 8130 uses only one card (A1J2) for hardware addressing (see Figure BU457-1).
- The 8140 uses two cards. In the AXX models they are located in positions A1K2 and A1L2; in the BXX models they are located in positions A1N2 and A1P2. The L2 and P2 cards contain a 2048 x 18 bit array used for the translation table, and also contain part of the checking circuitry (see Figures BU457-2 and BU457-3).

These cards contain the following major functions:

- All logic used for dynamic address relocation (DAR) and dynamic address translation (DAT).
- Checking circuits that detect if there are any zeros in the high-order bits of the program status vector (PSV) instruction address field (bits 0–31). These circuits also check the format of both the address control vector (ACV) and the data to be stored in the translation table.

The address overlay mask (AOM) combines the contents of the ACV with the logical address. This operation, called dynamic address relocation, generates the relocated address used to access a translation table entry.

Dynamic address translation uses a 22-bit (4M) logical address to generate a 19-bit (512K) real address. The address bus supplies 16 bits of the logical address, while either the EIC, R1E, or R2E logic of the adjunct register storage card (BU458) indirectly supplies the remaining six bits through the R-register out bus. The 11 low-order bits of the address bus (5–15) are not used for DAR or DAT, but are sent directly to other processor instruction/execution cards. The AOM uses the remaining 11 bits (R-Reg Out 10–15 and Address Bus 0–4), together with the ACV (or the channel control ACV for CHIO operations) to create an 11-bit translation table entry address (TTEA).

TTEA use differs according to the ACV (or channel control ACV) bit 15 status. This bit specifies whether DAT must be performed to generate the actual storage address.

- If on, DAT must be performed. The TTEA addresses one of the 2K translation table entries (TTE), which has a 4-bit access code and an 8-bit address field. The 8-bit address field is then added to the 11 low-order address bus bits to generate a 19-bit (512K) real storage address.
- If off, the TTEA and the 11 low-order address bus bits are directly used to generate the real storage address.

Note: *In this mode, TTEA bits 8–10 are zero, since the maximum real address must be below 512K.*

The address is encoded once more before addressing storage. The eight bits of either the TTE or TTEA are divided into two groups:

- The five low-order bits are combined with address bus bits 5–15 as S Adr Bus Bits 0–4, to form a 16-bit intra-storage select address.
- The three high-order bits are encoded using the 3:8 encoder to create one of eight storage select bits (S Sel 0–7).

These cards maintain the active ACV. Because there is only one ACV for each PSV or channel pointer, the extended register space loads this ACV through the 'ext stk out bus' during each PSV swap or CHIO operation. The DAR operation uses the contents of the ACV or channel control ACV as described above.

Refer to Figures BU457-1 and BU457-2 for storage addressing card data flow and to Figure BU457-3 for 8140 translation table card data flow.

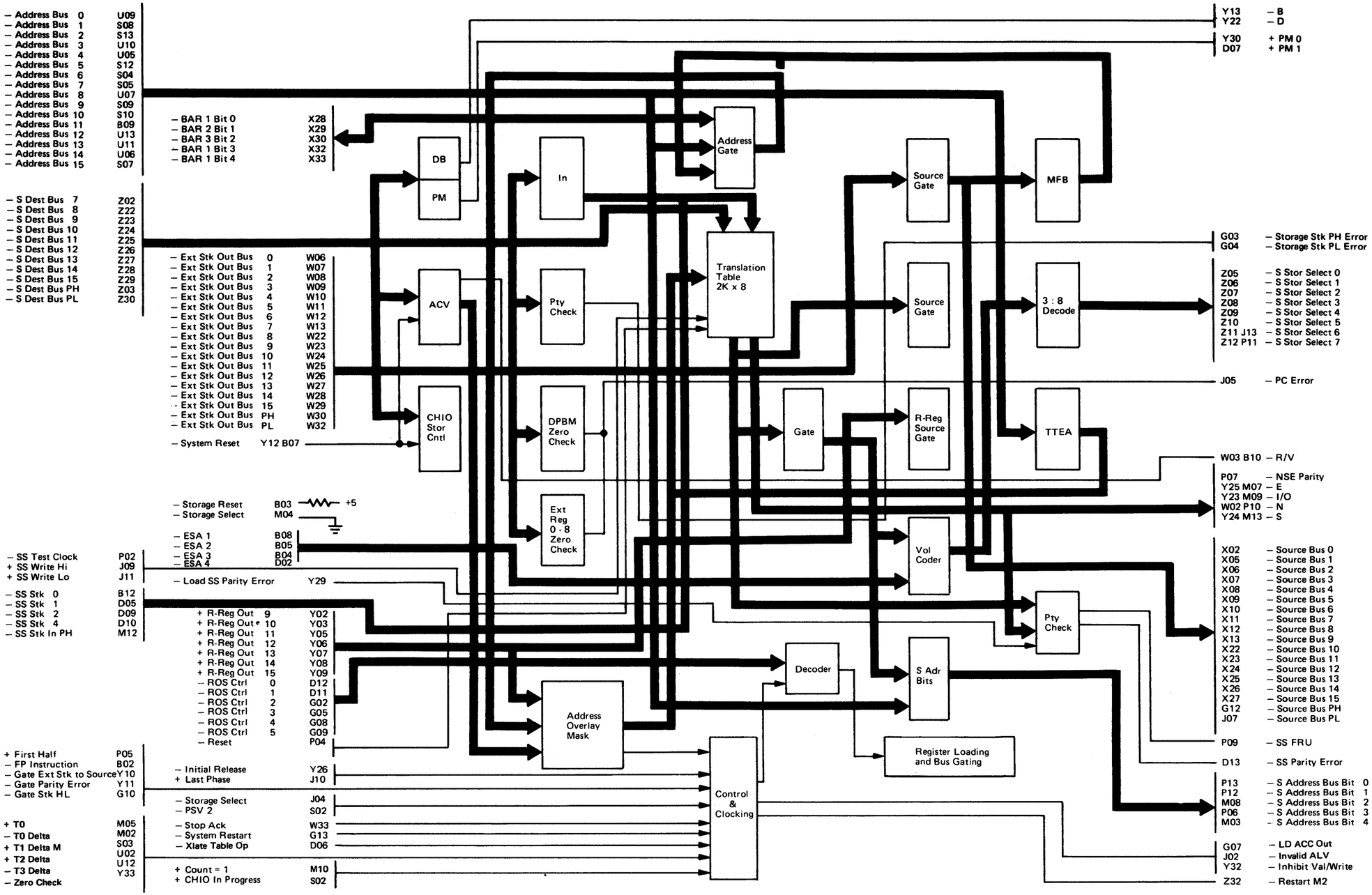


Figure BU457-1. 8130 Storage Addressing Card Data Flow

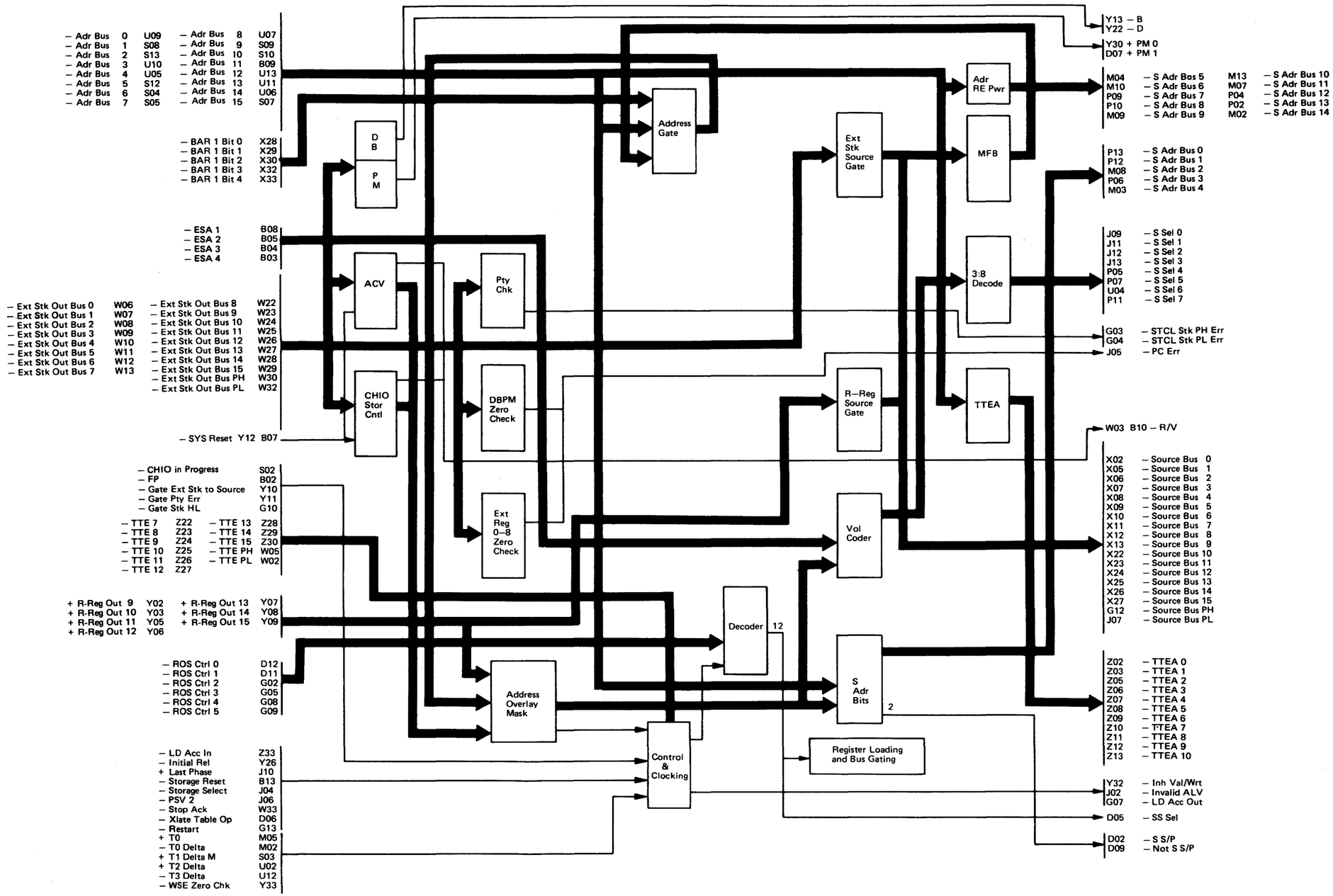


Figure BU457-2. 8140 Storage Addressing Card Data Flow

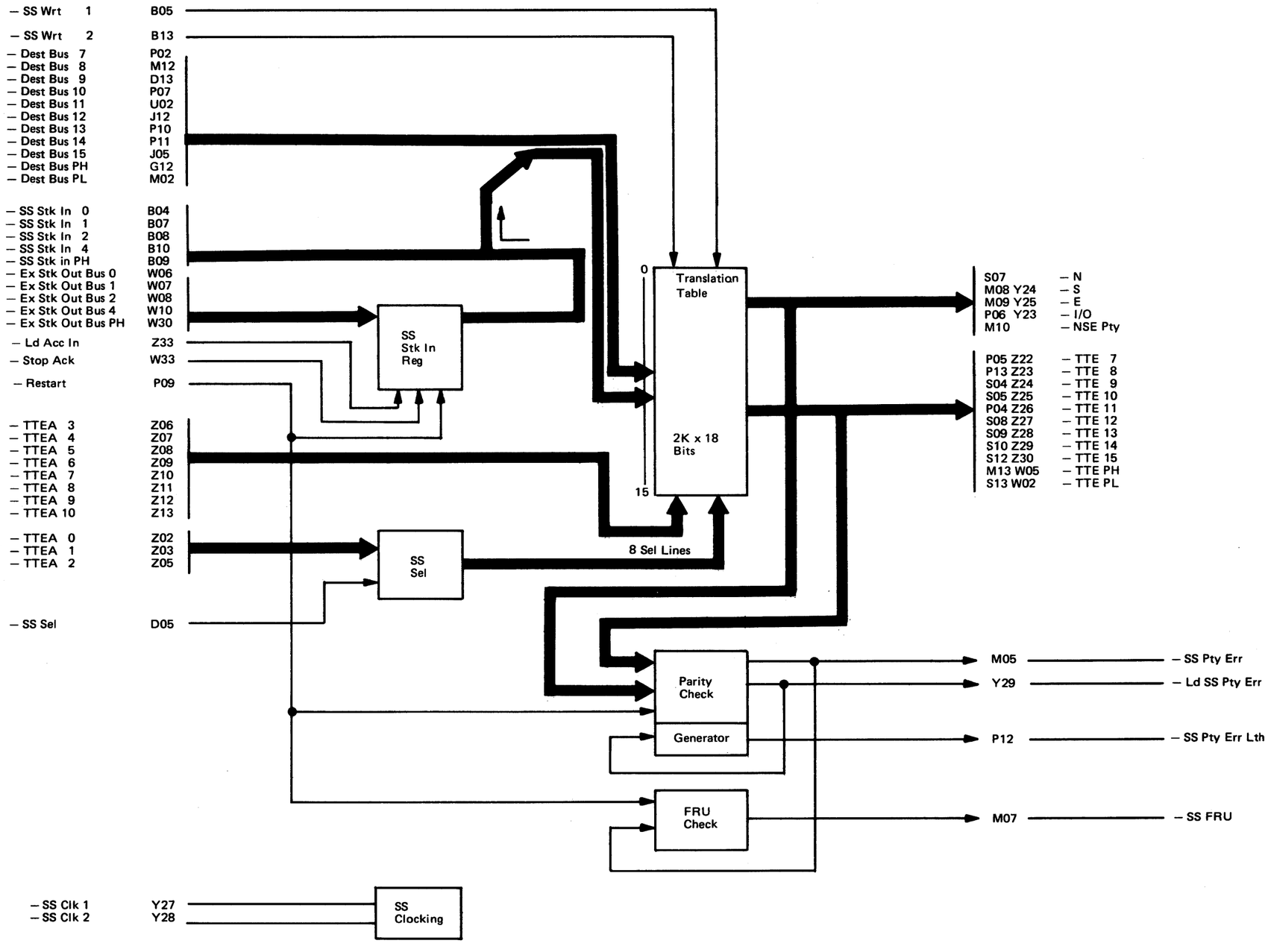


Figure BU457-3. 8140 Translation Table Card Data Flow

BU458 8130/8140 Adjunct Register Storage Card

- 8130 Card Location = A1H2
- 8140 Models AXX Card Location = A1J2
- 8140 Models BXX Card Location = A1M2

This card contains the following major functions:

- Adjunct register storage used to contain the address control vectors (ACVs).
- Address extension pointer.

A single 1K x 18 array physically contains the adjunct registers used to store the address control vector. The card also contains the extended instruction counter (EIC) and the R1E and R2E operands of the instruction being executed. These three registers output to both the incrementer/decrementer and a recovery register.

The recovery register is an extension of the BAR 3 register contained on the instruction decode card (BU456), and is used to hold the previous EIC value for error recovery purposes, and the present EIC value during a CHIO operation.

The incrementer/decrementer updates the EIC, R1E, or R2E registers during instruction execution.

Decoding the eight ROS Stor Ctrl bits determine all gate and register controls for these three registers.

Figures BU458-1 and BU458-2 are data flow diagrams of the 8130 and 8140 respectively. They are shown separately, as some pins are not identical; they are logically the same, but have different part numbers.

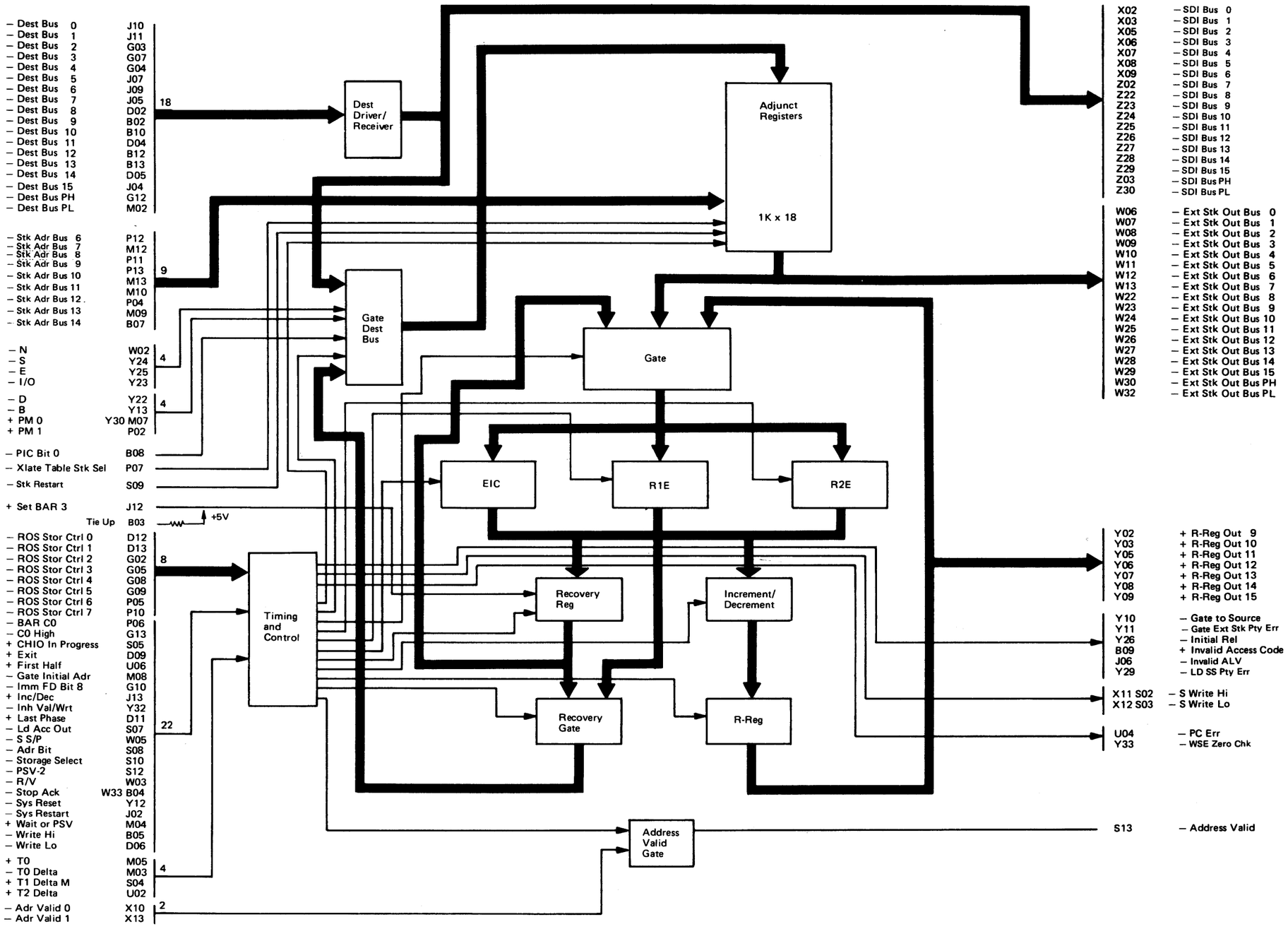


Figure BU458-1. 8130 Adjunct Register Storage Card Data Flow

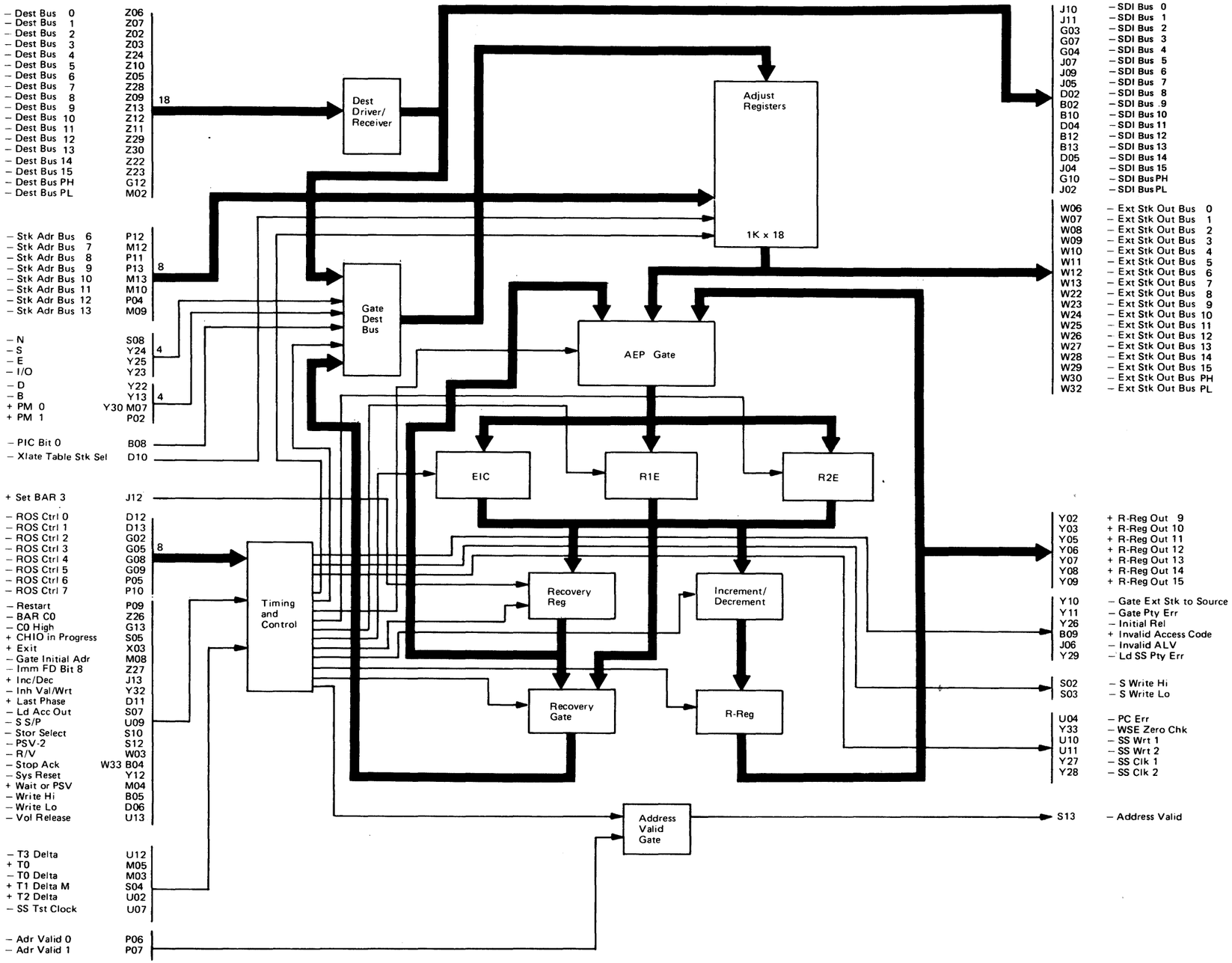
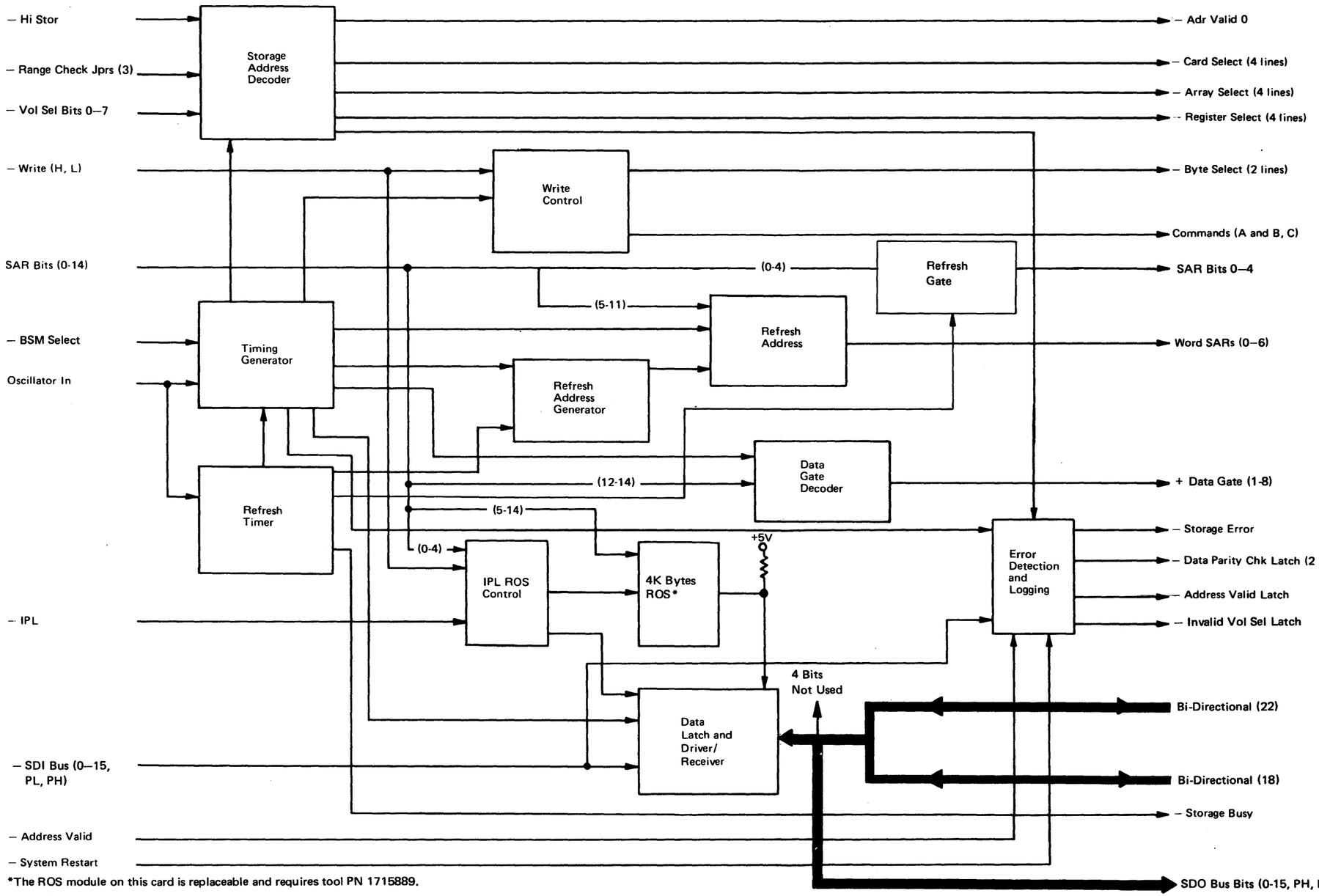


Figure BU458-2. 8140 Adjunct Register Storage Card Data Flow

BU459 8130 ROS and Storage Control Card

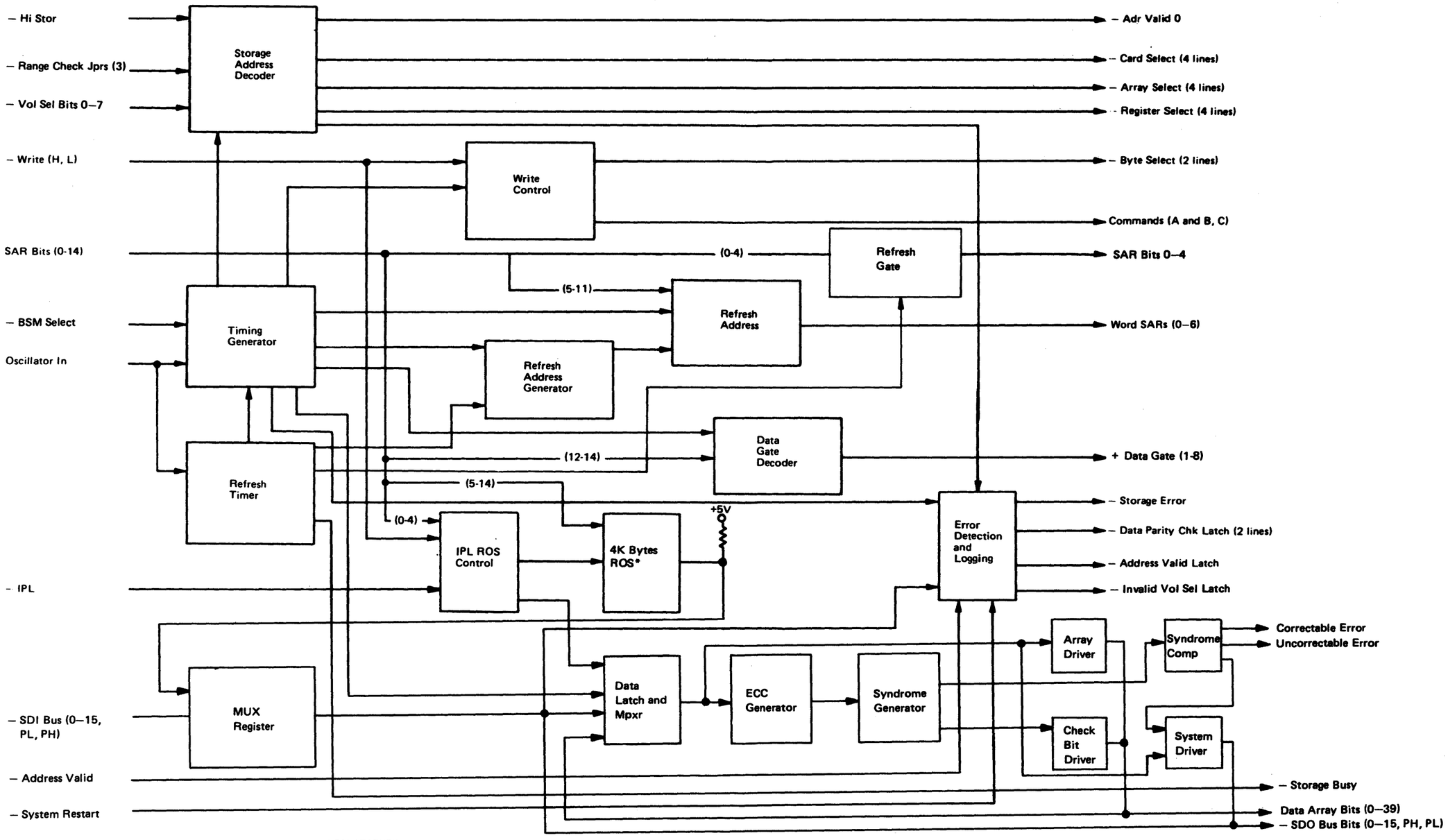
- Card Location = A1F2

This card contains both the ROS and storage control functions for the 8130. Refer to Figure BU459-1 for 8130 ROS and storage control card data flow without ECC and to Figure BU459-2 for 8130 ROS and storage control card data flow with ECC.



*The ROS module on this card is replaceable and requires tool PN 1715889.

Figure BU459-1. 8130 ROS and Storage Control Card Data Flow (without ECC)



*The ROS module on this card is replaceable and requires tool PN 1715889.

Figure BU459-2. 8130 ROS and Storage Control Card Data Flow (with ECC)

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BU460 Processor Storage Card, Detailed Description and Data Flow

Sections BU461 and BU462 describe and show the data flow of the storage cards used for the 8130 and 8140 Processors.

BU461 8130 Read/Write Storage Card

- Card Location = A1A2 (basic); A1B2, A1C2, and A1D2 (feature).

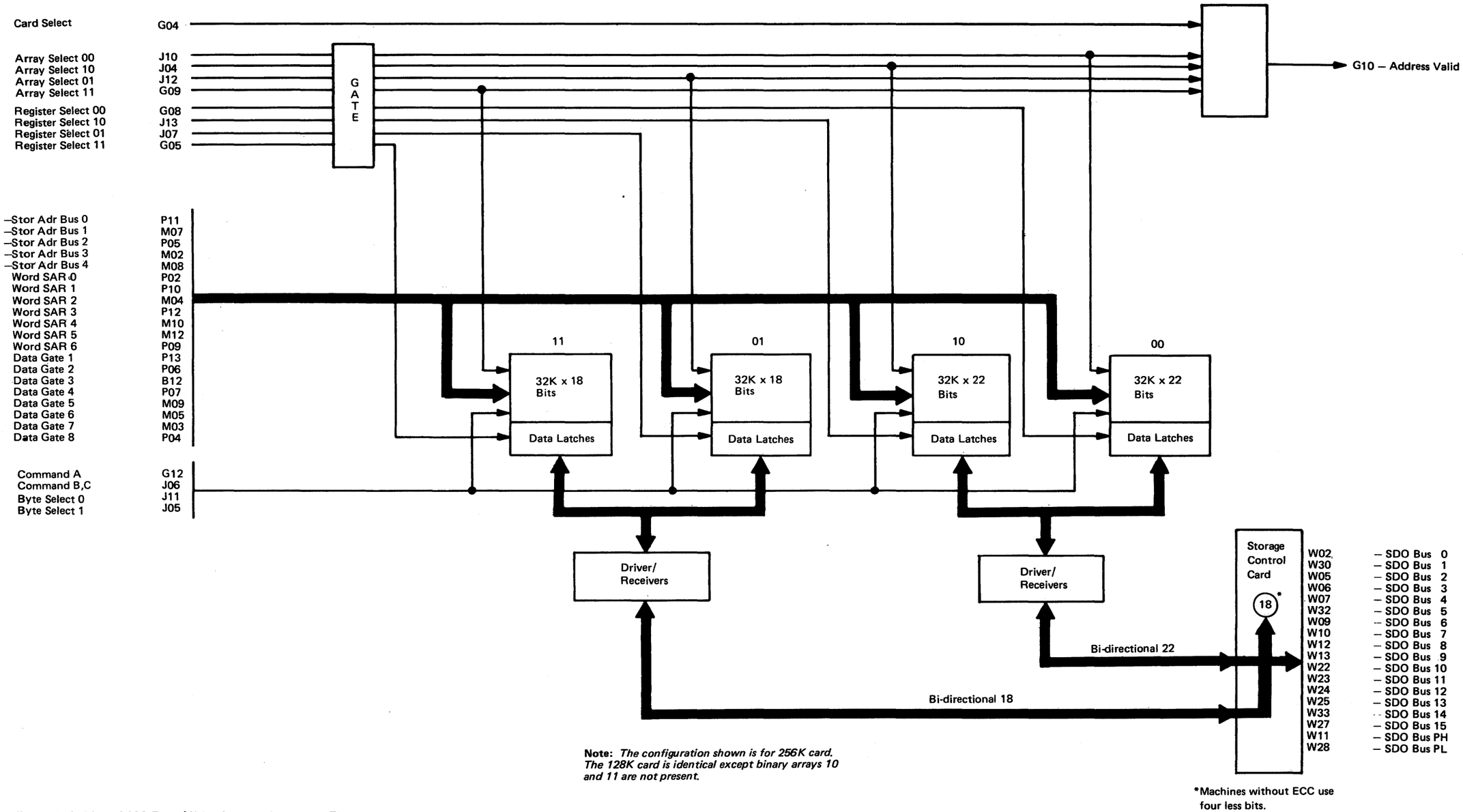
The 8130 storage cards are available in two functionally identical versions that differ only in storage capacity: one can store 128K bytes and the other 256K bytes.

The status of the Card Select, Array Select (0—11), and Byte Select lines determine the individual array module addressing. Decoding the Storage Address Bus 0—4 lines selects the group. The Data Gate 1—8 lines, which are encoded by the storage control card (BU459) from Adr Bus 12—14, determine the specific bit.

The state of the Command A and Command B, C lines determine the storage card operation performed.

- Command A active and Command B, C inactive specifies a read operation.
- Command A inactive and Command B, C active specifies a store operation.
- Command A and Command B, C inactive with Array Select active specifies a refresh operation.

Refer to Figure BU461-1 for 8130 read/write storage card data flow.



Note: *The configuration shown is for 256K card. The 128K card is identical except binary arrays 10 and 11 are not present.*

*Machines without ECC use four less bits.

Figure BU461-1. 8130 Read/Write Storage Card Data Flow

BU462 8140 Models A3X, A4X, and A5X Read/Write Storage Card

Note: *Card locations depend on 8140 model. Refer to BU111.*

Each 8140 A3X, A4X, and A5X storage card contains 32K bytes of read/write storage with the exception of the first card, which contains 4K ROS and 28K read/write storage. Eighteen bits (16 + 2 parity) input these cards from the SDI bus and output the SDO bus.

The S sel vol lines determine which card is addressed:

- S Adr Bus bits 1—4 select one of 16 array modules on each card.
- S Adr Bus bits 5—14 select the address within the module.

Note: *The Adr Valid line indicates to the processor that storage recognized a valid address.*

On a write operation, the 8140 Processor I/E unit presents a halfword of data to storage on the SDI bus, together with the byte or halfword selection information as required by the operation. Activating either the S Write Hi or S Write Low lines designates byte selection for a write operation, while both lines are used for halfword operations.

Read operations are used to fetch either data or an instruction. The S Write Hi and S Write Low lines are deactivated, which signifies a read operation. Storage fetches the contents of the halfword location specified by the address bus value, and places the fetched halfword and associated parity bits on the SDO bus.

The 8140 Processor I/E unit checks parity on a data read from storage, and generates parity on data written into storage.

Refer to Figure BU462-1 for 8140 Models A3X—A5X read/write storage card data flow.

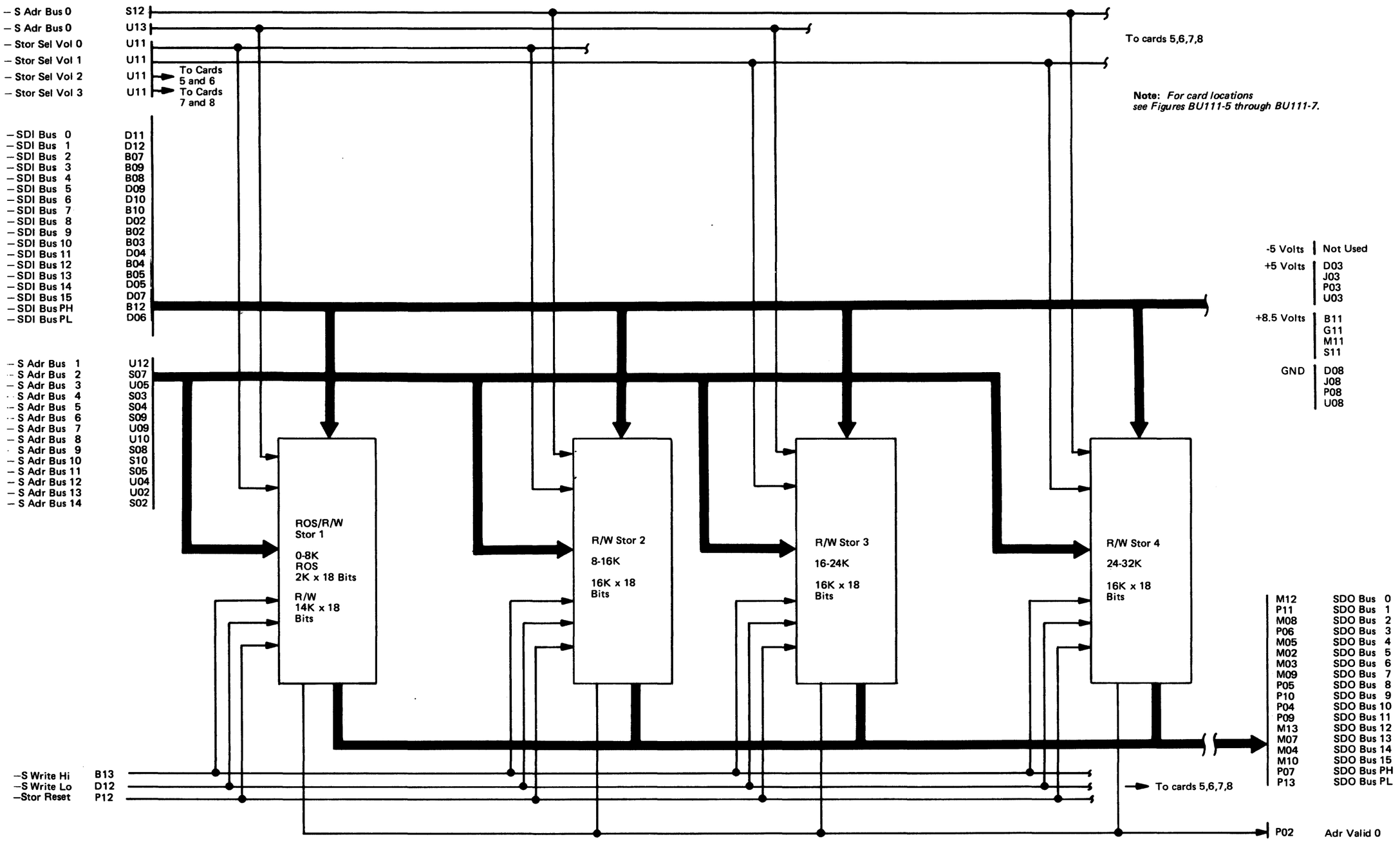


Figure BU462-1. 8140 Models A3X, A4X and A5X Read/Write Storage Card Data Flow

BU463 8140 Models A6X, A7X, and BXX Read/Write Storage and ECC Cards

Each 8140 Model A6X, A7X, and BXX storage card contains 128K bytes of read/write storage. For addressing purposes, these cards are arranged in pairs such that each pair contains four 64K byte volumes of storage, each of which is split between the pair of cards. The two high-order bytes of each fullword storage location reside on one of the cards of the pair while the two low-order bytes reside on the other. Refer to BU111 for storage card locations.

Storage addressing is accomplished in the following manner:

- The Stor Sel volume lines and the M S/P and Not M S/P lines combine to select the volume of storage to be accessed.
- S Addr Bus Bits 0-13 then decode to select the 4-byte fullword of storage within the selected volume.

Note: *Storage accesses, whether on read, write, or refresh operations, always involve 40 bits: 32 data bits and 8 check bits.*

The read/write storage area of 8140 Models A6X, A7X, and BXX also contains two additional storage control cards. These cards, called ECC cards 1 and 2, contain an oscillator to time storage operations, logic which is used to control the refresh operation of the dynamic storage used in these models, and ECC logic. This ECC logic monitors all transfers between the processor I/E unit and storage and can thus detect and correct single bit data failures and detect multiple bit data failures.

On a write operation, the processor places the byte or halfword to be stored on the SDI Bus while storage places the accessed fullword location on the Stor Out Bus. The ECC logic monitors both of these buses, decodes the S Write Hi, S Write Lo, and S Addr Bus Bit 14 lines to determine where within the fullword the data is to be stored, and then merges the data into this fullword. The logic then generates check bits for this modified fullword and places both the fullword of data and the check bits on the Stor In Bus. Storage then takes this information and stores it in the appropriate location.

On a read operation, storage presents four bytes of data and its 8-bit check field to the ECC logic on the Stor Bus Out. ECC determines if the data is correct by examining the check bits. The hardware corrects the data if a single bit is found to be in error, and alerts the processor by altering parity if more than one data bit has failed. Note that while the processor generates parity when storing data, the parity bits are never stored, as in Models A3X, A4X and A5X. Rather, parity is regenerated by the ECC logic on a read operation and then gated, with the data to be read, to the processor on the SDO bus. In this way, multiple data bit failures result in a storage parity check when the processor I/E unit decodes the parity.

Refer to Figures BU463-1 and BU463-2 respectively for 8140 Models A6X, A7X, and BXX read/write storage card data flow and for data flow for both ECC cards.

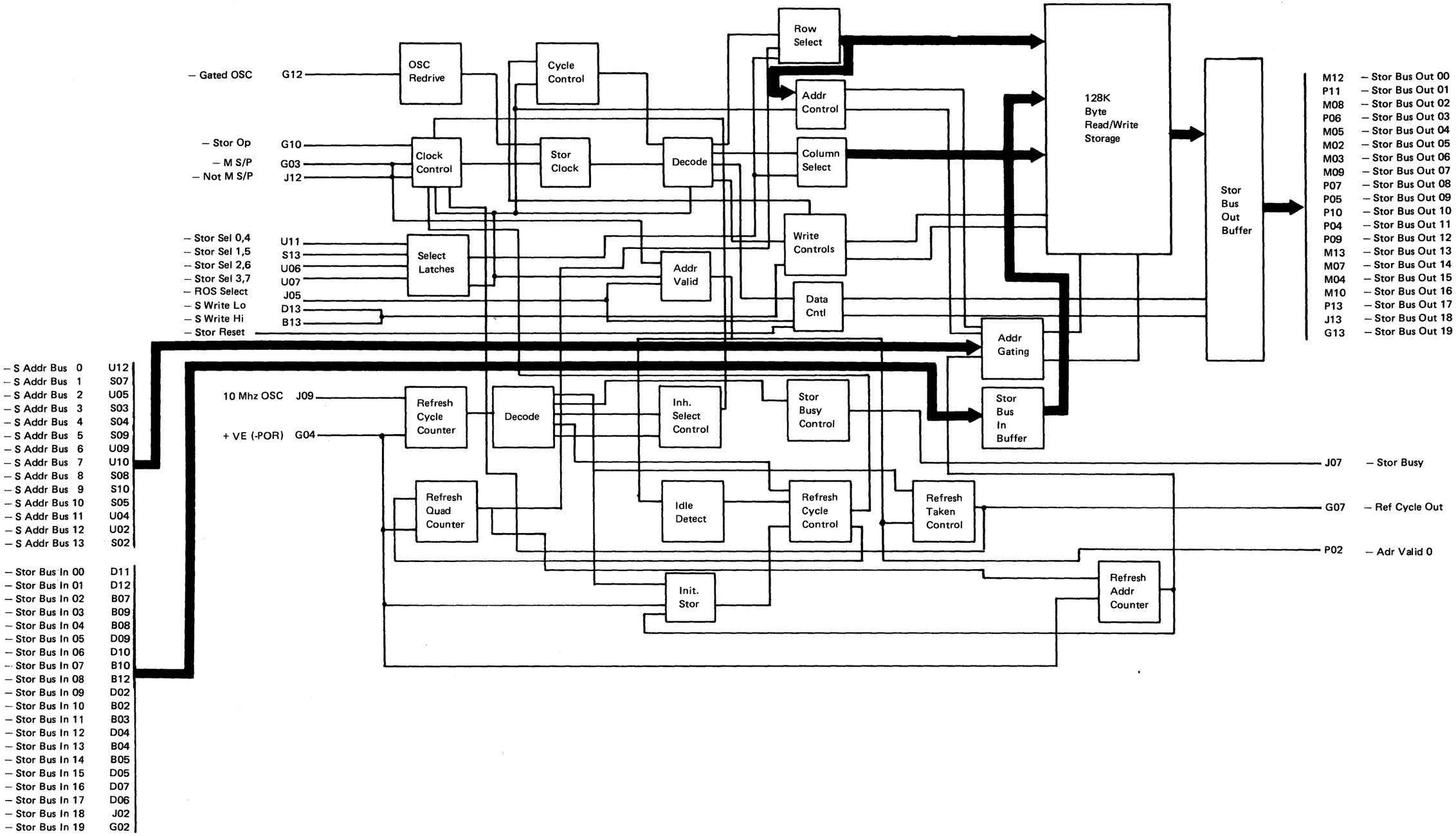


Figure BU463-1. Models A6X, A7X and BXX Read/Write Storage Card Data Flow

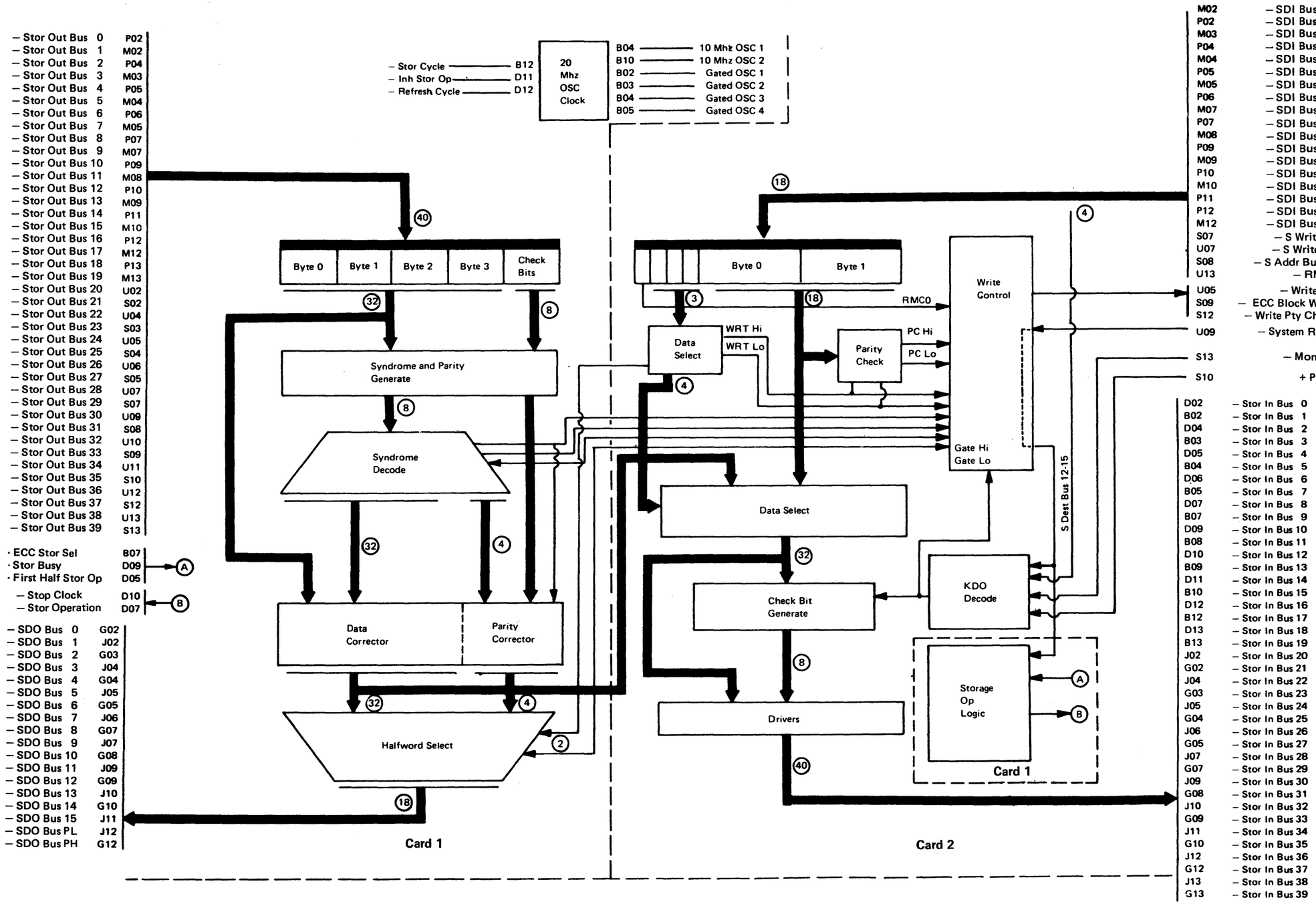


Figure BU463-2. 8140 Models A6X, A7X and BXX Data Flow for ECC

BU470 BOP Adapter Detailed Description and Data Flow

The following sections describe and show information not directly related to fault isolation, but which can aid in further understanding how the BOP operates. Refer to Figure BU470-1 for a detailed data flow diagram of the BOP adapter card.

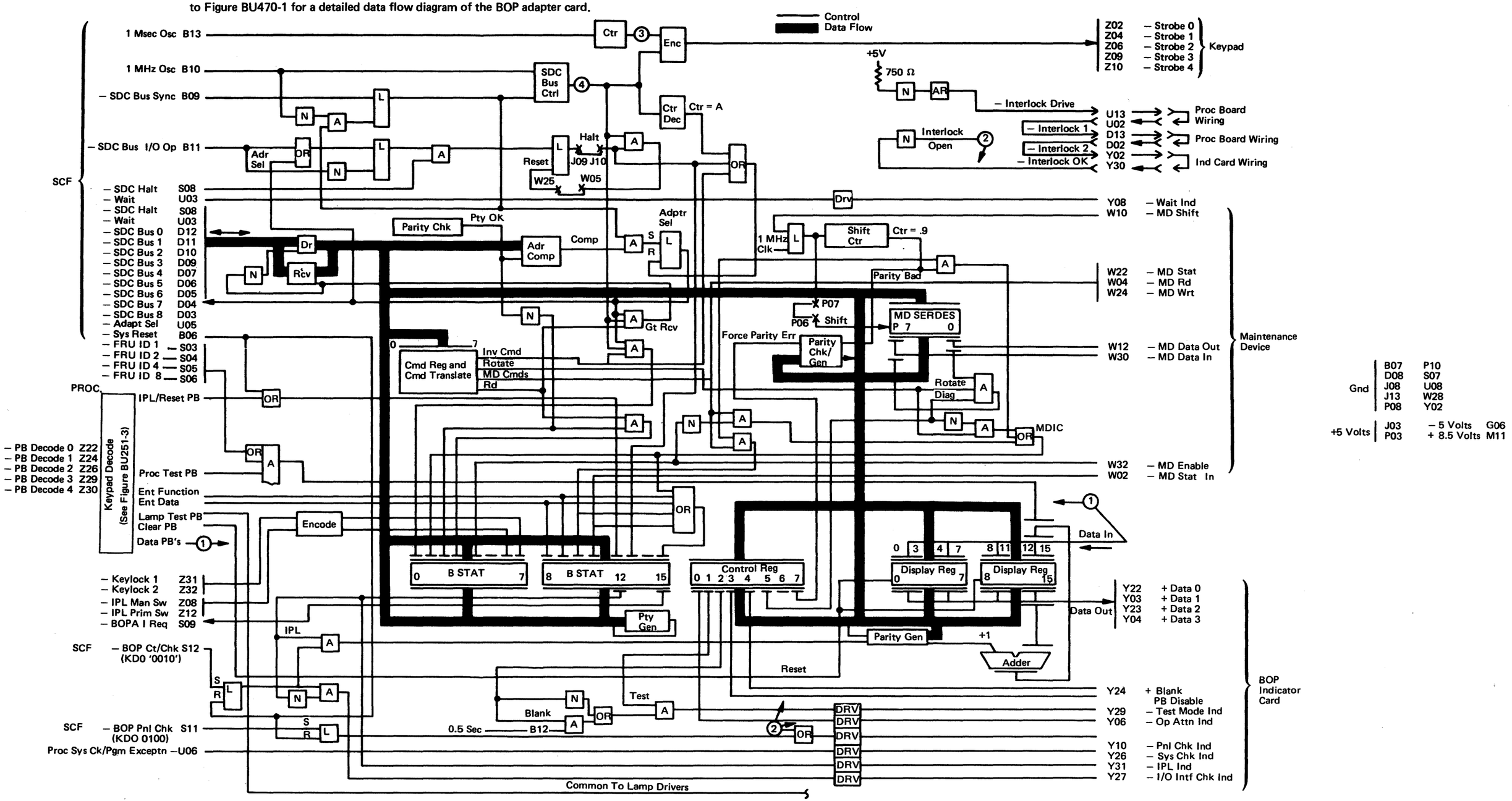


Figure BU470-1. BOP Adapter Card Detailed Data Flow

BU471 BOP Registers

This section describes the BOP control register and the BOP basic status register and their bit meanings. It also describes the maintenance device data register and the BOP display register.

BOP Basic Status Register

The 18 bit (16 + 2 parity) BOP status register permits indication of various conditions of the BOP adapter, panel and switch settings, BOP interrupt request logic, and the MD. All 16 bits with the exception of 4, 6, and 7 can be modified by programs, and all can be read to analyze status information. The BOP basic status register presents interrupt requests to the processor, and bits 13–15 are respectively the same as all other 8130/8140 adapter basic status register bits.

The following table describes the format and meaning of the BOP basic status register bits:

Bit	Meaning When Active
0	Invalid command/command parity check – The BOP adapter received either an invalid or out of parity command.
1*	MD – Turns on: (1) when the MDDR detected a parity error after a Set Read command, (2) when more than nine shift pulses were detected during an MD read or write sequence, (3) during the decoding of an MD command with BOP basic status register bit 4 off, or (4) when decoding a rotate command with BOP control register bit 5 off (MD diagnose mode).
2	BOP write check – The BOP adapter received incorrect parity from the processor I/E unit.
3	BOP read check – The processor I/E unit detected a BOP parity error.
4	MD enabled – The MD is connected and enabled.
5	Reserved
6 & 7	IPL keylock encode 0 & 1 – Reflect the setting of the keylock and IPL switches.
8*	Data entry – Indicates data input from the Data/Function pushbuttons.
9*	Function entry – Indicates function input from the Data/Function pushbuttons.
10*	MD transfer complete – Indicates completion of one byte of data transfer to or from the MD.
11*	MD status – MD is ready to send message status.
12	IPL – Set by system reset or a program, and causes the IPL indicator to turn on.
13	Equipment check – Turns on for the following conditions: (1) the processor I/E unit abnormally terminated operation, (2) any bit 0–3 of the BSTAT is on, or (3) set by the processor I/E unit if detecting a bus parity error while decoding a rotate command when not in MD diagnose mode (BOP control register bit 5 off).
14	BOP enabled – Allows BOP interrupt presentation to the processor I/E unit.
15*	BOP interrupt request – Operates in conjunction with bit 14. Indicates a pending BOP interrupt condition to the processor I/E unit.

*Generates an interrupt request through the BOP status register bit 15, if permitted by bit 14.

BOP Control Register

The 9-bit (8 bits + parity) BOP control register permits the processor I/E unit to control operation of certain functions and indicators through programming. Read and write operations to this register permit the analyzing and changing of these values. The following table describes the format and function of the BOP control register bits:

Bit	Meaning When Active
0	Operator attention – Turns on the Operator Attention indicator.
1	Test mode – Turns on the Test Mode indicator.
2	Blink test mode – Meaningful only with bit 1 on and permits the Test Mode indicator to blink twice each second.
3	Pushbutton disable – Functionally disables all pushbuttons except Lamp Test, Processor Test, Reset/IPL, and the Power On/Power Off switch. The keylock switch position overrides this bit function.
4	Blank BOP display – makes BOP display blank (dark).
5	MD diagnose mode – (1) Enables an MDDR command, (2) wraps the MDDR serdes, and (3) enables the Rotate command. **Note:** *This occurs without maintenance device connection.*
6	Reserved
7	Force MDDR parity error – Reverses the parity bit value in the MDDR and BOP MD adapter.

BOP Display Register

The BOP display register enters and retains information in the four-position (16-bit) hexadecimal display. This register receives information either by input from the Data/Function pushbuttons, providing the keylock switch (if installed) is in the Enable position, or by the processor I/E unit when executing a Write command to the adapter. The BOP control register can block access to this register from the processor I/E unit, but not from the Data/Function pushbuttons.

Maintenance Device Data Register (MDDR)

The MDDR permits data transfer in both directions between the MD and the processor I/E unit. This 9-bit (8 + parity) SERDES buffer can be written, read, and shifted by programs. Test capability permits the register to be wrapped, and also permits the parity bit to be reversed to check the MDDR parity error detection logic.

BU472 BOP Interrupts and Levels

The BOP status register presents interrupt requests to the processor I/E unit for certain conditions previously explained in the BOP basic status register description. The program assigns primary and secondary interrupt levels to the BOP, which load into the PSCF. The primary level assignment and the active program level assignment are the same, and the secondary level assignment (8–F) differentiates the BOP adapter from any other adapter assigned to the same primary level.

BU473 BOP Error Detection

Various methods determine error conditions for all data transfer operations involving the BOP:

- Parity checking to and from the adapter.
- Parity and validity checking of commands.
- Parity checking of the BOP display register.
- Parity checking of the MDDR and its data path.
- The use of a common interlock line in certain BOP and BOP adapter cables that causes a panel check when interrupted.

Errors cause either a check condition or presentation of an interrupt request, which must then be handled through interrupt processing by the program receiving the request.

BU480 8140 Floating-Point Card Description and Data Flow

Note: *Card location depends on 8140 model. Refer to BU111.*

Floating-point instructions are used to perform calculations on operands that use many significant digits and to yield results designed to maintain precision. Floating-point is basic on 8140 Models A41–A44, available as an RPQ on 8140 Models A6X and A7X, and a feature on 8140 Models BXX.

The floating-point (FP) function of the 8140 Processor uses two cards that logically contain an FP processor, as well as the data and control lines to the processor instruction/execution and storage cards. The pico ROS card (BU451) controls FP functions. Data can be in either 32-bit (short precision) or 64-bit (long precision) formats. The control card contains eight sets of registers used only for FP operation, and each register set contains four 64-bit registers.

Note: *The processor I/E cards control the system check and condition value decodes for the FP function.*

The FP processor receives instructions and data from the storage data out (SDO) bus, while the processor instruction/execution cards receive information from the FP processor on the destination bus. The processor I/E cards also generate parity on the high and low bytes sent to the FP processor to ensure that correct data transfer occurs.

The processor I/E card internal 18-bit common bus, as well as the output of the 512 x 48 ROS bits on this card, perform parity checking. The FP ROS contains the pico code used to correctly sequence the FP instructions, and also controls the gating of data between FP registers.

The FP function uses the FPT02 and FPT02 delta clocks generated in the processor I/E cards to create the four basic clocks (TA, TB, TC, and TD) used by the FP function.

Refer to Figures BU480-1 and BU480-2 respectively for FP fraction card data flow and FP control card data flow.

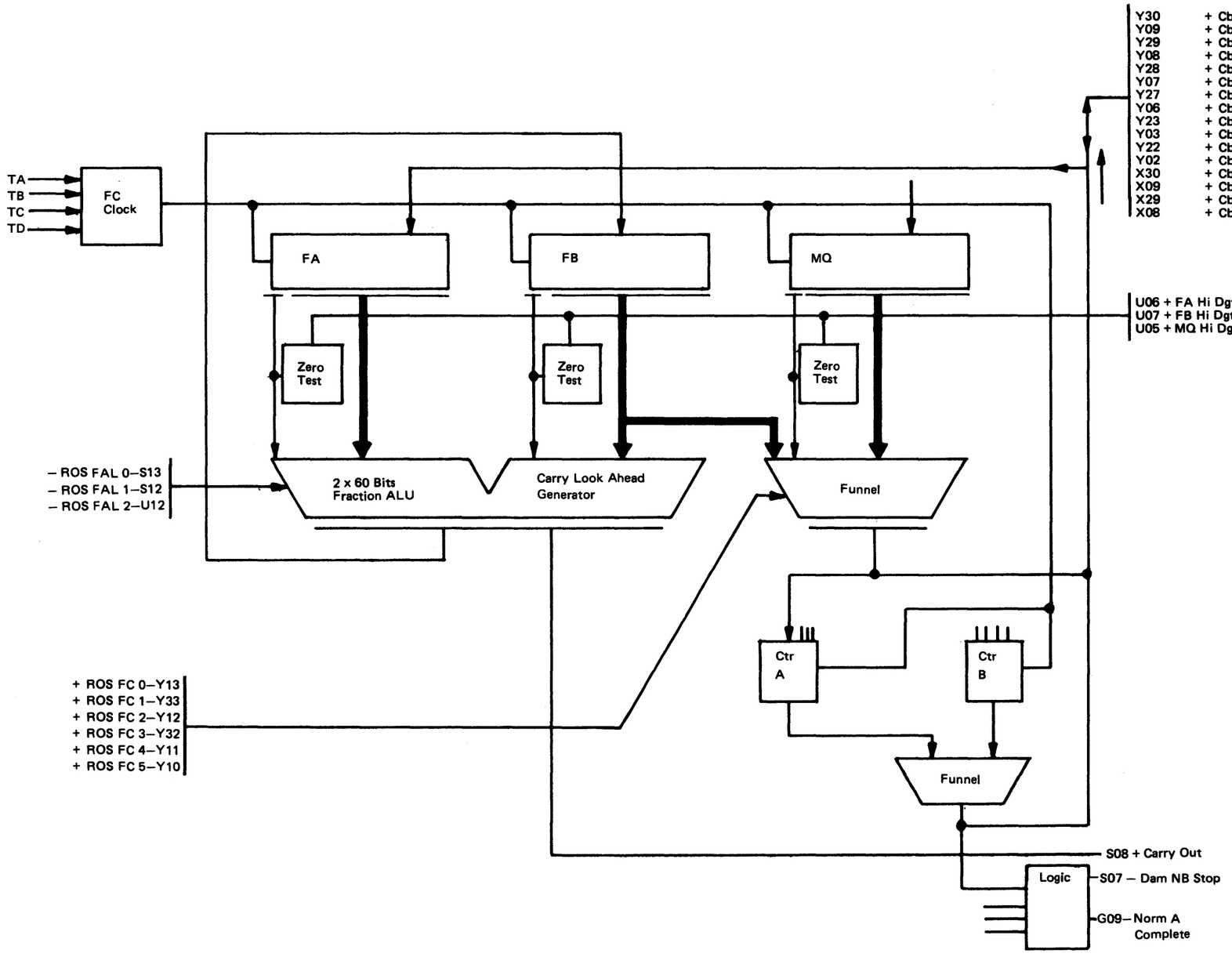


Figure BU480-1. 8140 Floating-Point Fraction Card Data Flow

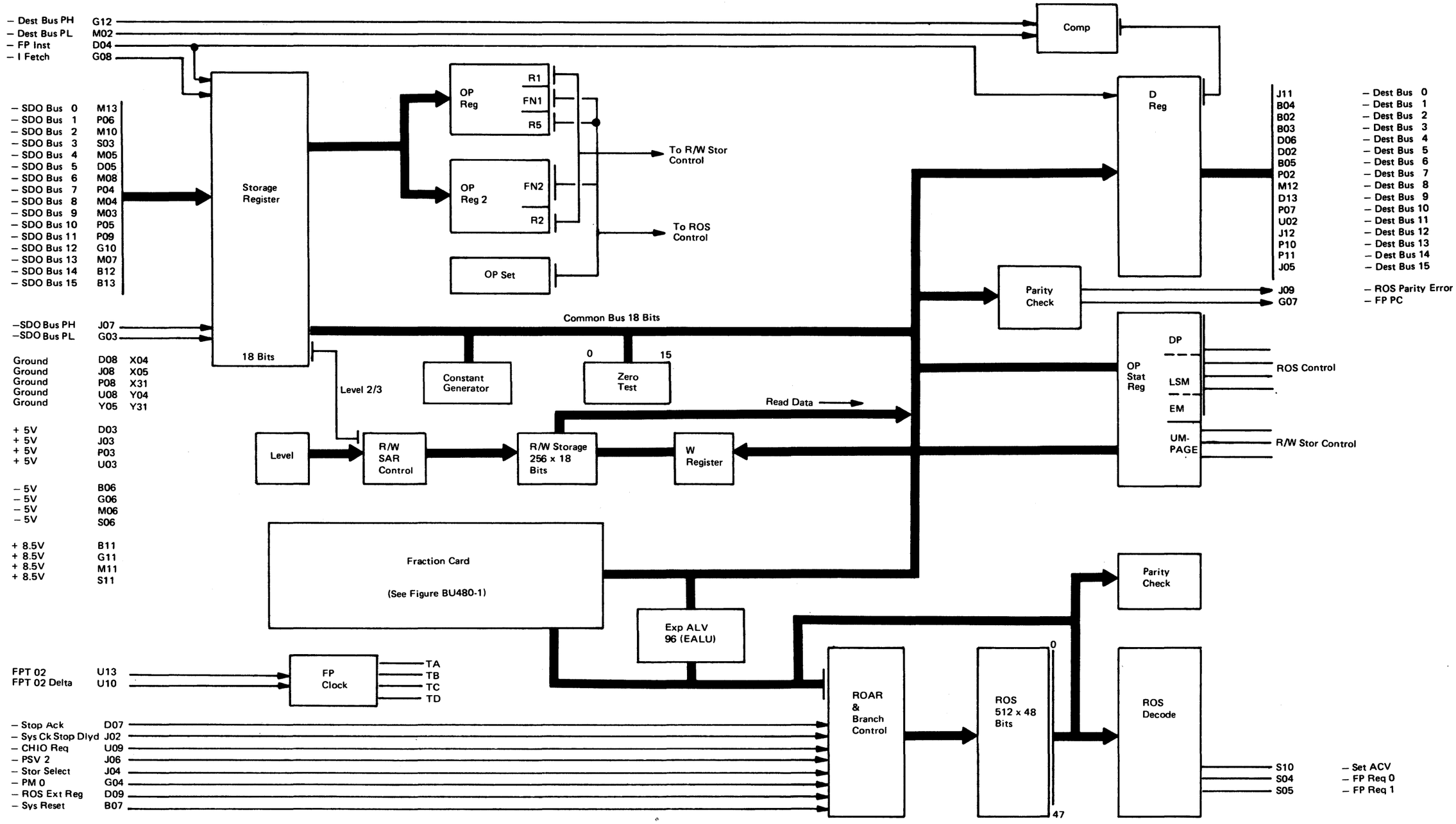


Figure BU480-2. 8140 Floating-Point Control Card Data Flow

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BU500 Adjustment, Removal, Replacement, and Voltage Check Procedures

BU510 BOP Adapter Card Removal and Replacment

Note: *In 8140 Models BXX, the BOP adapter card is located beneath the operator panel. First use the procedure in BU520 to gain access to the area beneath the panel, then remove the adapter card.*

Referring to Figure BU510-1, proceed as follows:

1. Remove the four front cables from the BOP adapter card connector at locations B2A2, B2A3, B2A4, and B2A5.
2. Remove the two retaining nuts from the front card/cable connector and bracket assembly.
3. Remove the BOP adapter card from the rear card/cable connector and bracket assembly with the front card/cable connector and bracket assembly still attached.
4. Remove the adapter card from the front card/cable connector and bracket assembly.
5. To replace the card, reverse the above steps.

Figure BU510-1. Basic Operator Panel Adapter Card (01B-A1A2)

BU520 How to Gain Access to 8130/8140 Operator Panel Components

To replace any operator panel component, you must first gain access to the rear of the panel. Referring to Figure BU520-1, proceed as follows:

1. Turn power off at the 8130/8140 operator panel and remove the power cord from the wall outlet. On 8140 Models BXX, you can turn off the line circuit breaker (CB1) instead of removing the power cord.
2. Open the 8130/8140 front covers. Remove the bezel by sliding the two retainer clips to the rear and lifting the front edge straight up and toward the front of the machine, ensuring that the studs are clear of the retainer clips.
3. Pivot the operator panel assembly towards the front of the 8130/8140 to gain access to the rear of the panel.

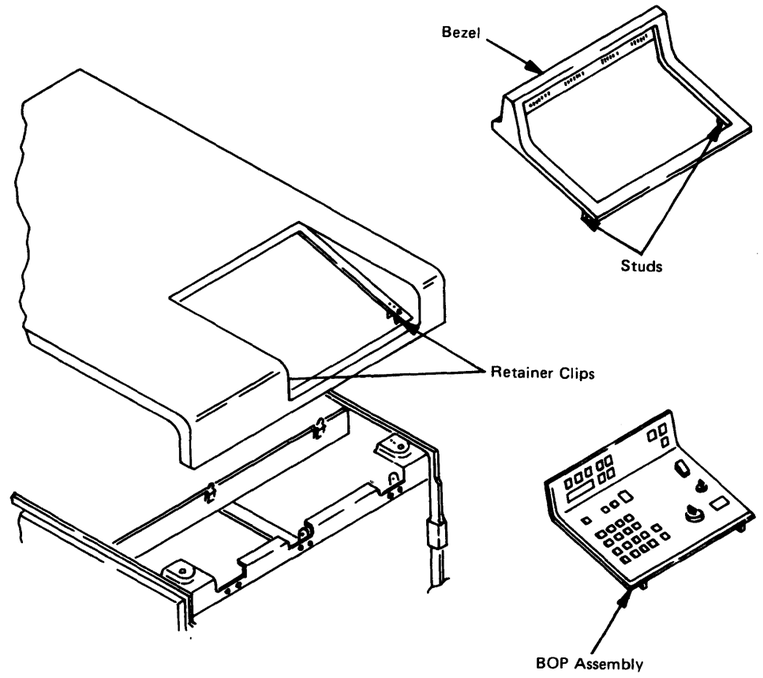

Figure BU520-1. BOP Frame Mounting

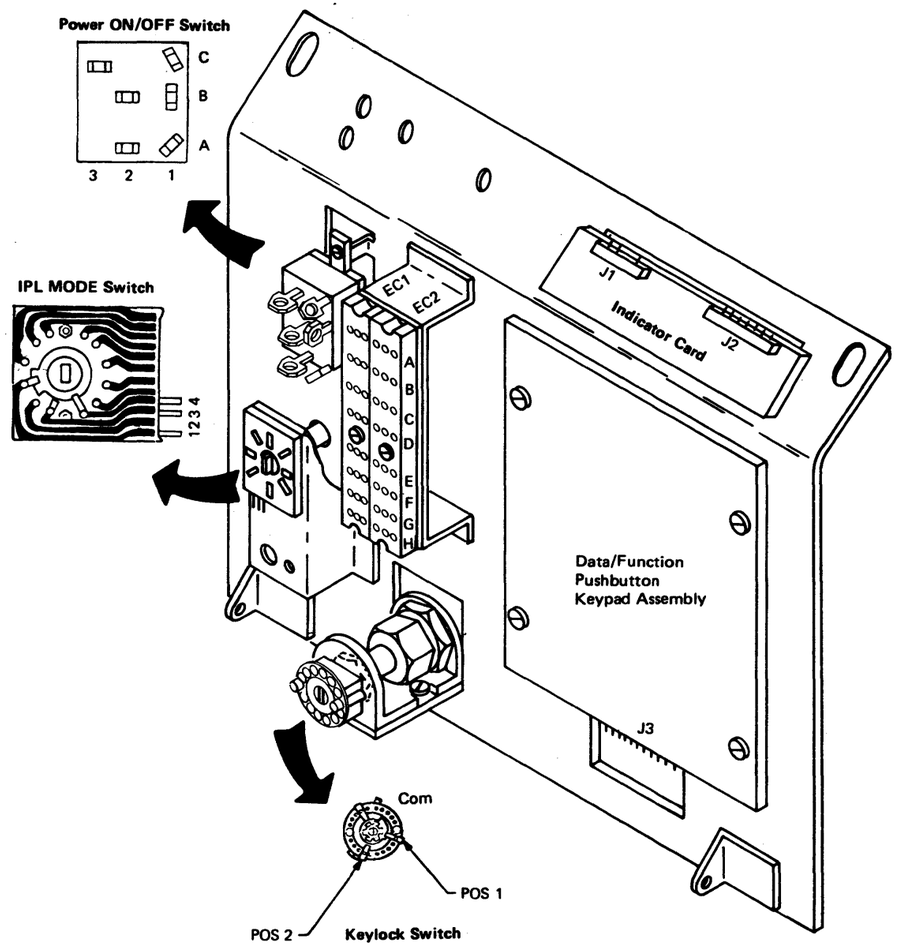

Figure BU520-2. Basic Operator Panel (Rear View)

Note: *Refer to Figures BU520-1 and BU520-2 for the following sections.*

BU521 BOP Indicator Card Removal

1. Access the rear of the BOP assembly. Refer to BU520, if necessary.
2. Unplug the P1 and P2 cable connectors from the indicator card.
3. Remove the indicator card mounting screws, and remove the card.

To install the indicator card, perform the above steps in reverse order and then verify the repair.

BU522 BOP Keypad Removal

1. Access the rear of the BOP assembly. Refer to BU520, if necessary.
2. Unplug the P3 cable connector from the keypad card.
3. Remove the keypad mounting screws, and remove the keypad.

To install the keypad, perform the above steps in reverse order and verify the repair.

Caution: Ensure that the pushbuttons do not bind on the top cover.

BU523 Keylock Switch Assembly Removal

1. Access the rear of the BOP assembly. Refer to BU520, if necessary.
2. Unplug the switch cable connections from ec1-g, ec1-h, and ec2-f. Refer to Figure BU256-1.
3. Remove the switch retaining hardware and then remove the switch.

To install the keylock switch, perform the above steps in reverse order and verify the repair.

BU524 IPL Mode Switch Assembly Removal

1. Access the rear of the BOP assembly. Refer to BU520, if necessary.
2. Unplug the P1 cable connector.
3. Remove the switch retaining hardware and then remove the switch.

To install the IPL mode switch, perform the above steps in reverse order and verify the repair.

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BU530 Voltage Checks

The following procedures should be performed when the BU MAP asks you to perform voltage checks for fault isolation.

BU531 8140 01A–A1, 01A–A2, and 01A–C1 Board DC Voltage Checks

Perform the following procedure to determine if the correct voltages for the 8140 processor and storage are present:

1. Check each voltage at a board destination pin using the tables in Figures BU531-1 through BU531-3.
2. If all voltages are correct, either return to the BU MAP or action plan that sent you here, or go to the BOP voltage check procedure in BU532.
3. If any voltage is missing or out of tolerance at the board destination pins, go to the PA MAP for further power fault isolation.
4. If all voltages are correct according to the PA MAP procedures but are missing or out of tolerance at the board destination pins, isolate the failure to either the board or wiring. Refer to Figures BU531-1 through BU531-5 and repair or replace as necessary.
5. Request aid if the problem is not resolved.

8140 Model	Voltage and Tolerance	Source* Plug/Pin	Board Destination Pins
AXX	+5V ± 9% +4.55 to +5.45	Y2, Y3, Y4/C04–C11	All D03, J03, P03, U03
	-5V ± 9% -5.45 to -4.55	P1/B3E01	All B06, G06, M06, S06
	+8.5V ± 9% +7.73 to +9.27	P1/B2A14, P3/B4A14	E2B11, E1G11, E2M11, E2S11
	Ground (DC Common)	Z2, Z3, Z4/C04–C11	All D08, J08, P08, U08
BXX	+5V ± 9% +4.55 to +5.45	P1/B3A01, P2/B4A01, P3/B5A01, P4/U3A01, P5/U4A01, P6/U5A01, Bus Bar Rows E, J, N, S	All D03, J03, P03, U03 except board locations V2 through V5
	-5V ± 9% -5.45 to -4.55	P1/B3E01, P2/B4E01, P3/B5E01, P4/U3E01, P5/U4E01, P6/U5E01	All B06, G06, M06, S06 except board locations V2 through V5
	+8.5V ± 9% +7.73 to +9.27	P1/B2A14, P2/B3A14, P3/B4A14, P4/U2A14, P5/U3A14, P6/U4A14	H2B11, H2G11, H2M11, H2S11
	Ground (DC Common)	P1/B2E14, P2/B3E14, P3/B4E14, P4/U2E14, P5/U3E14, P6/U4E14, Bus Bar Rows C, G, L, Q	All D08, G08, P08, U08 and board location V2 pins D03, J03, P03, U03, B06, G06, M06, and S06.

*See Figure BU531-4 for 8140 model AXX locations and Figure BU531-5 for BXX.

Figure BU531-1. 8140 01A-A1 Board DC Voltage Distribution

8140 Model	Voltage and Tolerance	Source* Plug/Pin	Board Destination Pins
A3X, A4X, and A5X	+5V ± 9% +4.55 to +5.45	Y2, Y3, Y4/C04–C11	All D03, J03, P03, U03
	-5V ± 9% -5.45 to -4.55	P1/B3E01	All B06, G06, M06, S06
	+8.5V ± 9% +7.73 to +9.27	P1/B2A14, P3/B4A14	All B11, G11, M11, S11
	-8.5V ± 9% -9.27 to -7.27		H2D07, K2D07, F2D07 [1]
	Ground (DC Common)	Z2, Z3, Z4/C04–C11	All D08, J08, P08, U08
A6X and A7X	+5V ± 9% +4.55 to +5.45	Y2, Y3, Y4/C04–C11	All D03, J03, P03, U03
	-5V ± 9% -5.45 to -4.55	P1/B3E01	All B06, G06, M06, S06
	+8.5V ± 9% +7.73 to +9.27	P1/B2A14, P3/B4A14	Locations A2–K2 Pins B11, G11, M11, S11
	+12V ± 9% +10.92 to +13.08	P4/U2A14, P5/U3A14, P6/U4A14	Locations N2–V2 Pins B11, G11, M11, S11
	Ground (DC Common)	Z2, Z3, Z4/C04–C11	All D08, J08, P08, U08

*See Figure BU531-4 for locations.

[1] 8140 Models A3X and A4X only.

Figure BU531-2. 8140 Models AXX 01A-A2 Board DC Voltage Distribution

8140 Model	Voltage and Tolerance	Source* Plug/Pin	Board Destination Pins
BXX	+5V ± 9% +4.55 to +5.45	P1/B3A01, P2/B4A01, P3/B5A01, Bus Bar Rows E, J	All D03, J03, P03, U03
	-5V ± 9% -5.45 to -4.55	P1/B3E01, P2/B4E01, P3/B5E01	All B06, G06, M06, S06
	+12V ± 9% +10.92 to +13.08	P1/B2A14, P2/B3A14, P3/B4A14	Locations C2–K2 Pins B11, G11, M11, S11
	Ground (DC Common)	P1/B2E14, P2/B3E14, P3/B4E14, Bus Bar Rows C, G	All D08, J08, P08, U08

*See Figure BU531-5 for locations.

Figure BU531-3. 8140 Models BXX 01A-C1 Board DC Voltage Distribution

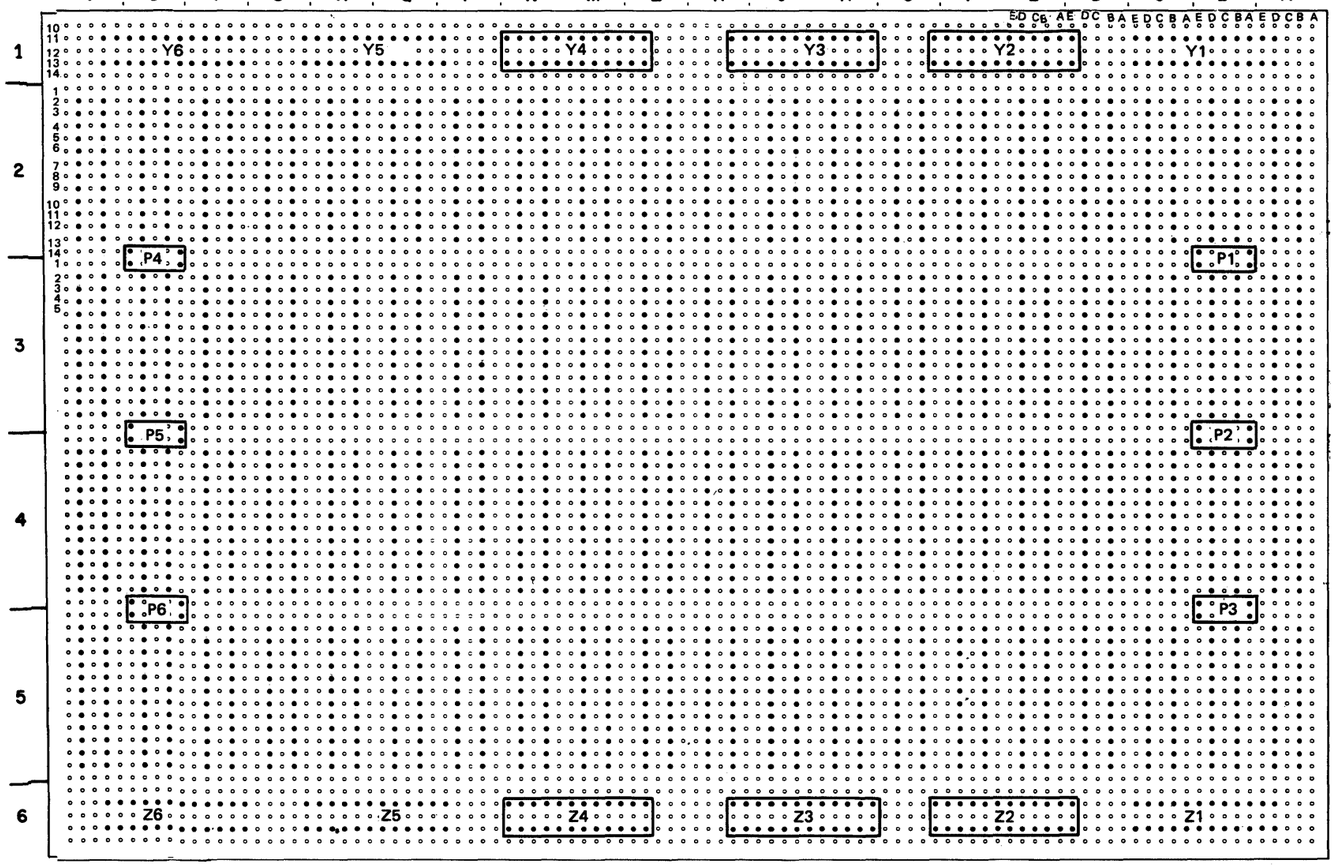


Figure BU531-4. 8140 01A–A1 Board and 8140 Models AXX 01A–A2 Board DC Voltage Connector Locations

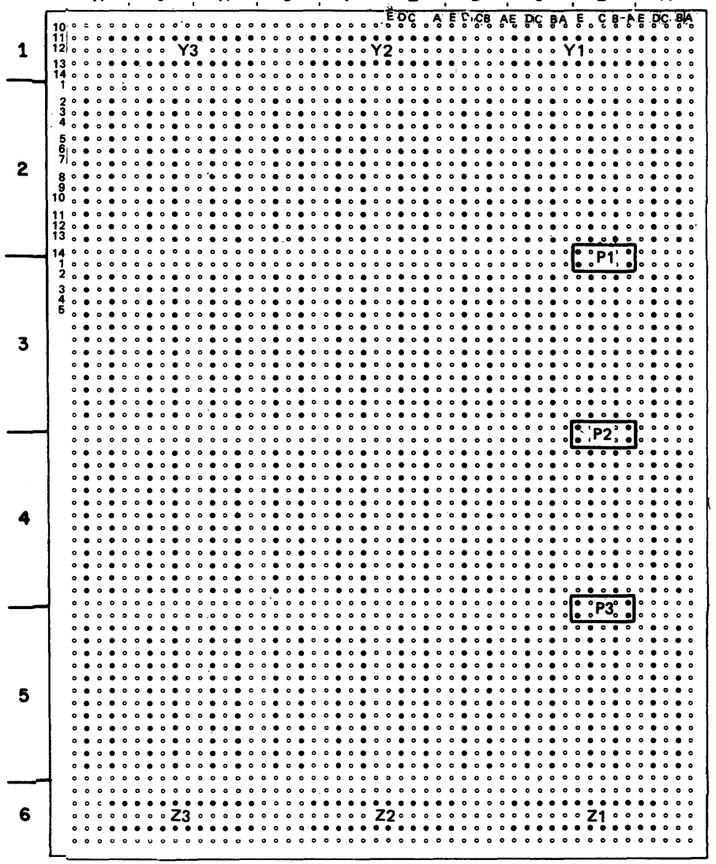


Figure BU531-5. 8140 Models BXX 01A–C1 Board DC Voltage Connector Locations

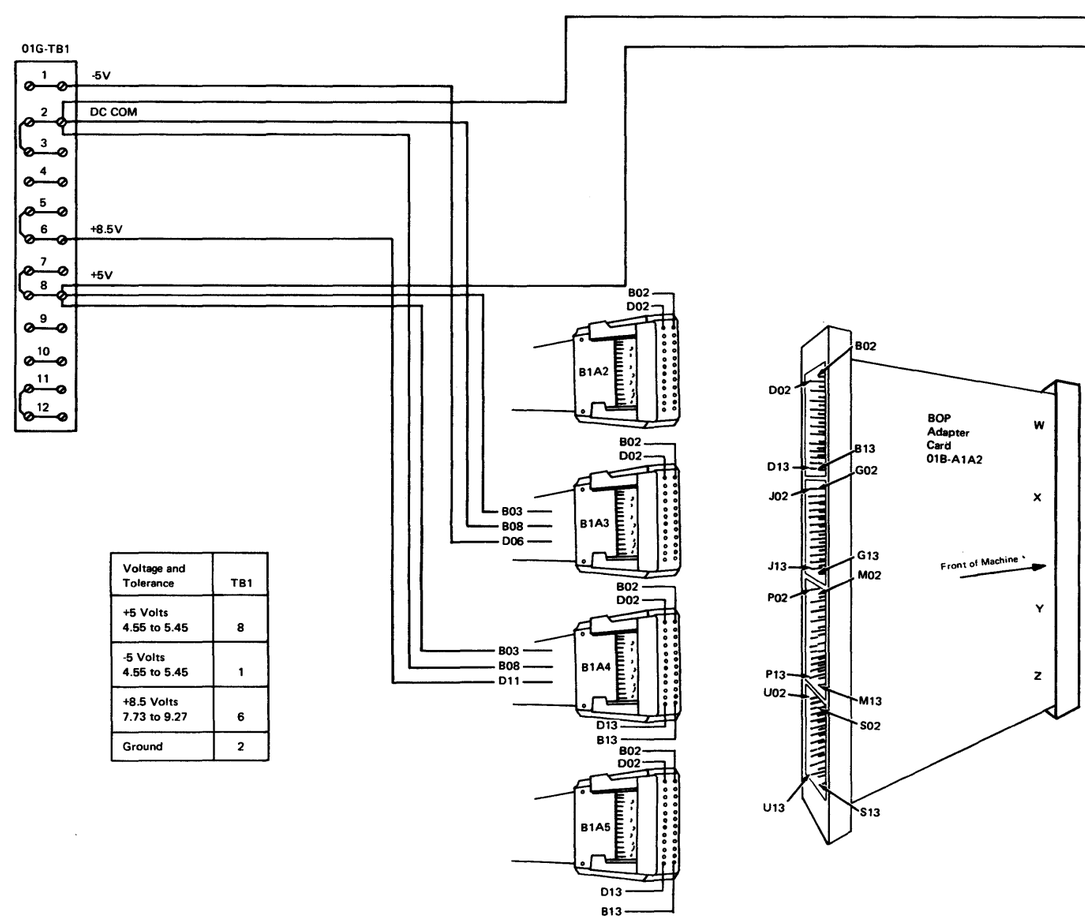
BU532 8140 BOP Adapter and Indicator Card Voltage Checks

Perform the following procedure to determine if the correct voltages for the BOP adapter card and BOP indicator card are present:

1. Check the voltage at 01G—TB1 by using the table in Figure BU532-1. (01G—TB1 is located next to the fuse holders at the top left of the service area.)
2. If any voltage is missing or out of tolerance at 01G—TB1, go to the PA MAP for further power fault isolation.

   Caution: Power down if performing the following steps.

3. If all voltages are correct at 01G—TB1, remove the connector at the indicator card (P1), and the cables at BOP adapter card locations B1A3 and B1A4. Check the voltages on the connector and cables using Figure BU532-1.
4. If all voltages are correct at the connector and cables, reseat the connector and cables and return to the BU MAP or action plan that sent you here.
5. If any voltage is either missing or out of tolerance at the cables or connector and correct at 01G—TB1, isolate the failure by using Figure BU532-1 and repair or replace as necessary.
6. Request aid if the problem is not resolved.



Voltage and Tolerance	TB1
+5 Volts 4.55 to 5.45	8
-5 Volts 4.55 to 5.45	1
+8.5 Volts 7.73 to 9.27	6
Ground	2

Figure BU532-1. 8140 BOP and Adapter Card Voltage Distribution

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