IBM Customer Engineering

Maintenance Manual

223-2712-1

IBM 7040-7044 Data Processing Systems

Channels B, C, D, and E

IBM

Customer Engineering Maintenance Manual

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Channels B, C, D, and E

PREFACE

This manual contains logic diagrams of tape operations, Simplex interface operations, and direct data operations. A brief description of each of these operations precedes the diagrams in each major section. A detailed description of the operations diagrammed can be found in Channels B, C, D, E CE Manual of Instruction, Form 223-2755.

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SAFETY

Accidents do not always happen to "the other fellow." Be smart! When servicing any equipment, remove rings and watches, roll up your sleeves, and tuck in your tie. Put on your safety glasses! If power must be on when working on power supplies, probe with one hand only; keep the other hand off the frame. You know the safety rules--follow them!

MAJOR REVISION (December 1963)
This edition, Form 223-2712-1, obsoletes Form 223-2712-0 and all earlier editions. The "Tape Interface" section has been updated and the "Simplex" and "Direct Data" sections are new.

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CONTENTS (TEXT)

CONTENTS (ILLUSTRATIONS)

CONTENTS (ILLUSTRATIONS)

ILLUSTRATIONS (ALPHABETICAL)

FRAME CONFIGURATION

The 7904-1 and 7904-2 are packaged in a standard rack and panel frame (Figure 1). The frame is divided into four panels that provide space for the logic circuitry required for two channels. Panels 1 and 3 accommodate the logic circuits for one channel, and panels 2 and 4 accommodate the circuits for the second channel.

The frame is identified as frame 02. In a system where two frames are used (more than two channels), the frames are designated as frames 02 A and 02 B. This designation would be used, for example, in a system containing two 7904-2 data channels.

To locate cards, pins, or components, each panel is divided into rows (A through K) and columns (1 through 28) as shown in Figure 1. The two adjacent rows identified as Y and Z are used to jumper card connections from panel 3 to panel 1, and from panel 4 to panel 2, respectively. Row Z of panels 3 and 4 provide connections for dot OR'ing signal lines from the two channels to the I-O connector panel.

Logic cards are on the rear side of the panels and are accessible through the rear of the machine.

I-O CONNECTOR PANEL

Cables containing the data and signal lines from the CPU and associated I-O units are connected to the I-O connector panel (Figures 1 and 2). The I-O connector panel consists of two rows of connectors designated as the upper row (U) and the lower row (L). Each row has 52 positions. Figure 2 shows the connector positions grouped according to functions.

POWER

Power Supplies

The dc power required for the operation of electronic circuitry in a 7904-1 or 7904-2 is furnished by five self-contained power supplies on a sliding gate at the rear of the frame (Figure 3). The dc power supplies are numbered 1 through 5, and in that order provide the following voltages: -12v, +12v, +6v, +12v, and +6v.

A -12v (mc) output from power supply 1 is used for marginal check purposes. A connector is provided so that a portable ±3-volt marginal check power supply may be connected in series with the -12 vm output. Refer to Figure 4 for the location of the marginal check connector.

Located on each dc power supply are two circuit breakers designated as CB 1 and CB 2. CB 2 is a thermal-type circuit breaker connected to the input of the power supply to protect it from damage in the event of a component failure within the supply. The contacts may be operated manually by means of a reset plunger, which resets the circuit breaker. The plunger has a white ring around its base that is exposed when the circuit breaker is tripped. CB 1 is connected on the output of each power supply and provides overload protection. This circuit breaker may be operated manually with an on-off switch used to reset the contacts.

Input power to the five dc power supplies is supplied by a 1,250 watt ferroresonant power supply that regulates the input voltage. The ferroresonant supply is also on the sliding gate at the rear of the frame, and provides a regulated output of approximately 133 vac.

Power Switches

Two power switches and a power on lamp are on the upper right portion of the front of the frame (Figure 4). The switches are the remote-local switch and the power on-off switch.

Input power to the 7904 is distributed from the CPU. With the remote-local switch in the remote position, input power to the 7904 is controlled solely by the CPU power switches. With the remote-local switch in the local position, input power may be locally controlled with the power on-off switch. Local power control is used primarily for off-line operation of the 7904. The power on-off switch is ineffective when the remote-local switch is in the remote position.

The power on lamp, when on, indicates that dc power is up.

Tape Drive Power Gate

The tape drive power gate is essentially a junction box from which 115 vac and 208v, 3 phase power is distributed to tape drives associated with a particular 7904. The tape drive power gate is mounted on the front of the frame (Figure 4), and is hinged so that it will swing out to permit access to the wiring directly behind it (panel 3). Four separate power outputs are available from the tape drive power gate. Each output provides power for a bank of five tape units. A circuit breaker for each separate tape power output is in the tape drive power gate. Input power to the tape drive power gate is supplied from the CPU.

Power Input And Output Connectors

There are six connectors for attaching power cables to a 7904 (Figures 1 and 2). The connectors are numbered 1 through 6 and are on each side of the I-O connector panel. Input power from the CPU is fed through connectors 1 and 2 to the 1,250 watt ferroresonant power supply and the tape drive power gate. The four power outputs from the tape drive power gate are fed to connectors 3, 4, 5, and 6.

CHANNEL INDICATOR LIGHTS

Neon indicators that show the status of various control triggers, error triggers, and register positions are on the wiring side of the panels associated with each channel. The location of the indicators and their Systems page reference are shown in Figure 5.

BASIC CABLE ARRANGEMENT BETWEEN CPU AND CHANNELS

This section describes the basic groups of interconnecting cables between the CPU and 7904 data channels. This information is not intended for use as a guide or as instructions for connecting the cables; a cable chart should be referred to for this purpose.

The interconnecting cables consisting of signal and data lines may be divided into three groups: the channel to CPU lines (Q lines), the CPU to channel lines (Q lines), and a group of mixed control lines (C lines). Q lines are distributed lines, or lines that are shared on either end. Two examples are shown in Figure 6. C lines are point-to-point lines as illustrated in Figure 6.

The three basic groups of cables are shown in Figure 7. Two 7904-2 data channels are used as an example in the figure. The channel to CPU lines are in eight cables that are divided into two banks, with each bank consisting of four cables from each 7904-2. Each bank of four cables contains the channel to storage bus lines, trap identification bit lines, and certain control lines (such as B cycle demand) for the two channels in the respective 7904-2. These lines are jumpered (dot OR'ed) in each 7904-2 and are shared by the two channels. The cables are attached to module C of the CPU.

The second group consists of five cables that contain the CPU to channel lines (Q lines). These lines are shared by all four channels and generally consist of:

1. Storage bus to channel lines.
2. Tape unit address lines.
3. Primary and secondary operation decoder lines.
4. Interface select (address) lines.
5. Clock pulse lines.
6. Miscellaneous control lines.

The method of distributing the lines contained in the five cables is shown in Figure 7. The lines from the CPU are attached to channel 1, where they are jumpered internally to channel 2, and then routed to the second 7904-2 by cables. The lines are internally distributed to channels 3 and 4 in a like manner. In the last channel, the lines are terminated with terminating resistor loads. The sequence in which the channels are connected to the lines establishes the relative remoteness of the channels with respect to the CPU. Therefore, the sequence determines the channel priority status for B cycle and trap requests. The channel with the terminating resistor loads (Figure 7), in this case, channel 4, is always the most remote channel and thus has priority over other channels for B cycle and trap service. Channel 3 has second priority, and the remaining two channels are connected in the order of decreasing priority.

The third group of cables contains mixed control lines (C lines): control lines from the CPU to channel, and lines from the channel to CPU. There is one cable for each channel in the system, and each cable contains control lines that are not shared by other channels. These lines are:

CPU to channel
1. Channel select.
2. Trap enable lines.
3. Tape density switch lines.

Channel to CPU
1. Channel in use.
2. Direct data interrupt.
3. Channel trap demand.
4. Channel check indicator.

The specific connector locations for attaching these cables to module C of the CPU are shown in Figure 7. These locations determine the identification (B, C, D, or E) of the respective channels, and thus the trap store location. Each location consists of two edge connector positions for attaching a cable.

Note: A channel's designation, B, C, D, or E, is not indicative of its priority status for B cycles and trap servicing. The priority status (remoteness from the CPU) is determined by the sequence in which the channels are connected to the CPU to channel lines.

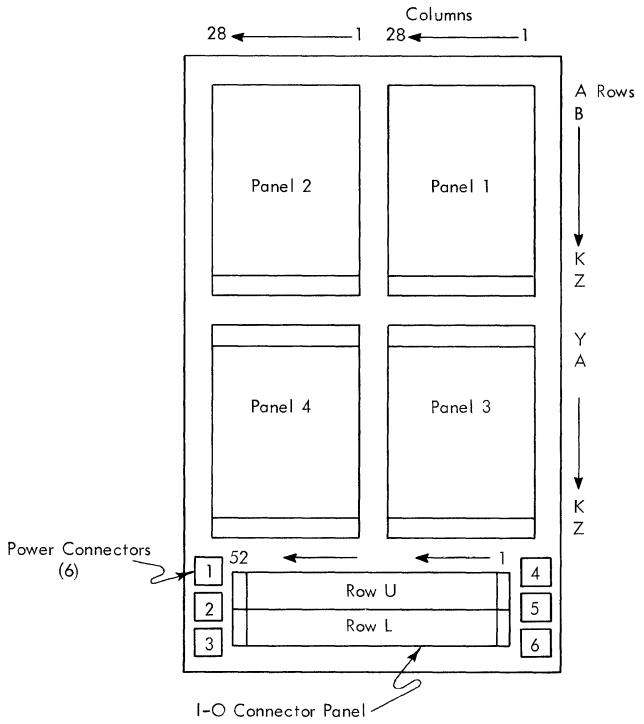


FIGURE 1. FRAME 02 - FRONT LAYOUT (WIRING SIDE)

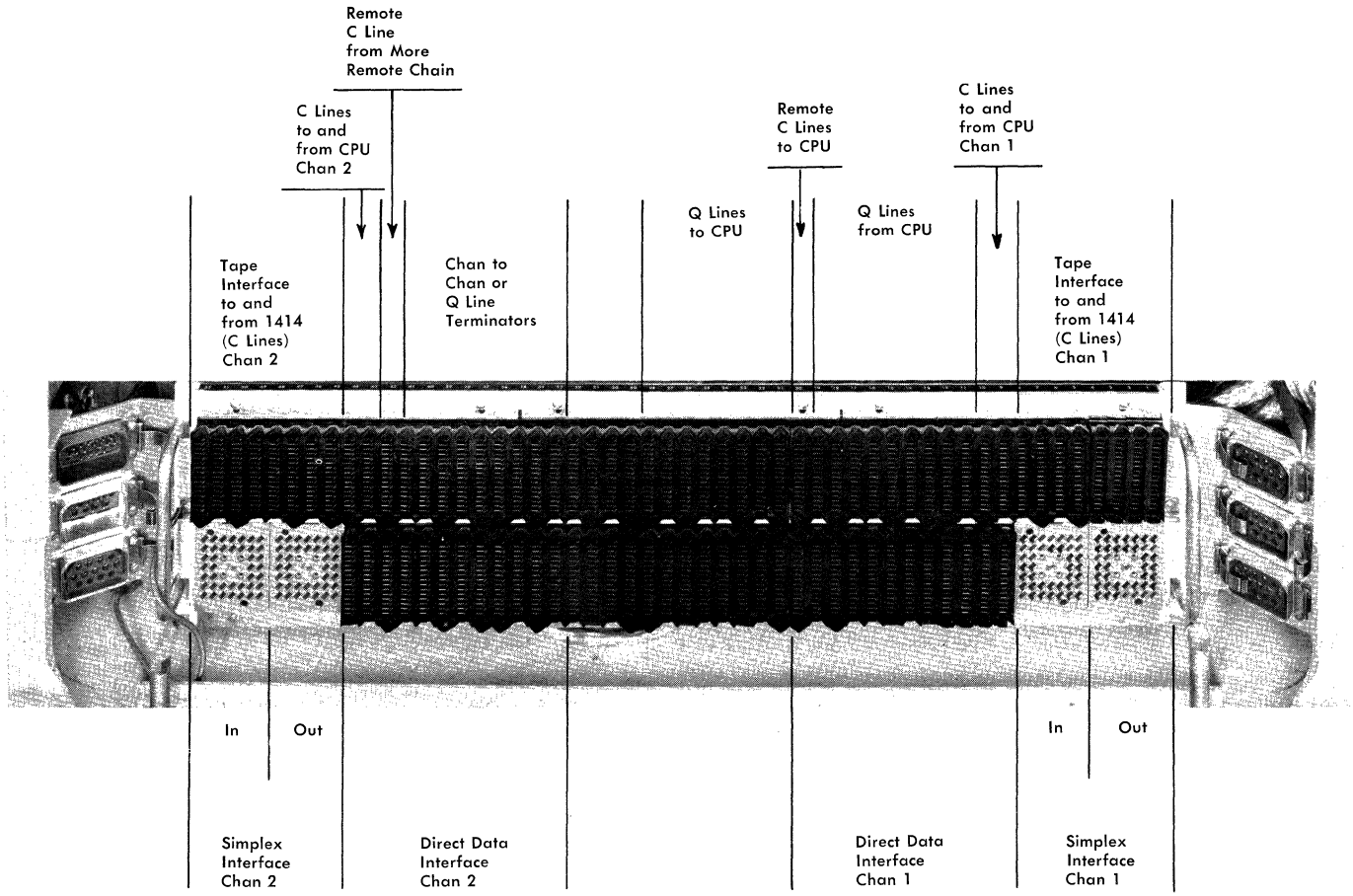


FIGURE 2. I-O CONNECTOR PANEL

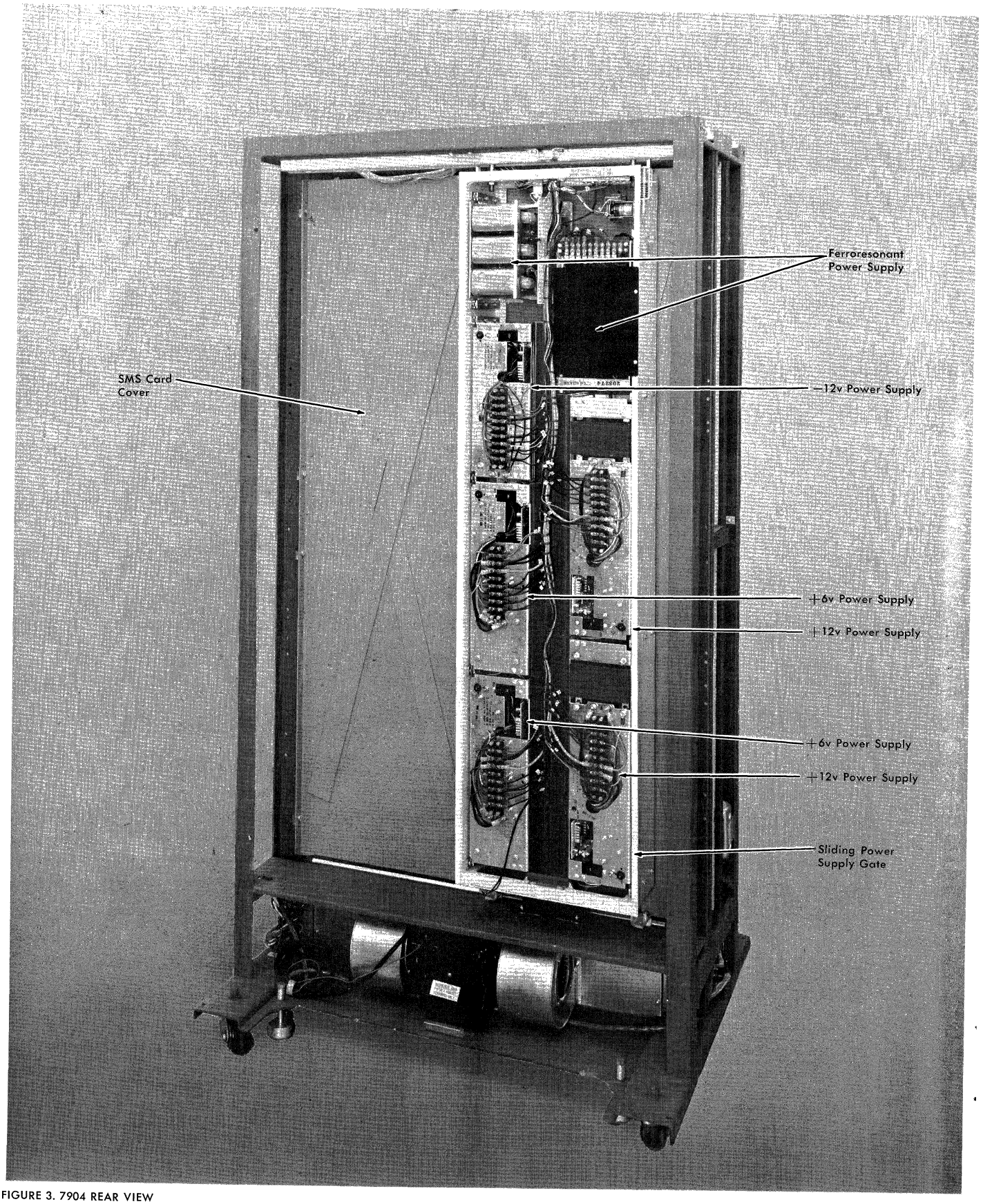


FIGURE 3. 7904 REAR VIEW

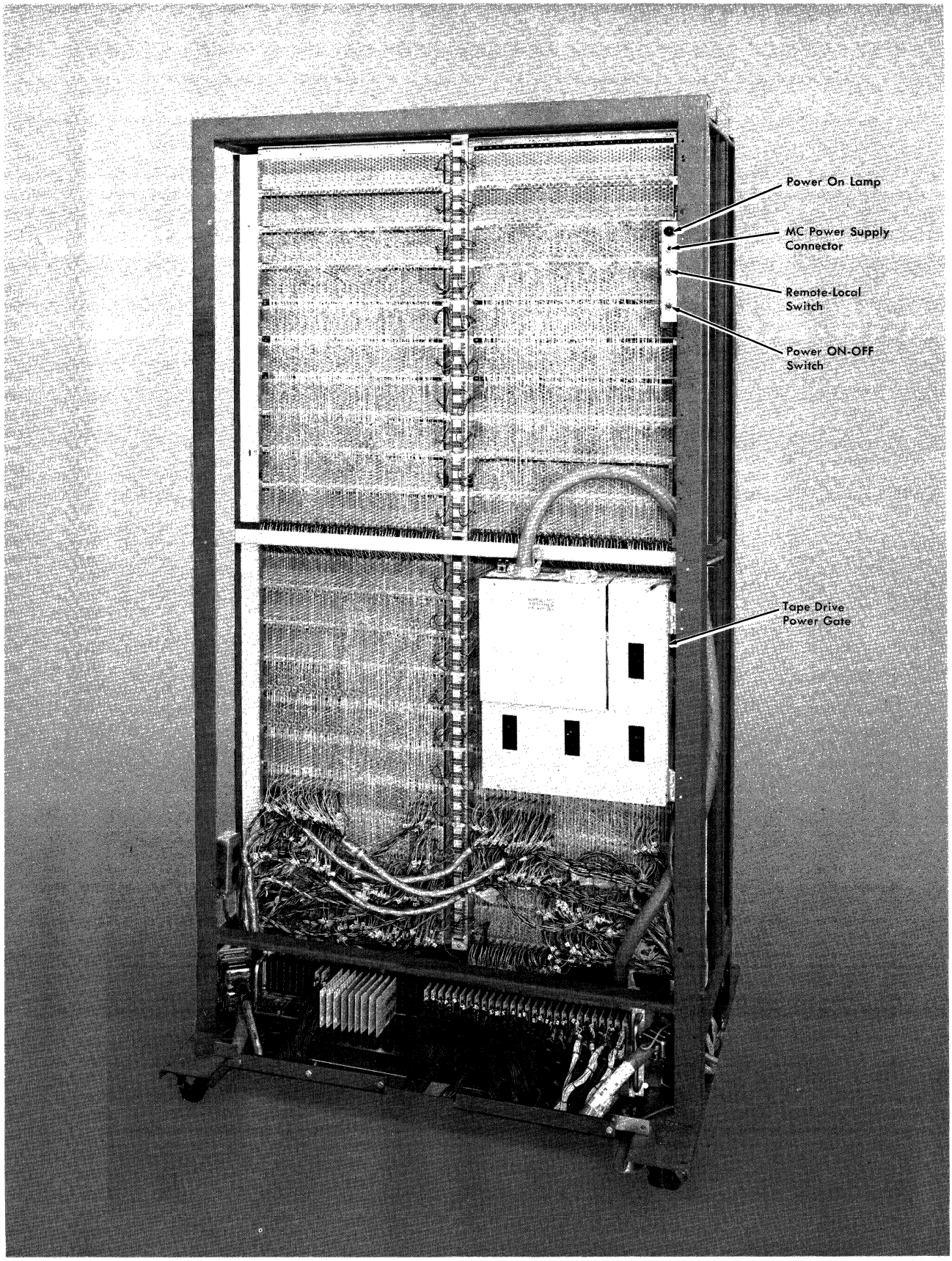
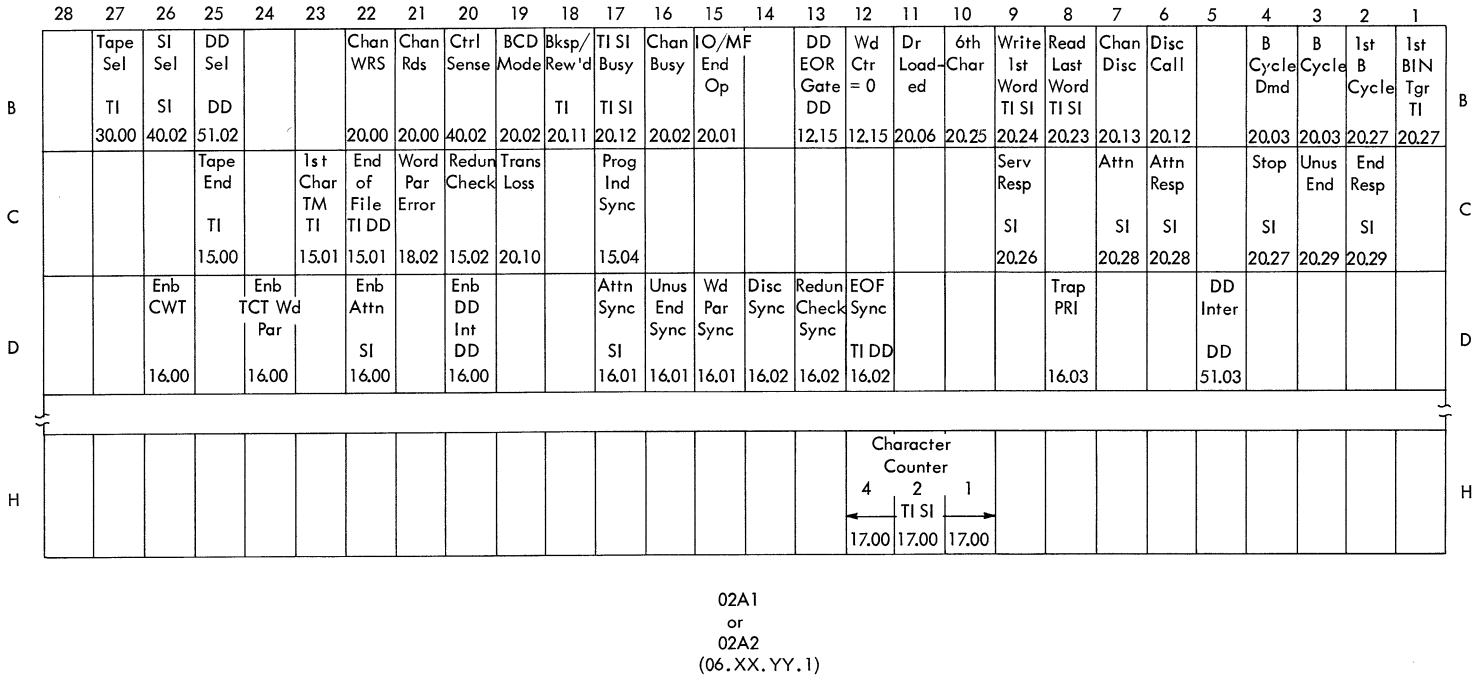


FIGURE 4. 7904 FRONT VIEW



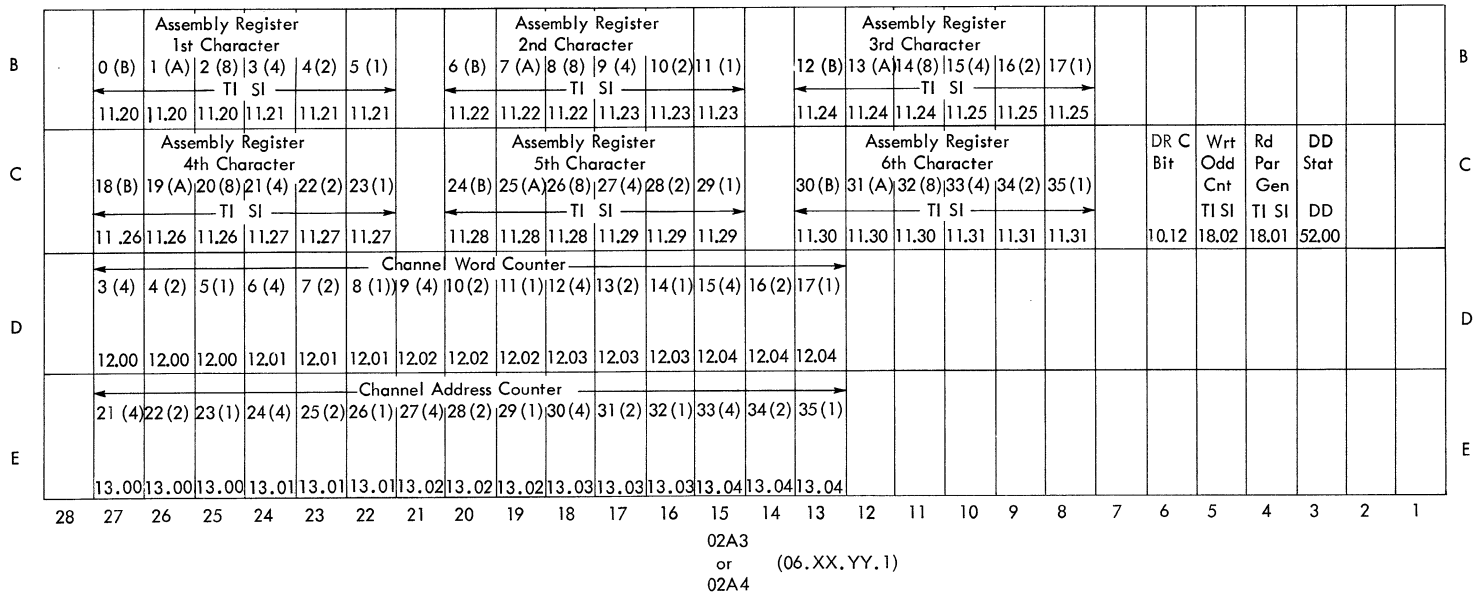


FIGURE 5. CHANNEL INDICATORS

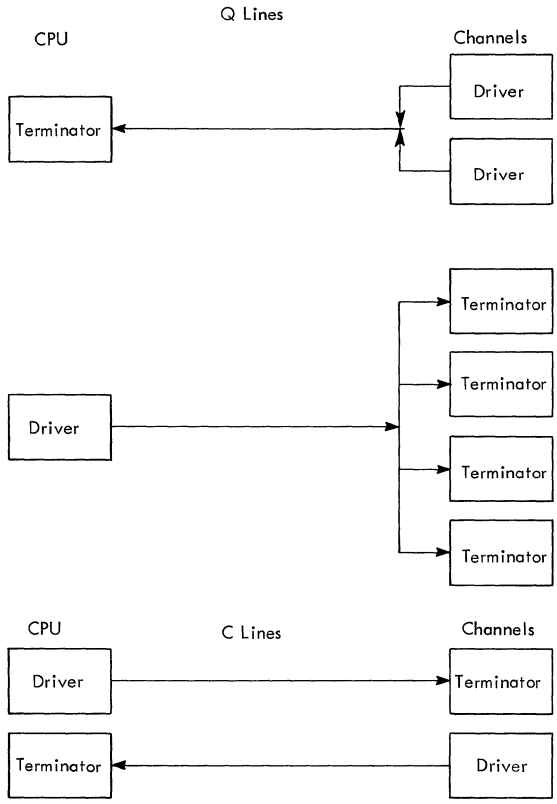


FIGURE 6. Q LINE AND C LINE EXAMPLES

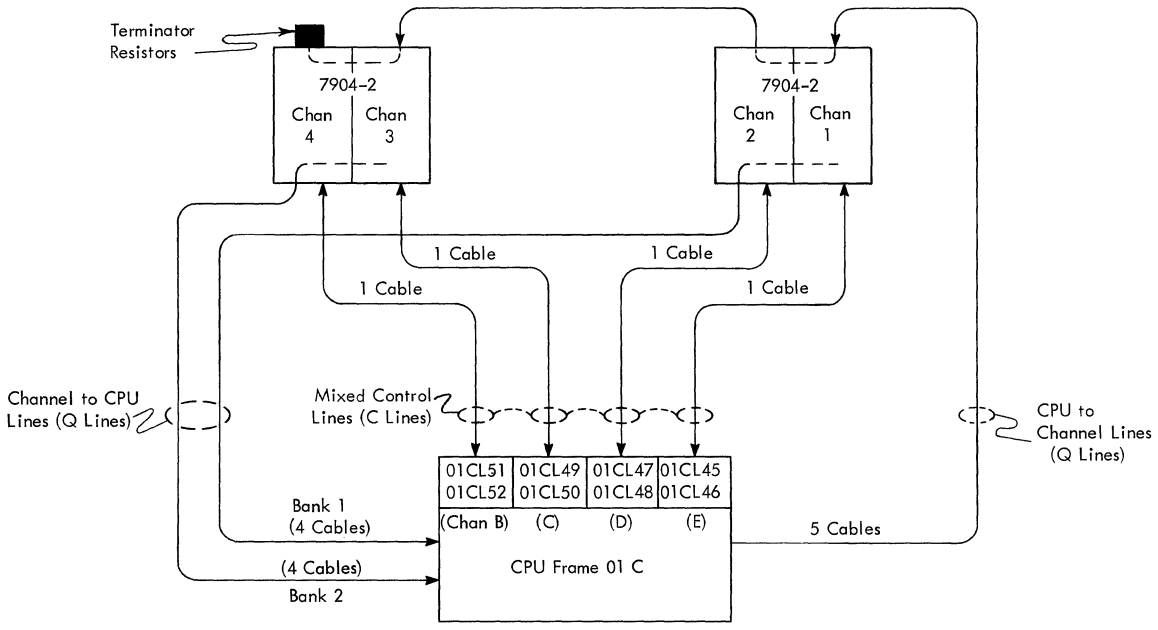


FIGURE 7. BASIC CABLE ARRANGEMENT, 7904 CHANNELS AND CPU

WRITE TAPE OPERATION (Figures 8-24)

Words are transferred (in parallel) from storage to a 7904 channel, and then sent a character at a time to the 1414 attached to the tape interface of that channel.

The word counter in the 7904 channel determines the number of words transmitted. It is initially set for the desired number of words, and reduced by one as each word is transmitted. When the counter reaches zero, transmission stops.

Figure 11 shows the sequence of the write tape operation.

Write Selecting the Channel (WRS)

The address portion of the WRS instruction selects channel B, C, D, or E, selects the tape interface of that channel, and selects a particular tape unit on that interface (Figure 12). The operation portion of the WRS instruction sets up the channel for writing; that is, it conditions certain circuits in the channel that will allow writing to the 1414 (and on to the tape unit) through the tape interface. During the WRS operation, tape motion is started. The WRS operation ends and the program goes on with the next instruction while the tape unit is getting up to speed.

Command Word Loading (RCH)

An RCH instruction for the channel just selected is executed, causing a command word to be sent from storage to the channel. The command word, when entered into the channel, sets the word counter and address counter. The RCH instruction requires an I cycle and an E cycle, after which the CPU proceeds with the next instruction.

The word counter not zero and the data register not loaded cause a B cycle demand. See Figure 13 for actions in the channel caused by the RCH.

B Cycle

The word counter not zero and the data register not loaded cause a B cycle demand to be sent to CPU (Figure 14). The next CPU cycle following the request becomes a B cycle, during which the first word to be transmitted is sent from storage to the channel's data register. During this first B cycle, the first word immediately moves on to the assembly register.

Because the data register is now empty, another B cycle is requested; during this B cycle, the data register is loaded with the second word. At this point, the tape unit is nearly up to writing speed, the first word is waiting in the assembly register, and the second word is in the data register.

Character Transmission

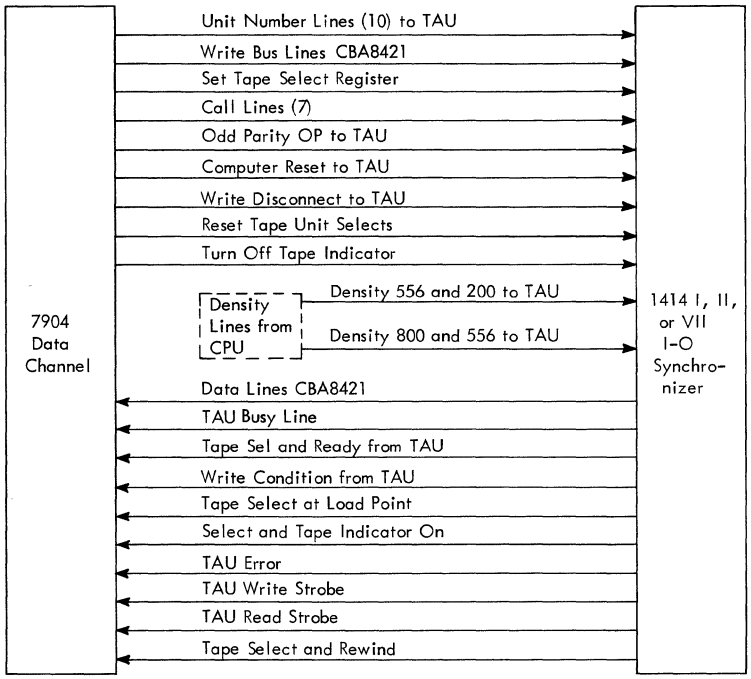
While the first word is in the assembly register, the first character of this word is being gated to the write bus (by the character counter). When the tape unit gets to writing speed, it writes the first character and sends a write strobe signal to the channel. The write strobe signal tells the channel that the tape unit has written a character and will soon need another one.

Each write strobe trips off a series of three single-shots in the channel (Figure 16). The single-shots check each character sent for the proper parity, and control the character counter (make sure each of the six characters is gated out of the assembly register in the proper order). After each group of six characters is transmitted, the next word (always waiting in the data register) moves to the assembly register. This action causes a B cycle, which again fills the data register.

As words move from storage to the data register on B cycles, the word counter is stepped down. When the word counter reaches zero, no more B cycles are allowed. The last word moves into the assembly register and is sent to the tape unit. After the tape unit writes the last character of the last word and sends the write strobe to the channel (firing the single-shots for the last time), all conditions are present in the channel to end the write operation. The channel initiates the ending of the write operation by sending a write disconnect signal to TAU.

End Operation and Disconnect

The disconnect signal at the 1414 causes the tape unit to write the check character, read-check the check character, and then turn off the write trigger in the 1414 (Figure 17). When this trigger goes off, the TAU busy line drops to the channel. In the channel, the fall of TAU busy turns on the disconnect call trigger, which subsequently turns on the channel disconnect trigger. The channel disconnect trigger resets the triggers that were maintaining the channel in a write tape status, and sets up trap sync triggers for any trap conditions that might have occurred during the write operation. The channel is now not busy and may be used by CPU for another read or write.



Note: 7904 line nomenclature shown.
Refer to Systems 06.03.01.1 for 1414 line nomenclature.

FIGURE 8. TAPE INTERFACE SIGNAL LINES

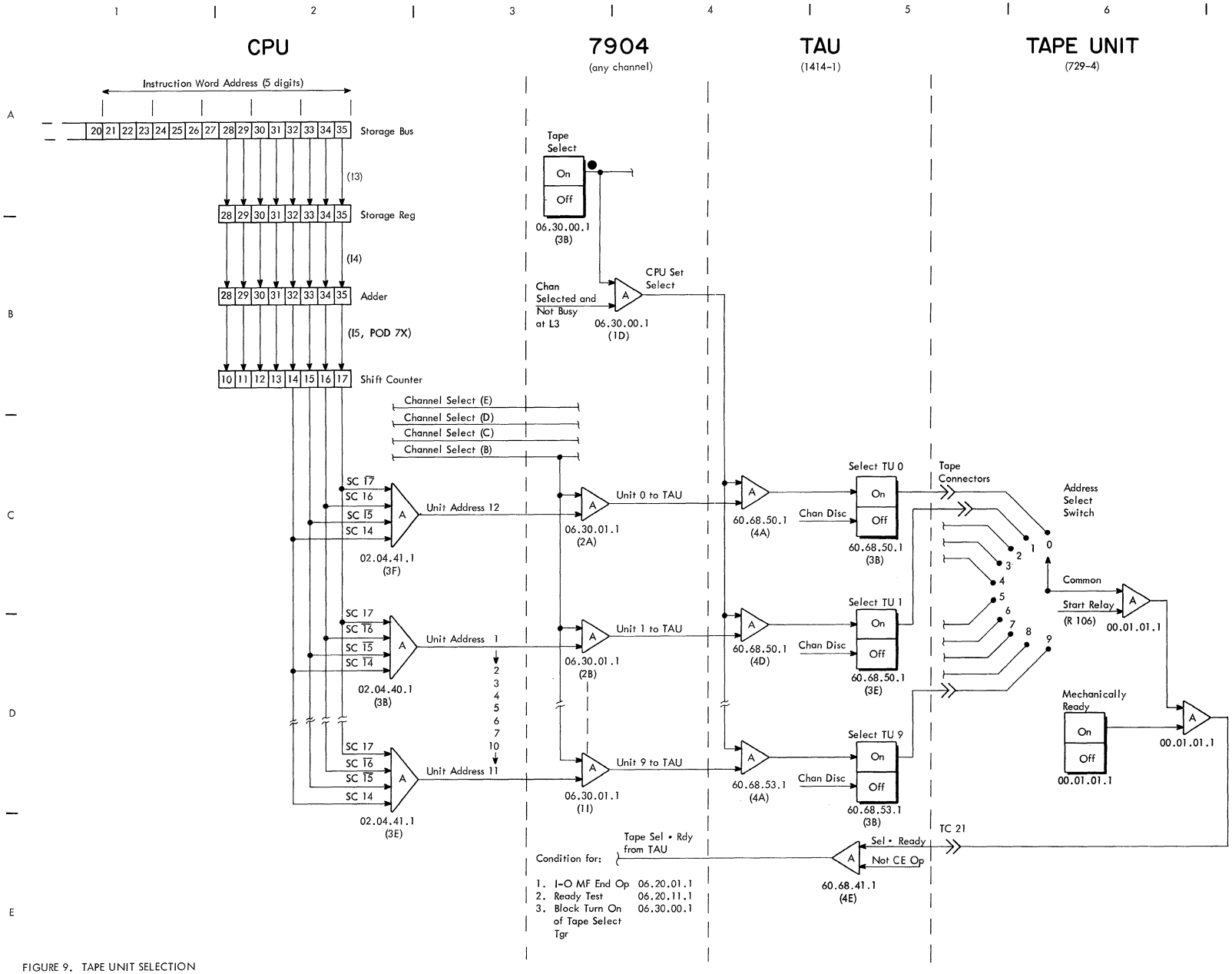
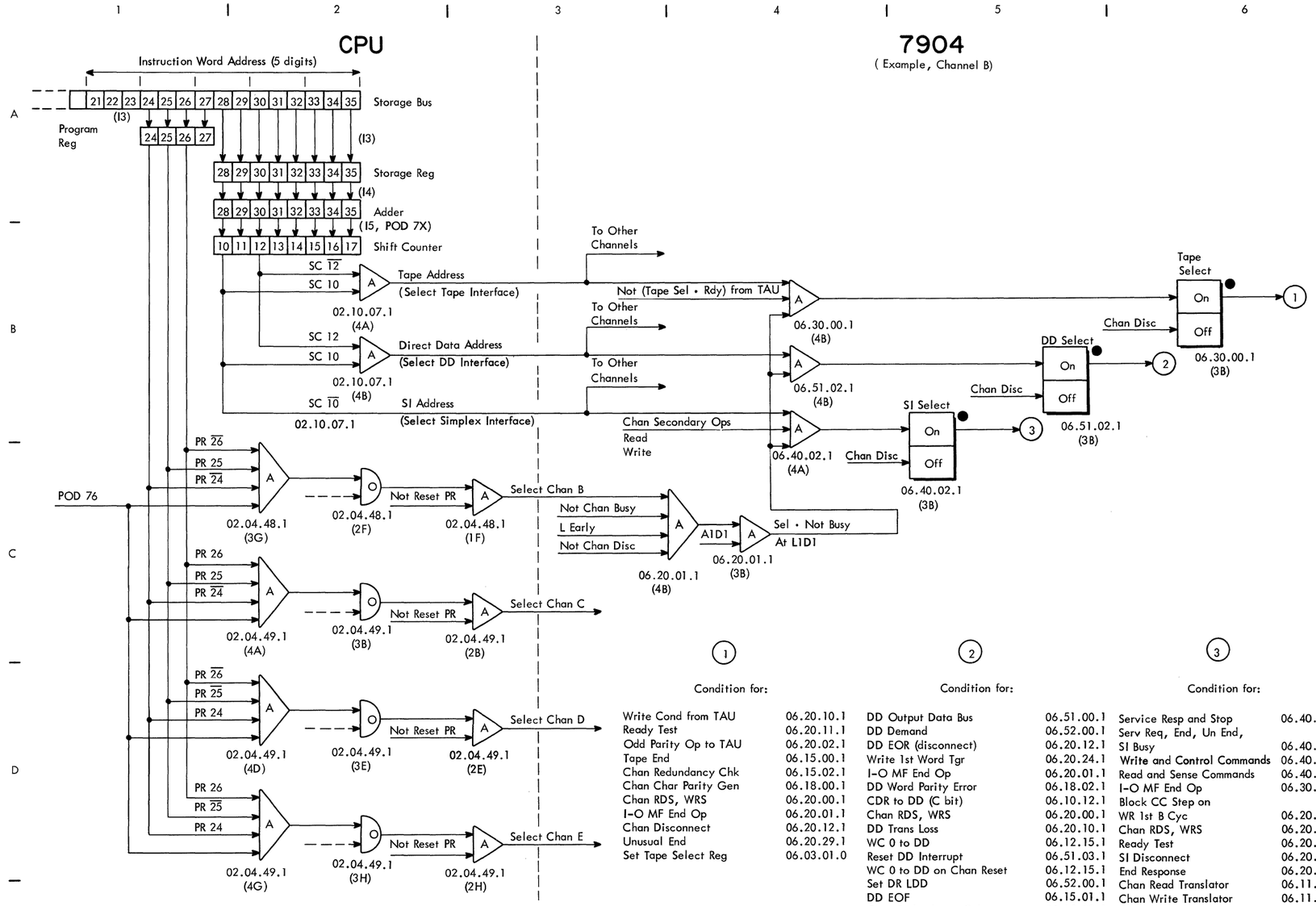


FIGURE 9. TAPE UNIT SELECTION



① Condition for:

Write Cond from TAU	06.20.10.1
Ready Test	06.20.11.1
Odd Parity Op to TAU	06.20.02.1
Tape End	06.15.00.1
Chan Redundancy Chk	06.15.02.1
Chan Char Parity Gen	06.18.00.1
Chan RDS, WRS	06.20.00.1
I-O MF End Op	06.20.01.1
Chan Disconnect	06.20.12.1
Unusual End	06.20.29.1
Set Tape Select Reg	06.03.01.0

② Condition for:

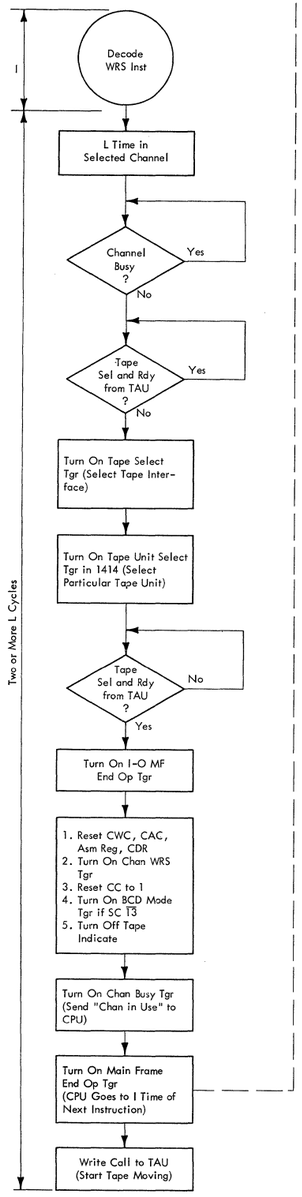
DD Output Data Bus	06.51.00.1
DD Demand	06.52.00.1
DD EOR (disconnect)	06.20.12.1
Write 1st Word Tgr	06.20.24.1
I-O MF End Op	06.20.01.1
DD Word Parity Error	06.18.02.1
CDR to DD (C bit)	06.10.12.1
Chan RDS, WRS	06.20.00.1
DD Trans Loss	06.20.10.1
WC 0 to DD	06.12.15.1
Reset DD Interrupt	06.51.03.1
WC 0 to DD on Chan Reset	06.12.15.1
Set DR LDD	06.52.00.1
DD EOF	06.15.01.1
Chan Redundancy Chk	06.15.02.1

③ Condition for:

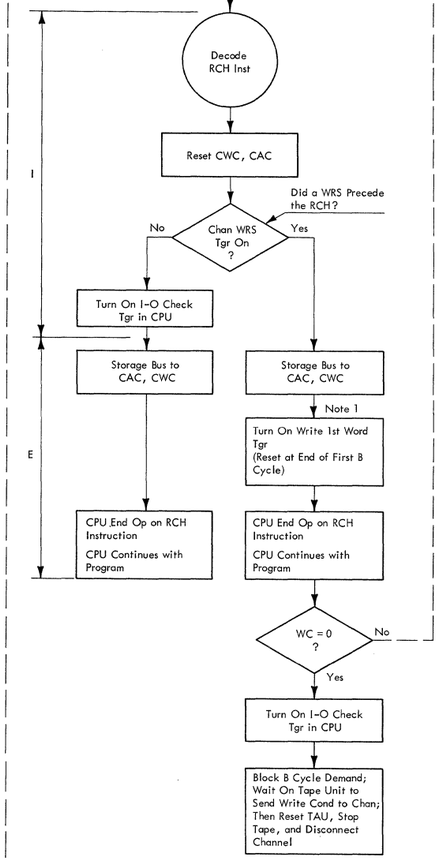
Service Resp and Stop	06.40.01.1
Serv Req, End, Un End, SI Busy	06.40.00.1
Write and Control Commands	06.40.01.1
Read and Sense Commands	06.40.01.1
I-O MF End Op	06.30.00.1
Block CC Step on WR 1st B Cyc	06.20.27.1
Chan RDS, WRS	06.20.00.1
Ready Test	06.20.11.1
SI Disconnect	06.20.12.1
End Response	06.20.29.1
Chan Read Translator	06.11.02.1
Chan Write Translator	06.11.05.1

FIGURE 10. CHANNEL AND INTERFACE SELECTION

WRS
(FIGURE 12)



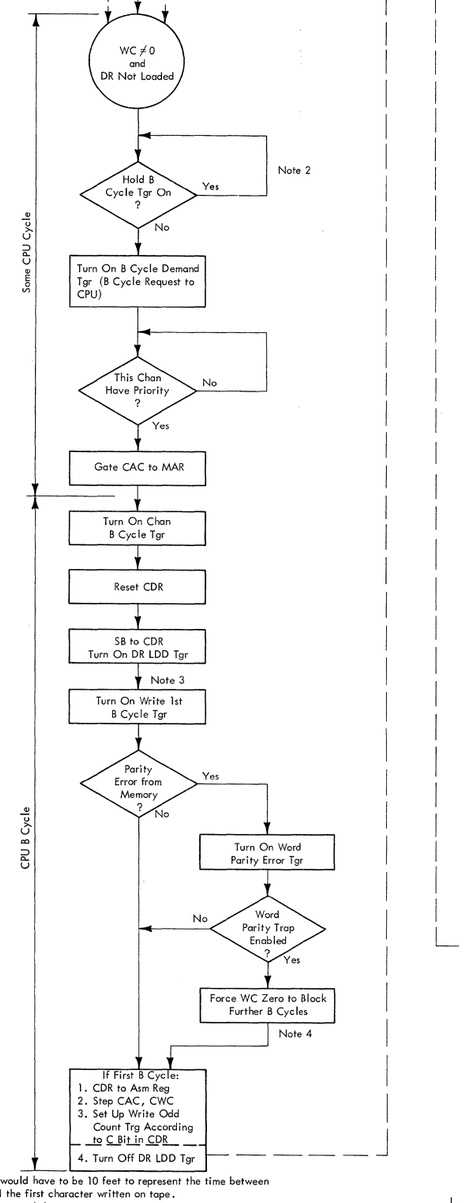
RCH
(FIGURE 13)



Note 1: Allows word obtained on first B cycle to be put into assembly register.

Note 2: The Hold B Cycle Tgr turns on with the Chan B Cycle Tgr and prevents the occurrence of successive B cycles; B cycles are permitted to occur no faster than once every three CPU cycles.

B CYCLE
(FIGURE 14)



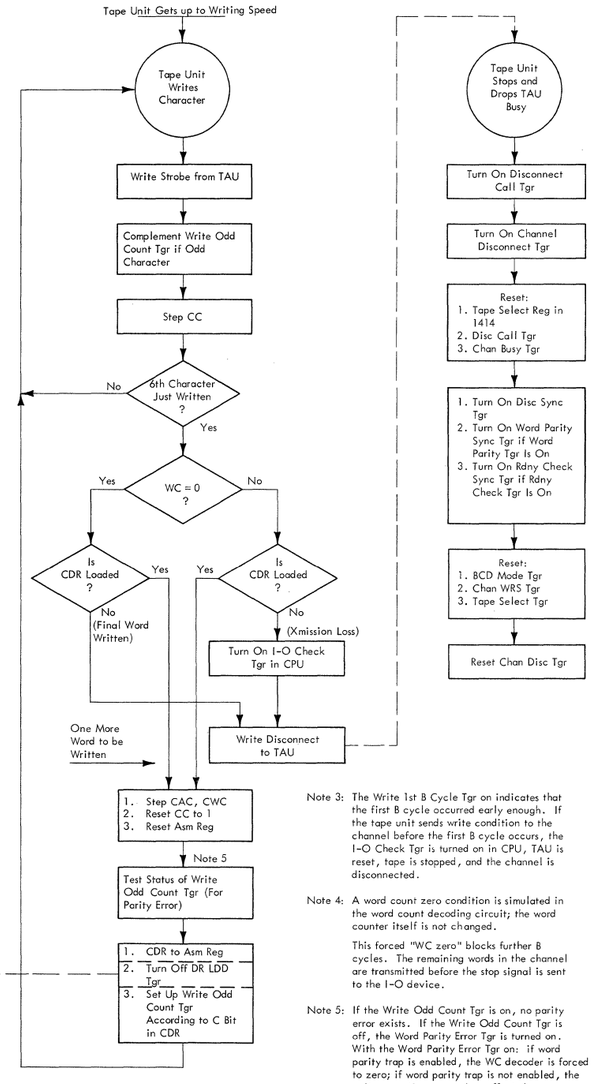
Note 3: The Write 1st B Cycle Tgr on indicates that the first B cycle occurred early enough. If the tape unit sends write condition to the channel before the first B cycle occurs, the I-O Check Tgr is turned on in CPU, TAU is reset, tape is stopped, and the channel is disconnected.

Note 4: A word count zero condition is simulated in the word count decoding circuit; the word counter itself is not changed.

This forced "WC zero" blocks further B cycles. The remaining words in the channel are transmitted before the stop signal is sent to the I-O device.

Note 5: If the Write Odd Count Tgr is on, no parity error exists. If the Write Odd Count Tgr is off, the Word Parity Error Tgr is turned on. With the Word Parity Error Tgr on: if word parity trap is enabled, the WC decoder is forced to zero; if word parity trap is not enabled, the write operation proceeds unaffected.

CHARACTER WRITING
(Figure 16)



DISCONNECT
(Figure 17)

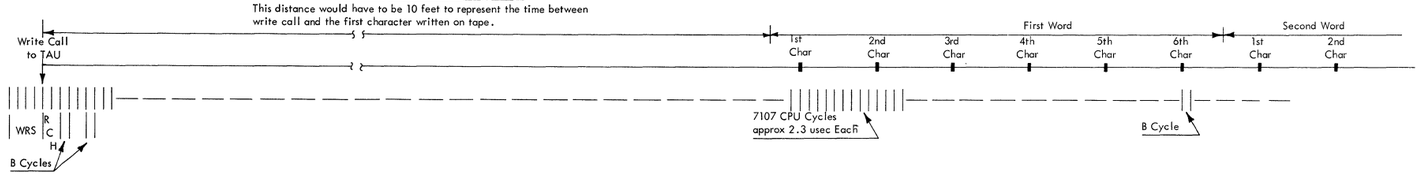


FIGURE 11. WRITE TAPE OPERATION SEQUENCE

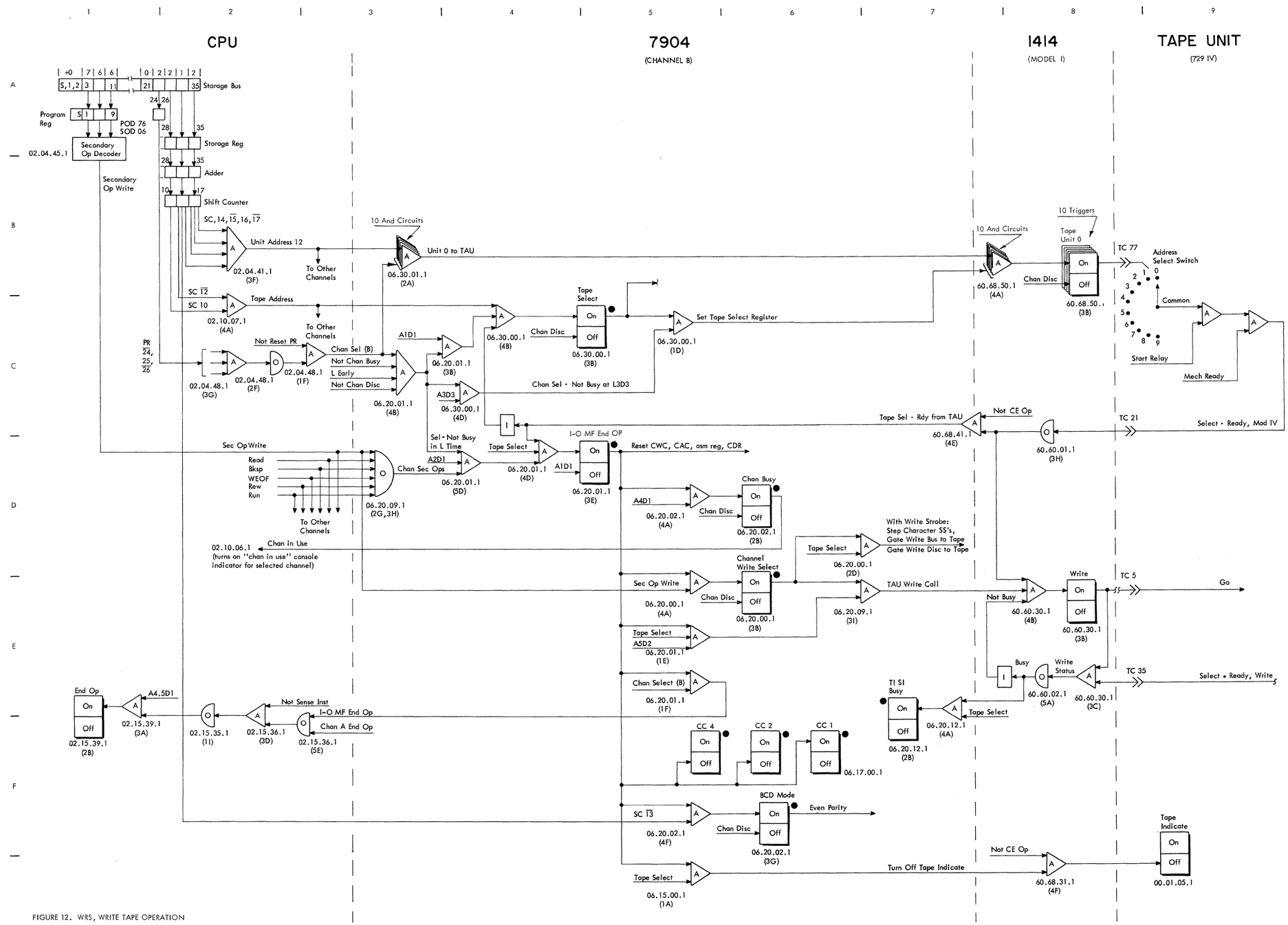


FIGURE 12. WRS, WRITE TAPE OPERATION

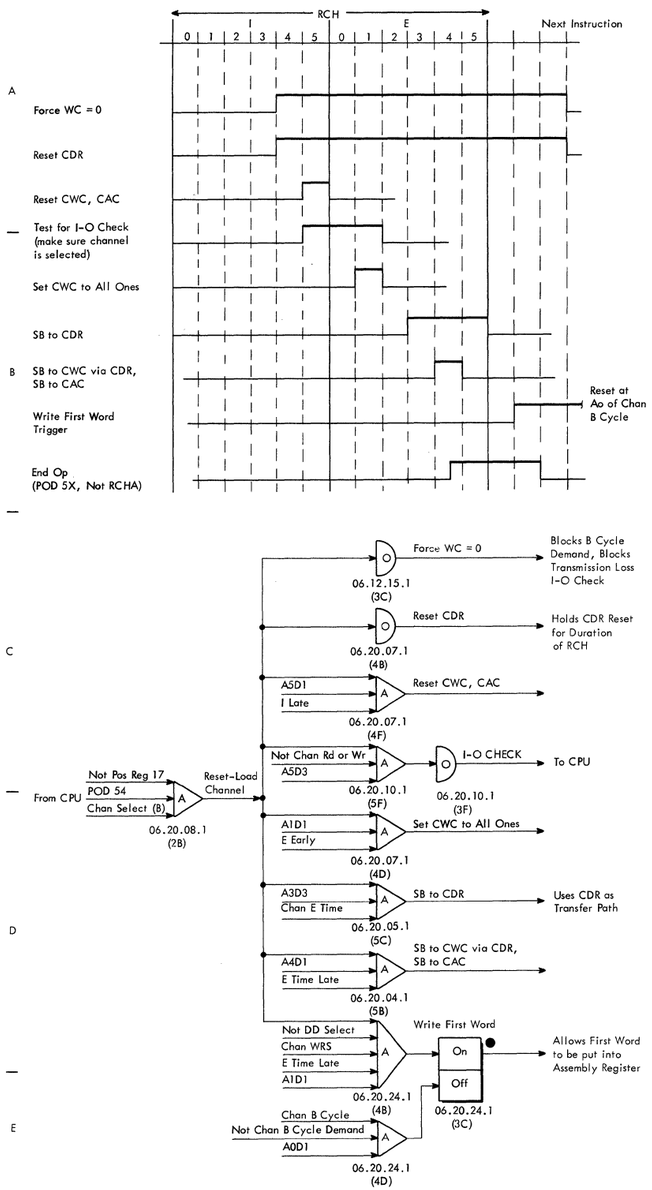


FIGURE 13. RCH, WRITE TAPE OPERATION

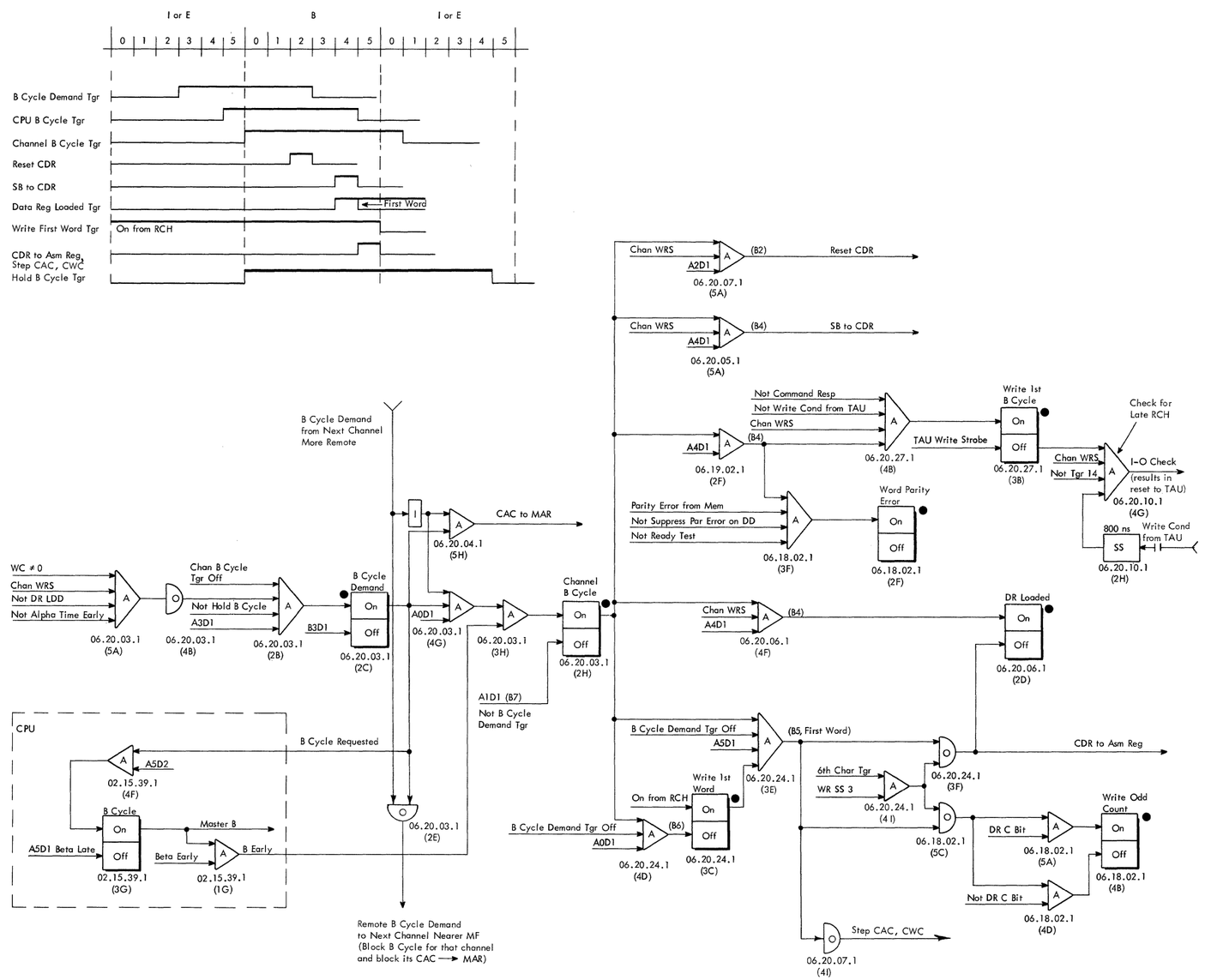


FIGURE 14. B CYCLE, WRITE TAPE OPERATION

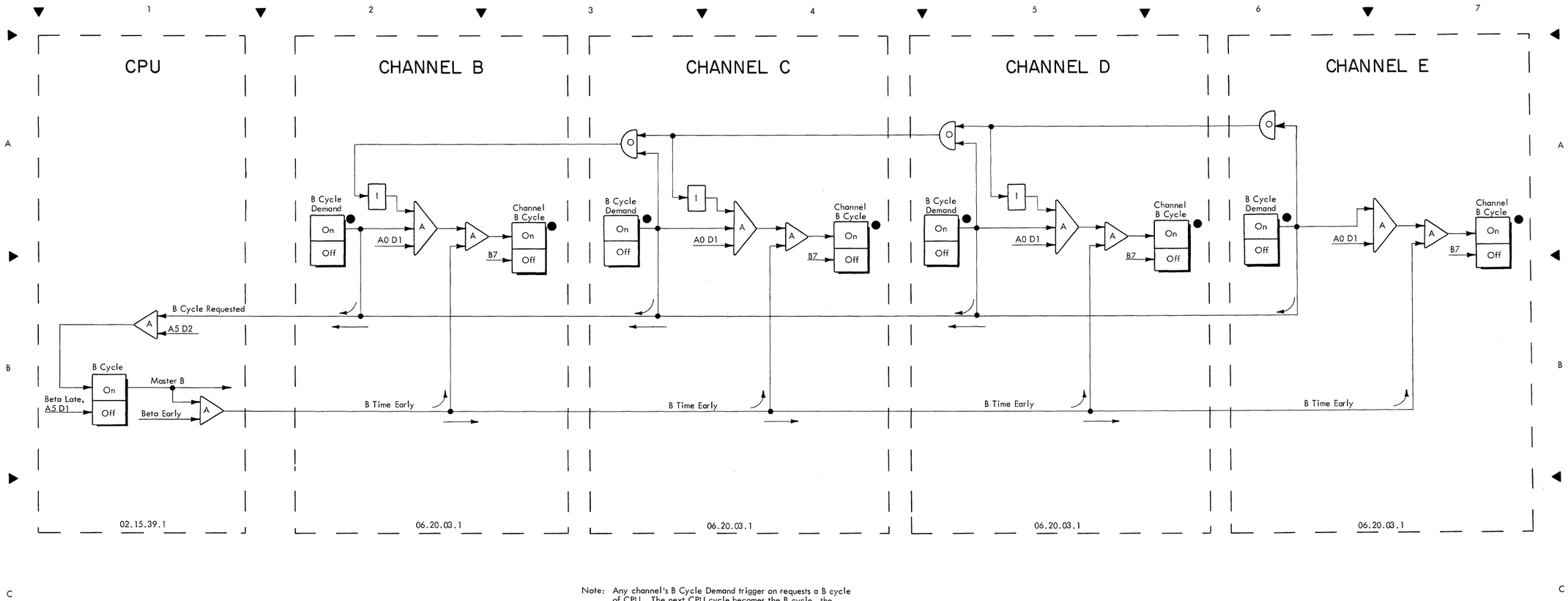


FIGURE 15. B CYCLE PRIORITY

Note: Any channel's B Cycle Demand trigger on requests a B cycle of CPU. The next CPU cycle becomes the B cycle, the B cycle being granted to the requesting channel.

If more than one channel requests a B cycle at the same time, the B cycle is granted to the most remote requesting channel.

Character counter set to 1 on WRS

1st B Cycle — Load CDR with first word, turn on DR LDD tgr, CDR to Asm reg, turn off DR LDD tgr

2nd B Cycle — Load CDR with second word, turn on DR LDD tgr

First Word

CC 1
- Tape unit writes first char from asm reg, TAU Write Strobe
- SS 1: Reset 6th Char tgr, Complement odd count tgr if odd char
- SS 2: Step CC
- SS 3:

CC 2
- Tape unit writes second char from asm reg, TAU write strobe
- SS 1: Complement odd count tgr if odd char
- SS 2: Step CC
- SS 3:

CC 3
- Tape unit writes third char from asm reg, TAU write strobe
- SS 1: Complement odd count tgr if odd char
- SS 2: Step CC
- SS 3:

CC 4
- Tape unit writes fourth char from asm reg, TAU write strobe
- SS 1: Complement odd count tgr if odd char
- SS 2: Step CC
- SS 3:

CC 5
- Tape unit writes fifth char from asm reg, TAU write stobe
- SS 1: Complement odd count tgr if odd char
- SS 2: Step CC
- SS 3:

CC 6
- Tape unit writes sixth char from asm reg, TAU write strobe
- SS 1: Complement odd count tgr if odd char; Test for xmission loss; Turn on 6th char tgr
- SS 2: Reset CC to 1; Reset asm reg; Step CAC,CWC; Sample odd count tgr for word parity error
- SS 3: CDR to asm reg (2nd word); Turn off DR LDD tgr; Turn on odd count tgr if data reg has C bit

3rd B Cycle — Load CDR with third word, turn on DR LDD tgr

Second Word

CC 1
- Tape unit writes first char from asm reg, TAU write strobe
- SS 1: Reset 6th char tgr; Complement odd count tgr if odd char
- SS 2: Step CC
- SS 3:

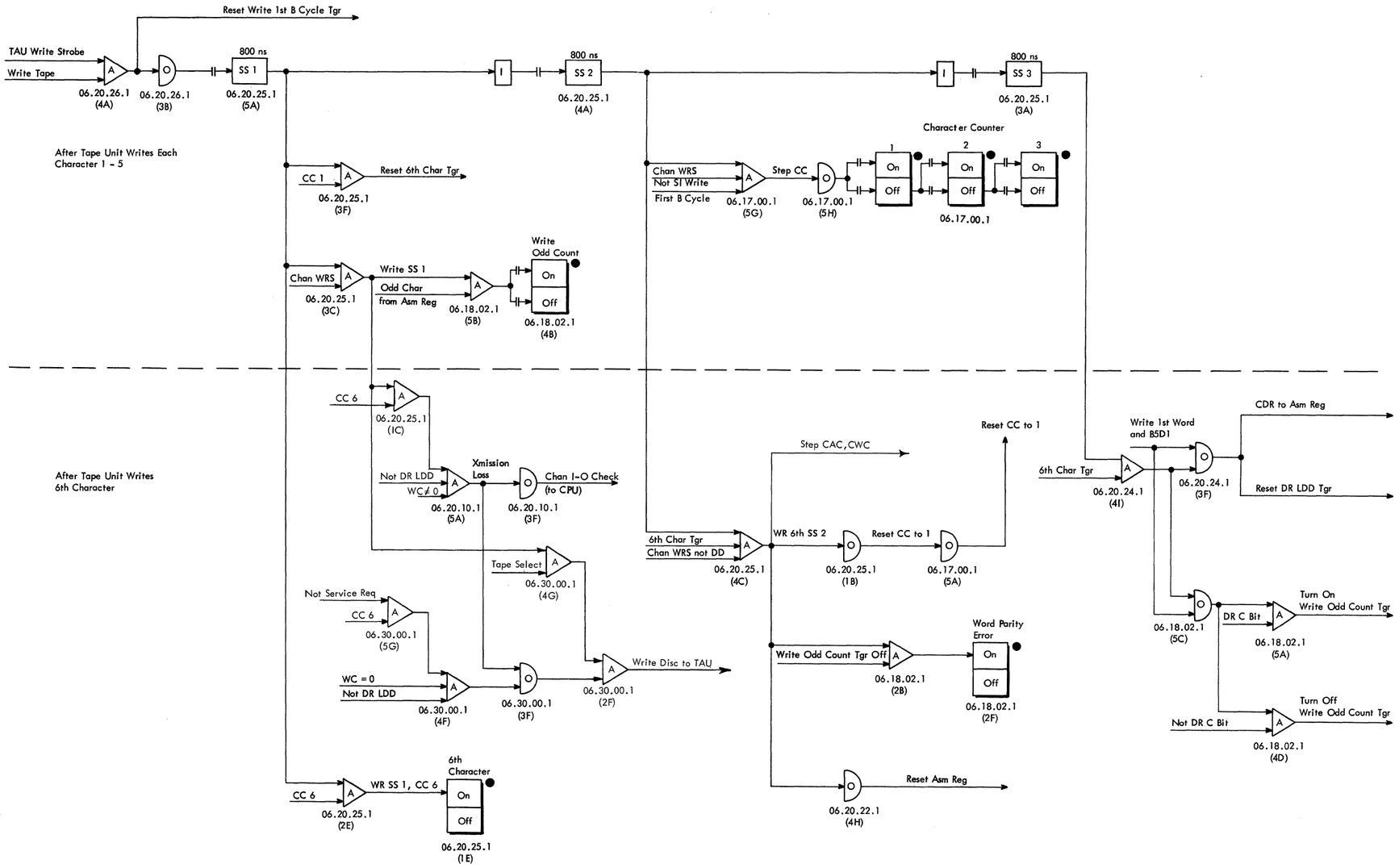


FIGURE 16. CHARACTER WRITING, WRITE TAPE OPERATION

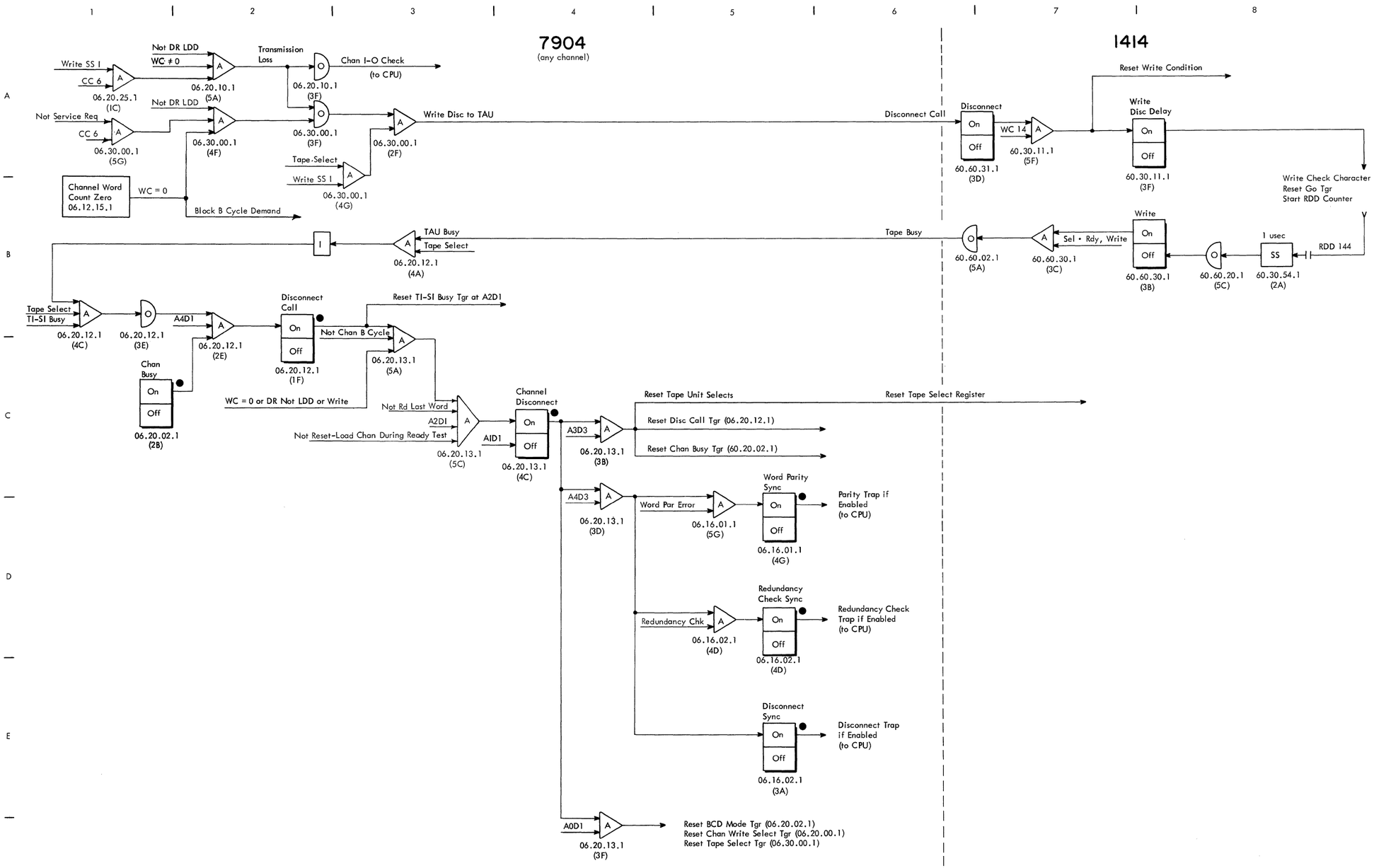


FIGURE 17. END OPERATION AND DISCONNECT, WRITE TAPE OPERATION

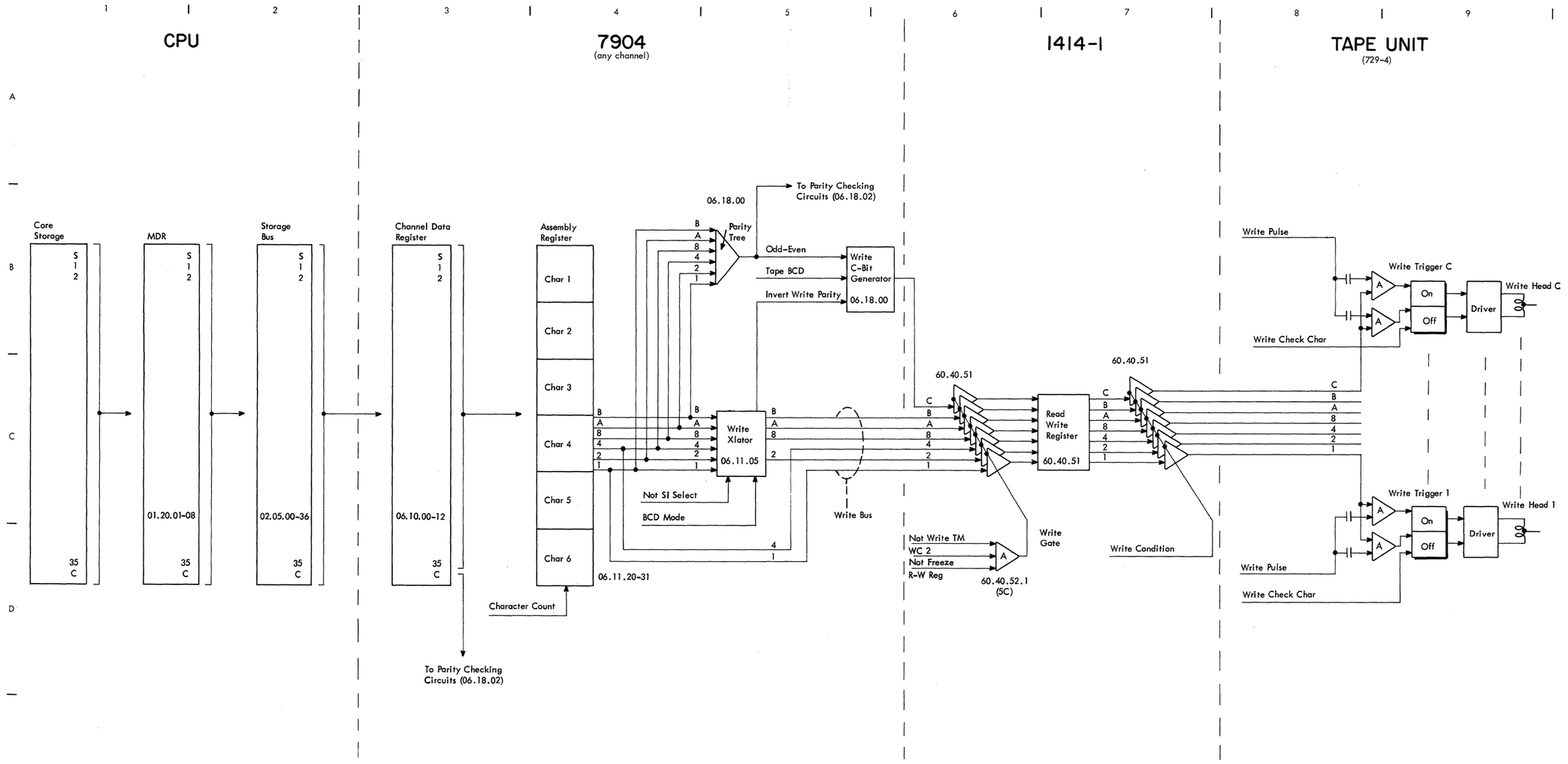


FIGURE 18. DATA FLOW, WRITE TAPE OPERATION

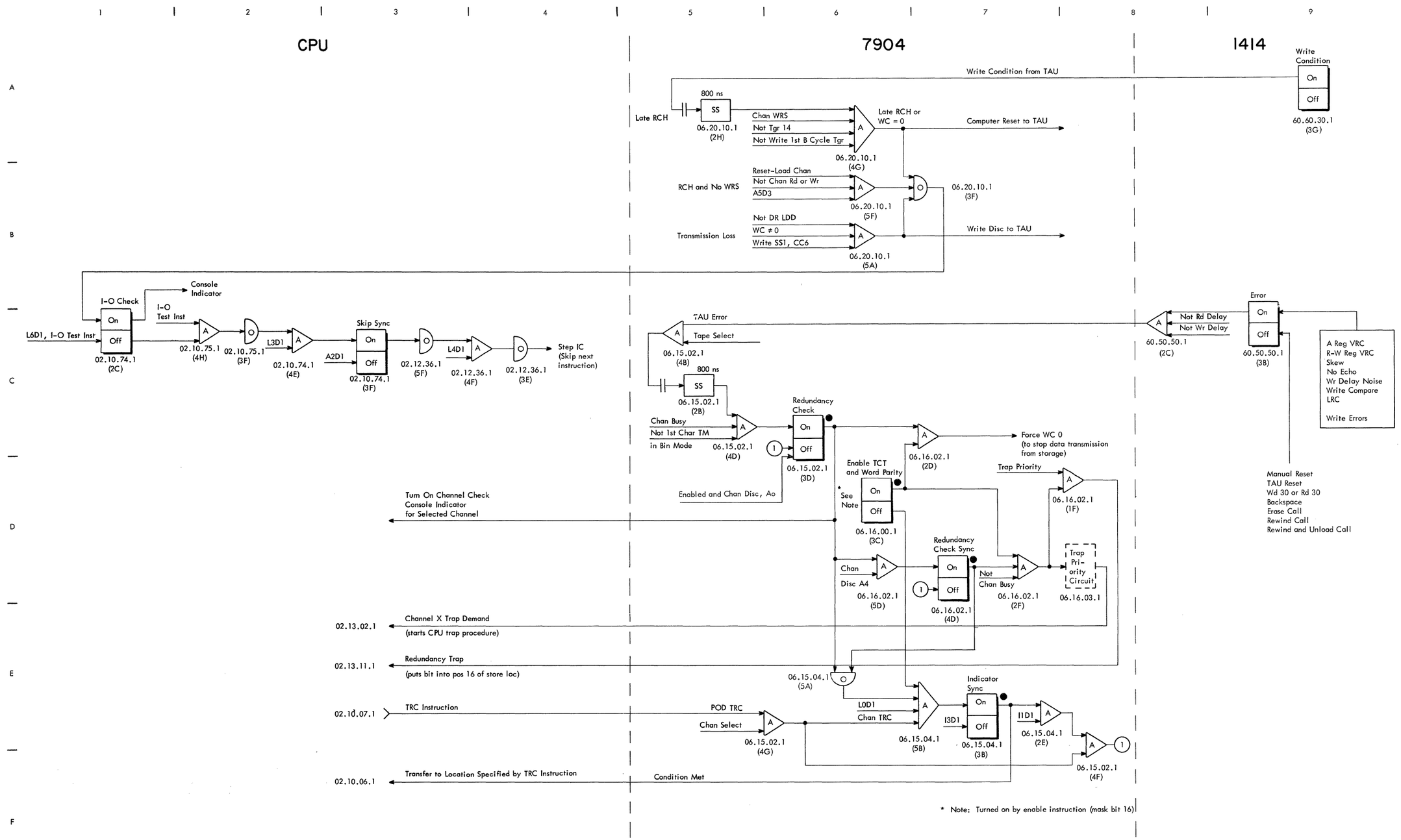


FIGURE 19. I-O CHECK AND REDUNDANCY CHECK, WRITE TAPE OPERATION

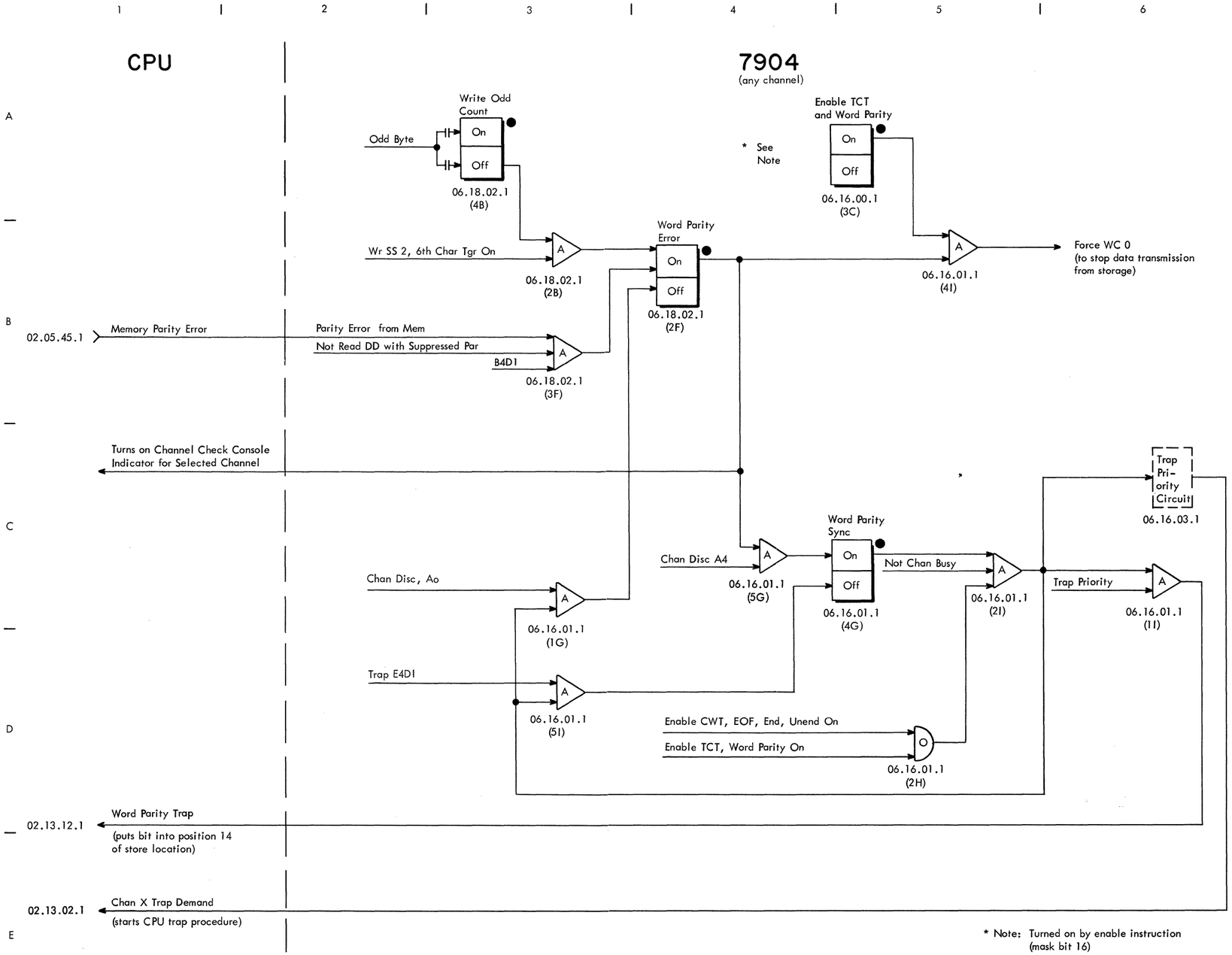


FIGURE 20. WORD PARITY ERROR, WRITE TAPE OPERATION

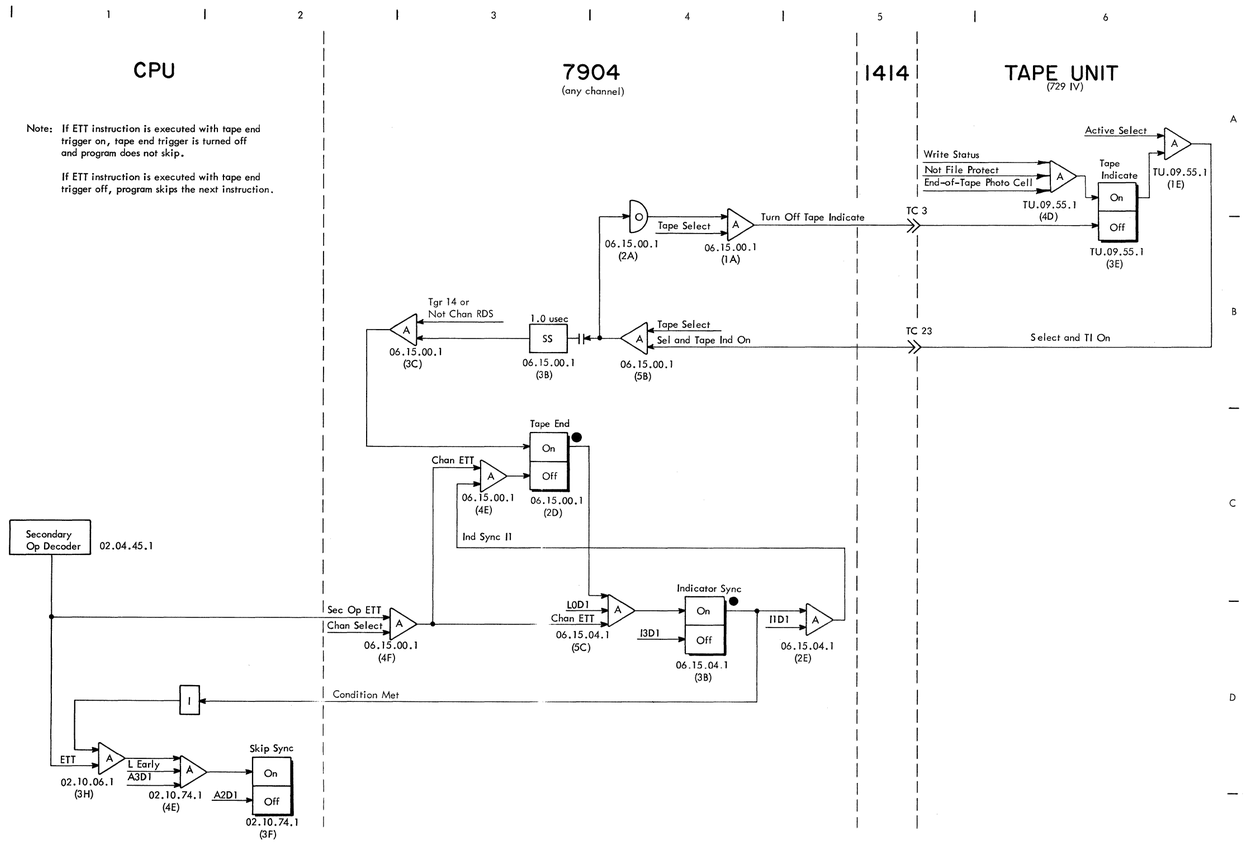


FIGURE 21. ETT, END-OF-TAPE OPERATION

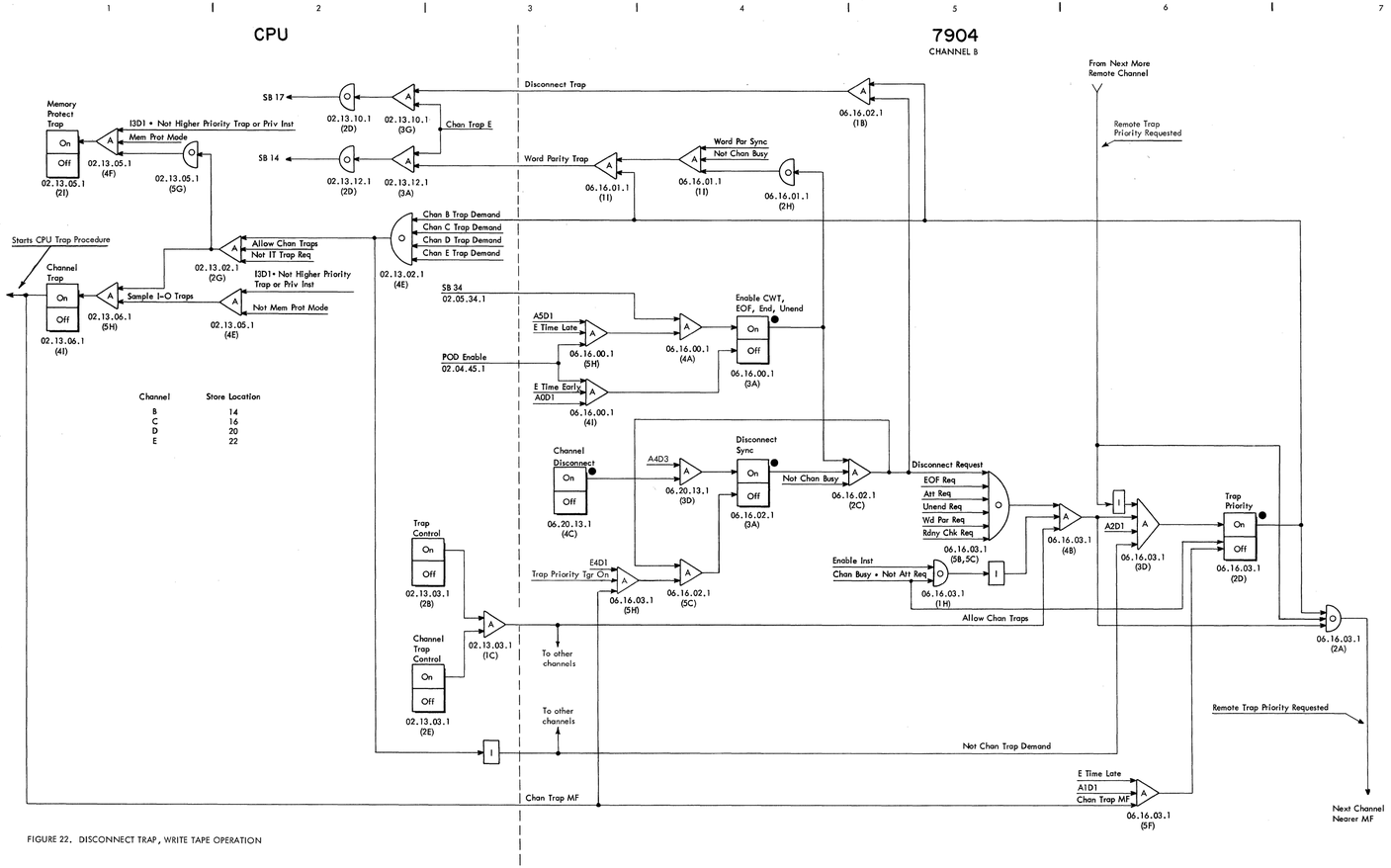


FIGURE 22. DISCONNECT TRAP, WRITE TAPE OPERATION

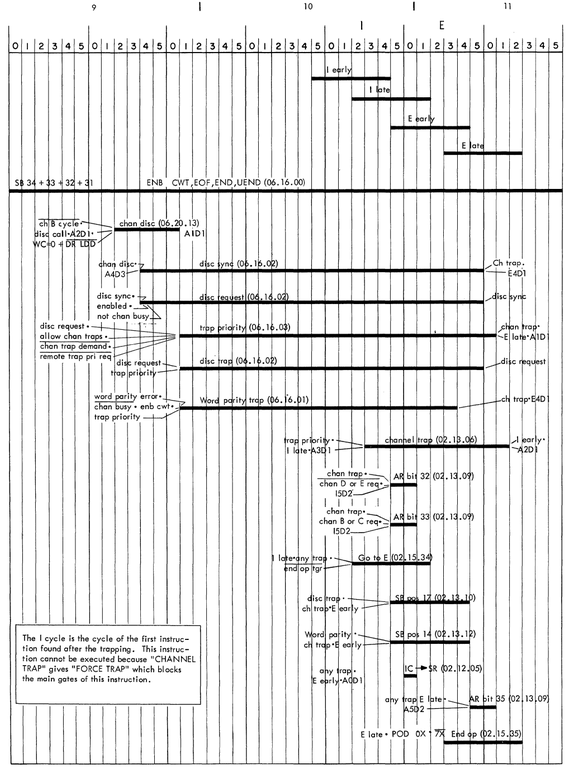


FIGURE 23. DISCONNECT TRAP TIMING

WRITE TAPE

I-O CHECK
(Turns on console I-O check light)

Caused by:

1. Late RCH or initial WC zero.
   (a) Causes computer reset to TAU at write condition time.
2. RCH and no WRS.
3. Transmission loss.
   (a) Causes write disconnect to TAU.

Error detection:

1. IOT instruction.
   (a) If I-O check, execute next instruction.
   (b) If not I-O check, skip next instruction.

REDUNDANCY CHECK
(Turns on console channel check light)

Caused by:

1. Tape write error.
   (a) A reg VRC
   (b) R-W reg VRC
   (c) Skew
   (d) No echo
   (e) Write delay noise
   (f) Write compare
   (g) LRC

Error detection:

1. If not enabled for trap, redundancy check is tested by TRC instruction.
   (a) If redundancy check, turn off redundancy check tgr and transfer.
   (b) If not redundancy check, proceed with program.
2. If enabled for trap, force WC zero on error and trap after disconnect.

WORD PARITY ERROR
(Turns on console channel check light)

Caused by:

1. B cycle storage bus parity.
2. Odd-even count of six characters does not agree with word C bit from CDR.

Error detection:

1. If enabled for word parity trap, force WC zero on error and trap after disconnect.
2. If not enabled for word parity trap, but disconnect trap is enabled, store parity flag bit along with disconnect flag bit when disconnect trap is taken.

TRAPS (Taken after channel disconnects)

1. Disconnect: enabled by "Enb CWT, EOF, End, Unend" trigger.
2. Redundancy check: enabled by "Enb TCT and Word Parity" trigger.
3. Word parity: enabled by "Enb TCT and Word Parity" trigger.

READ TAPE

I-O CHECK
(Turns on console I-O check light)

Caused by:

1. RCH and no RDS.
2. Transmission loss.

Error detection:

1. IOT instruction.
   (a) If I-O check, execute next instruction.
   (b) If not I-O check, skip next instruction.

REDUNDANCY CHECK
(Turns on console channel check light)

Caused by:

1. Tape read error.
   (a) R-W reg VRC
   (b) LRC
2. Bit count of character does not agree with C bit received with character.

Error detection:

1. If not enabled for trap, redundancy check is tested by TRC instruction.
   (a) If redundancy check, turn off redundancy check tgr and transfer.
   (b) If not redundancy check, proceed with program.
2. If enabled for trap, force WC zero on error and trap after disconnect.

WORD PARITY ERROR
(Turns on console channel check light)

Caused by:

1. B cycle storage bus parity.

Error detection:

1. If enabled for word parity trap, force WC zero on error and trap after disconnect.
2. If not enabled for word parity trap, but disconnect trap is enabled, store parity flag bit along with disconnect flag bit when disconnect trap is taken.

TRAPS (Taken after channel disconnects)

1. Disconnect: enabled by "Enb CWT, EOF, End, Unend" trigger.
2. Redundancy check: enabled by "Enb TCT and Word Parity" trigger.
3. Word parity: enabled by "Enb TCT and Word Parity" trigger.
4. Unusual end (last tape word incomplete): enabled by "Enb CWT, EOF, End, Unend" trigger.
5. End of file (tape mark read from tape): enabled by "Enb CWT, EOF, End, Unend" trigger.

FIGURE 24. ERROR AND TRAP CONDITIONS, TAPE OPERATION

READ TAPE OPERATION (Figures 25-41)

Characters are read from the tape unit through the 1414 into the assembly register of the channel. When each group of six characters is assembled, the 6-character word is transferred to the data register and then to storage.

The word counter in the channel is normally set higher than the number of words in the record; transmission stops when the tape reaches the inter-record gap. Figure 25 shows the sequence of the read tape operation.

Read Selecting the Channel (RDS)

The RDS instruction initiates the read operation (Figure 26). The address portion of the RDS instruction selects channel B, C, D, or E, selects the tape interface of that channel, and selects a particular tape unit on that interface. The operation portion of the RDS instruction sets up the channel for reading; that is, it conditions certain circuits that will allow data read from the tape unit (through the 1414) to enter the channel through the tape interface. The RDS operation ends, and the program goes on with the next instruction while the tape unit is getting up to speed.

Command Word Loading (RCH)

An RCH instruction for the channel just selected is executed, causing a command word to be sent from storage to the channel. The command word, when entered into the channel, sets the word counter and address counter. The word count in a tape read operation is usually insignificant, because if the tape inter-record gap is to stop the data transmission, the tape will reach the gap before the word counter reaches zero. The RCH instruction requires an I cycle and an E cycle, after which the program proceeds with the next instruction. See Figure 27 for actions in the channel caused by the RCH.

Character Transmission

The tape unit reads the first character, puts it on the read bus, and sends a read strobe signal to the channel (Figure 28). The read strobe signal trips off a series of three single-shots in the channel. The single-shots check each character received for proper parity, control the character counter (make sure each character goes into its proper place in the assembly register), and control a circuit that keeps track of the odd-even count of each group of six characters. This latter job is necessary because a parity bit must be assigned to the assembled word before the word is put into storage.

After each group of six characters is received, the 6-character word moves from the assembly register to the data register. The assembly register is now empty and ready to receive the next group of characters. Because the data register is loaded, a B cycle is requested to move the word from the data register to storage.

B Cycle

On a read operation, the word counter not zero and the data register loaded cause a B cycle demand to be sent to CPU (Figure 29). The next CPU cycle following the request becomes a B cycle, during which the word in the data register moves to storage. The data register is now empty and ready to receive the next word from the assembly register.

As words move from the data register to storage on B cycles, the word counter steps down. If the word counter was initially set lower than the number of words in the record, it will reach zero before the tape reaches the inter-record gap. No more B cycles are allowed, but the tape continues to the inter-record gap.

End Operation and Disconnect

The tape moves into the inter-record gap, causing the read only trigger in the 1414 to turn off (Figure 30). This action drops the TAU busy line to the channel. The fall of TAU busy at the channel turns on the disconnect call trigger. When the last word moves from the CDR to storage, the channel disconnect trigger turns on. This trigger resets all the triggers that were maintaining the channel in a read tape status, and sets up the trap sync triggers for any trap conditions that might have occurred on the read operation. The channel is now not busy and may be used by CPU for another read or write.

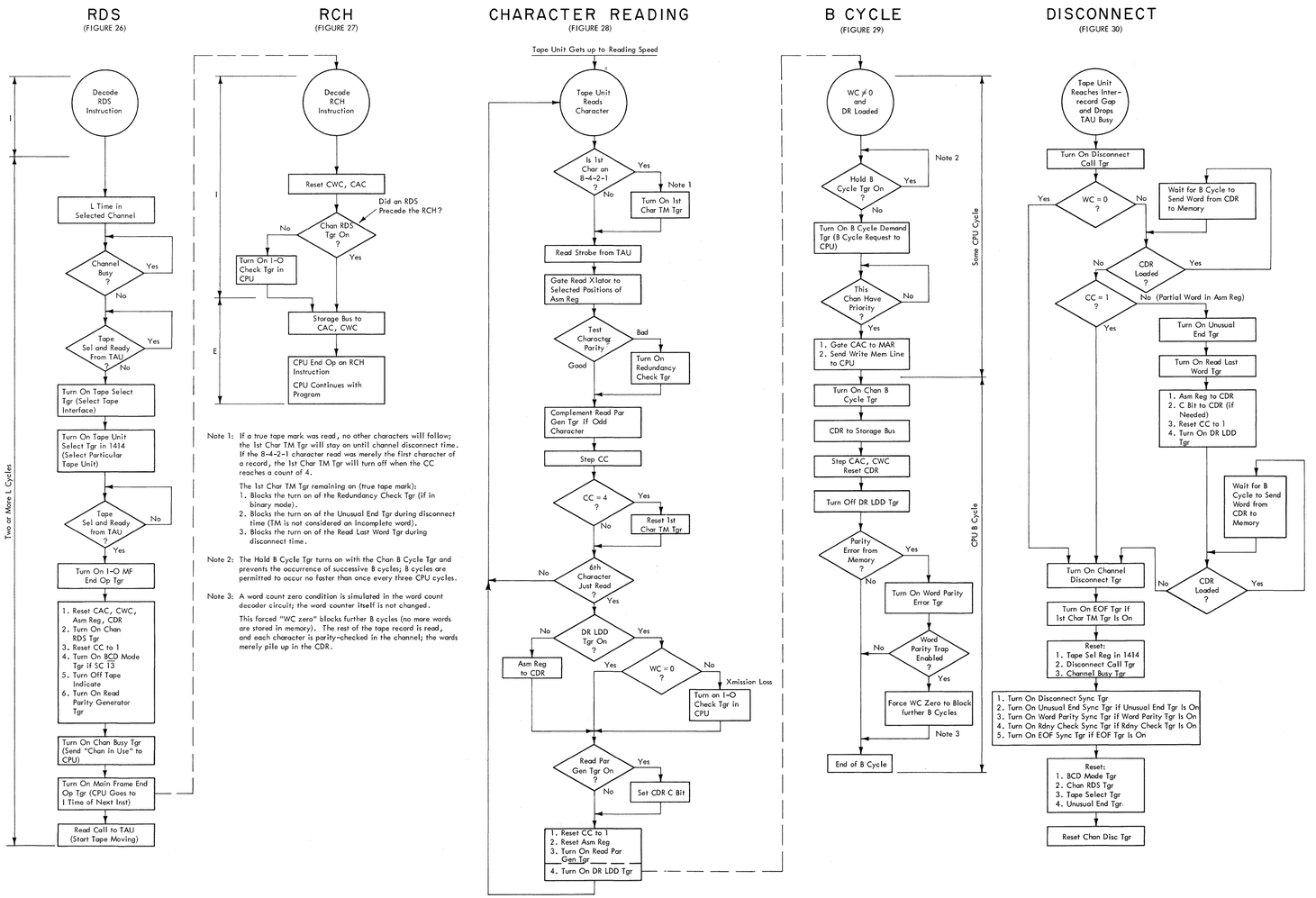


FIGURE 25. READ TAPE OPERATION SEQUENCE

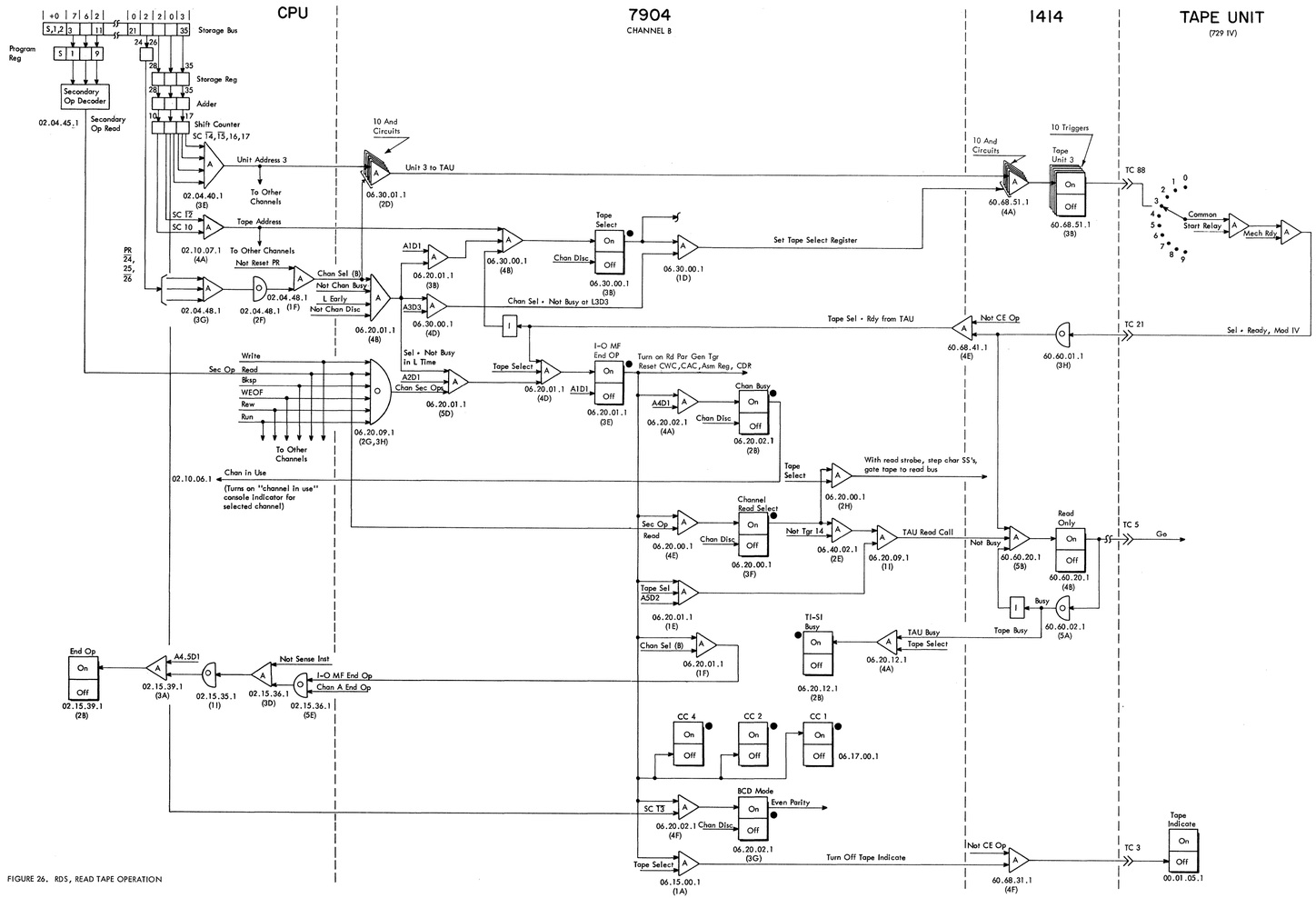
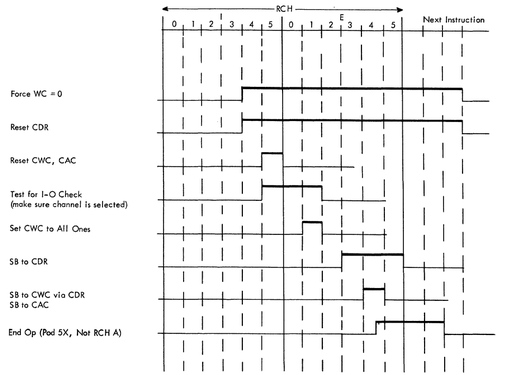


FIGURE 26. RDS, READ TAPE OPERATION



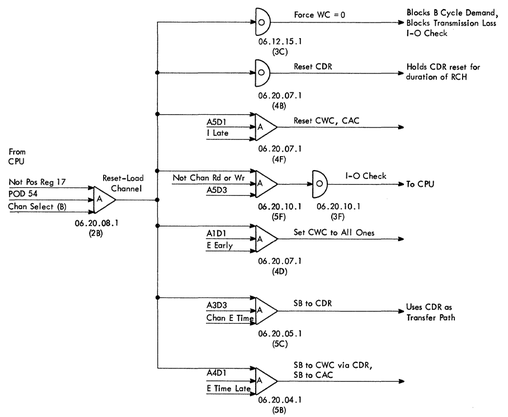


FIGURE 27. RCH, READ TAPE OPERATION

RDS sets CC to 1, turns on read parity generator tgr, and starts tape moving.
RCH clears channel registers, and sets address counter and word counter.

CC 1
Tape unit reads first character; puts it on read bus.
TAU read strobe.

SS 1	SS 2	SS 3
Reset 6th char tgr Gate 1st char to asm reg Test for byte parity Complement read parity gen tgr if odd char		Step CC

CC 2
Tape unit reads second character; puts it on read bus.
TAU read strobe.

SS 1	SS 2	SS 3
Gate 2nd char to asm reg Test for byte parity Complement read parity gen tgr if odd char		Step CC

CC 3
Tape unit reads third character; puts it on read bus.
TAU read strobe.

SS 1	SS 2	SS 3
Gate 3rd char to asm reg Test for byte parity Complement read parity gen tgr if odd char		Step CC

CC 4
Tape unit reads fourth character; puts it on read bus.
TAU read strobe.

SS 1	SS 2	SS 3
Gate 4th char to asm reg Test for byte parity Complement read parity gen tgr if odd char		Step CC

CC 5
Tape unit reads fifth character; puts it on read bus.
TAU read strobe.

SS 1	SS 2	SS 3
Gate 5th char to asm reg Test for byte parity Complement read parity gen tgr if odd char,		Step CC

CC 6
Tape unit reads sixth character; puts it on read bus.
TAU read strobe.

SS 1	SS 2	SS 3
Gate 6th char to asm reg Test for byte parity Complement read parity gen tgr if odd char Test for transmission loss Asm reg to CDR Turn on 6th char tgr	Sample read parity gen tgr to assign C bit to CDR	Reset CC to 1 Reset asm reg Turn on read parity gen tgr Turn on DR LDD Tgr

First Word

1st B Cycle
Send first word from CDR to storage. Turn off DR LDD tgr.

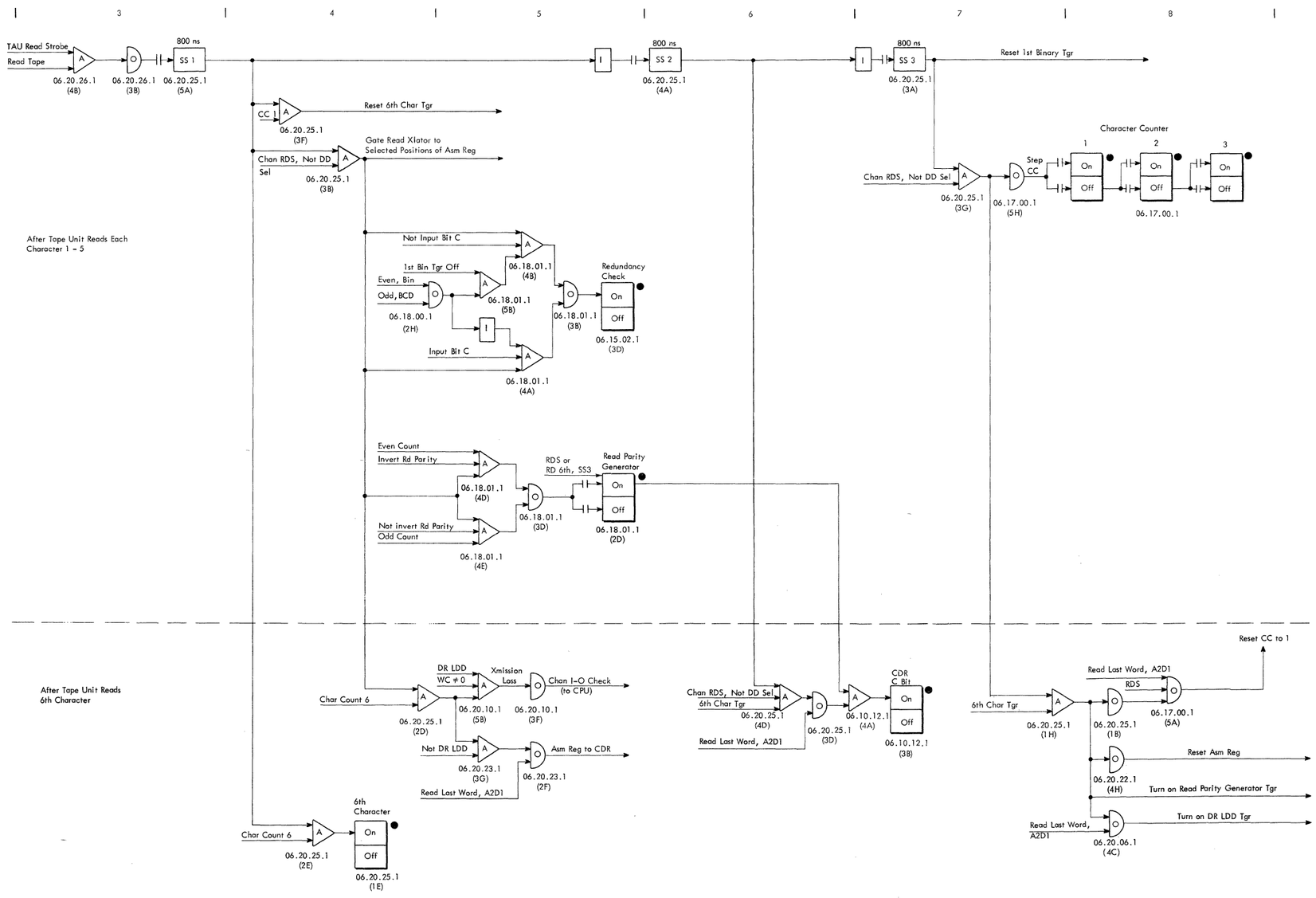


FIGURE 28. CHARACTER READING, READ TAPE OPERATION

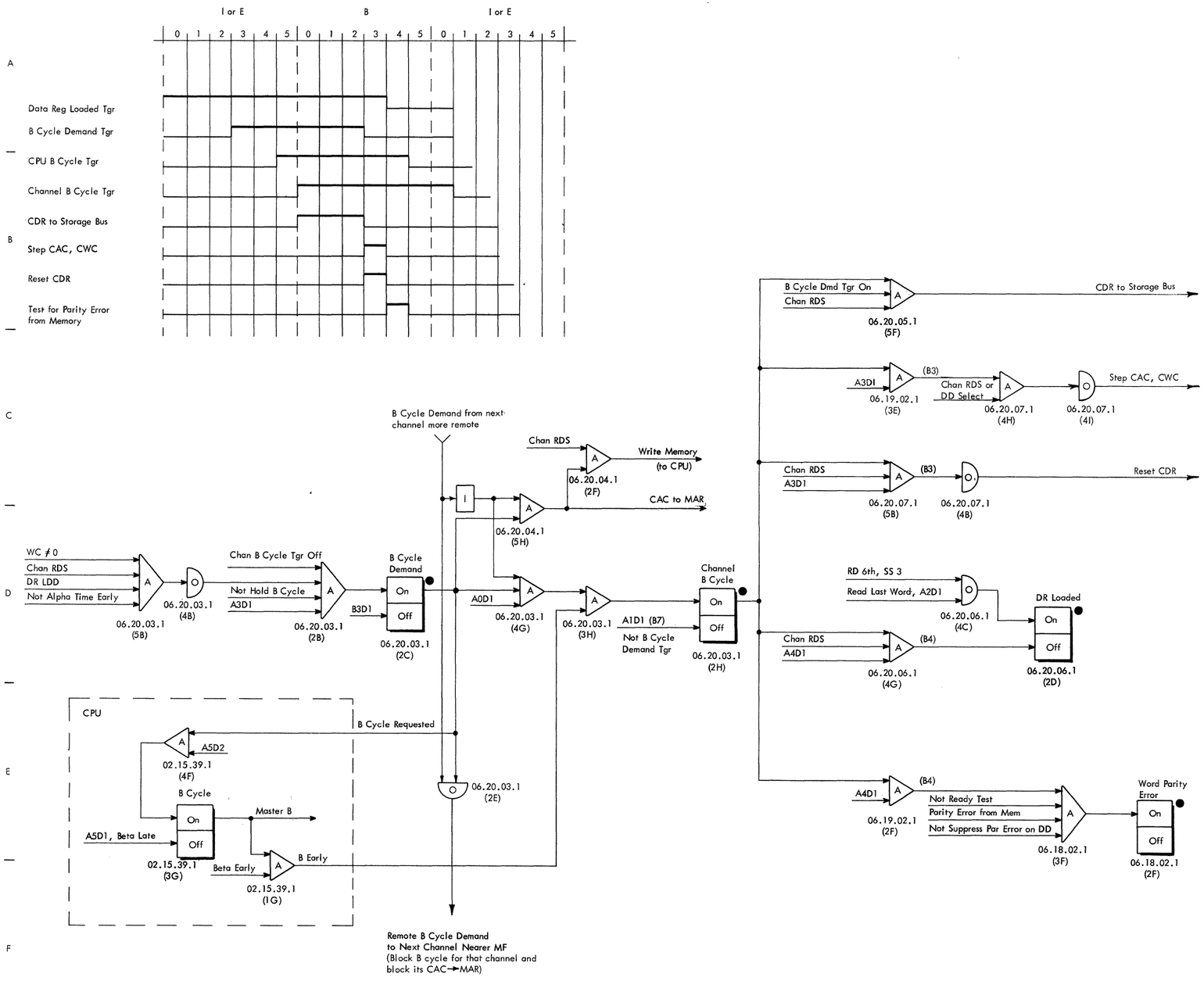


FIGURE 29. B CYCLE, READ TAPE OPERATION

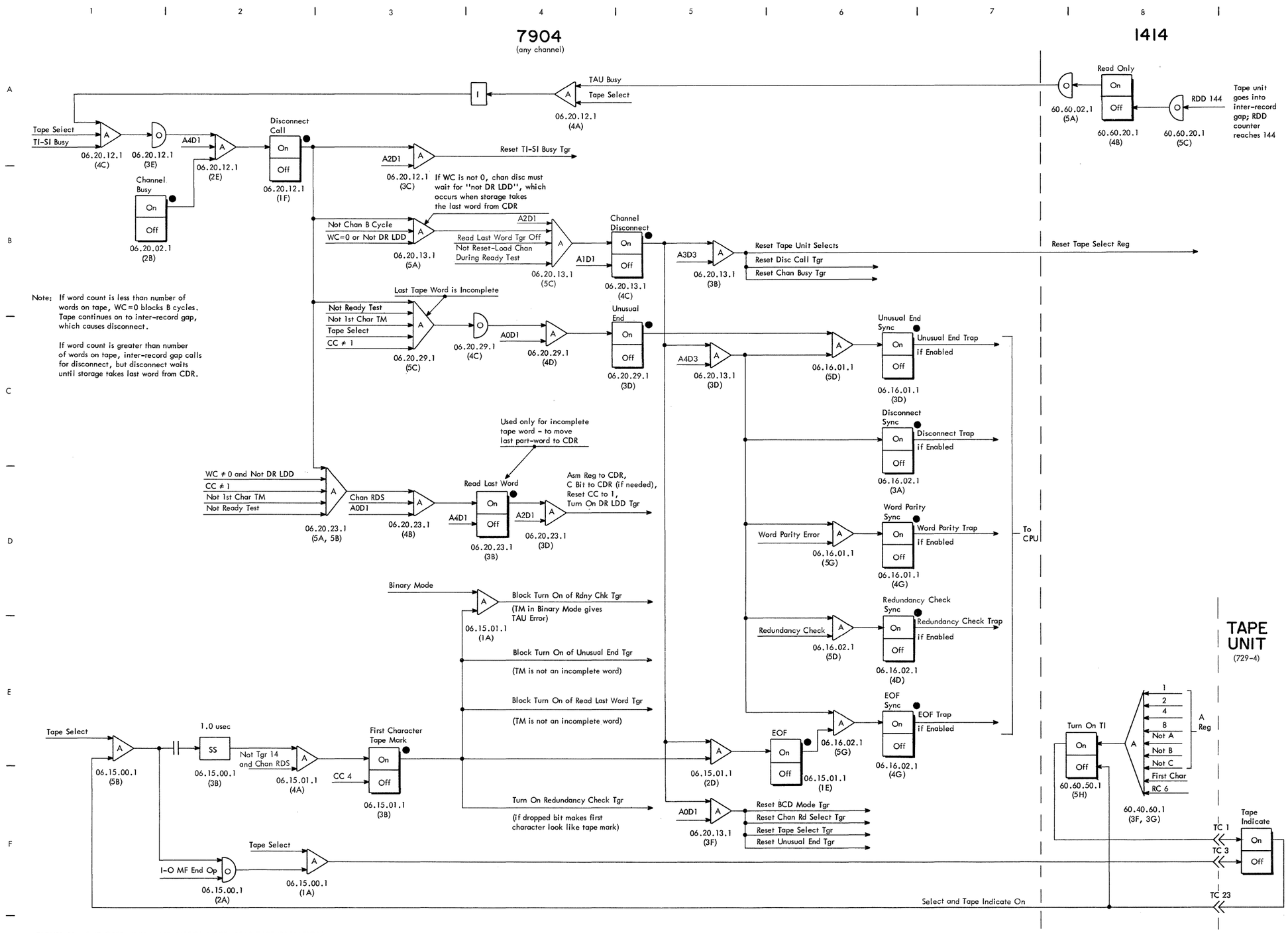


FIGURE 30. END OPERATION AND DISCONNECT, READ TAPE OPERATION

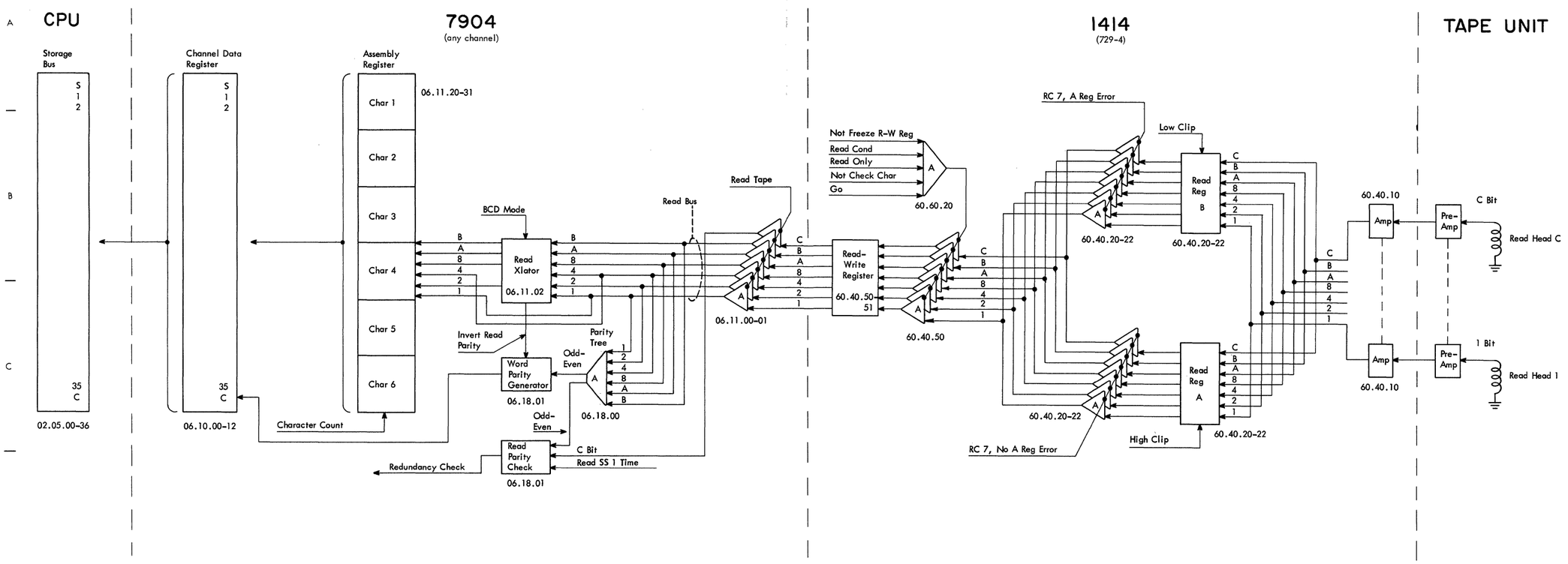


FIGURE 31. DATA FLOW, READ TAPE OPERATION

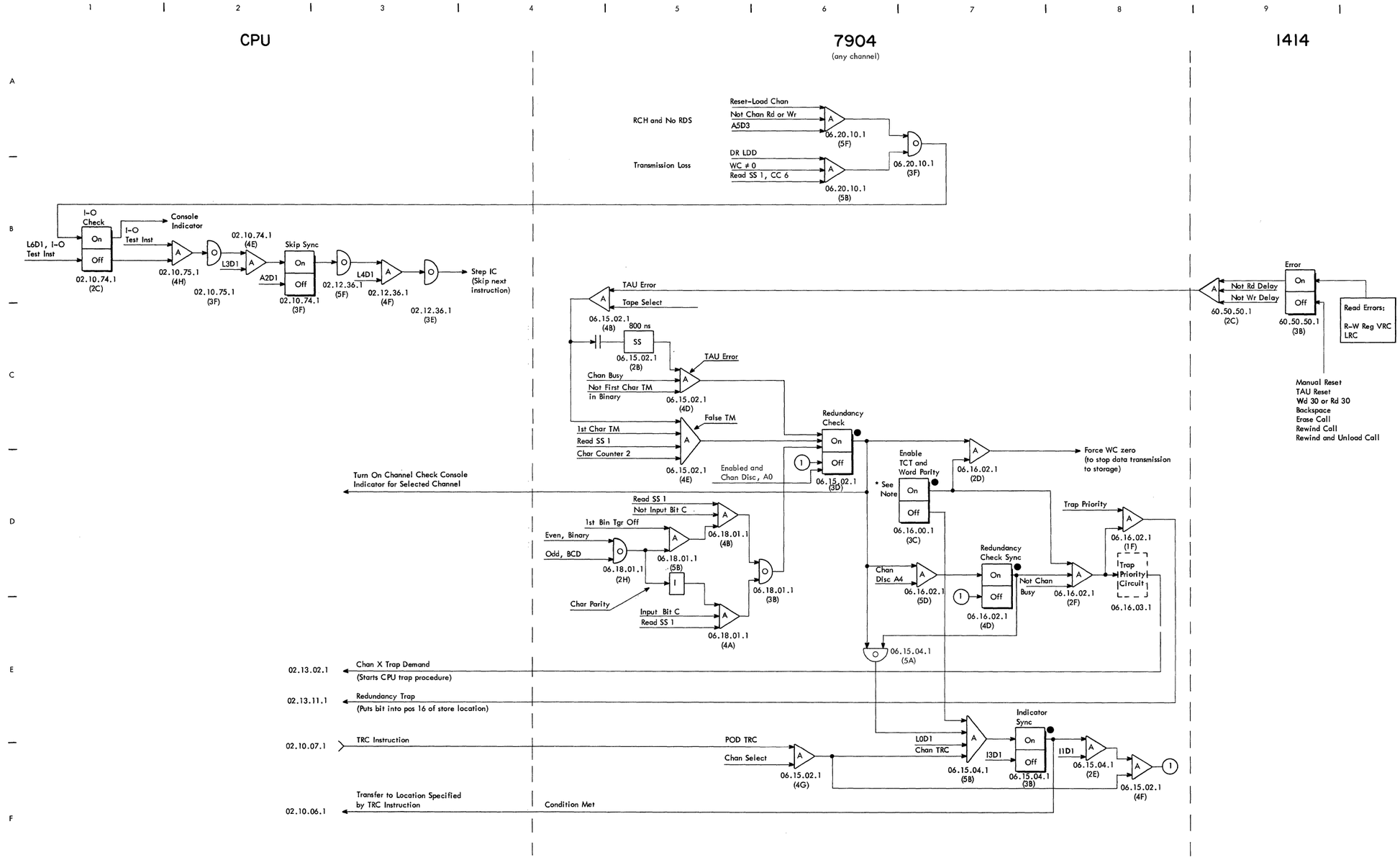


FIGURE 32. I-O CHECK AND REDUNDANCY CHECK, READ TAPE OPERATION

* Note: Turned on by unable instruction (mask bit 16)

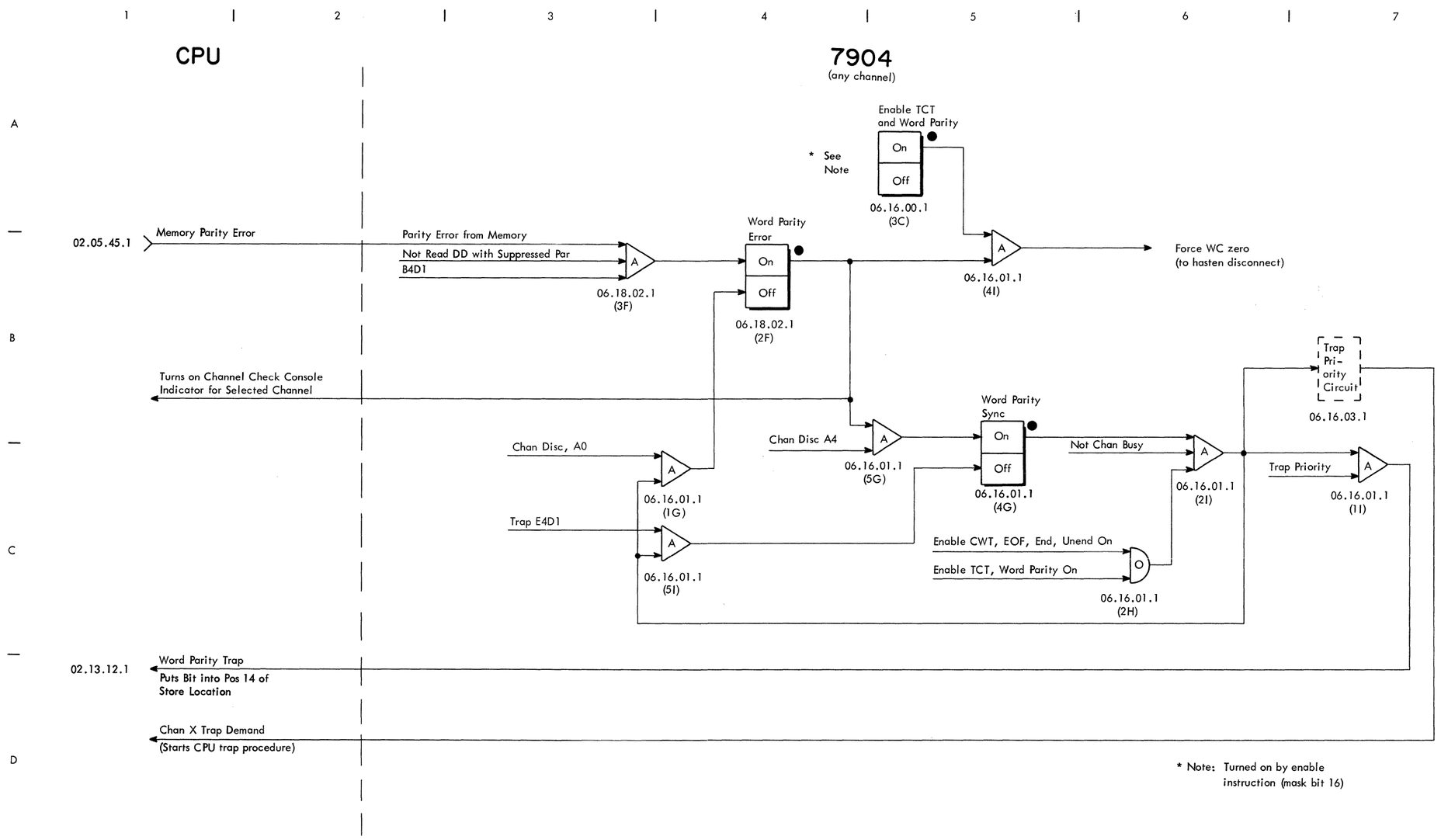


FIGURE 33. WORD PARITY ERROR, READ TAPE OPERATION

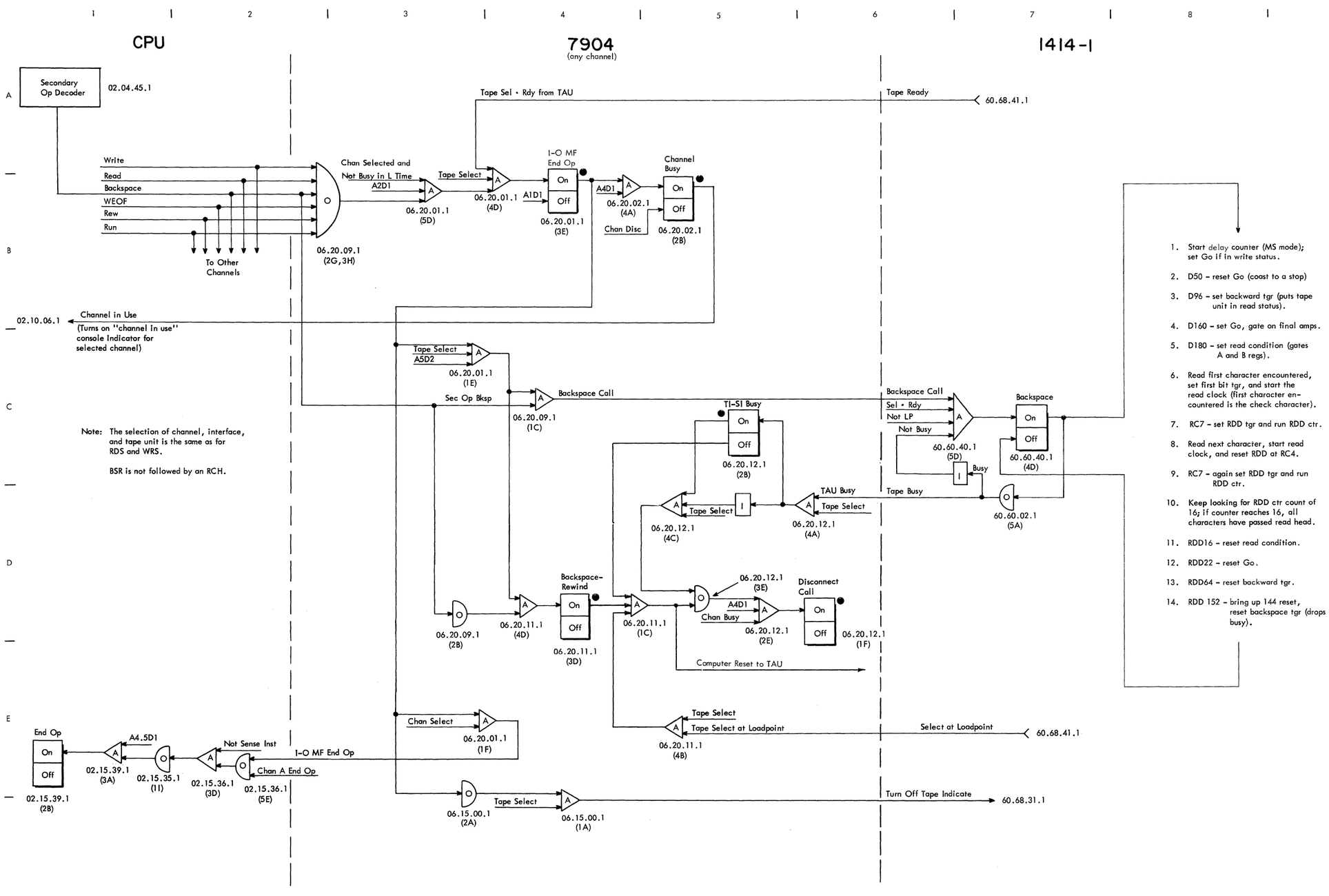


FIGURE 34. BSR, BACKSPACE OPERATION

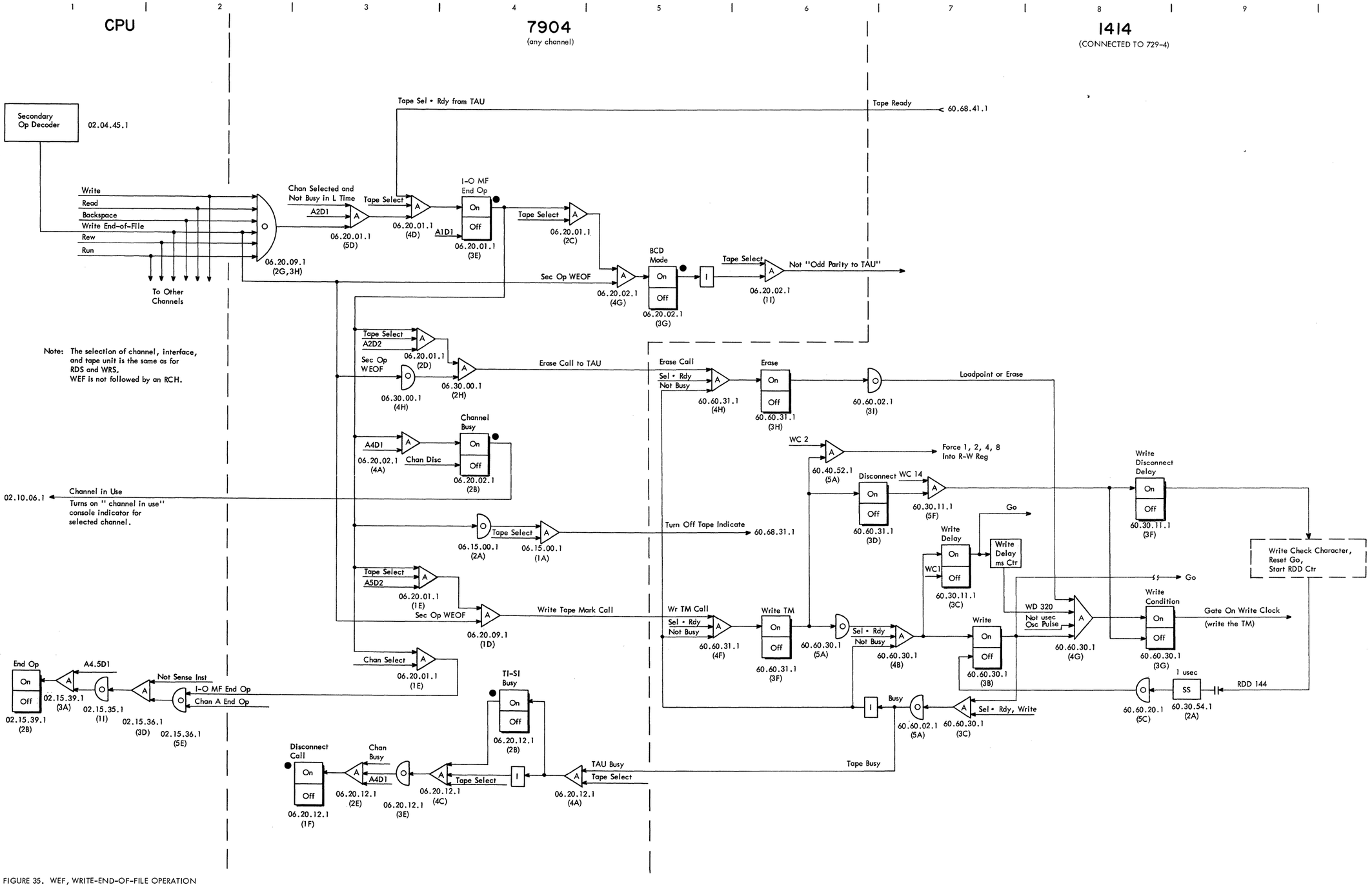
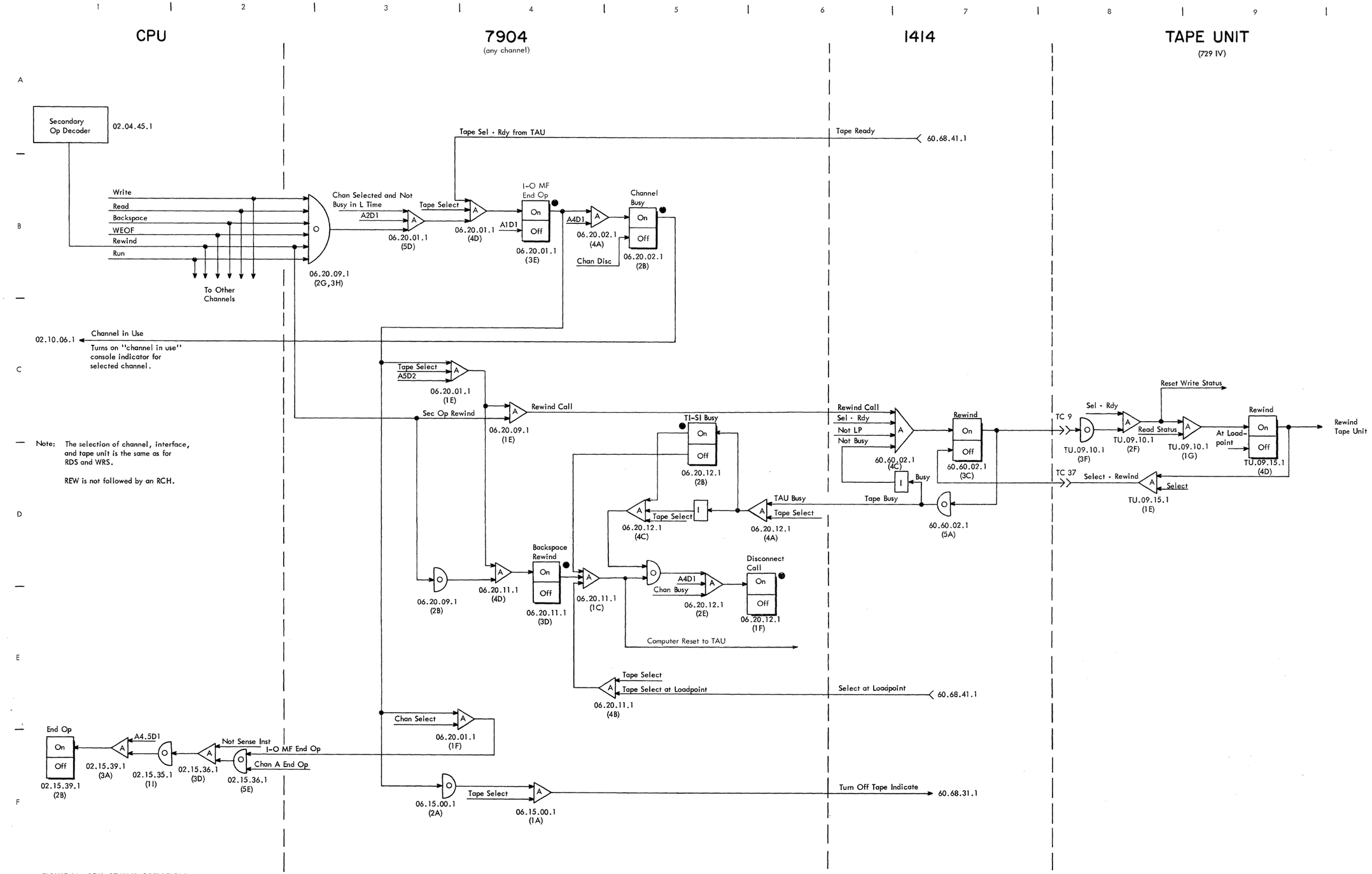


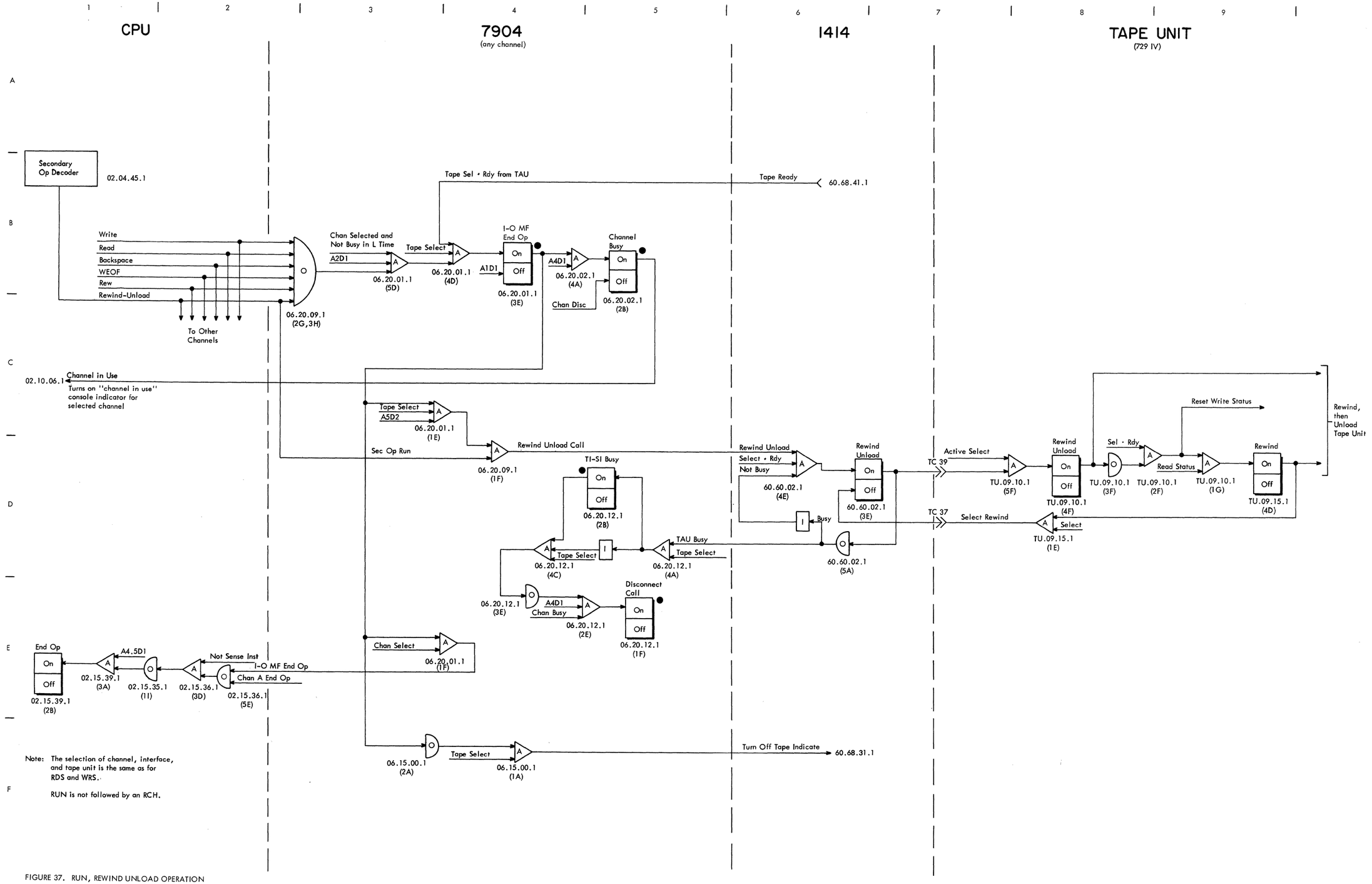
FIGURE 35. WEF, WRITE-END-OF-FILE OPERATION



Note: The selection of channel, interface, and tape unit is the same as for RDS and WRS.

REW is not followed by an RCH.

FIGURE 36. REW, REWIND OPERATION



Note: The selection of channel, interface, and tape unit is the same as for RDS and WRS.

RUN is not followed by an RCH.

FIGURE 37. RUN, REWIND UNLOAD OPERATION

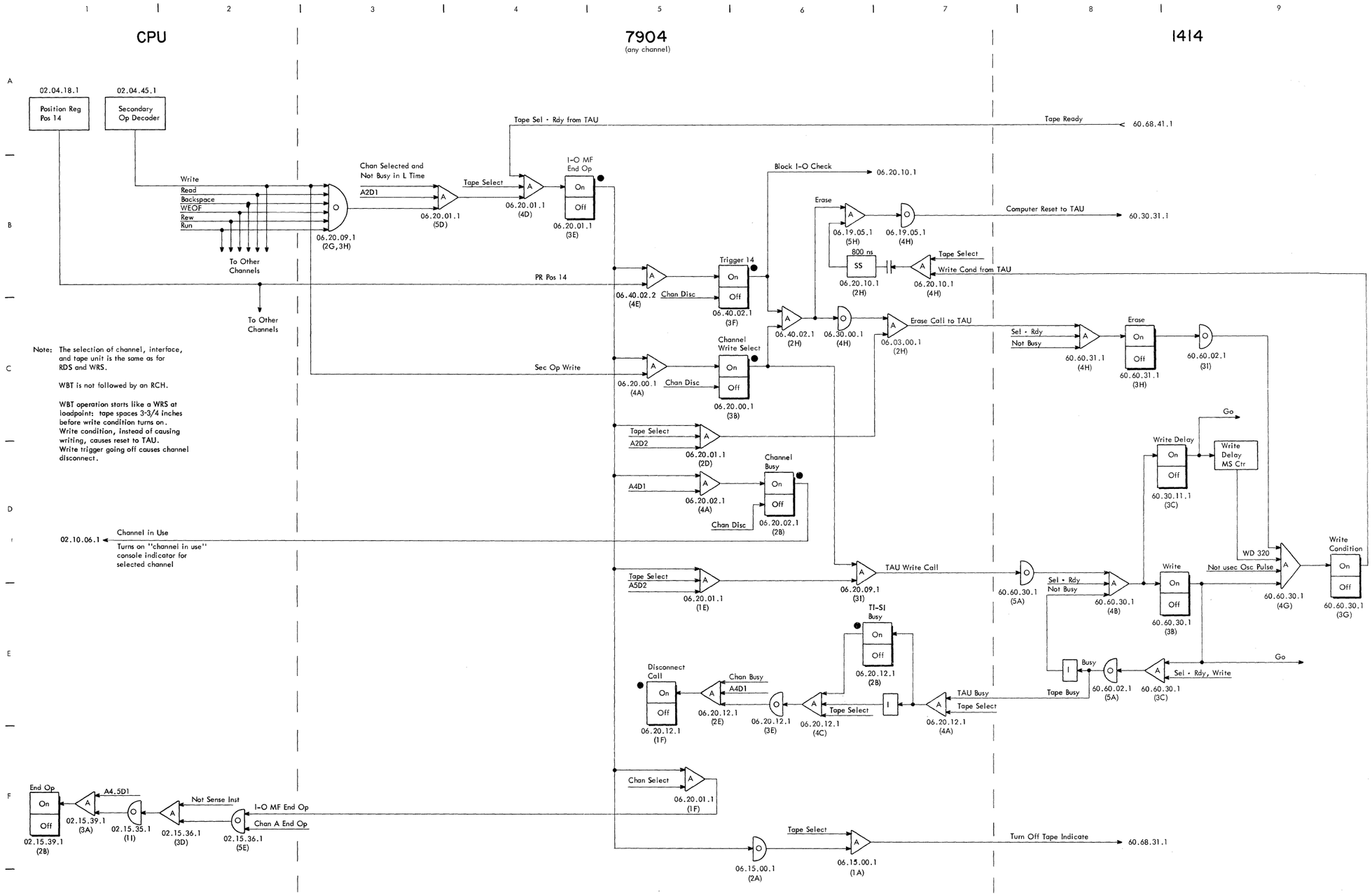


FIGURE 38. WBT, WRITE BLANK TAPE OPERATION

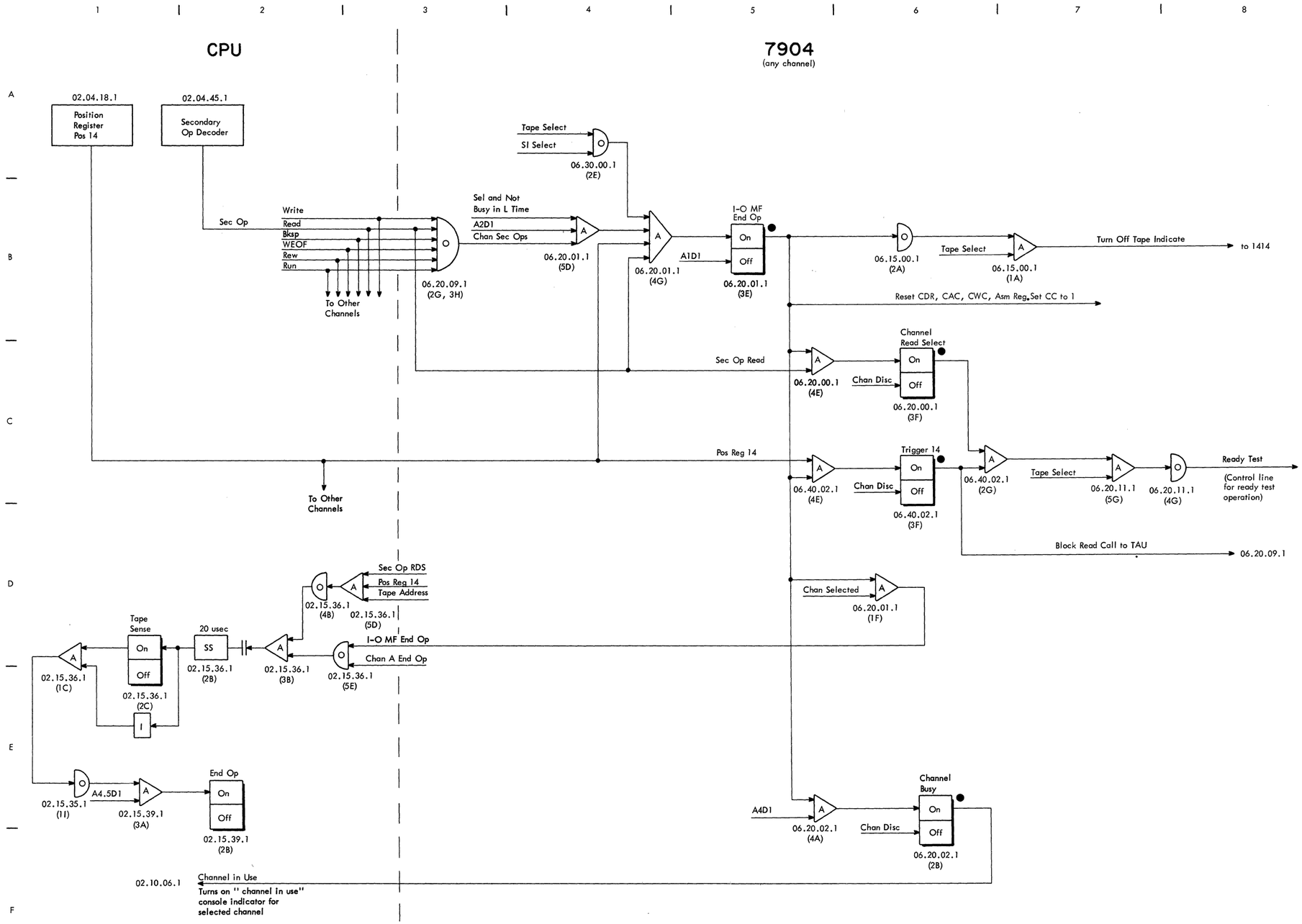


FIGURE 39. SEN, TAPE READY TEST OPERATION

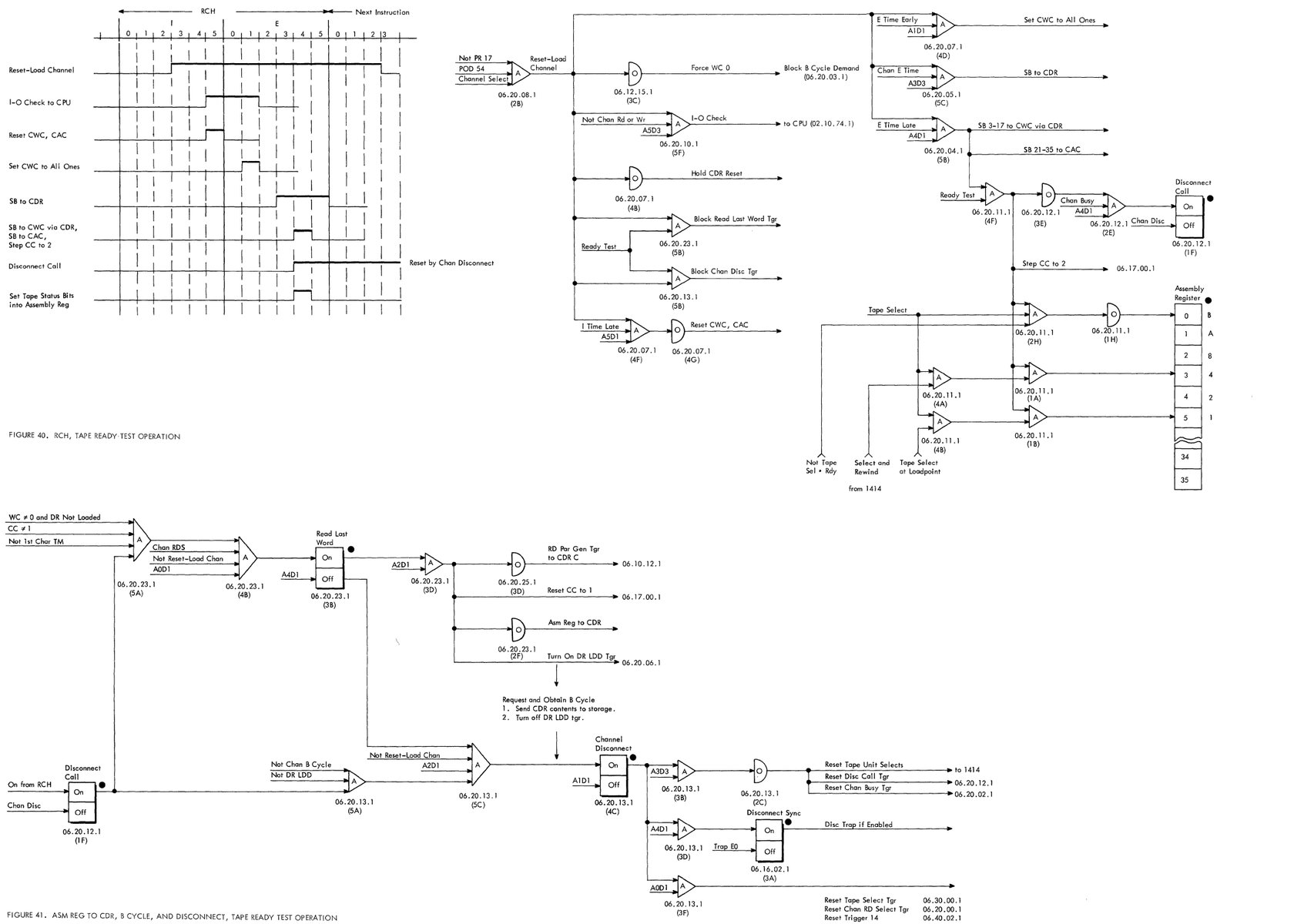


FIGURE 40. RCH, TAPE READY TEST OPERATION

FIGURE 41. ASM REG TO CDR, B CYCLE, AND DISCONNECT, TAPE READY TEST OPERATION

SIMPLEX INTERFACE WRITE OPERATION (Figures 42-47)

Words are transferred (in parallel) from storage to a 7904 channel, and then sent a character at a time to the I-O device attached to the Simplex interface of that channel.

The word counter in the 7904 channel determines the number of words transmitted. It is initially set for the desired number of words, and reduced by one as each word is transmitted. When the counter reaches zero, transmission stops.

Figure 43 shows the sequence of the write Simplex operation.

Write Selecting the Channel (WRS)

The WRS instruction initiates the write operation (Figure 44). The address portion of the instruction selects channels B, C, D, or E, and selects the Simplex interface of that channel. The operation portion of the instruction sets up the channel for writing; that is, it conditions certain circuits in the channel that will allow writing to the I-O device through the Simplex interface. If the device is ready to receive data, the WRS operation ends, and the program goes on with the next instruction.

Command Word Loading (RCH)

An RCH instruction for the channel just selected is executed, causing a command word to be sent from storage to the channel. The command word, when entered into the channel, sets the word counter and address counter. The RCH instruction requires an I cycle and an E cycle, after which the program proceeds with the next instruction.

The word counter not zero and the data register not loaded cause a B cycle demand. See Figure 13 for actions in the channel caused by the RCH. Although this figure is in the write tape section of the manual, it is valid for RCH, Simplex interface write.

B Cycle

The word counter not zero and the data register not loaded cause a B cycle demand to be sent to CPU (Figure 45). The next CPU cycle following the request becomes a B cycle, during which the first word to be transmitted is sent from storage to the channel's data register. During this first B cycle, the first word immediately moves on to the assembly register, and a write command is sent to the I-O device.

Because the data register is now empty, another B cycle is requested; during this B cycle, the data register is loaded with the second word. At this point, the I-O device has been told that the channel wants to write, the first word is waiting in the assembly regiser, and the second word is in the data register. The channel now waits for the first service request from the I-O device.

Character Transmission

Characters are transmitted on demand of the I-O device. The device asks for a character by sending a service request signal to the channel. The channel places the proper character on the write bus and tells the I-O device to take it by sending a service response signal to the device.

Each service request trips off a series of three single-shots in the channel (Figure 46). The single-shots check each character sent for the proper parity, control the character counter (make sure each of the six characters is gated out of the assembly register in the proper order), and generate the service response signal. After each group of six characters is transmitted, the next word (always waiting in the data register) moves to the assembly register. This action causes a B cycle, which again fills the data register.

As words move from storage to the data register on B cycles, the word counter is stepped down. When the word counter reaches zero, no more B cycles are allowed. The last six characters are sent to the I-O device. The I-O device does not know this is the last word and asks for another character (service request). Because the word counter is zero and the data register is not loaded, the channel sends a stop signal to the I-O device in place of a service response. The stop signal causes the I-O device to start the procedure that will end the write operation and disconnect the channel.

End Operation and Disconnect

The stop signal is received by the I-O device. The device checks to see that the transmission was correct, and if it was, sends the end signal to the channel (Figure 47). The end signal in the channel generates end response, which is sent to the I-O device. If the transmission had not been correct, the I-O device would have sent unusual end instead of end. Unusual end would have also generated end response, but, in addition, would have caused an unusual end trap.

End response at the I-O device makes the I-O device write circuits inactive. This action results in command response being dropped. The fall of command response at the channel turns on the disconnect call trigger, which subsequently turns on channel disconnect. The channel disconnect trigger resets the triggers that were maintaining the channel in a write Simplex status, and sets up trap sync triggers for any trap conditions that might have occurred during the write operation. The channel is now not busy and may be used by CPU for another read or write.

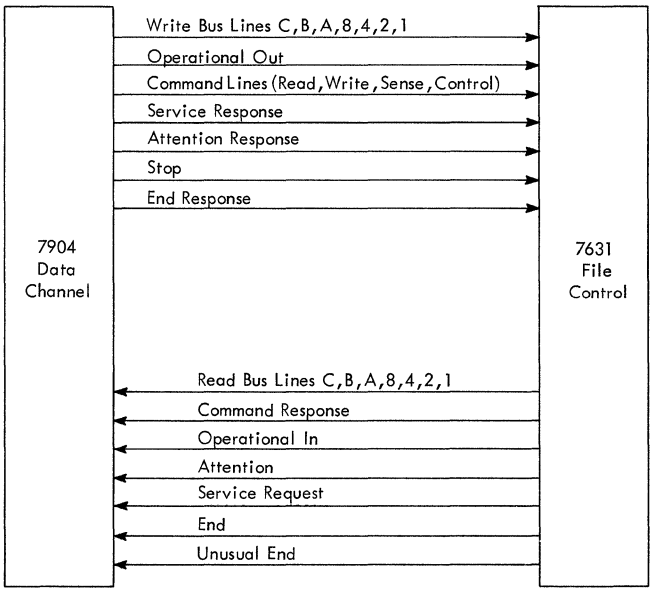
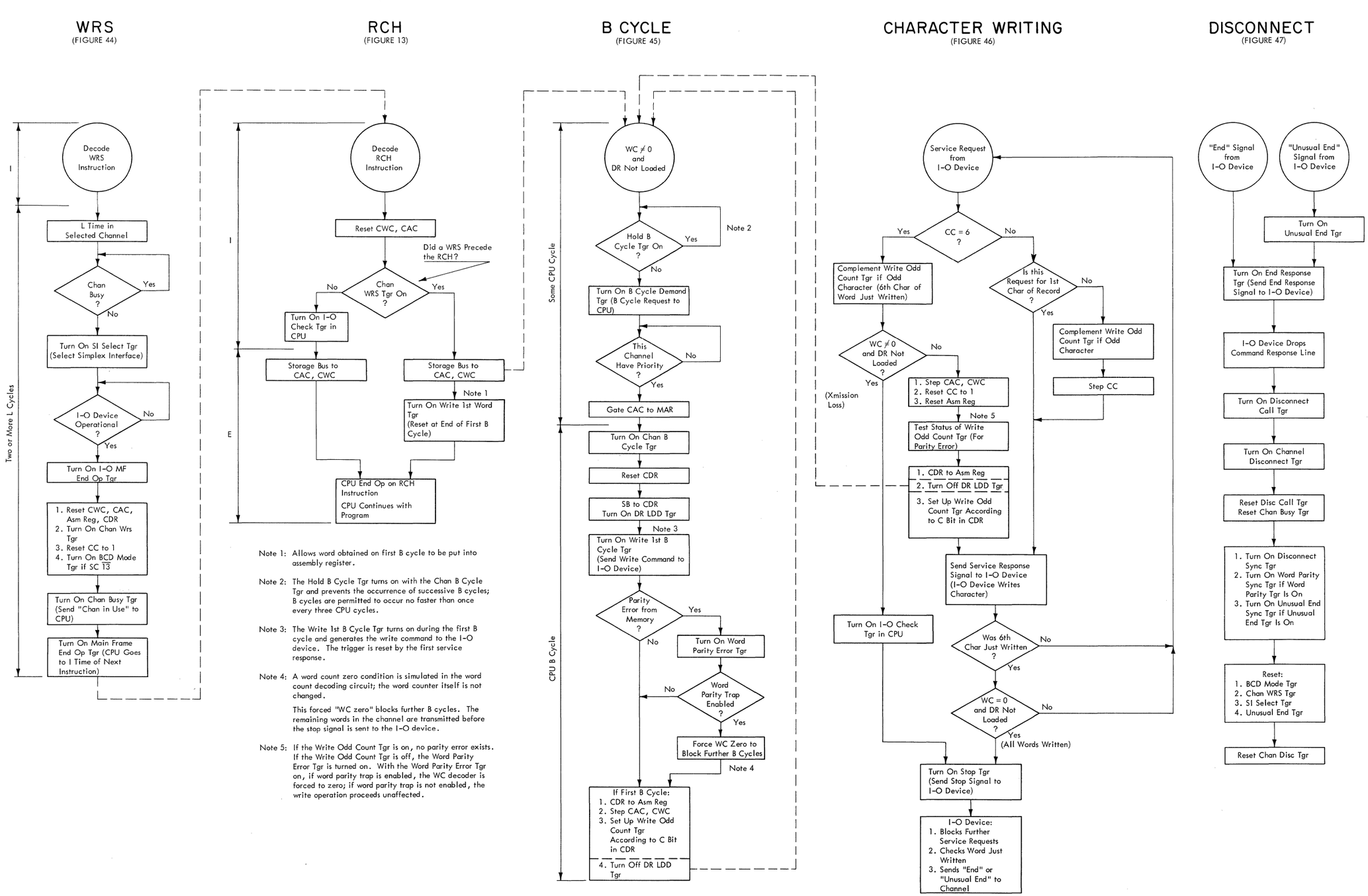


FIGURE 42. SIMPLEX INTERFACE SIGNAL LINES



Note 1: Allows word obtained on first B cycle to be put into assembly register.

Note 2: The Hold B Cycle Tgr turns on with the Chan B Cycle Tgr and prevents the occurrence of successive B cycles; B cycles are permitted to occur no faster than once every three CPU cycles.

Note 3: The Write 1st B Cycle Tgr turns on during the first B cycle and generates the write command to the I-O device. The trigger is reset by the first service response.

Note 4: A word count zero condition is simulated in the word count decoding circuit; the word counter itself is not changed.

This forced "WC zero" blocks further B cycles. The remaining words in the channel are transmitted before the stop signal is sent to the I-O device.

Note 5: If the Write Odd Count Tgr is on, no parity error exists. If the Write Odd Count Tgr is off, the Word Parity Error Tgr is turned on. With the Word Parity Error Tgr on, if word parity trap is enabled, the WC decoder is forced to zero; if word parity trap is not enabled, the write operation proceeds unaffected.

FIGURE 43. WRITE SIMPLEX OPERATION SEQUENCE

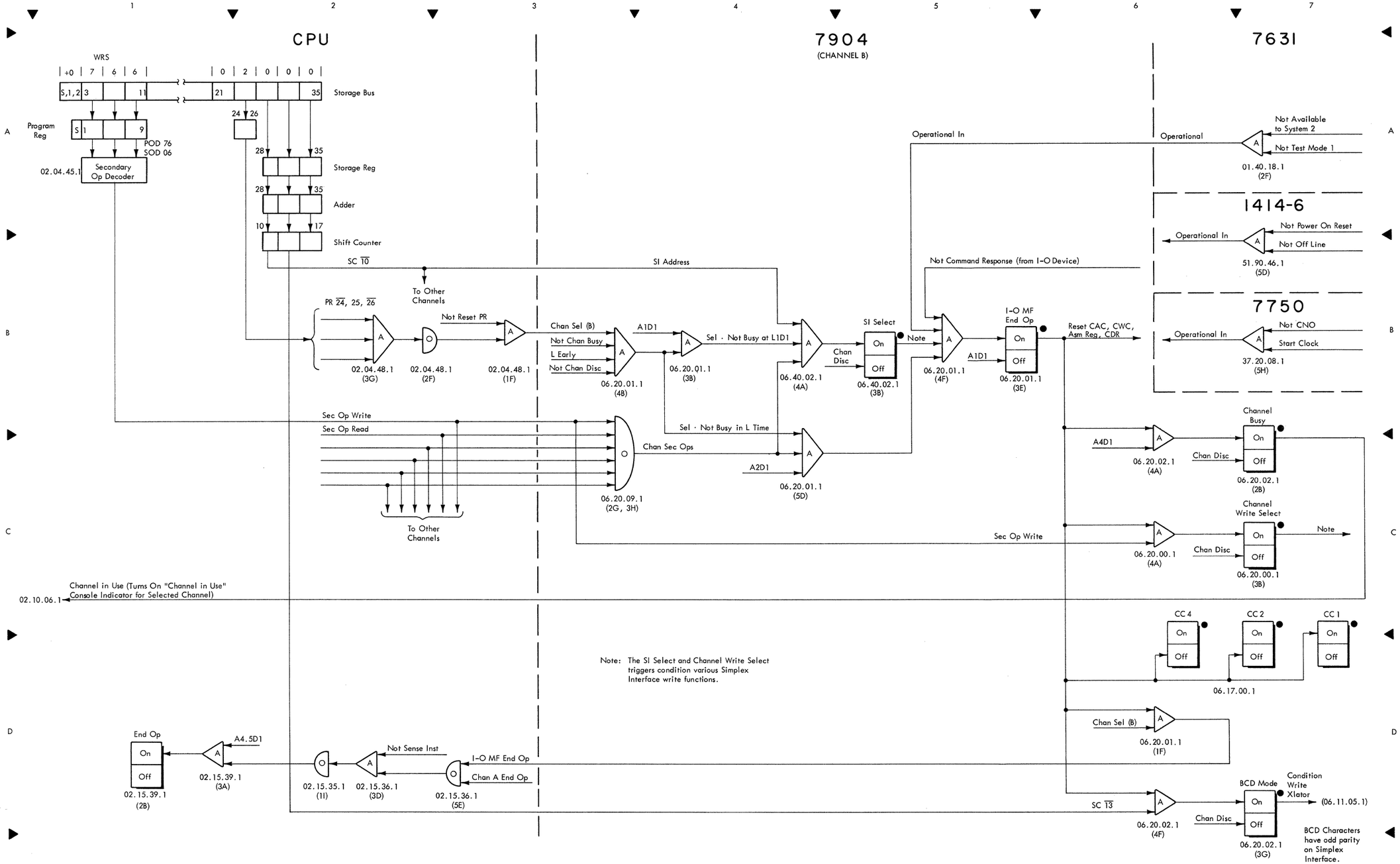


FIGURE 44. WRS, SIMPLEX INTERFACE WRITE OPERATION

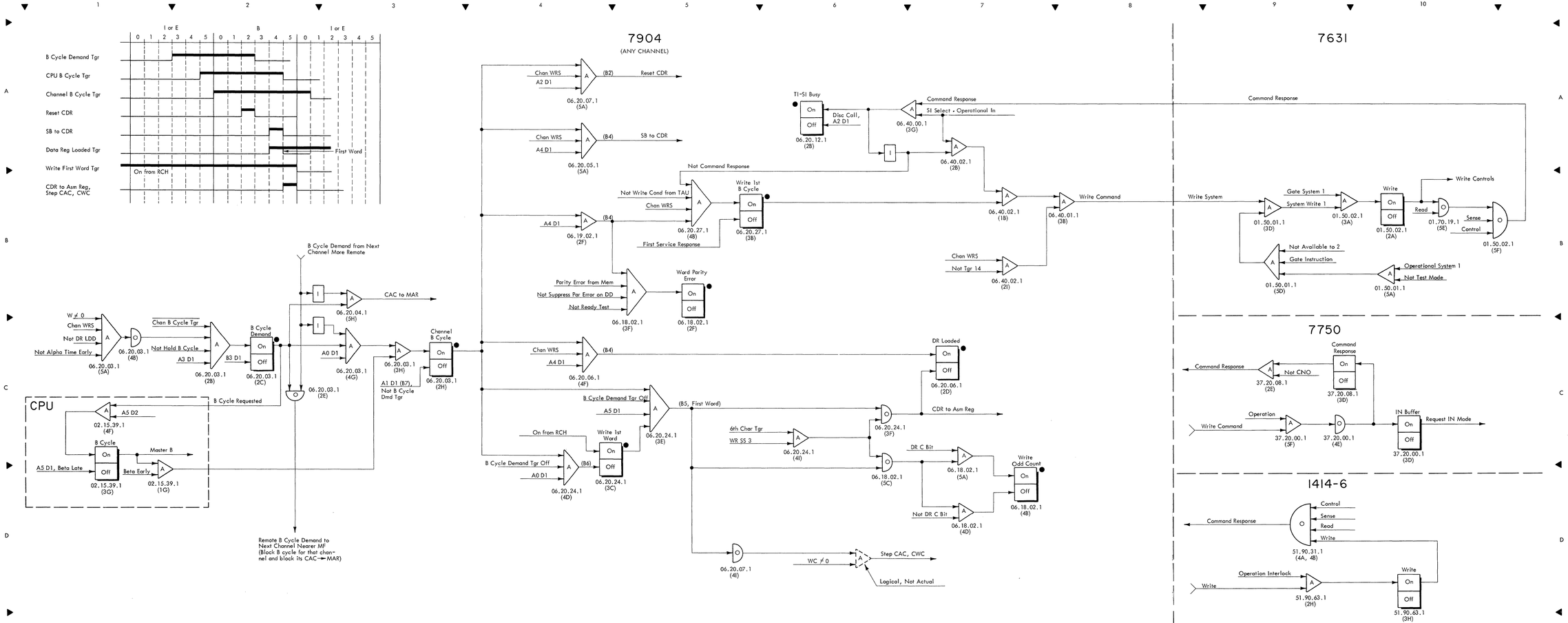


FIGURE 45. B CYCLE, SIMPLEX INTERFACE WRITE OPERATION

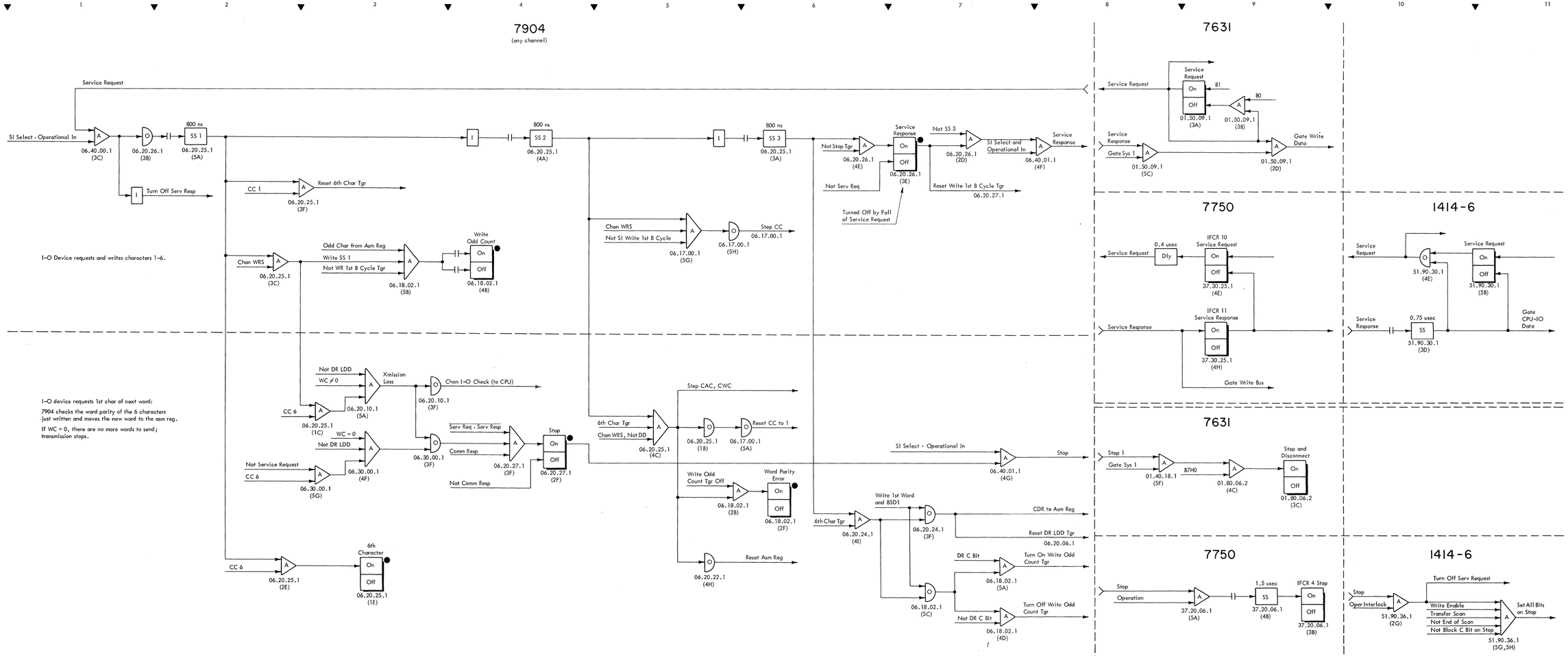


FIGURE 46. CHARACTER WRITING, SIMPLEX INTERFACE WRITE OPERATION

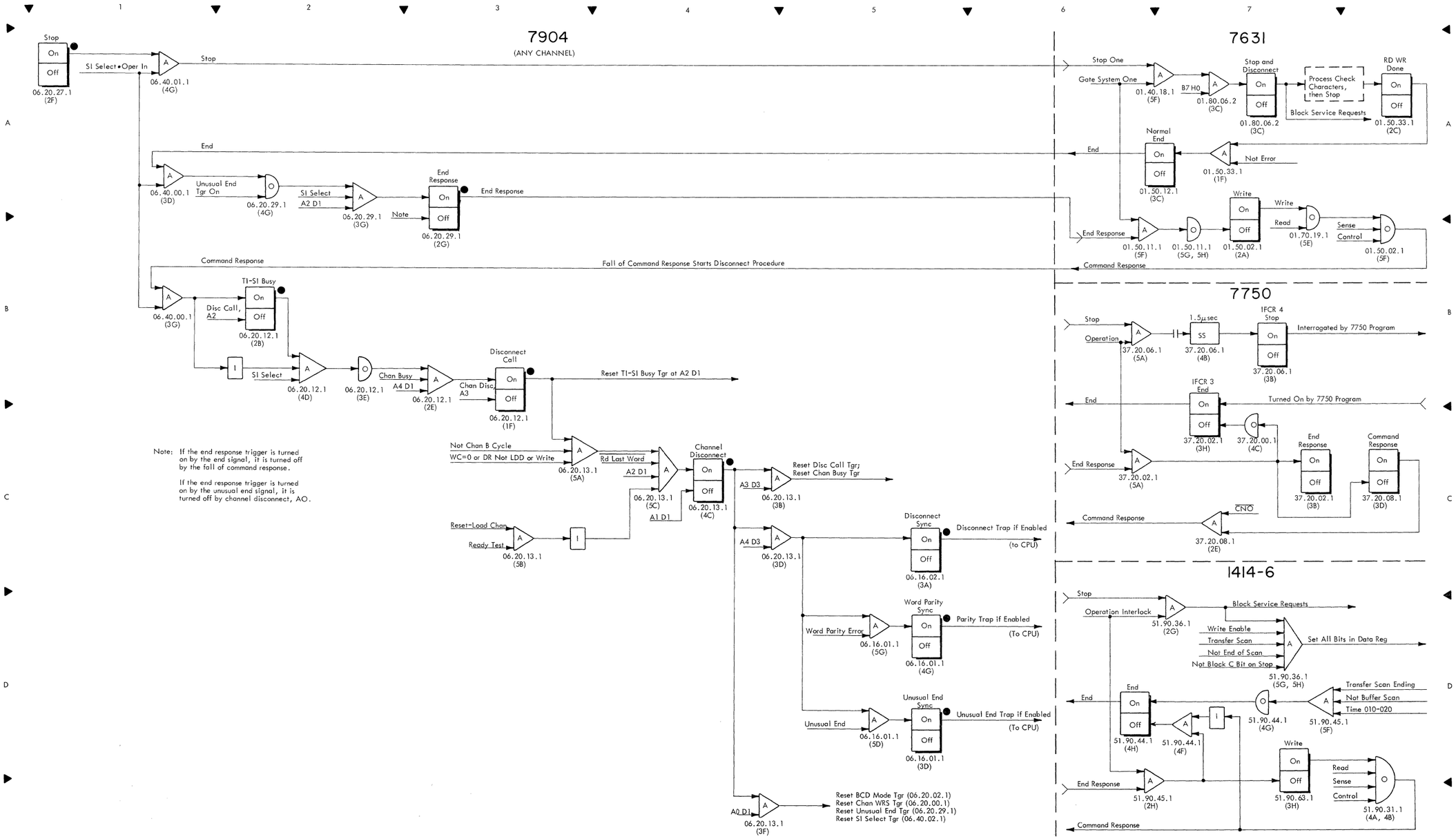


FIGURE 47. END OPERATION AND DISCONNECT, SIMPLEX INTERFACE WRITE OPERATION

SIMPLEX INTERFACE CONTROL OPERATION
(Figures 48, 49)

A control operation is almost identical to a write operation. The difference is that in a control operation, a control command is sent to the I-O device instead of a write command.

The CTR instruction has a bit in position 14; the WRS instruction does not. Bit 14 causes trigger 14 to turn on during the channel selection portion of the write operation (Figure 48). The control command is issued during the first B cycle. Words are transferred to the I-O device in the same manner as for a write operation; transmission stops when the word counter goes to zero.

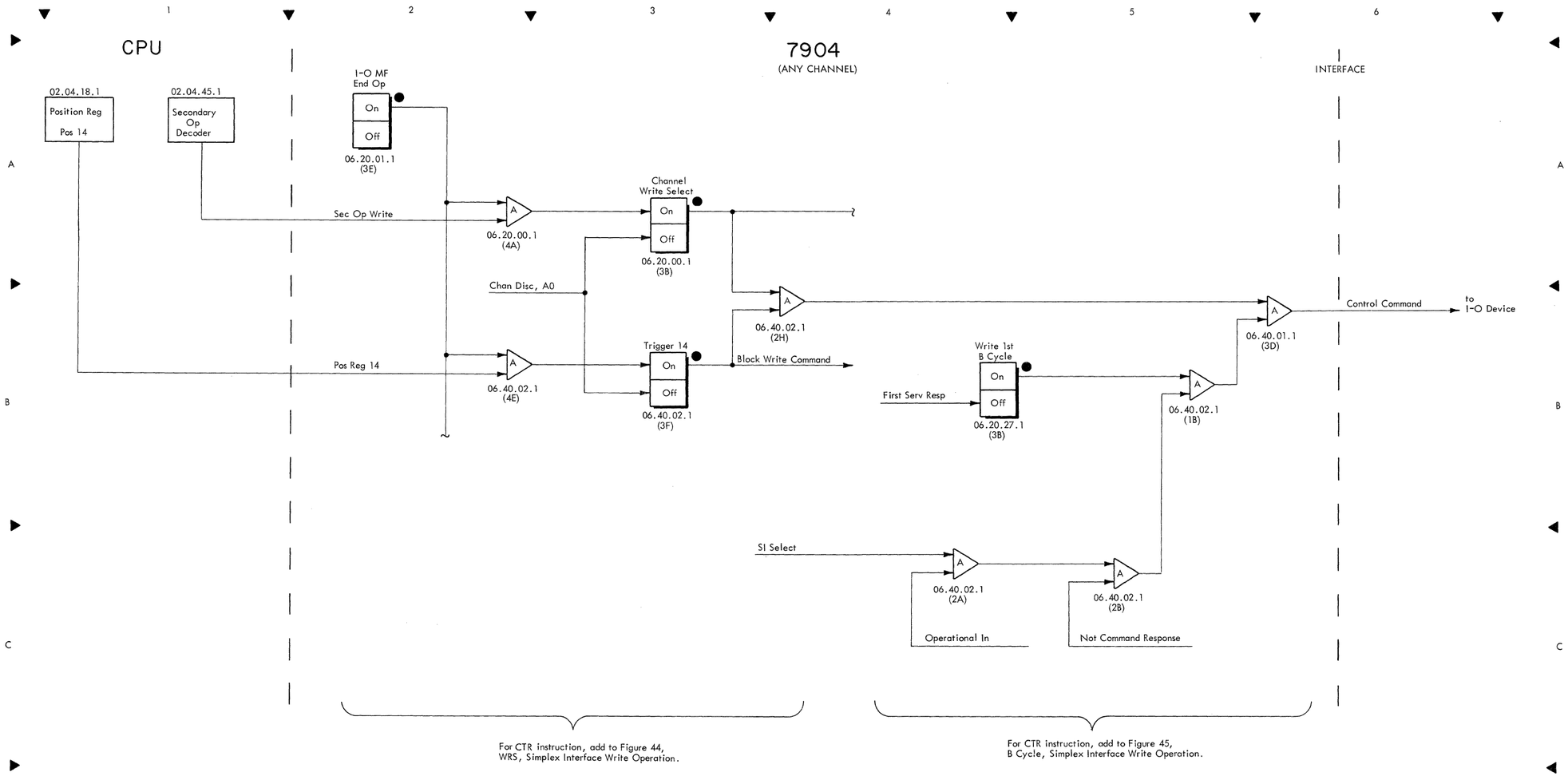
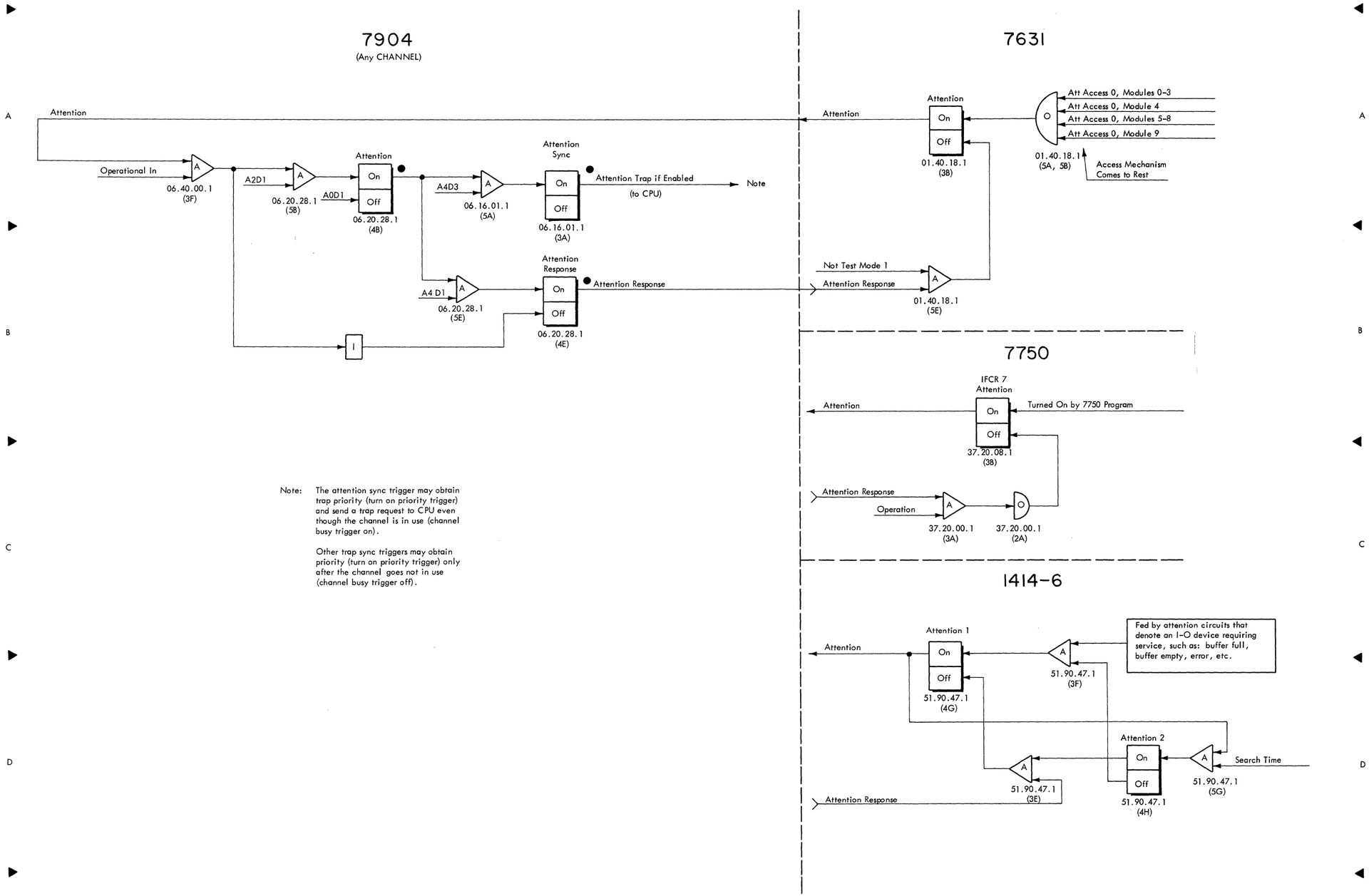


FIGURE 48. CONTROL COMMAND, SIMPLEX INTERFACE CONTROL OPERATION



Note: The attention sync trigger may obtain trap priority (turn on priority trigger) and send a trap request to CPU even though the channel is in use (channel busy trigger on).

Other trap sync triggers may obtain priority (turn on priority trigger) only after the channel goes not in use (channel busy trigger off).

FIGURE 49. ATTENTION, SIMPLEX INTERFACE

SIMPLEX INTERFACE READ OPERATION (Figures 50-55)

Characters are read from the I-O device attached to the Simplex interface into the assembly register of the channel. When each group of six characters is assembled, the 6-character word is transferred to the data register and then on to storage.

The word counter in the channel is normally set higher than the number of words in the record; transmission stops when the I-O device reaches the end of its record.

Figure 50 shows the sequence of the read Simplex operation.

Read Selecting the Channel (RDS)

The RDS instruction initiates the read operation (Figure 51). The address portion of the instruction selects channel B, C, D, or E, and selects the Simplex interface of that channel. The operation portion of the instruction sets up the channel for reading; that is, it conditions certain circuits in the channel that will allow reading from the I-O device through the Simplex interface. If the device is ready to send data, the RDS operation ends, and the program goes on with the next instruction.

Command Word Loading (RCH)

An RCH instruction for the channel just selected is executed, causing a command word to be sent from storage to the channel. The command word, when entered into the channel, sets the word counter and address counter. The word count in a Simplex interface read operation is usually insignificant, because if the I-O device is to stop the data transmission, the I-O device will reach end-of-record before the word counter reaches zero.

The RCH instruction requires an I cycle and an E cycle, after which the program proceeds with the next instruction. During the E cycle of the RCH, a read command signal is sent to the I-O device. The channel now waits on the first service request from the I-O device.

See Figure 52 for channel actions caused by the RCH.

Character Transmission

The I-O device reads the first character, puts it on the read bus, and sends a service request signal to the channel (Figure 53). The service request signal trips off a series of three single-shots in the channel. The single-shots check each character received for proper parity, control the character counter (make sure each character goes into its proper place in the assembly register), and control a circuit that keeps track of the odd-even count of each group of six characters. This latter job is necessary because a parity bit must be assigned to the assembled word before the word is put into storage. The single-shots finally send a service response signal to the I-O device; this signal tells the I-O device that the channel has received the character and that the I-O device may send the next one.

After each group of six characters is received, the 6-character word moves from the assembly register to the data register. The assembly register is now empty and ready to receive the next group of characters. Because the data register is loaded, a B cycle is requested to move the word from the data register to storage.

B Cycle

On a read operation, the word counter not zero and the data register loaded cause a B cycle demand to be sent to CPU. The next CPU cycle following the request becomes a B cycle, during which the word in the data register moves to storage. The data register is now empty and ready to receive the next word from the assembly register.

See Figure 29 for B cycle actions in the channel. Although this figure is in the read tape section of the manual, it is valid for B cycle, Simplex interface read.

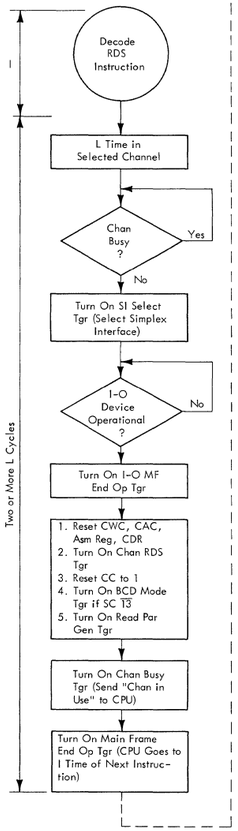
End Operation and Disconnect

The I-O device reaches the end of its record, checks to make sure that the transmission was correct, and sends an end signal to the channel (Figure 54). The end signal in the channel generates end response, which is sent to the I-O device. If the transmission had not been correct, the I-O device would have sent unusual end instead of end. Unusual end would have also generated end response, but, in addition, would have caused an unusual end trap.

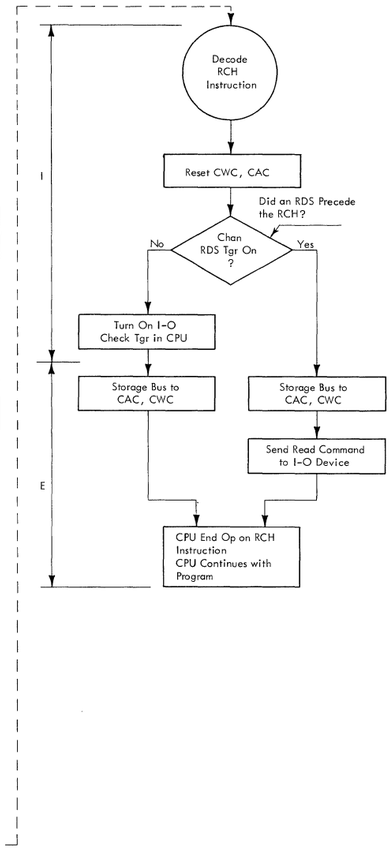
End response at the I-O device makes the I-O device read circuits inactive; this action results in command response being dropped. The fall of command response at the channel turns on the disconnect call trigger. When the last word moves from the CDR to storage, the channel disconnect trigger turns on. This trigger resets all the triggers that were maintaining the channel in a read Simplex interface status, and sets up the trap sync triggers for any trap conditions that might have occurred on the read operation. The channel is now not busy and may be used by CPU for another read or write.

As words move from the data register to storage on B cycles, the word counter steps down. If the word counter was initially set lower than the number of words in the record, it will reach zero before the I-O device reaches its end-of-record. In this event, no more B cycles are allowed, and a stop signal is sent to the I-O device. The I-O device then sends an unusual end signal to the channel, starting the channel disconnect procedure.

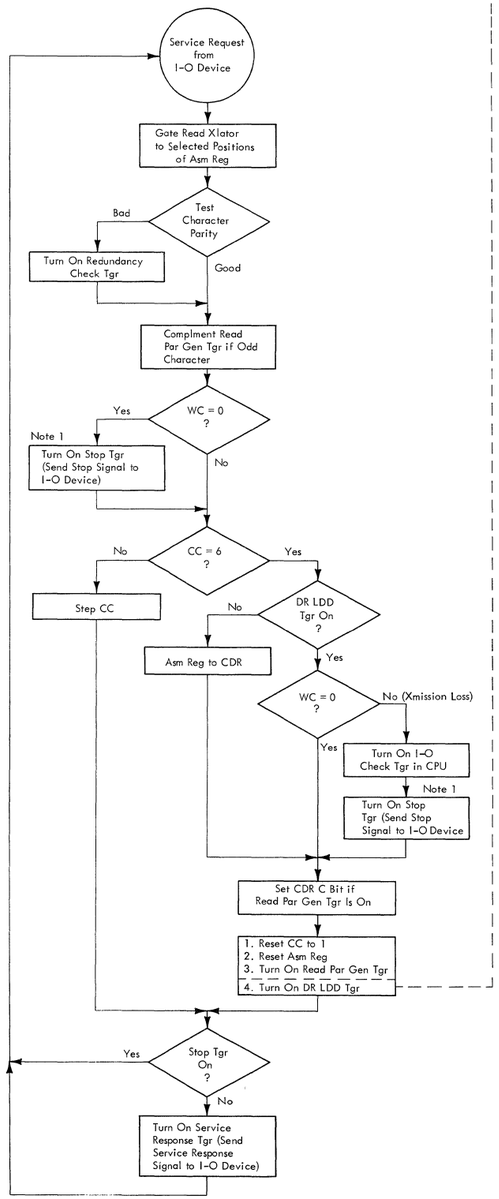
RDS
(FIGURE 51)



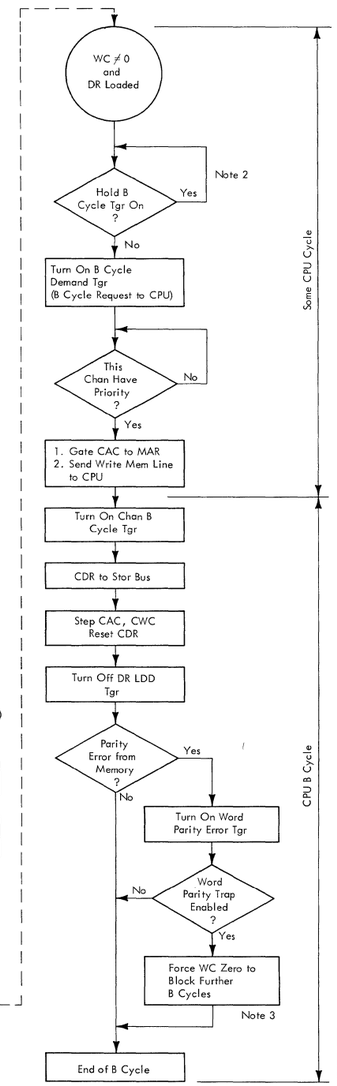
RCH
(FIGURE 52)



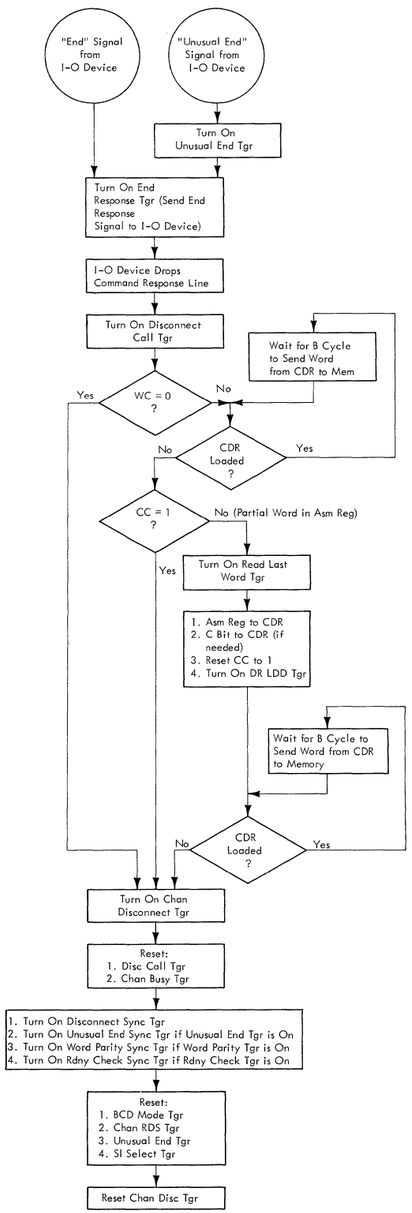
CHARACTER READING
(FIGURE 53)



B CYCLE
(FIGURE 29)



DISCONNECT
(FIGURE 54)



Note 1: The Stop Tgr on blocks further service response signals to the I-O device. The I-O device sends no more characters to the channel.

Note 2: The Hold B Cycle Tgr turns on with the Chan B Cycle Tgr and prevents the occurrence of successive B cycles; B cycles are permitted to occur no faster than once every three CPU cycles.

Note 3: A word count zero condition is simulated in the word count decoder circuit; the word counter itself is not changed.

This forced "WC zero" blocks further B cycles (no more words are stored in memory) and turns on the Stop Tgr on the next service request.

FIGURE 50. READ SIMPLEX OPERATION SEQUENCE

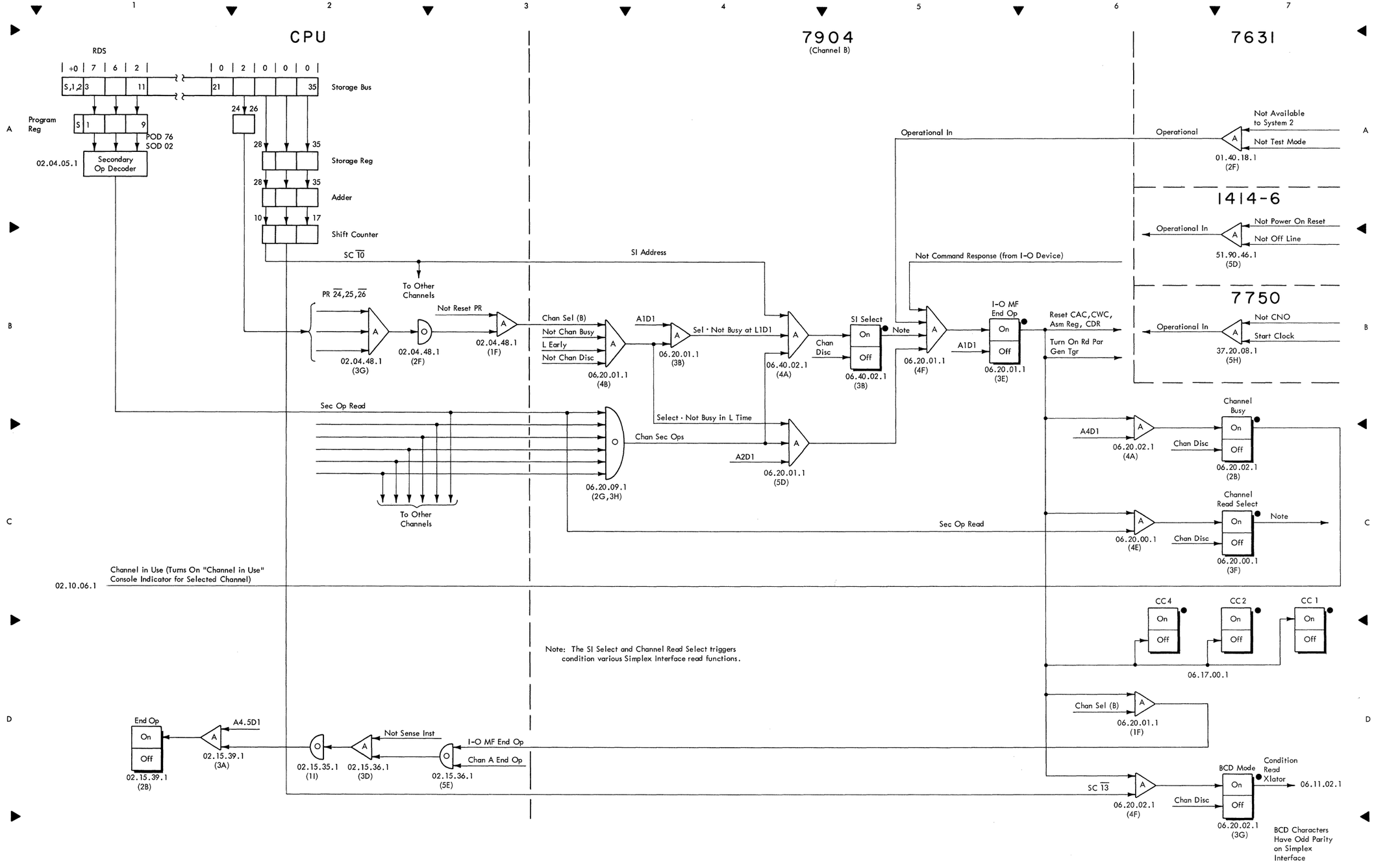


FIGURE 51. RDS, SIMPLEX INTERFACE READ OPERATION

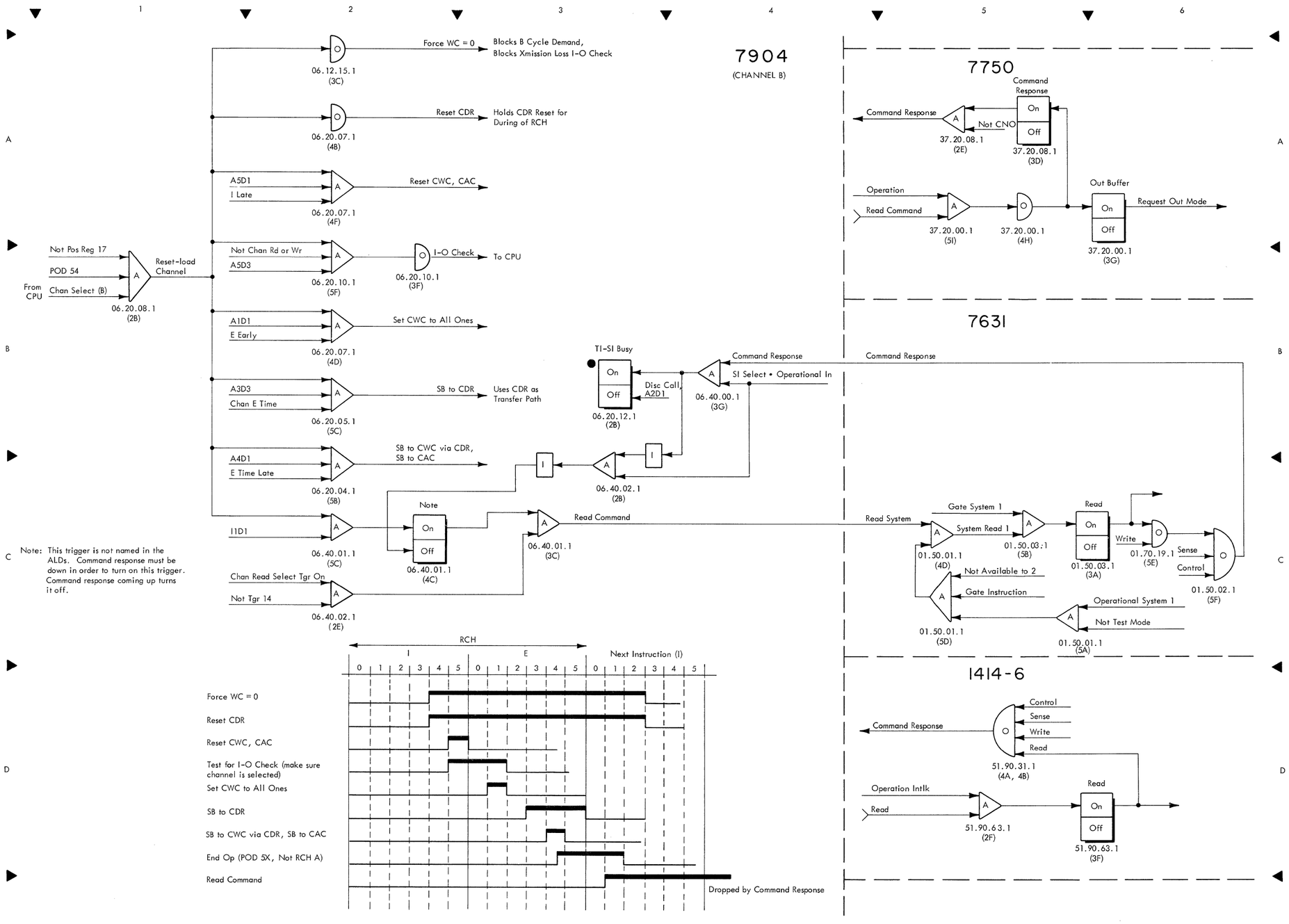


FIGURE 52. RCH, SIMPLEX INTERFACE READ OPERATION

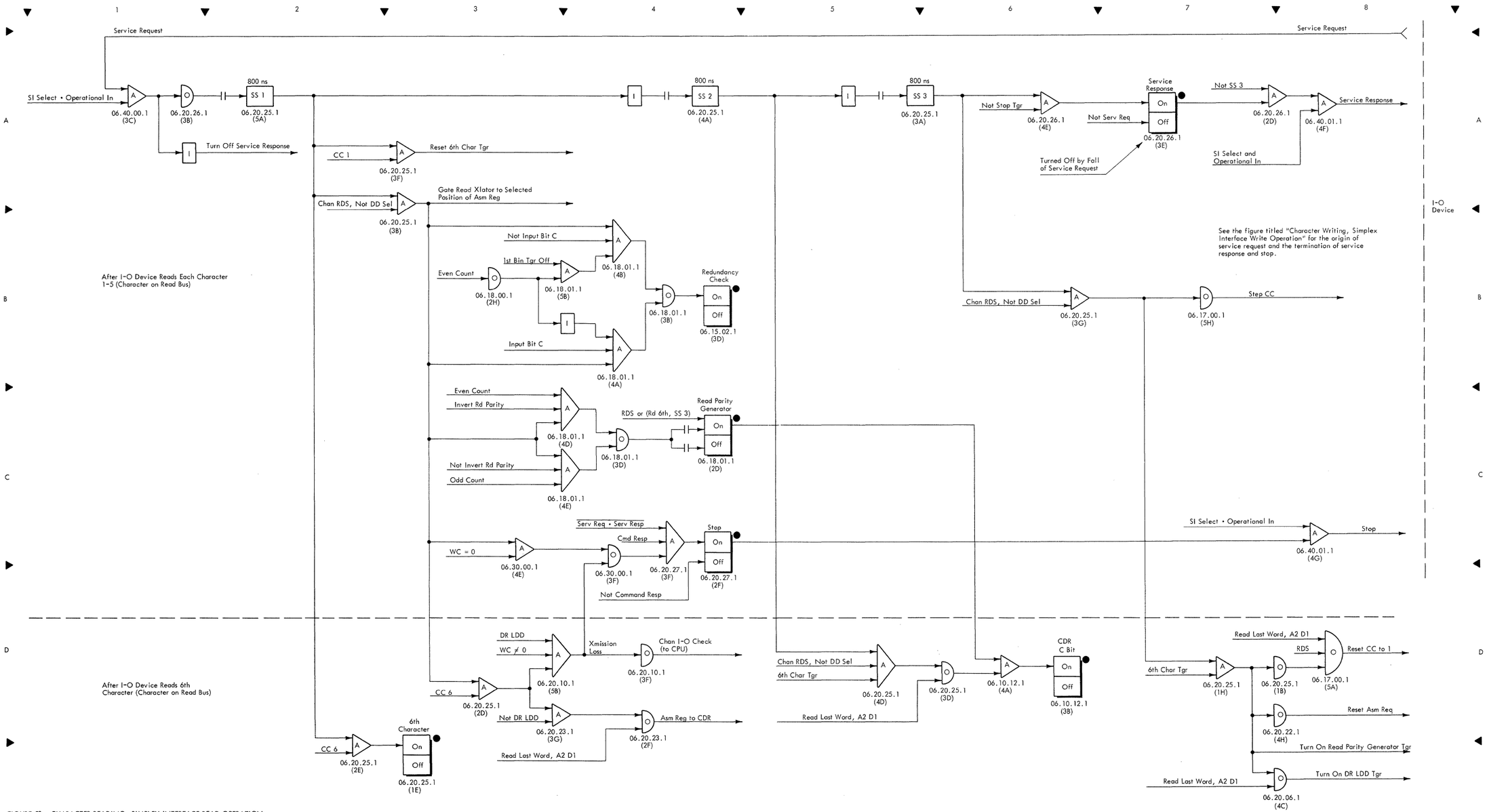


FIGURE 53. CHARACTER READING, SIMPLEX INTERFACE READ OPERATION

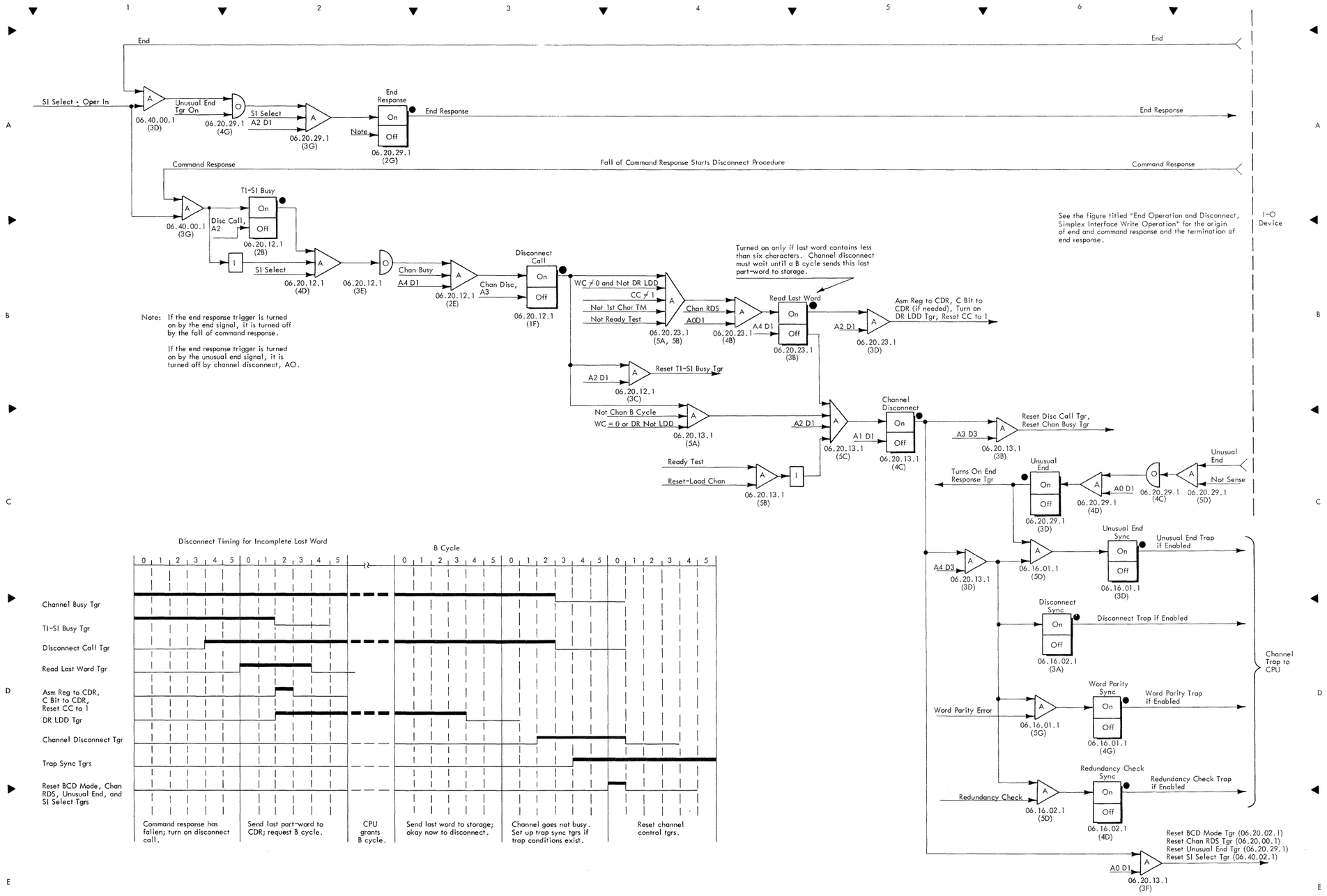


FIGURE 54. END OPERATION AND DISCONNECT, SIMPLEX INTERFACE READ OPERATION

WRITE SIMPLEX

I-O CHECK
(Turns on console I-O check light)

Caused by:

1. RCH and no WRS.
2. Transmission loss.
   (a) Sends stop signal to I-O device.

Error detection:

1. IOT instruction.
   (a) If I-O check, execute next instruction.
   (b) If not I-O check, skip next instruction.

WORD PARITY ERROR
(Turns on console channel check light)

Caused by:

1. B cycle storage bus parity.
2. Odd-even count of six characters does not agree with word C bit from CDR.

Error detection:

1. If enabled for word parity trap, force WC zero on error, send stop signal to I-O device, and trap after disconnect.
2. If not enabled for word parity trap, but disconnect trap is enabled, store parity flag bit along with disconnect flag bit when disconnect trap is taken.

UNUSUAL END

Caused by:

1. Error or unusual condition in I-O device.

Error detection:

1. If enabled for unusual end trap, trap after disconnect.
2. If not enabled for unusual end trap, error is not detected.

TRAPS (Taken after channel disconnects)

1. Disconnect: enabled by "Enb CWT, EOF, End, Unend" trigger.
2. Word parity: enabled by "Enb TCT and Word Parity" trigger.
3. Unusual end: enabled by "Enb CWT, EOF, End, Unend" trigger.

Attention Trap

The channel attention trigger may be turned on at any time by the attention signal from the I-O device. If the channel is enabled for attention trap (Enb Attention trigger on), CPU executes a channel trap, storing the attention flag bit.

READ SIMPLEX

I-O Check
(Turns on console I-O check light)

Caused by:

1. RCH and no RDS.
2. Transmission loss.
   (a) Sends stop signal to I-O device.

Error detection:

1. IOT instruction.
   (a) If I-O check, execute next instruction.
   (b) If not I-O check, skip next instruction.

REDUNDANCY CHECK
(Turns on console channel check light)

Caused by:

1. Bit count of character does not agree with C bit received with character.

Error detection:

1. If not enabled for trap, redundancy check is tested by TRC instruction.
   (a) If redundancy check, turn off redundancy check tgr and transfer.
   (b) If not redundancy check, proceed with program.
2. If enabled for trap, force WC zero on error, send stop signal to I-O device, and trap after disconnect.

WORD PARITY ERROR
(Turns on console channel check light)

Caused by:

1. B cycle storage bus parity.

Error detection:

1. If enabled for word parity trap, force WC zero on error, send stop signal to I-O device, and trap after disconnect.
2. If not enabled for word parity trap, but disconnect trap is enabled, store parity flag bit along with disconnect flag bit when disconnect trap is taken.

UNUSUAL END

Caused by:

1. Error or unusual condition in I-O device.

Error detection:

1. If enabled for unusual end trap, trap after disconnect.
2. If not enabled for unusual end trap, error is not detected.

TRAPS (Taken after channel disconnects)

1. Disconnect: enabled by "Enb CWT, EOF, End, Unend" trigger.
2. Redundancy check: enabled by "Enb TCT and Word Parity" trigger.
3. Word parity: enabled by "Enb TCT and Word Parity" trigger.
4. Unusual end: enabled by "Enb CWT, EOF, End, Unend" trigger.

Attention Trap

The channel attention trigger may be turned on at any time by the attention signal from the I-O device. If the channel is enabled for attention trap (Enb Attention trigger on), CPU executes a channel trap, storing the attention flag bit.

FIGURE 55. ERROR AND TRAP CONDITIONS, SIMPLEX INTERFACE OPERATION

SIMPLEX INTERFACE SENSE OPERATION

The sense operation is essentially the same as a read operation. The main difference is that in a sense operation, the 7904 sends a sense command to the I-O device instead of a read command.

The SEN instruction has a bit in position 14; the RDS instruction does not. Bit 14 causes trigger 14 to turn on during the channel selection portion of the operation (Figure 56). The sense command is issued during the RCH. Words are transferred from the I-O device to storage in the same manner as for a read operation; the I-O device stops the transmission.

Trigger 14 on holds the BCD mode trigger off, forcing binary mode; the sense words are transferred to storage without translation.

If the sense instruction is executed for an I-O device that is not ready (operational in line inactive), a bit is put in assembly register position 0, and the disconnect call trigger is turned on. The channel disconnects after the word in the assembly register is stored in memory.

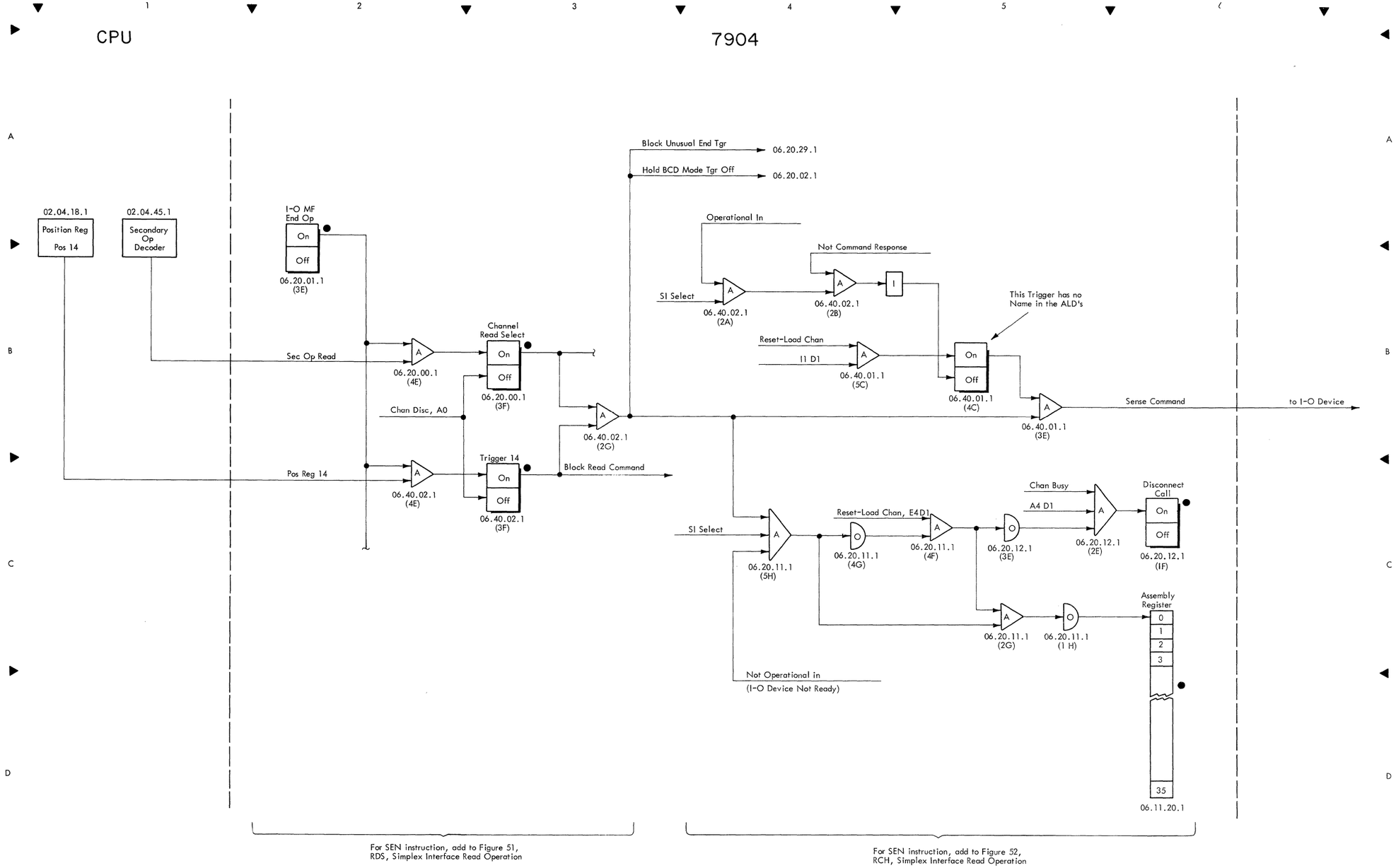


FIGURE 56. SENSE COMMAND, SIMPLEX INTERFACE SENSE OPERATION

DIRECT DATA LOGIC

DIRECT DATA WRITE OPERATION (Figures 57-66)
Words are transferred in parallel from the CDR of the writing computer's channel to the CDR of the reading computer's channel. (The reading computer is assumed to be another 7040/7044 System.) When a word is sent to the reading computer:

1. The writing computer's channel requests a B cycle to fill its CDR with a new word from memory.
2. The reading computer's channel requests a B cycle to store its CDR contents into memory.

The write operation ends when either computer's CWC goes to zero.

Figure 59 shows the sequence of the direct data write operation.

Write Selecting the Channel (WRS)

The WRS instruction initiates the write operation (Figure 60). The address portion of the instruction selects channel B, C, D, or E, and selects the DD interface of that channel. The operation portion of the instruction sets up the channel for writing; that is, it conditions certain circuits in the channel that will allow writing to the I-O computer through the direct data interface. The WRS operation ends, and the program goes on with the next instruction.

Command Word Loading (RCH)

An RCH instruction for the channel just selected is executed, causing a command word to be sent from storage to the channel. The command word, when entered into the channel, sets the word counter and address counter. The RCH instruction requires an I cycle and an E cycle, after which the program proceeds with the next instruction.

The word counter not zero and the data register not loaded cause a B cycle demand. See Figure 61 for actions in the channel caused by the RCH.

B Cycle

The word counter not zero and the data register not loaded cause a B cycle demand to be sent to CPU (Figure 62). The next CPU cycle following the request becomes a B cycle, during which the first word to be transmitted is sent from storage to the channel's data register. The 37 outputs of the writing channel's CDR are immediately available at the input AND circuits of the reading channel's CDR. The word is not set into the reading channel's CDR, however, until certain transfer controls are activated.

Data Transfer

The controls for transferring words from the writing to the reading computer are shown in Figure 63.

The reading computer's channel must have been previously read selected by an RDS instruction, and must have had its CWC and CAC set by the RCH instruction.

The data register loaded trigger on in the writing channel (word waiting in the CDR to be transmitted) causes a ready write signal to be sent to the reading computer's channel. The data register loaded trigger off and the CWC not zero in the reading channel (reading channel ready to accept the word) cause a ready read signal to be sent to the writing computer's channel. In the reading channel, ready read and the receipt of ready write cause the 37 bits from the writing channel's CDR to be gated into its own CDR. In the writing channel, ready write and the receipt of ready read indicate that the word has been taken by the reading channel, and that the writing channel may now request another B cycle to get the next word from memory. When the reading channel gated the word into its own CDR, it also requested a B cycle to store the word into its memory.

When the B cycles for both computers have been completed, ready write and ready read are again generated and the next word is transmitted. This process continues until the CWC of either channel (transmitting or receiving) goes to zero.

End Operation and Disconnect

Either channel's (transmitting or receiving) CWC going to zero initiates the disconnect procedure that results in the disconnection of both channels. Normally, the CWC of the writing channel goes to zero before the CWC of the reading channel. This is the assumption here. Refer to Figure 64.

The CWC is stepped on each B cycle, and when stepped to zero, the CWC indicates that the last word to be transmitted is in the CDR. After each word is transmitted, the DD EOR gate trigger tests the CWC for a zero condition. If the CWC is zero on this test, the last word has been transmitted. A WC zero signal is then sent to the reading channel, turning on that channel's disconnect call trigger. A DD EOR signal is returned to the writing channel, turning on the writing channel's disconnect call trigger.

The disconnect call triggers subsequently turn on their respective channel disconnect triggers. The channel disconnect triggers reset the triggers that were maintaining the channels in their respective read and write statuses, and set up the trap sync triggers for any trap conditions that might have occurred during the DD operation. The channels are now not busy and may be used by their CPU's for another read or write.

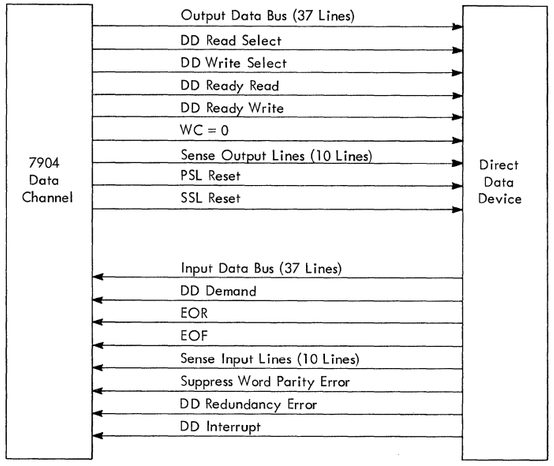
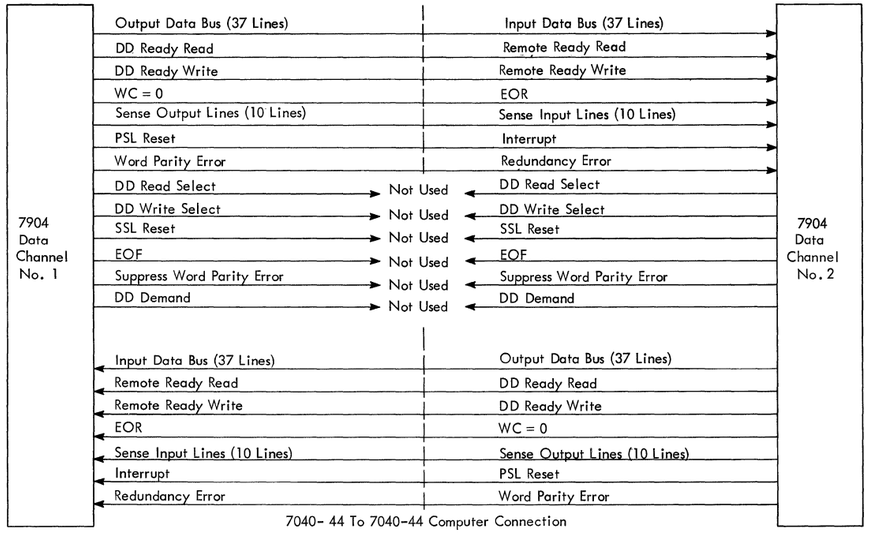
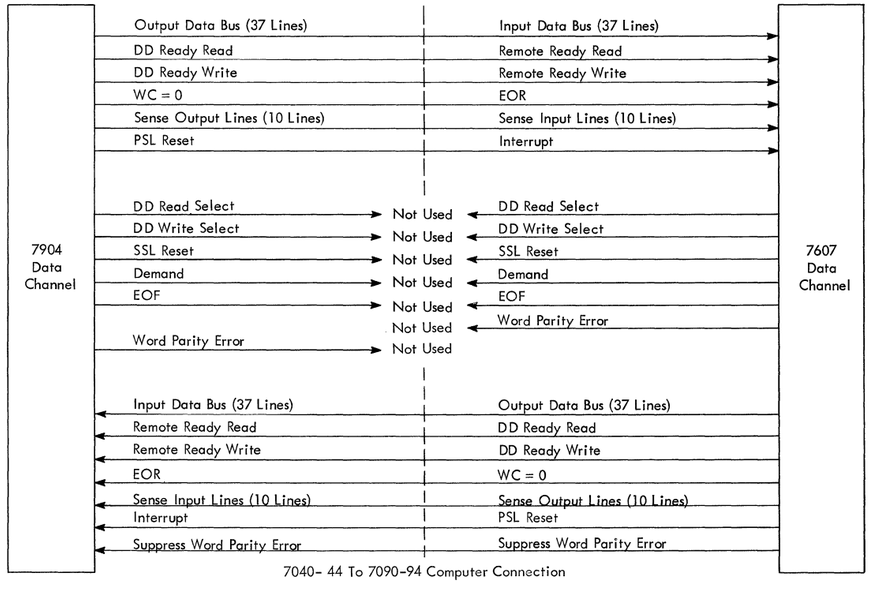


FIGURE 57. DIRECT DATA CONNECTION SIGNAL LINES

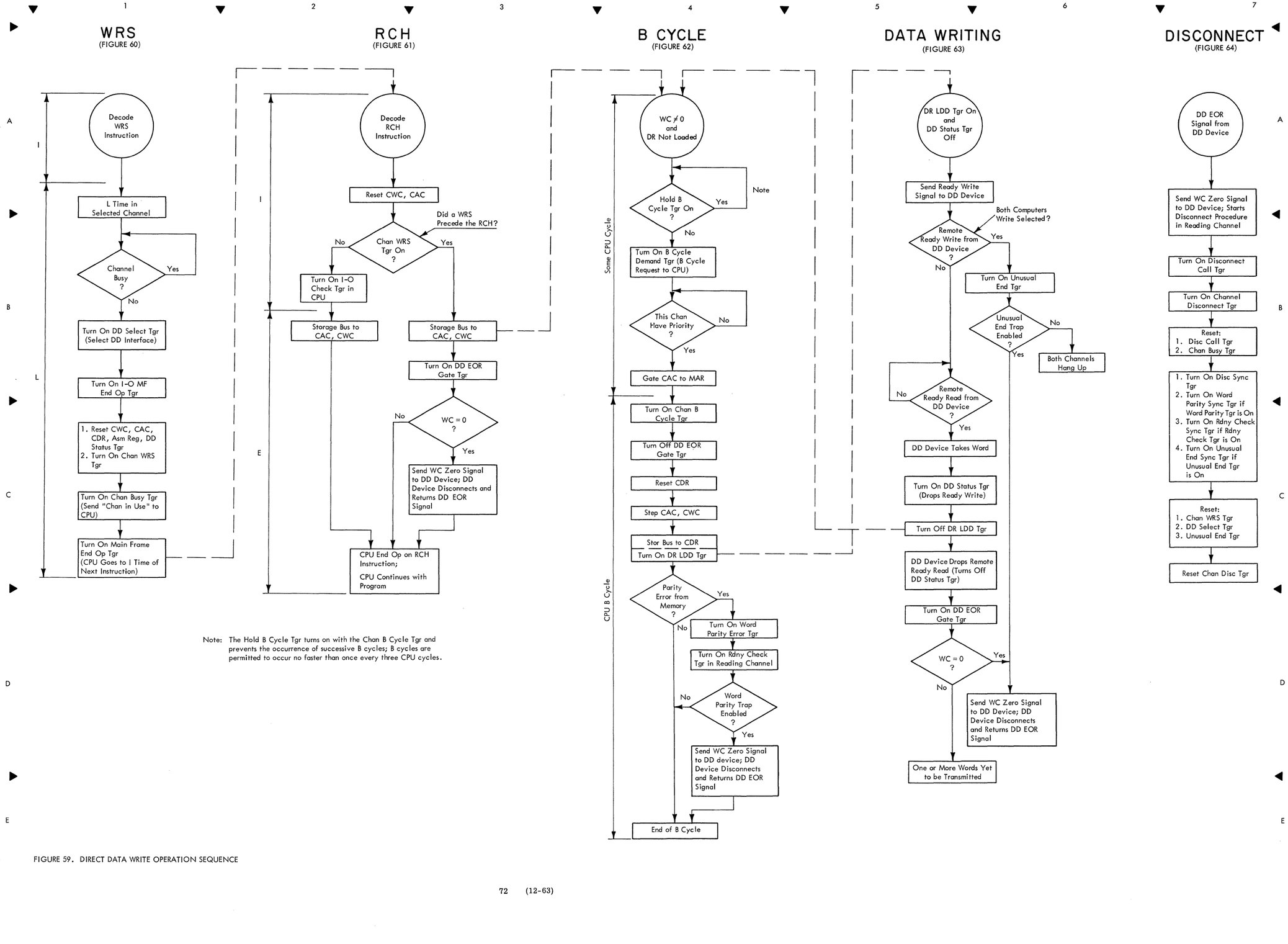


7040- 44 To 7040-44 Computer Connection



7040- 44 To 7090-94 Computer Connection

FIGURE 58. DIRECT DATA SIGNAL LINES FOR 7040-44 AND 7090-94



Note: The Hold B Cycle Tgr turns on with the Chan B Cycle Tgr and prevents the occurrence of successive B cycles; B cycles are permitted to occur no faster than once every three CPU cycles.

FIGURE 59. DIRECT DATA WRITE OPERATION SEQUENCE

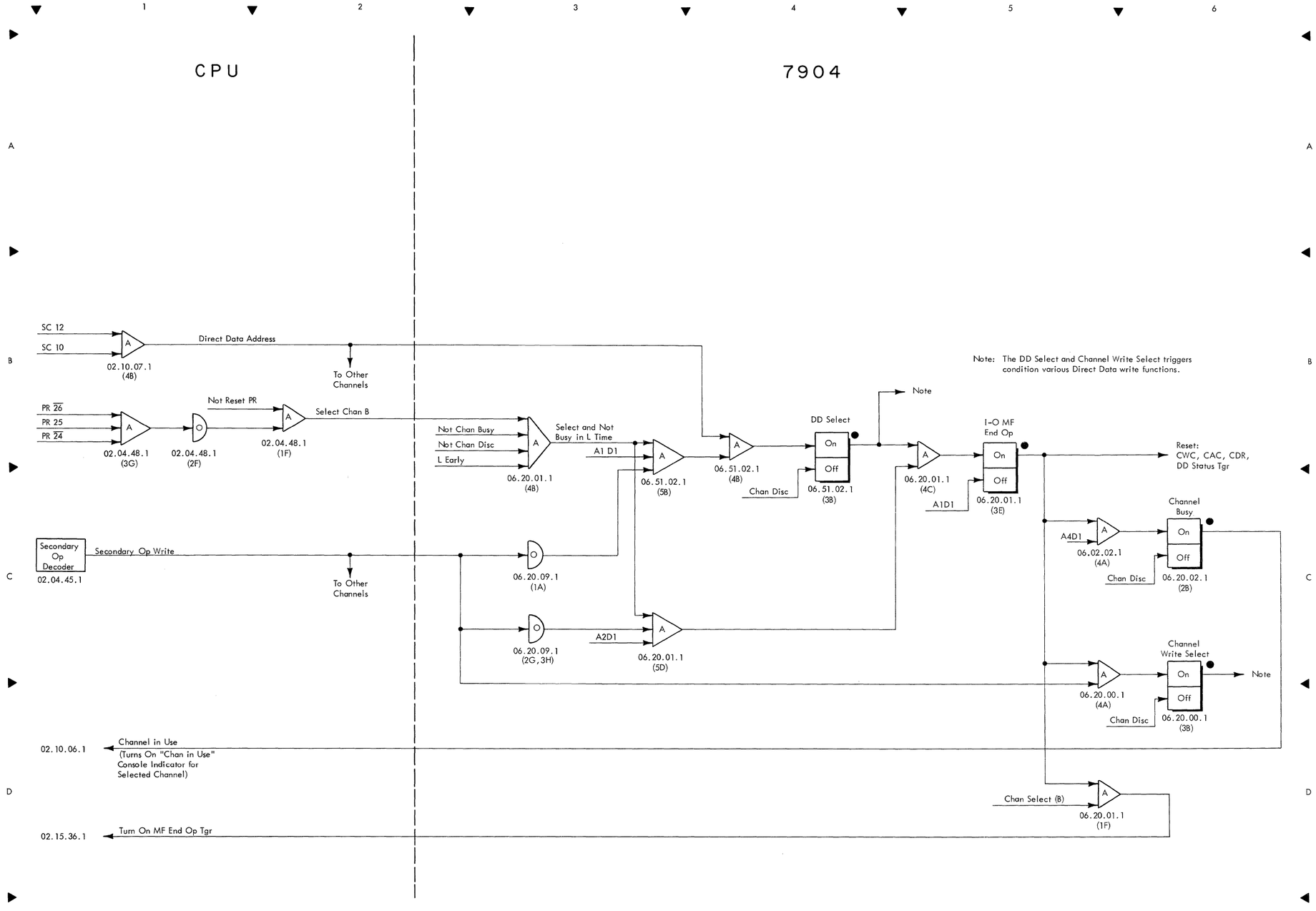


FIGURE 60. WRS, DD WRITE OPERATION

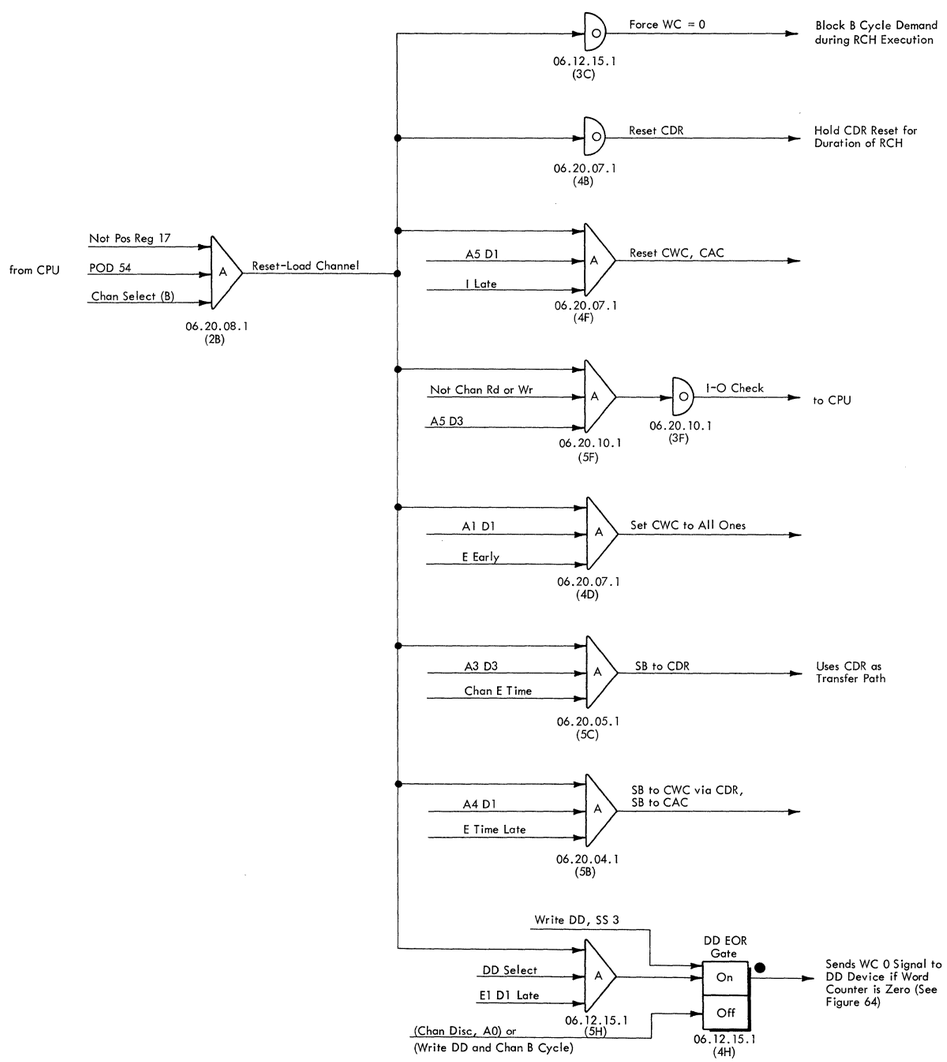
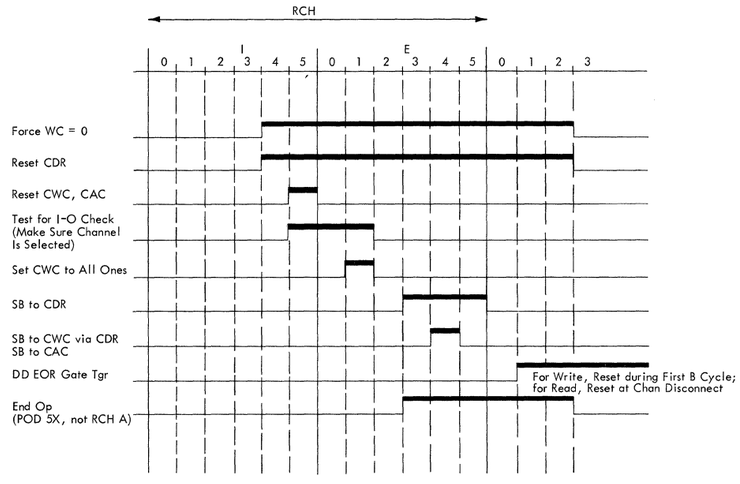


FIGURE 61. RCH, DIRECT DATA OPERATION



Note: The DD EOR Gate Tgr determines when the word counter is tested for a WC zero condition.

For the reading channel, the DD EOR Gate Tgr is on from the RCH until disconnect time; therefore, if the WC goes to zero anytime during the read operation, a disconnect occurs.

For the writing channel, the DD EOR Gate Tgr tests the word counter immediately after the RCH (for an initial word count of zero), and thereafter as each word is sent to the reading channel. If the WC is zero at any time it is tested, a disconnect occurs.

A WC zero signal from the transmitting channel to the receiving channel (or vice versa) results in a disconnect of both channels.

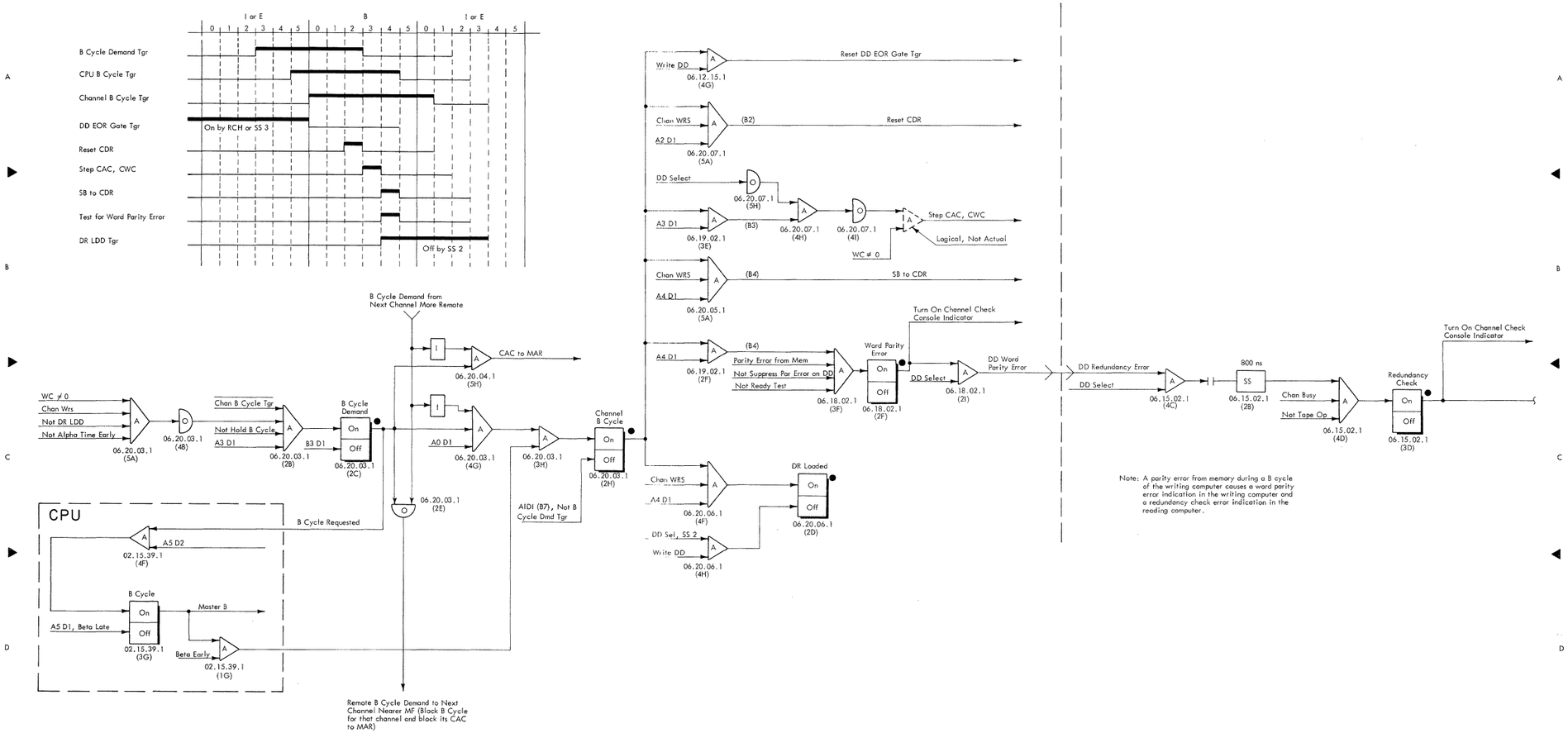
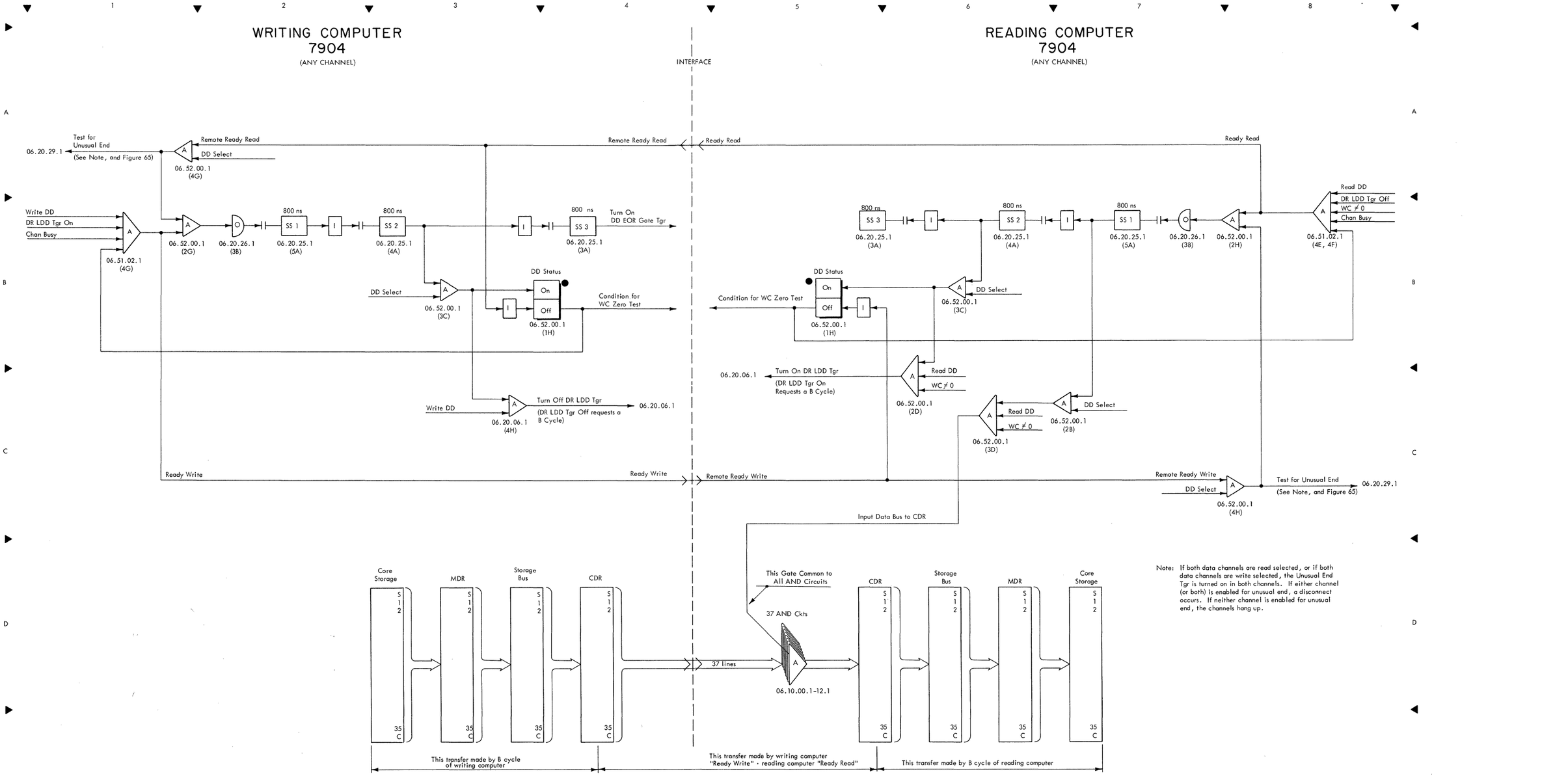


FIGURE 62. B CYCLE, DD WRITE OPERATION



Note: If both data channels are read selected, or if both data channels are write selected, the Unusual End Tgr is turned on in both channels. If either channel (or both) is enabled for unusual end, a disconnect occurs. If neither channel is enabled for unusual end, the channels hang up.

FIGURE 63. DATA TRANSFER CONTROL, DIRECT DATA OPERATION

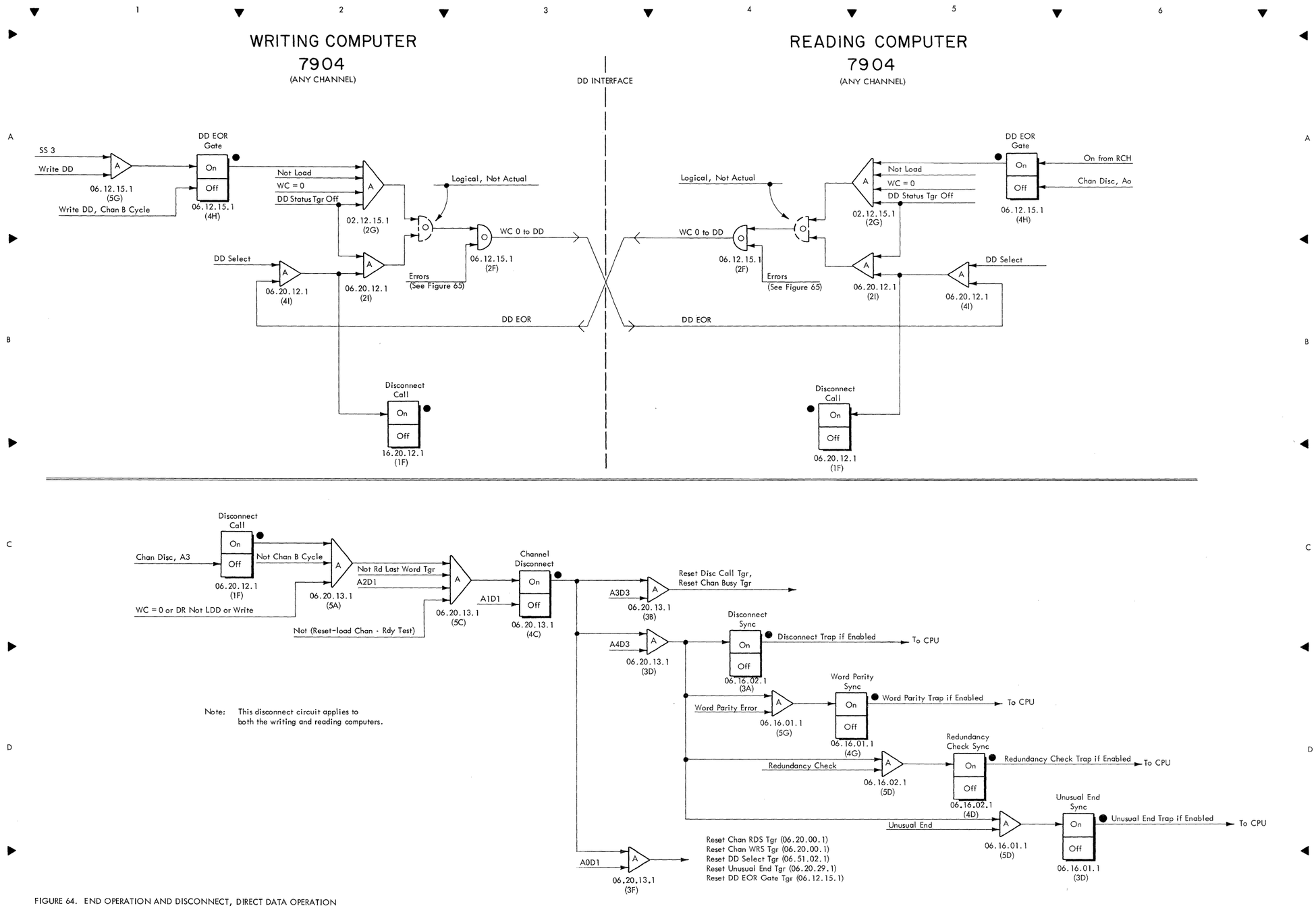
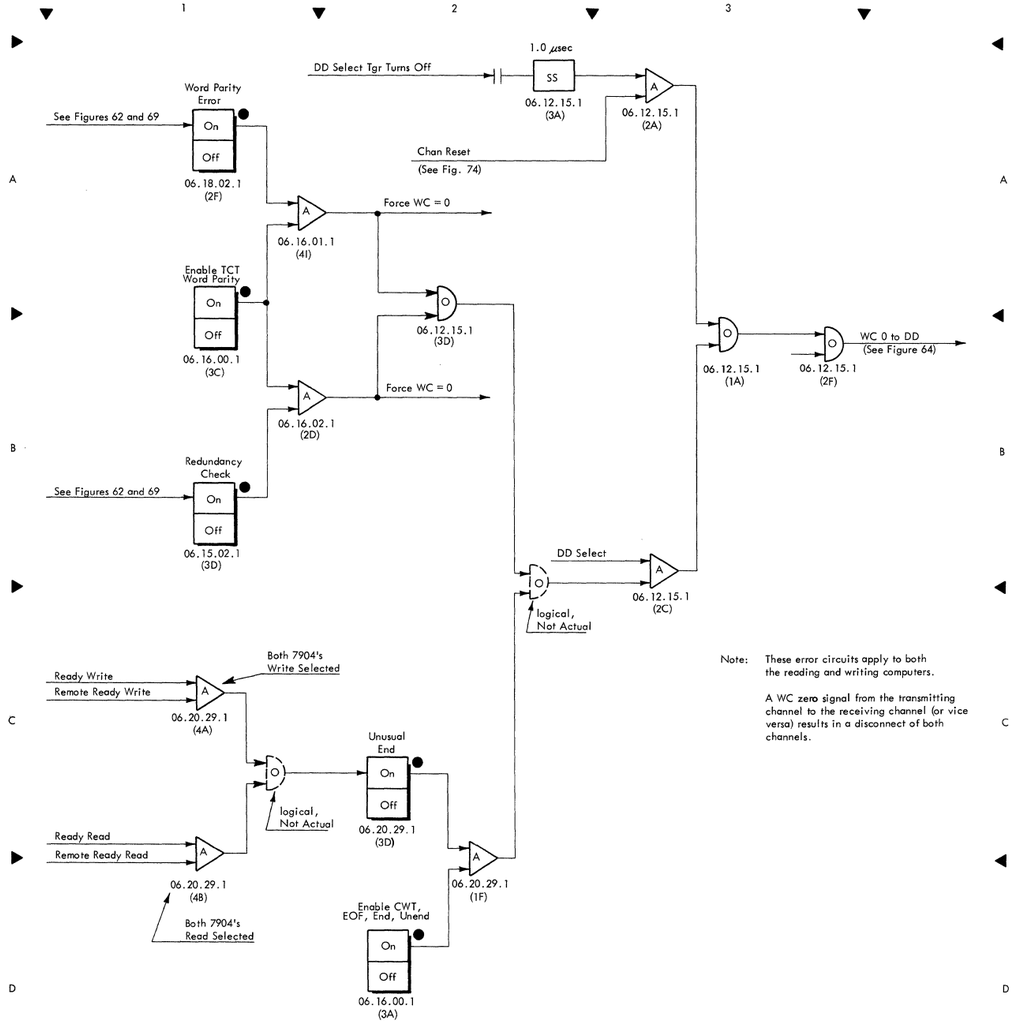


FIGURE 64. END OPERATION AND DISCONNECT, DIRECT DATA OPERATION



Note: These error circuits apply to both the reading and writing computers.

A WC zero signal from the transmitting channel to the receiving channel (or vice versa) results in a disconnect of both channels.

FIGURE 65. ERROR CONDITIONS, DIRECT DATA OPERATION

WRITE DIRECT DATA

I-O CHECK
(Turns on console I-O check light)

Caused by:

1. RCH and no WRS.

Error detection:

1. IOT instruction
   (a) If I-O check, execute next instruction.
   (b) If not I-O check, skip next instruction.

UNUSUAL END

Caused by:

1. Channel of receiving computer is write selected instead of read selected.

Error detection:

1. If enabled for unusual end trap, force WC zero to block further B cycles, send WC zero signal to receiving channel, and trap after disconnect.
2. If not enabled for unusual end trap, no data is transferred and both channels hang up.

REDUNDANCY CHECK
(Turns on console channel check light)

Caused by:

1. B cycle storage bus parity in channel of receiving computer.
   (a) Writing channel receives signal on DD redundancy error line, which turns on redundancy check tgr.

Error detection:

1. If not enabled for trap, redundancy check is tested by TRC instruction.
   (a) If redundancy check, turn off redundancy check tgr and transfer.
   (b) If not redundancy check, proceed with program.
2. If enabled for trap, force WC zero on error, send WC zero signal to receiving channel, and trap after disconnect.

WORD PARITY ERROR
(Turns on console channel check light)

Caused by:

1. B cycle storage bus parity.
   (a) Sends DD word parity error signal to channel of receiving computer, which turns on redundancy check tgr in that channel.

Error detection:

1. If enabled for word parity trap, force WC zero on error, send WC zero signal to receiving channel, and trap after disconnect.
2. If not enabled for word parity trap, but disconnect trap is enabled, store parity flag bit along with disconnect flag bit when disconnect trap is taken.

TRAPS (Taken after channel disconnects)

1. Disconnect: enabled by "Enb CWT, EOF, End, Unend" trigger.
2. Redundancy check: enabled by "Enb TCT and Word Parity" trigger.
3. Word parity: enabled by "Enb TCT and Word Parity" trigger.
4. Unusual end: enabled by "Enb CWT, EOF, End, Unend" trigger.

DD Interrupt Trap

The DD interrupt trigger may be turned on at any time by an interrupt signal (PSL instruction) from the I-O computer. The DD interrupt trigger on and enabled (Enb DD Interrupt trigger) results in a CPU DD trap.

READ DIRECT DATA

I-O CHECK
(Turns on console I-O check light)

Caused by:

1. RCH and no RDS.

Error detection:

1. IOT instruction.
   (a) If I-O check, execute next instruction.
   (b) If not I-O check, skip next instruction.

UNUSUAL END

Caused by:

1. Channel of writing computer is read selected instead of write selected.

Error detection:

1. If enabled for unusual end trap, force WC zero to block B cycles, send WC zero signal to writing channel, and trap after disconnect.
2. If not enabled for unusual end trap, no data is received and both channels hang up.

REDUNDANCY CHECK
(Turns on console channel check light)

Caused by:

1. B cycle of storage bus parity in channel of writing computer.
   (a) Receiving channel receives signal on DD redundancy error line, which turns on redundancy check tgr.

Error detection:

1. If not enabled for trap, redundancy check is tested by TRC instruction.
   (a) If redundancy check, turn off redundancy check tgr and transfer.
   (b) If not redundancy check, proceed with program.
2. If enabled for trap, force WC zero on error, send WC zero signal to writing channel, and trap after disconnect.

WORD PARITY ERROR
(Turns on console channel check light)

Caused by:

1. B cycle storage bus parity.
   (a) Sends DD word parity error signal to channel of writing computer, which turns on the redundancy check tgr in that channel.

Error detection:

1. If enabled for word parity trap, force WC zero on error, send WC zero signal to writing channel, and trap after disconnect.
2. If not enabled for word parity trap, but disconnect trap is enabled, store parity flag bit along with disconnect flag bit when disconnect trap is taken.

TRAPS (Taken after channel disconnects)

1. Disconnect: enabled by "Enb CWT, EOF, End, Unend" trigger.
2. Redundancy check: enabled by "Enb TCT and Word Parity" trigger.
3. Word parity: enabled by "Enb TCT and Word Parity" trigger.
4. Unusual end: enabled by "Enb CWT, EOF, End, Unend" trigger.

DD Interrupt Trap

The DD interrupt trigger may be turned on at any time by an interrupt signal (PSL instruction) from the I-O computer. The DD interrupt trigger on and enabled (Enb DD Interrupt trigger) results in a CPU DD trap.

FIGURE 66. ERROR AND TRAP CONDITIONS, DD OPERATION

DIRECT DATA READ OPERATION (Figures 67-70)

Words are transferred in parallel from the CDR of the writing computer's channel to the CDR of the reading computer's channel. (The writing computer is assumed to be another 7040/7044 System.) When a word is received by the reading computer:

1. The reading computer's channel requests a B cycle to store its CDR contents into memory.
2. The writing computer's channel requests a B cycle to fill its CDR with a new word from memory.

The read operation ends when either computer's CWC goes to zero.

Figure 67 shows the sequence of the direct data read operation.

Read Selecting the Channel (RDS)

The RDS instruction initiates the read operation (Figure 68). The address portion of the instruction selects channel B, C, D, or E, and selects the DD interface of that channel. The operation portion of the instruction sets up the channel for reading; that is, it conditions certain circuits in the channel that will allow reading from the I-O computer through the direct data interface. The RDS operation ends, and the program goes on with the next instruction.

Command Word Loading (RCH)

An RCH instruction for the channel just selected is executed, causing a command word to be sent from storage to the channel. The command word, when entered into the channel, sets the word counter and address counter. The RCH instruction requires an I cycle and an E cycle, after which the program proceeds with the next instruction.

See Figure 61 for channel actions caused by the RCH.

Data Transfer

The controls for transferring words from the writing computer to the reading computer are shown in Figure 63.

The writing computer's channel must have been previously write selected by a WRS instruction, and must have had its CWC and CAC set by an RCH instruction. The writing channel would then have obtained a B cycle, setting the first word to be transmitted into its CDR. The 37 outputs of the writing channel's CDR would have been immediately available at the input AND circuits of the reading channel's CDR. The data register loaded trigger on in the writing channel (word waiting in the CDR to be transmitted) causes a ready write signal to be sent to the reading computer's channel.

The RCH in the reading channel sets the CWC to some value. The CWC not zero, the data register loaded trigger off, and the ready write signal from the writing channel cause the 37 bits from the writing channel's CDR to be gated into the reading channel's CDR.

In the writing channel, ready write and the receipt of ready read indicate that the word has been taken by the reading channel, and that the writing channel may now request another B cycle to get the next word from its memory. When the reading channel gated the word into its own CDR, it also turned on its data register loaded trigger.

B Cycle

The data register loaded trigger on and the word counter not zero cause a B cycle demand to be sent to CPU (Figure 69). The next CPU cycle following the request becomes a B cycle, during which the word just received is sent from the channel's data register to storage. This action also turns off the data register loaded trigger; if the CWC is not zero, the reading channel again generates ready read. When ready write is again received from the writing channel, the next word is received into the reading channel's CDR. This process continues until the CWC of either channel (receiving or transmitting) goes to zero.

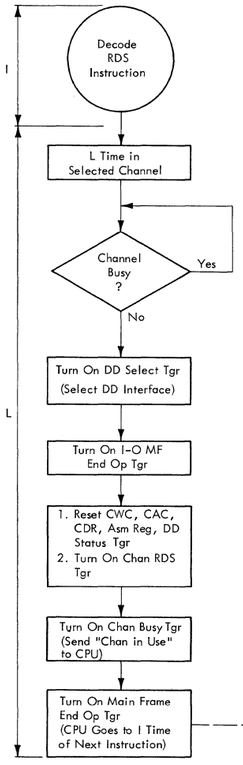
End Operation and Disconnect

When either channel's (receiving or transmitting) CWC goes to zero, it initiates the disconnect procedure that results in the disconnection of both channels. Normally, the CWC of the writing channel goes to zero before the CWC of the reading channel; this was described in the section "Direct Data Write Operation." In this current description of the reading channel disconnection, however, assume that the reading channel's CWC goes to zero first. Refer to Figure 64.

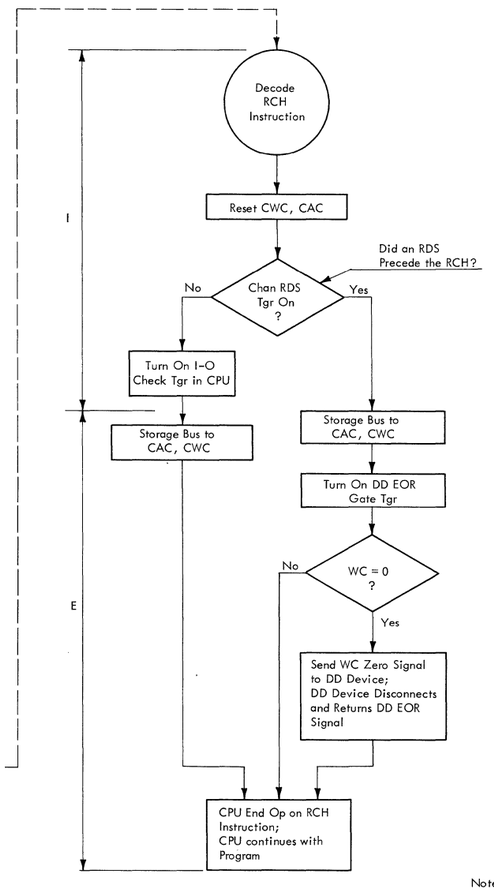
The DD EOR gate trigger in the reading channel, as in the writing channel, tests for a word count zero condition; but unlike the writing channel, the reading channel's DD EOR gate trigger is turned on during the RCH and left on during the entire read operation. Since the CWC is stepped during B cycles, any B cycle during which the CWC steps to zero becomes the last B cycle for the reading channel. A WC zero signal is sent to the writing channel, turning on that channel's disconnect call trigger. A DD EOR signal is returned to the reading channel, turning on the reading channel's disconnect call trigger.

The disconnect call triggers subsequently turn on their respective channel disconnect triggers. The channel disconnect triggers reset triggers that were maintaining the channels in their respective read and write statuses, and set up the trap sync triggers for any trap conditions that might have occurred during the DD operation. The channels are now not busy and may be used by their CPU's for another read or write.

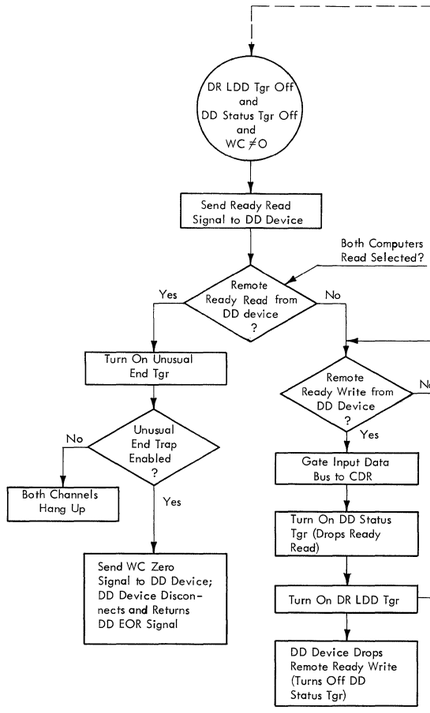
RDS
(FIGURE 68)



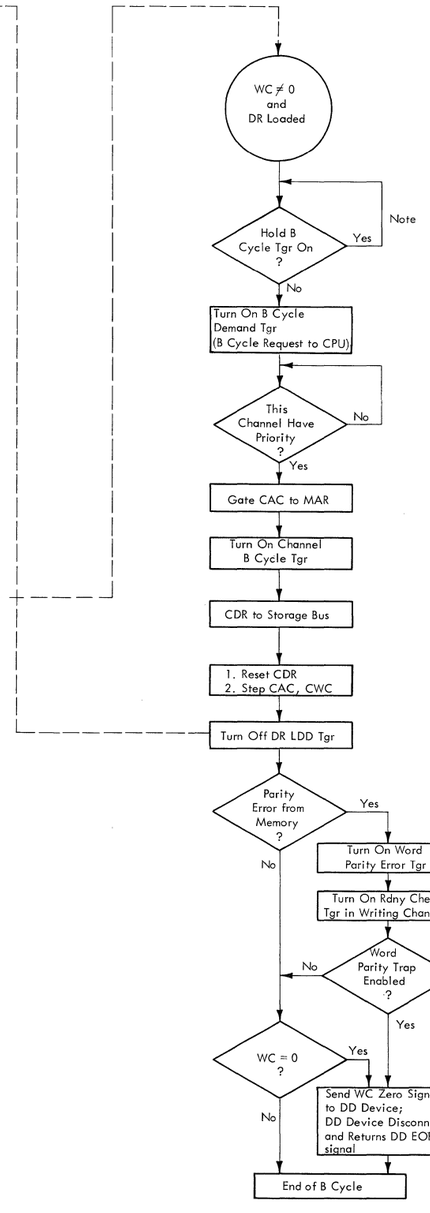
RCH
(FIGURE 61)



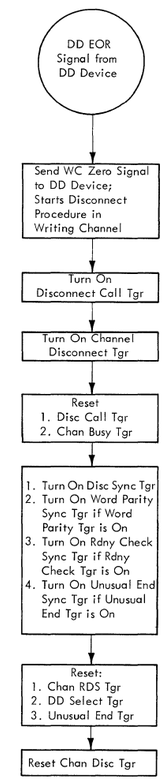
DATA READING
(FIGURE 63)



B CYCLE
(FIGURE 69)



DISCONNECT
(FIGURE 64)



Note: The Hold B Cycle Tgr turns on with the Chan B Cycle Tgr and prevents the occurrence of successive B cycles; B cycles are permitted to occur no faster than once every three CPU cycles.

FIGURE 67. DIRECT DATA READ OPERATION SEQUENCE

CPU

7904
(CHANNEL B)

Note: The DD Select and Channel Read Select triggers condition various Direct Data read functions.

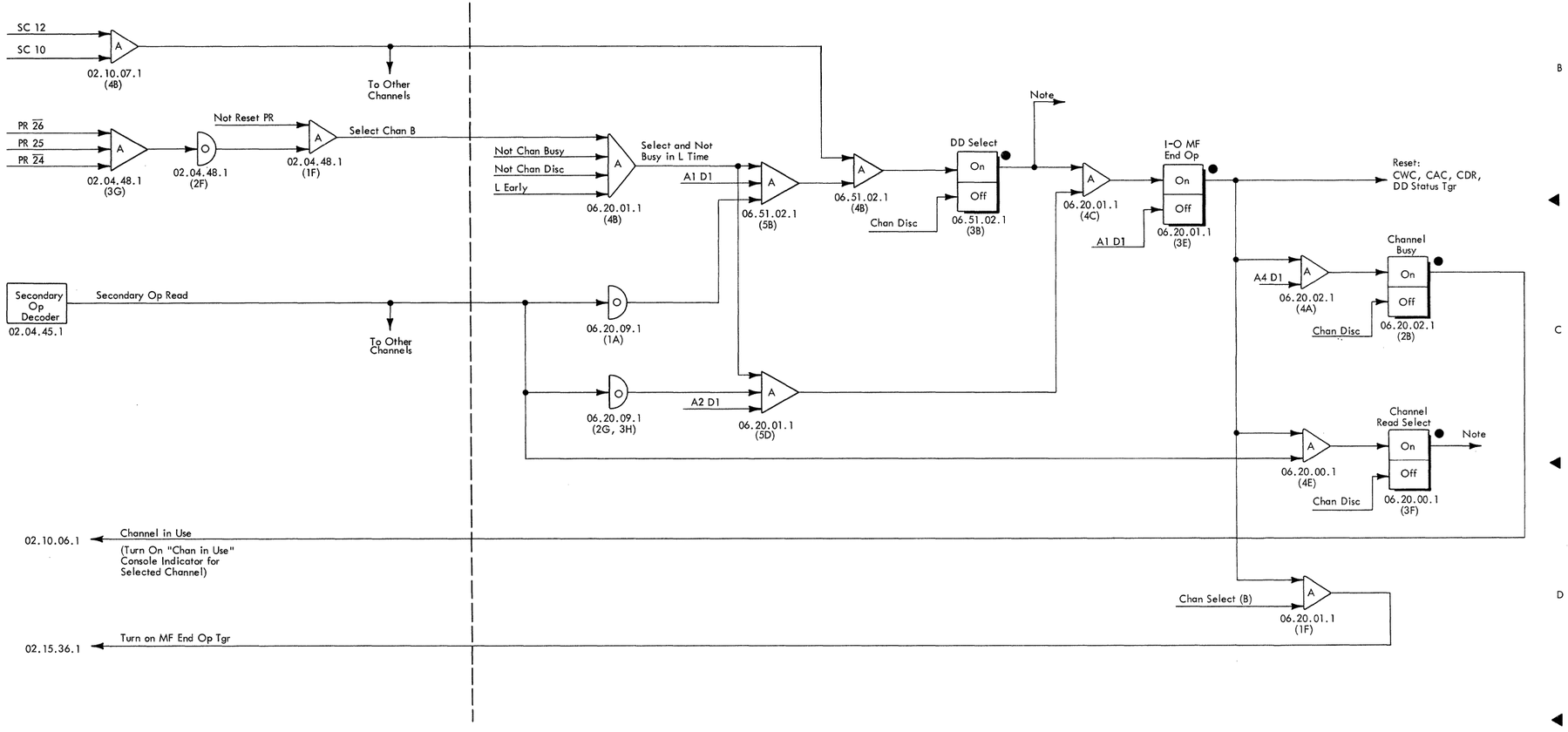


FIGURE 68. RDS, DD READ OPERATION

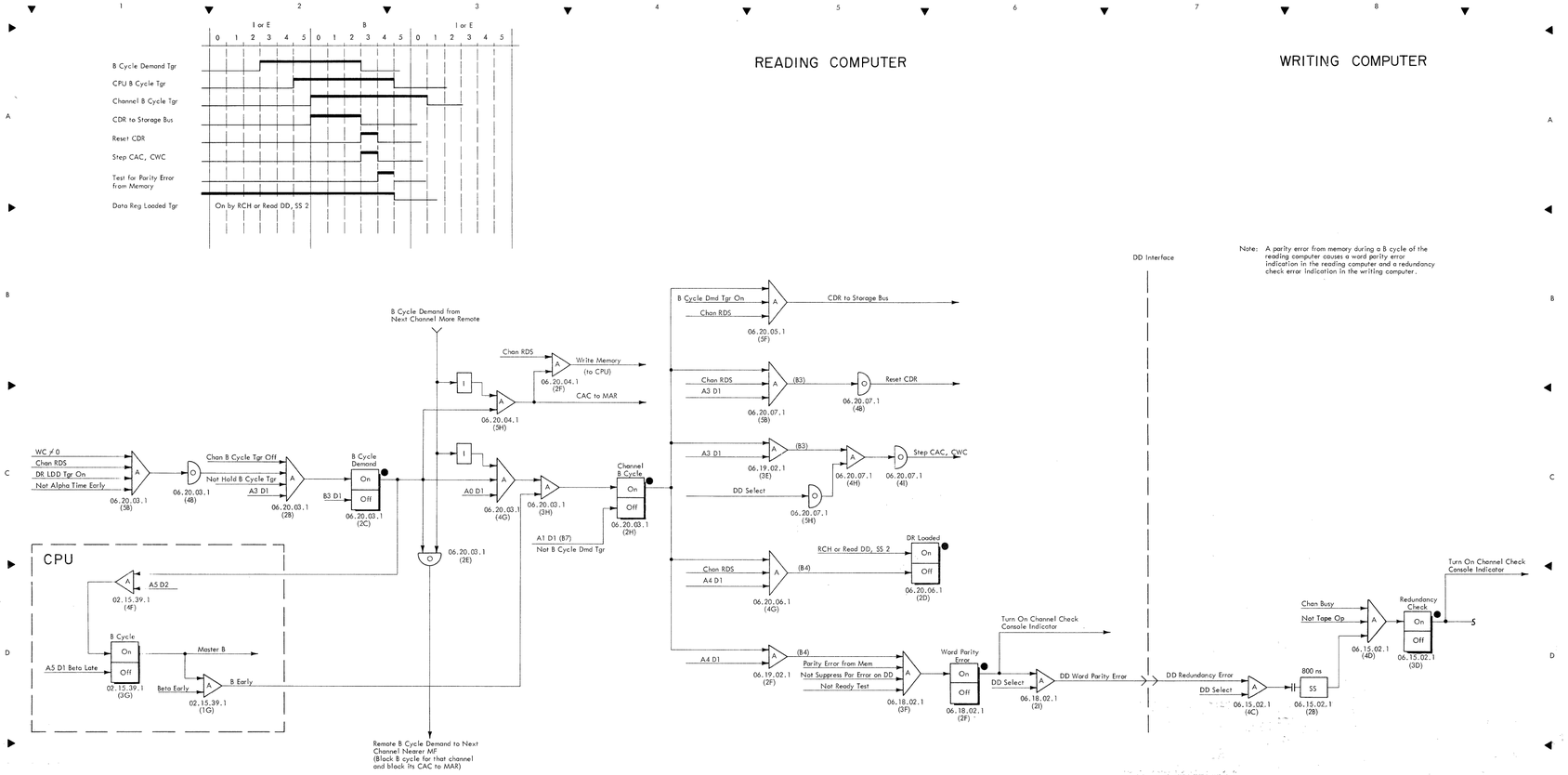


FIGURE 69. B CYCLE, DD READ OPERATION

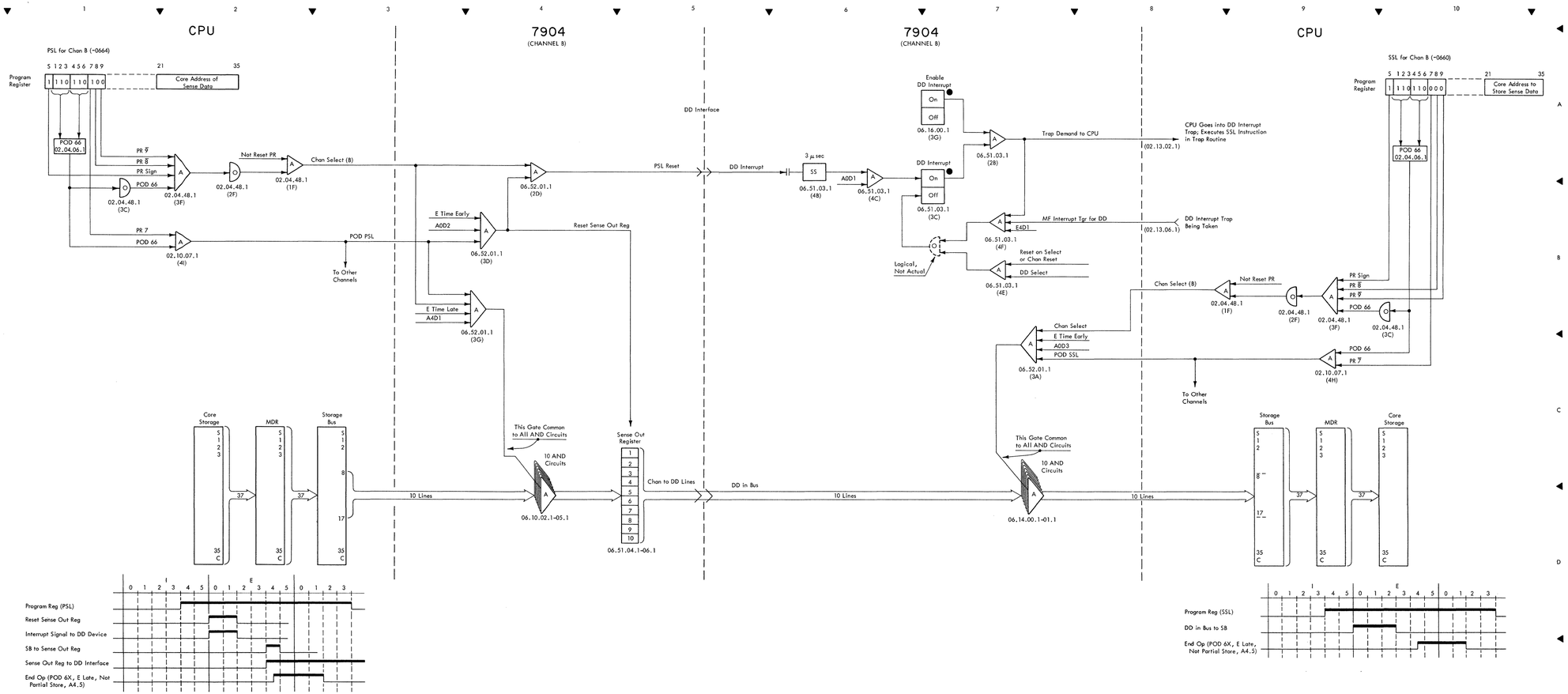


FIGURE 70. PSL AND SSL, DIRECT DATA OPERATION

DIAGNOSTIC INSTRUCTIONS AND RESETS

Figures 71 through 73 show the logic and circuits of the diagnostic instructions LDL, SDR, and SCH.

Figure 74 shows the reset logic.

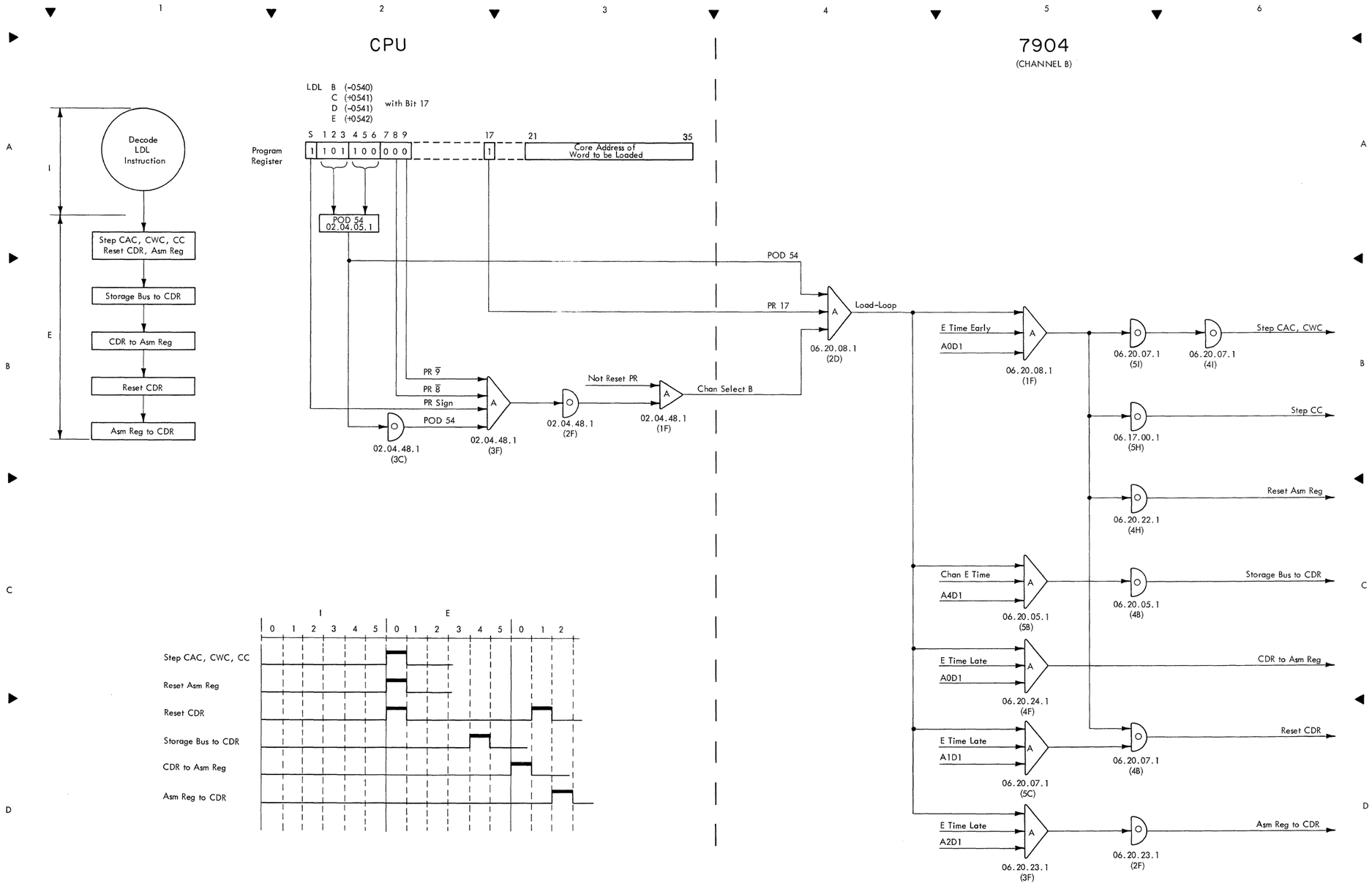
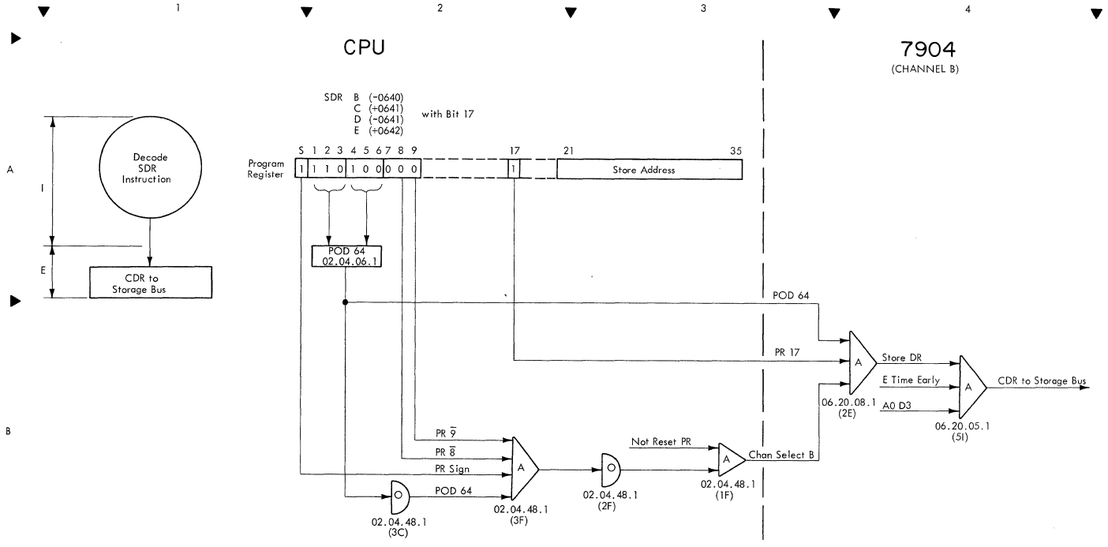


FIGURE 71. LOAD DATA REGISTER AND LOOP (LDL)



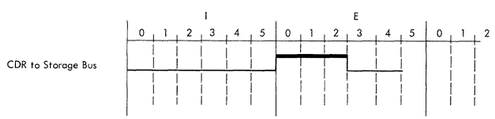
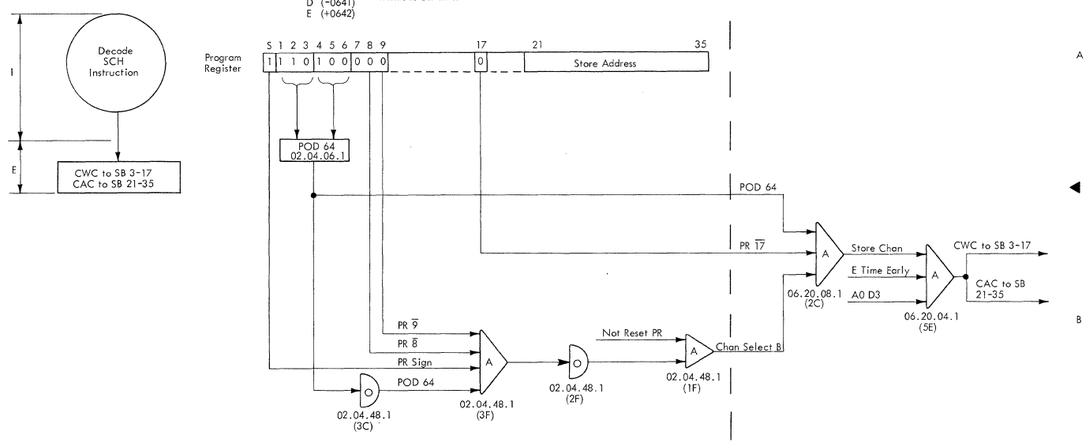


FIGURE 72. STORE DATA REGISTER (SDR)



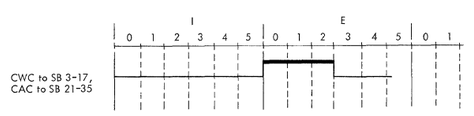


FIGURE 73. STORE CHANNEL (SCH)

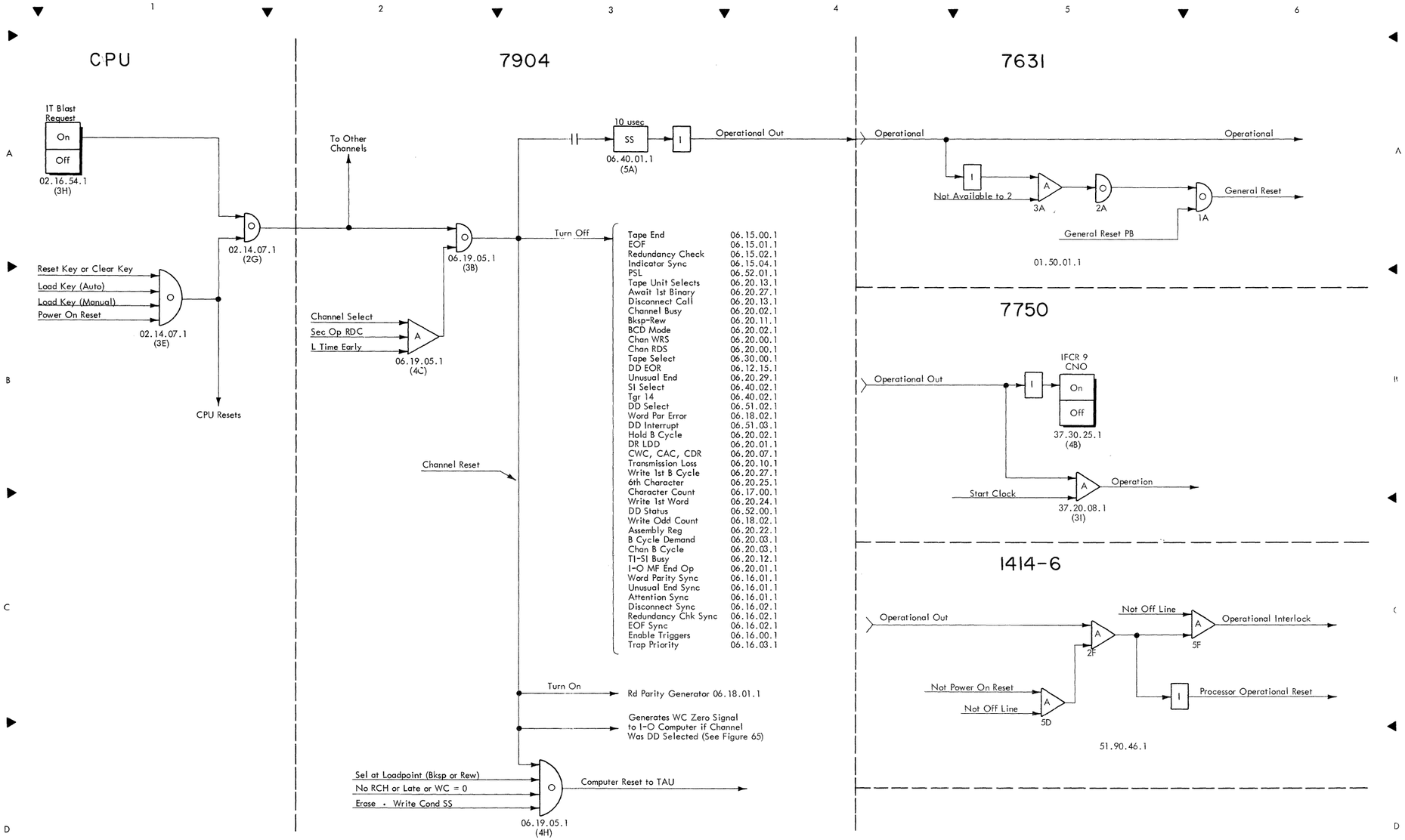


FIGURE 74. CHANNEL RESETS

COMMENT SHEET

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