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IBM System/360 Model 50

Operating Procedures

This manual describes operator procedures for an IBM 2050 Processing Unit, operating with or without an associated IBM 1052 Printer-Keyboard. The manual describes machine functions, machine procedures, program-oriented procedures, and operator-intervention procedures. In addition, an appendix of reference material and an index are included.

The reader is assumed to have a knowledge of the following SRL publications:

IBM System/360 Principles of Operation, Form A22-6821

IBM System/360 Model 50 Functional Characteristics,
Form A22-6898

IBM System/360 Basic Programming Support Operating Guide for Basic Assembler and Utilities, Form C28-6557

IBM System/360 Basic Programming Support Operating Guide,
Form C24-3391

IBM System/360 Basic Operating System Operating Guide,
Form C24-3450

IBM System/360 Operating System Operator's Guide, Form C28-6540

For information pertaining to the operation of units attachable to the System/360 Model 50, refer to the appropriate SRL publication. SRL publications that pertain to IBM System/360 and attachable units are abstracted and referenced by form number in *IBM System/360 Bibliography,* Form A22-6822.

Contents

Model 50 System Control Panel

Operational control of IBM System/360 Model 50 is centralized in the system control panel (frontispiece). The control panel contains indicators, switches, keys, and register displays for the operator's use. Mounted on the 2050 Processing Unit, the system control panel, in conjunction with the reading board (also mounted on the 2050), comprises the operator's console. The operator may monitor system operation on both the control panel and with the associated printout on the optional 1052 Printer-Keyboard from the operator's console.

The control panel is used to:

1. Turn system control on and off.
2. Reset the system.
3. Load initial program information.
4. Store, display, and alter information in storage, registers, and program status word (PSW).
5. Provide operator-to-machine communication.
6. Permit operator intervention.
7. Perform customer engineering (CE) maintenance.

Control Panel Functions

The control panel performs three general functions: operator control, operator intervention, and customer engineering control. The controls described in this section are additionally referenced in a later section, "Machine Procedures," and again, where applicable, in the section, "Program-Oriented Procedures."

Operator Control

The main functions provided by the operator controls are the control and indication of power, the indication of system status, operator-to-machine communication, and initial program loading.

Operator controls and indicators are:

NAME	PANEL	TYPE
Emergency Pull	C	Pull switch
Power On	N	Key
Power Off	N	Key
Prefix Select	N	Key switch
Load Unit	N	Rotary switch
Load	N	Key
Interrupt	N	Key
System	N	Light
Manual	N	Light
Wait	N	Light
Test	N	Light
Load	N	Light

NOTE: Operator intervention controls are described later in this section.

Keys and Switches

Emergency Pull: Pulling this switch turns off all power beyond the power-entry terminal on every unit that is part of the system or that can be switched onto the system. The switch latches in the out position and can be restored to its normal position by maintenance personnel only. When the emergency pull switch is in the out position, the power-on key is ineffective.

Power On: Pressing this key (Figure 1) initiates the power-on sequence of the system. As part of the power-on sequence, a system reset is performed in such a way that the system performs no instructions or I/O operations until explicitly directed. The contents of main storage are preserved.

The power-on key is backlighted to indicate when the power-on sequence is completed. The key is effective only when the emergency pull switch is in the normal in position.

Power Off: Pressing this key initiates the power-off sequence of the system. The contents of main storage (but not the keys in storage associated with the protection feature) are preserved, provided that the CPU is in the stopped state. The key is effective while power is on the system.

Prefix Select: This switch is used only when shared storage option is utilized (multisystem feature). The
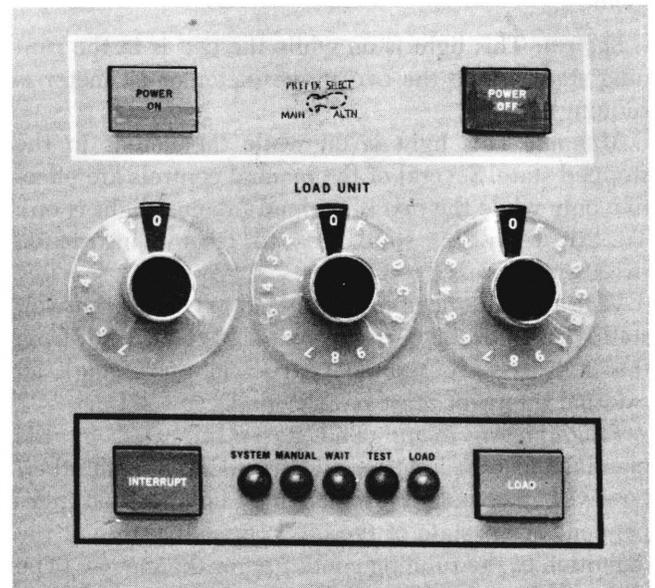

Figure 1. Section N Panel

switch provides the choice between main and alternate prefix during manually initiated initial program load (IPL). The setting of the switch determines the state of the prefix circuit following the system reset after the load key is pressed. The alternate-prefix light (in top row of lights, Panel L) is on when the prefix select switch is in the ALTN position.

Load Unit: Three rotary switches provide the 11 rightmost I/O address bits used for IPL.

The leftmost rotary switch has eight positions labeled 0-7 that are used for the channel address. The middle 16-position rotary switch is labeled with the hexadecimal characters 0-9, A-F for the control unit address. The third switch has 16 positions, and is used for the unit address. (Actual IPL does not commence until the load key is pressed.) These switches may be set without disturbing CPU operation.

Load: Pressing this key starts IPL. The key is effective while power is on the system. The loading is from the I/O unit specified in the three load unit switches. Pressing the load key causes execution of the system reset internal diagnostic sequence, then loads the first 24 bytes of information from the load unit into the first 24 bytes of main storage. (This key is normally used while the CPU is in the stopped state.)

Interrupt: Pressing this key requests an external interruption. The interruption is taken when not masked, and when the CPU is not stopped. Otherwise, the interruption request remains pending. Bit 25 in the interruption-code portion of the current PSW is made 1 to indicate that the interrupt key is the source of the external interruption. The key is effective while power is on the system.

Lights

System: This light is on while the CPU is in the running state (while the CPU usage meter or CE meter is running).

Manual: This light is on while the CPU is in the stopped state. Several of the manual controls are effective only while the CPU is stopped (manual light is on). To exit from this state (i.e., to resume instruction processing), press the start key.

Wait: This light is on while the CPU is in the wait state. (Bit 14 of the current PSW equals 1.) To exit from this state (i.e., to resume instruction processing), an external interrupt must be provided.

Programming Note: The states indicated by the manual and wait lights are independent of each other; however, the state of the system light is not independent of the state of these two lights because of the definition of the running condition for the meters. (The system light is the meter light.) The possible conditions when power is on are:

SYSTEM LIGHT	MANUAL LIGHT	WAIT LIGHT	CPU STATE	I/O STATE
off	off	off	*	*
off	off	on	Wait	Not Working
off	on	off	Stopped	Not Working
off	on	on	Stopped, wait	Not Working
on	off	off	Running	Undetermined
on	off	on	Wait	Working
on	on	off	Stopped	Working
on	on	on	Stopped, wait	Working

* Abnormal condition.

Test: This light is on when a manual control is not in its normal position or when a maintenance function is being performed for CPU, channels, or storage. The normal position for rotary switches is straight up, and for key switches is straight out.

The test switches described are shown in Figures 2, 3, and 4. These switches cause the test lights to be on if any are not in their normal position:

SWITCHES	PANEL
Rate switch not to PROCESS	M
Check Control switch not to PROCESS	M
FLT CONTROL switch not to PROCESS	M
FLT Mode key switch not to OFF	M
Lamp Test switch not straight out	M
Disable Interval Timer key switch not straight out	M
Address Compare (SAR) key switch to STOP	M
Repeat Insn (IAR or ROS) key switch not straight out	M
Address Compare (IAR) key switch not to PROCESS	M
Address Compare (ROS) key switch not to SYNC	M
Rev Data Pty key switch not straight out	L
Storage Test switch not to PROCESS	B
Invert SAR Bit 16 key switch not straight out	B
Manual Op key switch not straight out	F
Meter switch in CE position	M

Load: This light is on during IPL; it is turned on when the load key is pressed, and is turned off after the IPL operation and the loading of the new PSW are completed successfully.

Operator Intervention

Sections L and M of the system control panel contain the controls required for the operator to intervene in normal programmed operation. Operator intervention controls provide the system reset and the store and display functions.

Intervention controls and indicators are (keys have momentary pushbutton action):

NAME	PANEL	TYPE
System Reset	M	Key
PSW Restart	M	Key
Check Reset	M	Key
Set IC	M	Key
Store	M	Key
Display	M	Key
Stop	M	Key
Start	M	Key
Log-Out	M	Key
Rate	M	Rotary switch
Check Control	M	Rotary switch
Address Compare (IAR)	M	Key switch
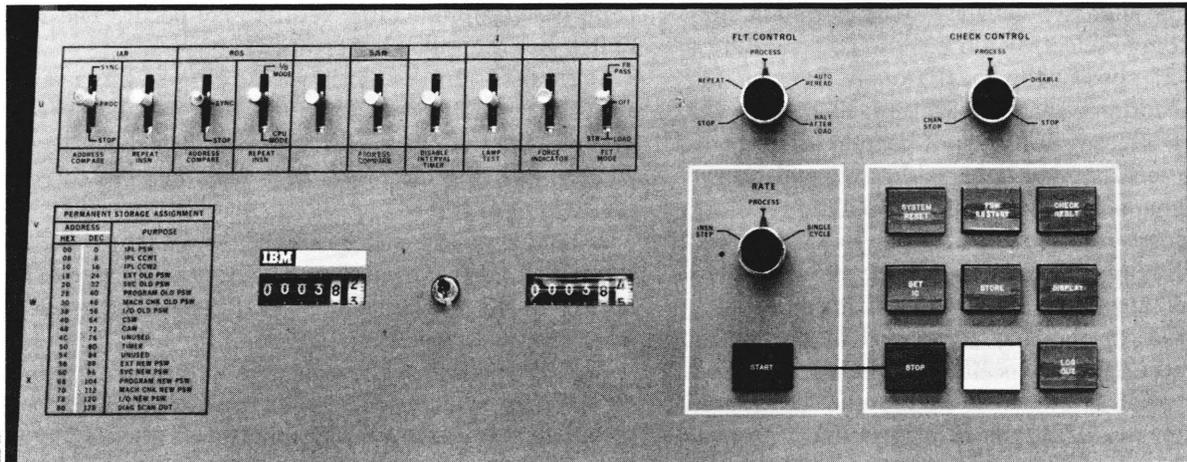
Figure 2. Section M Panel

Figure 3. Section B Panel

Figure 4. Section F Panel

NAME	PANEL	TYPE
Address Compare (SAR)	M	Key switch
Storage Select	L	Rotary switch
Address	L	Key switches
Data	L	Key switches

NOTE: Operator controls are listed in a previous table.
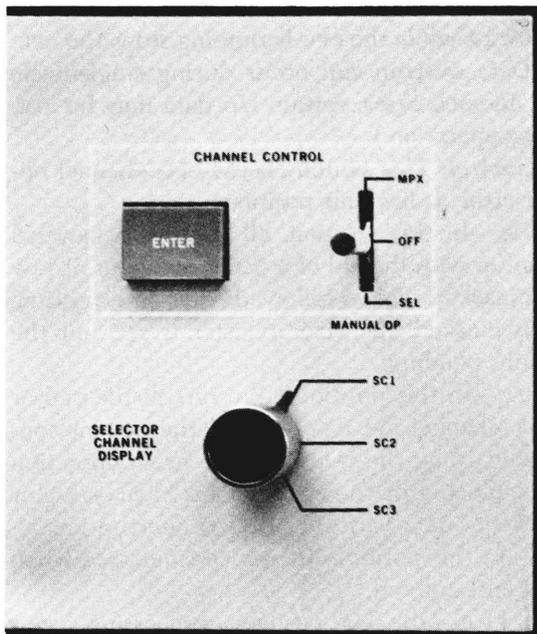
System Reset: This key resets the channels and control units, and places the CPU in the stopped state; all pending interruptions are eliminated, and all error indicators are reset. The instruction address register is set to zero. The key is effective while power is on the system. (The reset function does not affect any off-line or shared device.) It is recommended to press the stop key before pressing system reset key.

PSW Restart: This key causes a system reset, after which a PSW is loaded from the double word starting at storage location 0 and the CPU is changed from stopped to operating state.

Check Reset: This key resets all CPU and channel check indicators (including some master checks) to the no-error state. Check reset is forced by CPU reset or system reset. It is active in all modes. Check lights remaining on after check reset must be cleared at the check source by use of appropriate manual controls.

Set IC: This key takes the address set in the address switches and enters it into the instruction counter portion of the active PSW. The key is effective only while the CPU is in the stopped state.

Store: This key is pressed to store information in the location specified by the storage select and address switches. Correct parity is automatically generated. Storage protection is ignored. The key is effective only while the CPU is in the stopped state. The contents of the data key switches are placed in specified locations in main storage, general registers, or floating-point registers.

If the storage select switch is set to MAIN, the entire contents of the data switches are stored in main storage. If the storage select switch is set to LOCAL, address switches 24-27 specify the local storage location address, while address switches 22 and 23 specify the local storage sector. Sector specification determines whether the local storage area addressed will be the multiplexor channel, working storage, general registers, or floating-point registers. When the location designated by the address switches and storage select switch is not available, data are not stored.

Display: The display key is pressed to display information in the location specified by the storage select switch and address switches. When the designated location is not available, the displayed information is unpredictable. The key is effective only while the CPU is in the stopped state, and while power is on the system.

If the storage select switch is set to MAIN, the data in main storage at the location specified are displayed in the storage data register. If set to LOCAL, the data in the local storage are displayed in the L register. If the storage select switch is set to MPX, the data specified are displayed in the SDR. If set to PROTECT, the data specified are displayed in the F register.

Stop: The stop key causes the CPU to enter the stopped state and turns on the manual light. The CPU completes the instruction being executed at the time the stop signal is recognized. All pending interruptions that are not masked are taken and any I/O operation in progress is completed.

Pressing the stop key has no effect when a continuous string of interruptions is performed or when the CPU is unable to complete an instruction because of machine malfunction.

Start: The start key is pressed to start instruction execution as specified by the rate switch. The key is effective only while the CPU is in the stopped state.

Pressing the start key after a normal stop causes instruction processing to continue as if no stop had occurred, provided that the rate switch is set to PROCESS or INSN STEP. If the start key is pressed after the system reset without first introducing a new instruction address, the results are unpredictable.

Log-Out: This key provides a means of logging the machine status into storage. Pressing the key causes the CPU and channel status to be stored in fixed locations in main storage. The log-out area occupies 44 words (176 bytes) of main storage, starting at byte 128. The log-out action is the same as that performed by programming when an error is detected. This key is operative only while the CPU is in the stopped state.

Rate: This three-position rotary switch is used to indicate the manner in which instructions are to be performed. The position of the switch should be changed only while the CPU is in the stopped state. Otherwise, unpredictable results may occur. The rate switch has the following settings:

1. PROCESS—In this position, the system starts operating at normal speed when the start key is pressed. The test light is on when the rate switch is not set to PROCESS. Moving the rate switch from PROCESS to INSN STEP stops the CPU.

2. INSN STEP—In this position, the system executes one instruction for each depression of the start key and returns to the stopped state. The timer is not updated when the switch is in this position.

Any instruction can be executed with the rate switch set to INSN STEP. Input/output operations are completed to the interruption point. While the CPU is in the wait state, no instruction is performed, but pending interruptions, not masked, are taken before the CPU returns to the stopped state. Initial program loading is completed with the loading of the new PSW before any instruction is performed.

3. SINGLE CYCLE—The system executes one machine cycle for each depression of the start key and returns to the stopped state. The stopped state for single cycle is one in which no CPU clocks are running. Otherwise, in the normal stopped state, the read only storage (ROS) is running, executing a halt loop.

Single cycle operates with I/O equipment to the point of the initiation of the asynchronous operation. The asynchronous operation starts with the next depression of the start key and runs to completion. If start is pressed during this time, the next cycle is taken. If an interruption results, the interruption sequence is not automatically executed but must be single cycled. Moving the rate switch from PROCESS to SINGLE CYCLE while the CPU is running stops the CPU.

NOTE: Data overrun can occur during single-cycle operation. In such cases, certain I/O data may be lost. (This is a CE operation.)

Check Control: This switch checks CPU/channel operation for error. It has four positions:

1. PROCESS—In this position, all errors are handled by the monitor with the aid of a general log-out, if PSW bit 13 is unmasked. This is followed by an interruption. If bit 13 is masked, the error register is set, but the error remains pending.

2. DISABLE—In this position, all errors in the CPU or multiplexor channel are ignored and the system continues, disregarding the error. The program operation can still be affected by the error. Errors in the selector channel (except data parity) cause I/O interruption.

3. STOP—In this position, the processing stops when an error is encountered.

4. CHAN STOP—In this position, processing stops when an error other than incorrect length indication (ILI) is encountered.

NOTE: Under normal circumstances, the system is run with the check control switch in the process position. At any other setting, this switch causes the test light to go on.

Address Compare (IAR): This switch provides a means of stopping the CPU on a successful instruction address comparison.

1. When set to STOP, an equal comparison between the address switches and the IAR causes the CPU to stop. The stop occurs at completion of the addressed instruction. (Comparison includes only the part of the instruction address that addresses the physical word size of storage.)

2. When set to PROCESS, no comparison occurs.

3. SYNC is for CE use.

The address compare switch can be manipulated without disrupting CPU operation other than causing the address-comparison stop. When this switch is set to any position except normal (straight out) the test light is on.

Address Compare (SAR): The storage address register compare switch provides a means of stopping the CPU on a successful data (not IAR) address comparison.

1. When set to STOP, an equal comparison between data switches 8-31 (low-order 24 positions) and a storage address may be used either to locate data or as a successful status-switching address. Either comparison causes the CPU to stop at the completion of the instruction containing the address. Data switches 0 and 1 (byte 0) may be set to effect the stop when the storage reference is made by either the CPU, the channels, or by both.

2. When set to SYNC, no stop occurs.

3. The address compare (SAR) switch can be manipulated without disrupting CPU operation other than causing the address-comparison stop. When this switch is set to STOP, the test light goes on.

The address compare (SAR) switch is normally left set to SYNC.

The following operator intervention controls are located on Panel L in Figure 5.

Storage Select: This four-position rotary switch is used to select the main storage area addressed by the address switches. The storage select switch is active only in the stopped state. The switch can be changed without disrupting CPU operations. The storage select switch has the following settings:

1. MAIN—Selects a main storage location specified by the address switches. The data are then displayed in the storage address register.

2. LOCAL—Selects a local storage location specified by the address switches. The data are then displayed in the L register.

3. PROTECT—Unconditionally selects the storage protect key register (used by the CE).

4. MPX—To select multiplexor (used by the CE).

When addressing general or floating-point registers, working storage, and the multiplexor, the sector addresses must be computed in conjunction with data posted on Panel J. (Addresses given in this manual already include this computation.) When storage select is switched to LOCAL, in conjunction with "Local Storage Procedures," the sector addresses are specifically stated. The storage select switch may be left on at any setting.

Address: The address switches on the instruction address register panel provide a means of manually selecting an addressable location in storage when used in conjunction with the storage select switch, or to identify the address to be compared when an address-comparison stop is desired. Correct parity is automatically generated. The switches can be manipulated without disrupting CPU operation. The 24 switches are arranged in hexadecimal groups, numbered like the data switches above them.

For main storage select, the address switches are used to manually address a main storage location when the storage select switch is set to MAIN. For an address-comparison stop, the address switches provide the stop address. When addressing main storage, the 24 switches represent a 24-bit binary address. The rightmost switch is the units position or low-order position. Because data in main storage is stored or displayed a word at a time, the two low-order position address switches (switch positions 30 and 31) are not involved in determining the address.

When an address switch is in the down position, it represents a 1 bit. Color coding is provided to identify the hexadecimal digit groupings. If the address switches are manipulated while address compare (IAR) is set to STOP, a machine check can occur.

The lights directly above the switches indicate the address selected. Three lights have a P below, indicating parity of the associated byte. Bytes identified are bits 8-15, 16-23, and 24-31.

Data: The 32 data switches on the storage data register panel are arranged in hexadecimal groups. The switches specify the data to be stored in the location indicated by the storage select switch and address switches. Correct data parity is automatically generated. Changing the switches does not affect CPU operation.

The data switches can be used to represent a full physical storage word of information. A data switch in the down position represents a 1 bit and in the center (restored) position, a 0 bit. The lights directly above the switches indicate the information being displayed or stored. Certain lights have a P below, indicating parity of the associated byte. Bytes identified are bits 0-7, 8-15, 16-23, and 24-31.
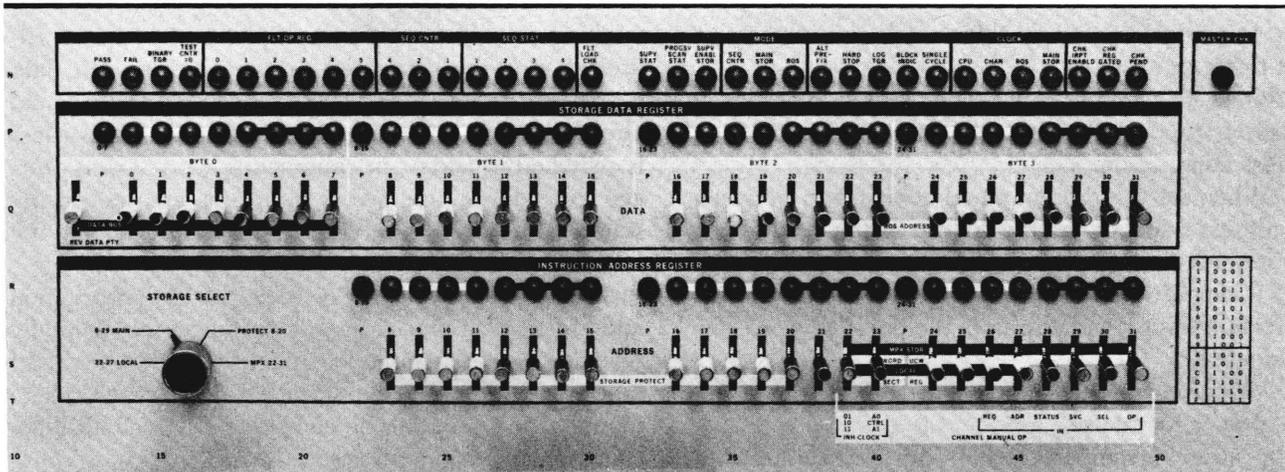
Figure 5. Section L Panel

Master Check

This indicator light turns on to indicate that a machine error has been detected. Press the check reset key to turn the indicator light off. (The error is not corrected by the check reset key.)

Customer Engineering (CE) Control

All other keys, switches, and controls not described in this manual are principally for customer engineering use. The usage meter and CE meter are on Panel M. A key switch controls the meter to be run when the machine is in process. When power is on and the key switch is in the customer operation position, the usage meter accumulates time (while the system light is on). If the key switch is in the customer engineer position, the test light is on, and the CE meter accumulates time while the system light is on.

Status Indicators (Rollers)

The status indicators on Panel G (Frontispiece) provide a display of CPU and channel status. The 144 indicators are arranged in four rows, 36 to a row. Each row is separated in the center, with 18 lights in the left half and 18 in the right half.

Eight different status words can be displayed in each row of indicators. The desired word is selected with an eight-position roller select switch (Panel K). The switch also positions a roller format to identify the information displayed. The significance of each switch position is identified by the label on the face of the panel by the related roller positioning switch (Figure 6).

Roller select switches display (detailed description of bit meanings in these displays is given in Appendix E):

ROLLER SWITCH	POSITION	
1	1	Common channel: I/O instruction
1	2	Common channel: I/O routine
1	3	Common channel: control registers, buffers
1	4	Multiplexor channel: data buffers
1	5	Multiplexor channel: interface and control
1	6	Multiplexor channel: control triggers
2	1	Selector channel: B register
2	2	Selector channel: C register
2	3	Selector channel: byte counter, miscellaneous registers, and channel checks
2	4	Selector channel: position, control, and request registers
2	5	Selector channel: A clock and control registers
2	6	Selector channel: general purpose and flag registers, and MP latches
3	1	CPU: L register (local storage, first half of current PSW)
3	2	CPU: R register
3	3	CPU: M register
3	4	CPU: H register
3	5	CPU: SAR, byte stats, and byte store stats
3	6	CPU: ROS (group #3, 56-89)
4	1	CPU: ROS (group #1, 0-30)
4	2	CPU: ROS (group #2, 31-55)
4	3	CPU: ROAR, external interrupt register, and stats (first byte of second word in current PSW)
4	4	CPU: byte counters, F register, edit and GP stats, and storage ring (storage protection key)
4	5	CPU: LSAR, J register, MD, G1, and G2
4	6	CPU: error register
4	7	CPU: current ROS address
4	8	CPU: previous ROS address

1052 Printer-Keyboard

In conjunction with the operator's console, the operator exercises control of the 1052 Printer-Keyboard. For detailed description of the 1052, see *IBM 1052 Printer-Keyboard Model 7*, Form A22-6877. The 1052

COMMON CHANNEL

1	I/O INSTRUCTION
2	I/O ROUTINE
3	CONTROL REGISTERS

MULTIPLEX CHANNEL

4	DATA BUFFERS
5	INTERFACE & CONTROL
6	CONTROL TRIGGERS
7	
8	

SELECTOR CHANNEL

1	B REGISTER
2	C REGISTER
3	BYTE CNTR. CHECKS
4	POS & REQ REGS. CC
5	A CLOCK. SP REG
6	GP & FLAG REGS. MP
7	
8	

CPU 1

1	L REGISTER
2	R REGISTER
3	M REGISTER
4	H REGISTER
5	SAR
6	ROS 56-89
7	
8	

CPU 2

1	ROS 0-30
2	ROS 31-55, MOVER FUNC
3	EXT IRPT. ROAR, STATS
4	BYTE CNTR . F REG . GP STATS
5	LSAR, J REG. MD, G1, G2
6	CHECKS
7	PM, ILC
8	

Figure 6. Section K Panel

is powered by the operator's console. Operation of the 1052 involves:

Ready: Pressing this key causes the 1052 to become ready. If the 1052 is in the not ready condition, this key overrides the condition and makes the 1052 ready if these conditions allow: not out of forms, not busy, and not in initial select sequence (from channel). The 1052 must be in the ready condition to perform read and write operations.

Request: This key is pressed (after the ready key) to initiate operator communication via the 1052. This key prohibits read/write operations until the system accepts the request.

Attn: This light, when on, indicates that the request is pending (the system hasn't accepted it yet).

Procd: The system has accepted the operator's request and the keyboard is unlocked.

Intvtn Reqd: The 1052 is not ready; operator intervention is required. (Example: lack of sufficient paper causes this light to go on when the keyboard is addressed by the system.)

Peripheral Equipment

The Model 50 has peripheral equipment (at least i/o devices) that may be under the operator's control. A customer's manual that describes the operation of each unit of peripheral equipment used in the system is available. Execution of the operator-information discussed in the pertinent manual is the operator's responsibility. Titles of the manuals and their form numbers may be found in *IBM System/360 Bibliography,* Form A22-6822. A partial list of peripheral i/o devices, with brief descriptions, is given in Appendix F.

Language Conventions Used in this Manual

1. When a letter or digit is used in the text, without modifier, conventional (plain English) alphameric value is implied; for example, addresses must end in 0, 4, or 8 for proper boundary byte locations. Up to this point in the manual this has been the only meaning for any letter or number in the text. (Exception: When 0 or 1 is used, it is the same in all number systems.)

2. When a digital value is followed by "hex" in parentheses, the decimal number has been converted to its hexadecimal equivalent, and is presented in the text, requiring only coding into bits for use by the machine; for example, caw location is 48 (hex). In this example, decimal location 72 has already been translated to 48 (hex) for use in the text. To enter location 48 (hex) into the address switches, the last (low-order) switches will code: 0100 1000. (See hexadecimal to decimal conversion table in "Appendix B.")

3. Low-order refers to "right-hand" end of the word, or byte.

4. To read hexadecimal (language used by the operator's console) picture the 8-bit byte
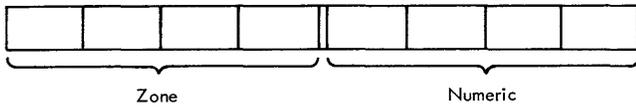
Zone   Numeric

divided into first half (zone portion) and second half (numeric portion). In all practical operator applications the zone portion will be all l's (F, in hex), representing the sign "positive," because the numerical values in operator communication are all positive. The numeric portion can be pictured in two parts, each part comprising a hex digit. Thus: 1111 0001 = (effective decimal) 1. Similarly, 1111 0011 = (effective decimal) 3.

5. Main storage refers to contiguous storage locations 0000 to the highest location (bytes) provided by the system. (Physical location of main storage is in the processor cabinet; additional main storage may be provided by auxiliary storage.) Local storage includes general and floating-point registers, channel registers, and "scratch pad" storage. Terms such as *memory* and *core* are obsolete insofar as this manual is concerned. Direct access replaces the obsolete term random access.

6. In describing the use of console switches, reference has been made to possible interference with cpu, if switch adjustments are made while cpu is in operation. A recommended practice is to stop the cpu before making any console switch adjustment.

7. The reader is urged to make use of the complete index provided in this document. All significant subjects and terms are referenced and cross-referenced.

This section describes specific machine procedures performed by the operator. (Operator procedures involving programs or the operating system are described in the next section.)

Operator's Machine Responsibility

The operator is responsible for turning on the system (if the power has been off), initializing the system (manual IPL procedures in conjunction with the appropriate operating system), entering into the system programs prepared by programmers, maintaining a running log of jobs, communicating with the system (through console indicators and printer-keyboard), making operator adjustments as required (to console and peripheral equipment), certain operator trouble-correction procedures, and turning off the system, as required. The operator notifies the CE when equipment trouble occurs in the system. See Appendix F for i/o operation, where typical i/o devices are briefly described.

Emergency Pull Switch

This switch (described previously under "Keys and Switches") is to be pulled out by the operator in *true emergency* only. For this purpose, a true emergency is defined as a system fire, or in any extreme case where real danger threatens personnel. Once pulled out, the switch locks, and can be reset only by the CE; therefore, notify him immediately. (Thermal overloads may also drop system power. If system power cannot be maintained, notify the CE.)

Turning On the System

1. Before turning on the system, check all peripheral units externally. Check that doors are properly closed, feeds not impeded, paper/card supply is sufficient. If any i/o units have been removed from powering sequence, it may be necessary to jumper their plugs.
CAUTION:
Do not operate any switches unless necessary.
2. Press power on key. This initiates a power-on sequence automatically. At the completion of the sequence, the backlighted power on key lights up. (Should this fail to occur, check emergency pull

switch to make certain it is all the way in.) Check sequence power plugs for i/o units. If these checks and operator check of the primary power source fail to disclose difficulty, call the CE. (The system light and other state lights may go on, depending on the state of the system at previous power turn off.) If the test light is on, check the position of the test switches as described under "Test." Restore the switches as required to turn the test light off. If the master check light is on, press the check reset key. The master check light should go off.
3. Turn on the power for shared/peripheral equipment not directly connected in the power-on sequence.

Turning Off the System

If manual light is not on, press the stop key. Manual light goes on.
1. Check all tape drives. Put them in an unload state; press reset, load rewind, and then the unload keys on each tape drive.
2. Check all disk drives. Put them in unload state by pressing start/stop key if they are running.
3. Press power off key. Power is removed automatically in an ordered sequence. The power on light goes out.
4. Continue power-off procedures for shared/peripheral equipment not connected to the powering sequence.

Program Loading

Programs can be initially loaded into the system by the manual IPL procedure or by loader programs. Manual IPL is an automatic technique of loading, performed by the operator and the system microprogram; it can load any program into main storage. Because manual IPL is a prime prerequisite for loading any program (loader, control, or problem) into storage, it is described in detail.

Manual IPL

The procedure to be followed after a power-on sequence following a shutoff of electrical power, after malfunctions that necessitate reloading the resident portion of the operating system into main storage, or for initial loading of any program is:

1. Place the appropriate program on the desired i/o device.

2. Make the i/o device ready.

3. Select the desired i/o device with the three load unit switches.

4. Press load key. The manual/wait light goes off, the load light turns on and system reset occurs. The first 24 bytes of information are loaded from the selected device into locations 0-23 of main storage. Depending on data content the exact procedure from this point varies. A typical illustration follows:

The IPL PSW is in locations 0-7, with two CCW's following in locations 8-23. Control of the system is passed to the channel, which obtains the first CCW (location 8) and uses it to continue reading from the input unit, placing the data in storage. When the input operation is completed, the IPL PSW is loaded into the CPU registers. When this PSW is successfully loaded, the load light turns off. If either the reading operation or the PSW loading is unsuccessful, the CPU idles, and the load light remains on. Under certain conditions, the IPL PSW may specify a wait state, in which case the load light turns off and the wait light goes on. (In this case, the operator provides the setup change required, and returns the system to running state by pressing the interrupt key.) When the current PSW specifies a running state, the loaded program is executed, beginning at the location specified at the current PSW (which may be the IPL PSW if it originally specified running state).

NOTE: If, at the beginning of a job, any individual device cannot be readied, press the system reset key. This resets all unusual conditions; however, if a job is already being run, information already on the channels or interface units will be lost. (Because this manual IPL procedure executes the same internal diagnostic sequence and reset functions that the system reset key performs, that key need not be pressed before manual IPL.)

Setting the Storage Protect Key

To change the protection information associated with a given block of storage (in blocks of 2,048 bytes):

1. Press stop key. Manual light goes on.

2. Set storage select switch to PROTECT.

3. Press display key.

4. Rotate roller 4 to position 4. The F register displays the old storage protect key.

5. Set address switches 12-19 for change of key.

6. Set new storage protect key data in data switches 24-27.

7. Press store key. The storage protect key has now been reset. The F register now displays the new storage protect key.

8. To resume processing, press start key. Manual light goes off.

Clear Storage Procedure

Under normal operating-system type operation, it is unnecessary to clear storage, because the operating system provides the function as required. For certain testing operations, however, it may be desirable to clear storage. The following procedure clears all main storage, but does not alter the contents of general purpose or floating-point registers:

1. Press system reset key. Manual light goes on.

2. Set rate switch to SINGLE CYCLE. Test light goes on.

3. Set IC to zero (by setting address switches to zero, then pressing set IC key).

4. Set data switches to 0200. (Data switch 22 down, all others remain straight out.)

5. Set repeat insn (ROS) switch in down position.

6. Press start key.

7. Restore repeat insn (ROS) switch to straight out position.

8. Restore data switches straight out.

9. Set rate switch to PROCESS. Test light goes out.

10. Press start key. All main storage (except registers) is now cleared.

11. Press system reset key. Manual light goes on.

12. Press store key.

Instruction Stepping

One method that is used to debug a program is to process one instruction at a time, service all interrupts, and stop:

1. Press stop key. Manual light goes on.

2. Set rate switch to INSN STEP. Test light goes on.

3. Press start key. The next instruction is processed; i/o operations are completed, and all pending interruptions are serviced. The program is run basically in the same way as during normal processing, except that the system returns to the stopped state at the completion of execution of that instruction. The address of the next instruction to be processed is displayed in the IAR.

4. Repeat Step 3 for each instruction step.

When the instruction-step processing is completed, reset the rate switch to PROCESS.

PSW Procedures

The current PSW governs control of the system. Because the PSW is a double word, it is necessary to display it in parts. All the parts are accessible, as described. (See PSW format in Appendix B.)

Display Current PSW (First Half)

1. Press stop key. Manual light goes on.
2. Set address switches to 170.
3. Set storage select switch to LOCAL.
4. Press display key.
5. Rotate roller 3 (CPU 1) to position 1, revealing the L register.

The first half of the current PSW is now displayed in the L register.

Alter Current PSW (First Half)

1. Perform the five steps to display PSW (shown above).
2. Set new information desired in the data switches.
3. Press store key. The PSW is now altered.
4. Press display key to display new PSW data in the L register.

Display First Byte of Second Word of Current PSW

1. Rotate roller 4 to position 3.
2. The first byte of second word of current PSW is now displayed in PSW portion of roller display labeled PSW (last 8 bits).

Display Remainder of Second Word of Current PSW

This is the three-byte instruction address. See the following procedure.

Display the Instruction Address (Instruction Counter)

The instruction counter is always on display in the instruction address register. To read the lights in that register, press stop key. Manual light goes on. To resume processing, press start key. Manual light goes off.

Alter the Instruction Counter in the Current PSW

1. Press stop key. Manual light goes on.
2. Set address switches to desired instruction address.
3. Press set IC key. The desired IC address is now in the current PSW. When the program resumes, the instruction at the desired IC address is executed, and the next IC address is displayed in the instruction address register. (If the instruction executed was a branch, and the branch was taken, the new address displayed in the IAR is the address of the branch instruction.)
4. To resume processing, press start key. Manual light goes off.

Storage Procedures

Data can be stored in main storage, general and floating-point registers, and in special local storage. Certain channel registers are also addressable.

Display Main Storage

1. Press stop key. Manual light goes on.
2. Set address switches to the desired storage address.
3. Set storage select switch to MAIN.
4. Press display key. The contents of main storage addressed is now displayed in the storage data register.

Store into Main Storage

1. Perform Steps 1-3 under "Display Main Storage."
2. Set data switches to data desired.
3. Press store key. Desired data are now stored at desired address. (Check for accuracy by displaying contents of stored location.) Note that main storage addresses must end in 0, 4, 8, or C for proper boundary byte locations.

CAW Display

1. This is a special case of display main storage. Follow that procedure.
2. The location (address switches setting) is 48 (hex).
3. When display key is pressed, the CAW is displayed in the storage data register. (See CAW format in Appendix B.)

Local Storage Procedures

Separate from main storage, the local storage contains 16 full word general registers (GR0-GR15), four double word floating-point registers (FP0, FP2, FP4, FP6), multiplexor channel registers, and working storage for scratch pad use. Each of these functions are specified as sectors. The four sectors are addressed by address switches 22 and 23. These switches address the local storage sectors as follows:

00 Multiplexor Channel
01 Working Storage
10 Floating-Point Registers
11 General Purpose Registers

The data in these registers are displayed one full word at a time. Generally this is all that is required. Floating-point registers, however, display only the single word of the double word capability. To display the second word, increment the address by 4 (bytes). When the display key is again pressed, the second word is displayed.

Display Local Storage or Registers

1. Press stop key. Manual light goes on.
2. Set sector to be displayed in address switches 22 and 23. Set location to be displayed in address switches 24-27.
3. Set storage select switch to LOCAL.
4. Press display key.
5. Rotate roller 3 (CPU 1) to position 1 (L register).

The contents of the specified location in local storage is now displayed in the L register.

6. To resume processing, press start key. Manual light goes off.

Store into Local Storage or Registers

1. Press stop key. Manual light goes on.
2. Set sector to be displayed in address switches 22 and 23. Set location of local storage or registers desired in address switches 24-27.
3. Set storage select switch to LOCAL.
4. Set data switches to data desired.
5. Press store key. Desired data is now stored in local storage or registers.
6. To resume processing, press start key. Manual light goes off.

The System/360 Model 50 may use any of four IBM-supplied operating systems, listed in order of increasing complexity:

1. Basic Assembly Program (System/360 BAP)
2. Basic Programming System (System/360 BPS)
3. Basic Operating System (System/360 BOS)
4. Operating System (System/360 OS)

Where no distinction is made for any operating procedure, it is understood that the procedure is common to all. Differences, even in single steps of a detailed procedure, are distinguished and noted in every case. For more detailed information on each of these operating systems, the operator is referred (in order) to: *IBM System/360 Basic Programming Support, Operating Guide for Basic Assembler and Utilities,* Form C28-6557; *IBM System/360 Basic Programming Support, Operating Guide,* Form C24-3391; *IBM System/360 Basic Operating System, Operating Guide,* Form C24-3450; and *IBM System/360 Operating System, Operator's Guide,* Form C28-6540.

I/O Unit Addressing

Implicit in any information processing system are the various I/O units, identified in this system by a unique three-digit address for each device. (This I/O device address is not to be confused with a storage location address.) In practical usage, the three-digit address is described: first digit for channel, and next two digits for subchannel (or device, with control unit implicitly contained). Example: I/O address 00A may be interpreted as being on multiplexor channel (0), with control-unit device 0A (i.e., Card Read Punch). Similarly, address 187 may be on selector channel 1, control-unit drive 87 (i.e., tape unit).

A typical I/O unit address table example is:

DEVICE	ADDRESS
Tapes (2402), Selector Channel 1	180, 181: 7-track, 182, 183: 9-track, 184-187: assigned locally
Tapes (2402), Selector Channel 2	280, 281: 7-track 282, 283: 9-track 284-287: assigned locally
Card Read Punch (1442)	00A
Printer (1443)	00B
Card Reader (2540)	00C
Card Punch (2540)	00D
Printer (1403)	00E
Printer-Keyboard (1052)	009
Disk Storage (2311)	190

If this installation uses System/360 BPS or BOS, then symbolic addresses may be used. Some of the most popular symbolic addresses have been standardized, and are listed in Appendix A.

SYSGEN Time

Given the particular machine and I/O configuration of this Model 50 installation, the programmer or operator places a complement of IBM-supplied operating system programs in residence in main storage (or disk drive), generating a specific operating system for this installation. This system generation procedure is abbreviated SYSGEN, and the time of its generation is referred to as SYSGEN TIME. Once generated, the control lasts (possibly through many problem programs) until a change in operating system is required. Specific SYSGEN procedures are given in the related publications for the operating system desired.

System-Operator Communications

If the current operating system has provision for communication with the operator, and if the current control cards specifying this provision have been incorporated in the SYSGEN assembly, system-operator communication is used, with a 1052 Printer-Keyboard, if available; otherwise, the communication is by operator console. The 1052 is assigned to SYSLOG (BPS/BOS) or an appropriate address. Detailed system-operator communication, with appropriate tables for all allowable codes, is included in the Operating Guides referenced at the beginning of this section.

Making an Entry: Printer-Keyboard

To originate an operator-request, start at Step 1. When the operator responds to a system request, omit Steps 1 and 2.

1. Press the ready key on the keyboard. The 1052 is now ready.

2. Press the request key. The attn light may go on, indicating that the request has been initiated, but not accepted yet by the system. If the request is accepted, an I/O interruption to the CPU occurs (unless the PSW is masked against it). After the procd light comes on, the operator may proceed. The read light is on when the system reads the operator's request and the subsequent message. Now the operator may type his message. (The procd light goes off and on in between each typed

character, but this is generally too rapid to be noticed by the operator. During the time the procd light is off, the keyboard is locked.) Most replies are a single character. Note that an operator response of 0 or 1 (even if transmitted inadvertently) terminates (aborts) the job in process if operating under System/360 BPS or BOS.

3. Position the carriage as desired. Normally the previous operation has done this automatically.

4. Make the desired entry by pressing the desired key(s). (A print-out occurs for each character entry.) Continue until entire entry is made.

NOTE: To cancel an entry, perform Steps 5 and 6; otherwise, omit these steps.

5. To cancel, press the altn code key and simultaneously press the cancel (numerical 0) key. This cancels all entries made during this typing. The procd light turns off momentarily, but comes back on again.

6. Re-enter the entire message. It is not necessary to press the request key again if the procd light is on. (Even if message is not re-entered, continue with following steps to terminate.)

7. Simultaneously press altn code and EOB (numerical 5) key to terminate. (If the program cannot wait, it may terminate by program operation.) In any case, termination locks the keyboard, turns off the procd and read lights, and returns the carriage to starting position. (Under System/360 OS control is turned over to the system.)

8. Under System/360 BPS or BOS an additional step is required; press interrupt key to turn control over to the system. (If the system has terminated the communication and has started processing, this step may be omitted.)

NOTE: If the system has entered the wait state (wait light is on), operator intervention is positively required. (This is a practical, rather than a theoretical consideration: Wait state frequently occurs in all-machine programming; at machine speed the wait state would hardly register on the operator's mind. If the system waits long enough for the wait light to remain on, and nothing is running, look for messages or some sign of operator intervention.) If under System/360 BPS or BOS a keyboard entry is not feasible, operator must restore control to the system by pressing start, then interrupt keys on the operator's console.

Messages: System Operator (1052)

Information messages in telegraphic plain English may appear on the 1052 as check reports. These may be for information only. When a message appears on the 1052 and the system goes into a wait state, operator intervention is indicated. Most system messages (BPS and BOS) are single 4- or 5-character coded words (possibly followed by comments in plain English). The meaning

and action required for the code are defined in the appropriate operating guides. (In System/360 OS the code is not necessarily the message.) If a 3-character code (System/360 BPS) or a 4-character code (System/360 BOS) is printed on the first line, with a 4- or 5-character code below it, the first line code is the address of the unit, and the second line code contains the error and action involved.

If System/360 BAP is in use, the system, on entering the wait state, prints a 3-character code on the 1052, identifying the reason for the program wait. In some cases a brief descriptive message in plain English follows. Code meaning and action required are defined in the appropriate operating guides for that system. In certain cases the code is not typed out on the 1052; it is then necessary to check the operator's console, which always displays the reason for the program wait in the last three bytes of the instruction address. (On the console, the 3-byte code is displayed in hexadecimal, appearing as six characters.)

Making an Entry: Operator's Console

To initiate communication, or to respond to a system request (the wait light will be on) start at Step 1.

1. Press stop key. Manual light goes on.

2. If any operating system except System/360 BAP or OS is in use, display main storage address 000. Locations 0-4 are displayed in the SDR. Read the hexadecimal characters, translate them to alphameric, and find the meaning in the appropriate operating guide for that system. If location 4 contains an alphameric A (1100 0001) then action/reply is required. After taking the required action, store into main storage address 005 (in hexadecimal) the single-character reply required. (Go to Step 4.) Note that an operator response of 0 or 1 (even if transmitted inadvertently) terminates (aborts) the job in process.

3. If System/360 BAP is in use, display three lowest-order bytes of the instruction counter. Code meaning and action required are defined in the appropriate operating guides for that system. (No provision is made for operator reply to the console. Go to Step 4.)

4. After appropriate operator action (and reply, if available) it is necessary to take the system out of the wait state. Press start key. Manual light goes off.

5. Press interrupt key. The system resumes processing.

Messages: System Operator (System/360 BPS and BOS) Operator's Console

Because of the limitation of the number of bytes of information provided by the console for system-operator communication, plain English statements are not included. The bytes will be code and hexadecimal characters. In certain cases, the system will issue two

coded messages—one for the device involved, and the second for the error and action desired. The following operator action is necessary between the two messages:

If the system is in the wait state (wait light is on) and the operator has pressed the stop key (manual light is on), he next displays main storage address 000. If location 4 in the sdr (locations 3 and 4 under System/360 bps) is all zeros, the message must be recorded (because it indicates the device-portion of a two-part message). He then presses the start key and the interrupt key. This passes control back to the system, which can then send the second part of the message. (System reply is almost instantaneous; therefore, it may seem to the operator that the interruption has not worked properly, because the system may go into the wait state immediately.) Now press the stop key to prevent interruption. When the contents of storage address 000 is displayed, note that the sdr has the second part of the message. After appropriate action, release the system with the same procedure, pressing the start key, then the interrupt key. (The operator must release the system in any event.)

Messages: System Operator (System/360 BAP) Operator's Console

If the 1052 is not available under this operating system, the sole communication between the system and the operator is via the operator's console. (The sdr is not used for this purpose.) The three lowest-order bytes of the instruction counter now contain a code that shows the reason for any system wait. Definition and procedures for the code are found in *IBM System/360 Basic Programming Support Operating Guide for Basic Assembler and Utilities,* Form C28-6557. Communication is provided only one-way (from system to operator). The only possible communication provided between operator and system is by pressing the start and interrupt keys, which returns control to the system. (See also "Analyzing an Unexpected Wait State Condition.")

Operator-Console Considerations (except under System/360 OS)

When the system goes into the wait state, providing the operator with a code message on the operator's console, press the stop key; this places the system in a manual stop. (This holds potential interruptions pending while displaying and reading the appropriate code.) The only way to return the system to control after a manual stop is to manually press the start key. Press the interrupt key to return to the program.

If the stop key is not pressed to read the console code, then control can be returned to the system by pressing the interrupt key alone. (It is not necessary to press the start key to return control unless a manual stop has been executed.)

Using the 1410/7010 Emulator

Detailed information on this feature can be found in *IBM System/360 Model 50 Emulation of the IBM 1410/7010 Data Processing Systems,* Form C28-6568. The emulator program, provided on cards, may use card format in actual programming. If it is desired to convert the card program to tape, the following procedures are recommended.

Object Generation of Emulator Program

This is a pre-sysgen (1410/7010) procedure used to establish the required i/o configuration for this installation.

1. Prepare the control cards for use with card-to-tape utility program 360p-ut-051 used to establish the tape drive as the output address. Integrate the control cards with the card-to-tape utility program, forming the card-to-tape deck. (See Appendix D for job control cards for utility programs. See detailed procedure, *System/360 BPS Specifications,* Form C24-3363 for card-to-tape [see only the sections on utility-modifier cards and field-select cards]. See *System/306 BPS Programmer's Guide,* Form C24-3354 for format [see section on job control cards for utility programs]. See *System/360 BPS Operating Guide,* Form C24-3392 for card sequence [see section on card-to-tape utility program].)

2. Prepare the necessary rep cards for storage size, channel identification, and device addressing required for the emulator program. (See detailed procedure in referenced manual, Form C28-6568.)

3. Take the ibm-supplied combined absolute-loader and emulator program in card form, together with the cards and utility program of the preceding steps and combine them as: card-to-tape utility program, absolute-loader, and emulator, with rep cards. Place the combined deck on the card reader. Make the device ready.

4. Mount a clean tape on another tape drive for the configurated emulator object program. Make the device ready.

5. Set disable interval timer switch to dsab intvl timer.

6. Select the desired card reader with the three load unit switches.

7. Press load key. Load light goes on.

8. Because device addresses have been patched in (rep cards), the entire updated combined-emulator object program is now written onto the output tape. (If the required device patch addresses are not constant enough to be a part of the combined emulator tape, at least enter rep cards with the 1052 address and card reader address. In this way the tape can still be used, picking up the rep patch data as required via

the 1052, during the wait state which occurs at the end of the emulator tape.) In any case, communication between emulated system and the operator during emulation is via the 1052. At the completion of object generation, the configurated emulator object program processed on tape has been tailored to this installation's i/o configuration. Remove the reels and decks. Reset disable interval timer switch to normal position (straight out).

Operating the 1052 in Emulator Mode

To make entries in the emulator program (when operator intervention is provided between the emulator program and the problem program):

1. Press the request key.

2. Press the single-character function key. (For example, press the numerical 3 key for a device assignment. See referenced manual, Form C28-6568 for detailed coding.)

3. Press the space bar. (The carriage returns.)

4. Enter the information desired. (Observe format described in the referenced manual, Form C28-6568.)

5. To correct typing errors—any line may be canceled by simultaneously pressing the altn code key and the numerical 0 key. (The system then returns the carriage. The last line has been canceled. It is necessary to retype it.) To delete the entire function—start a new line (perform the cancel function if necessary), then simultaneously press the altn code key and the numerical 5 (EOB) key.

6. To release data, at the end of the information line or message, simultaneously press the altn code key and the numerical 5 (EOB) key. (This function is similar to the release of the 1415 console.)

Operating the 1052 in Problem Mode

To make entries required by the problem program:

1. Press the request key. The read and procd lights go on.

2. Press the I key.

3. Press the space bar. (Carriage returns.)

4. The read and procd lights go out and the system responds by typing an I. (If the system does not respond by typing an I, press the numerical 2 key, then press the space bar. The lights go out and the system then responds by typing an I.)

5. Enter the information desired.

6. To correct typing errors—simultaneously press the altn code key and the numerical 0 key. Any cancellation in problem mode requires return to Step 1, as the entire communication has been canceled.

7. To release—simultaneously press the altn code key and the numerical 5 (EOB) key.

Using the Configurated Emulator Program (Load-and-Go)

This is a single-phase operation where emulator, control cards, and problem program are set into appropriate initialized i/o units; manual IPL starts load-and-go.

1. Prepare the CTL and LOAD control cards (described in detail in the referenced manual, Form C28-6568). If the problem program is on cards, insert the control cards in front of the problem program deck and place the combined deck on the card reader. Otherwise, place the control cards on the card reader and the problem program on an appropriate device. Make the device(s) ready.

2. Mount the configurated emulator program tape on the tape drive. Make the tape drive ready.

3. Select the tape drive with the three load unit switches.

4. Press load key. Load light goes on. The combined-emulator program is IPL-loaded. Control is passed to the emulated IBM 1410/7010 System, which immediately takes up the control cards from the card reader, and continues with execution of the problem program from its i/o device.

Using the Configurated Emulator Program (Operator Intervention between Emulator Mode and Problem Mode)

This is a two-phase operation. First the emulator program is loaded, causing the system to emulate a 1410/7010 system; the card reader is deliberately not made ready. Accordingly, the emulated system, when loaded, goes into a wait state, awaiting operator intervention.

1. Mount the configurated emulator program tape on a tape drive. Make the tape drive ready.

2. Select the tape drive with the three load unit switches.

3. Press load key. Load light goes on. The configurated emulator program is IPL-loaded. The emulated system goes into a wait state.

During the wait state the operator intervenes, as required (see "Operating the 1052 in Emulator Mode"). When the operator is ready to start the problem program:

1. Prepare the CTL and LOAD problem-program control cards (described in detail in the referenced manual, Form C28-6568). If the problem program is on cards, insert the control cards in front of the problem program deck and place the combined deck in the card reader. Otherwise, place the control cards in the card reader and the problem program on an appropriate device. Make the device(s) ready. (If the card reader is not available, the control functions can be entered via 1052; see "Operating the 1052 in Emulator Mode," using "a" as the single-character function key.)

2. Press request key.

3. Press numerical 8 key. The system now executes the problem program.

Operator Considerations

During emulation procedures, the system operates with minimum burden to the operator. When the operator is involved, however, certain minimal differences involved in emulator operation must be recognized:

1. Certain dissimilar graphics occur in the print-out during emulation, because of typeface difference in systems. These differences are shown in comparison tables in the emulation publication referenced. Normal alphabetic and numerical values are identical to those conventionally used.

2. Device assignment addresses (1410/7010) are in different format from the 3-digit group normally used in System/360 addressing. The emulator manual describes the technique for relating addresses between systems, and techniques for causing a print-out of the device assignment table in use by the emulator.

3. Operator communication code format (specifically set in any system) is similarly described in the referenced emulator manual.

4. The 1052 keyboard, in addition to providing system-operator communication, is used by the operator as an emulated 1415 Console Printer. These console functions are described in Table 1.

Table 1. Correlations of 1415 Functions with 1052 Functions

FUNCTIONS OF THE 1415	CORRESPONDING 1052 KEY/FUNCTION	1052 PRINTOUT IDENTIFICATION
Programmed Halt		S
Error Halt		E
Reply		R
Table Display	6	6
Alter	A	A
Restart	8	8
Address Set	B	B
Display	D	D
Inquiry Request	I	I
Clear Storage	7	7
Computer Reset	4	4
Program Reset	5	5
Start Key	2	2
Stop Key	S	S
7010 Tape Load	L	L
Release	Altn Code and '5' Key	None
Cancel	Altn Code and '0' Key	None

NOTE: All print-out identifications except E, R, and S (programmed halt) are produced by keying.

Halt Instructions

When the emulator executes a programmed halt:

1. The 1410/7010 IAR, AAR, BAR, the operation code, the d-modifier, and the last I/O instruction executed (if any) on each channel are displayed on the printer-keyboard.

2. The system enters the wait state.

To continue after a program halt, the operator may perform on the 1052 keyboard any of several operations that simulate 1410/7010 restart procedures (see Table 1).

Using the 7070/7074 Emulator

Detailed information on this feature can be found in *IBM System/360 Conversion Aids: the 7074 Emulator Program for IBM System/360 Models 50 and 65*, Form C27-6908. A summary of operator requirements follows.

Object Generation of Emulator Program

This is a pre-SYSGEN (7070/7074) procedure used to establish the required I/O configuration for this installation.

1. Mount the IBM-supplied combined absolute-loader and emulator program reel on an input tape drive. Make the drive ready.

2. Prepare the necessary /BCFG and /BCFGBEND control cards (described in detail in the referenced manual, Form C27-6908).

3. Mount a clean tape on the desired output tape drive (or initialize the desired disk drive). Make the device ready.

4. Set disable interval timer switch to DISAB INTVL TIMER.

5. Select the input tape drive device with the load unit switches.

6. Press load key. Load light goes on.

7. The IPL procedure loads the absolute loader, which in turn reads the emulator program into main storage. Control is passed to the emulator program, which places the system in wait state. Operator intervention (via the 1052) is now indicated, to provide certain control information to the system; operation of the 1052 under emulation is discussed in the next paragraph. (The control information required in this case informs the system in what form the data will be supplied, provides the address of the I/O device on which the data are available, and contributes any control information not available elsewhere. The system, utilizing this control data, writes the resulting configurated emulator program onto the output device.)

8. When the configurated emulator program has been written onto the output tape (or disk), remove the reel (if tape) and reset the disable interval timer switch to normal position (straight out).

Operating the 1052 under Emulation

The 1052 is virtually a communication device and operator's console during emulation. Console orders emulate certain console switch functions. To enter typewriter control information:

1. Press request key. (To cancel a typewriter entry, simultaneously press altn code key and numerical 0 key.)

2. Enter the information desired. (Observe format described in referenced manual, Form C27-6908.)

3. To terminate—simultaneously press the altn code key and the numerical 5 (EOB) key.

Using the Configurated Emulator Program with Problem Program

This is a two-phase operation. First the configurated emulator program is loaded, causing the system to emulate a 7070/7074 system. The emulated system goes into wait state. Then the problem program is loaded into the emulated system, by operator load order, and the system executes the program.

1. If necessary to make assignment changes, prepare CTL and CTLEND control cards (described in detail in referenced manual, Form C27-6908). Place the control cards on the card reader. Make the card reader ready.

2. Place the problem program on appropriate i/o device. Make the device ready.

3. Mount the configurated emulator program on an input drive. Make the drive ready.

4. Select the input drive with the three load unit switches.

5. Press load key. Load light goes on.

6. Configurated emulator program is IPL-loaded. The system goes into wait state.

7. Press request key.

8. Issue a load order via the 1052, or enter initializa-

tion instructions in the same manner as on the 7070/7074. The emulator then executes the program.

Operator Considerations

The basic differences between emulation and actual system 7070/7074 operation include:

1. Device assignment addresses in the emulated program use 2-digit instead of the 3-digit value of System/360. Designation of the 2-digit addresses is described in control-card descriptions in the appropriate operating guide.

2. Operator communication code format, specifically prescribed in any system, is similarly prescribed in emulator operation. (The 7070/7074 codes are different from the codes used in System/360 operation.)

3. Operator communication via the 1052 is slightly different from the technique used in System/360. The differences are described here under "Operating the 1052 under Emulation."

4. The functions of the 7070/7074 operating panel are provided to the operator through a comprehensive set of console orders via the 1052.

5. Start and stop actions are simulated by pressing the interrupt key on the operator's console. (The same key causes both start and stop, and changes the current status.)

Halt Instruction

When the emulator executes a programmed halt, the emulator displays the contents of the IC and the program register. The system enters the wait state. Now the operator may enter console orders via the 1052. Normal operator communication message is terminated by holding down the altn code and EOB (numerical 5) key. The operator then restarts the system by pressing the interrupt key on the operator's console.

Various conditions may arise that require some type of manual operation to be performed. For example, the hopper on a card reader may empty (it must be reloaded by the operator). Lights on the various i/o units indicate the condition of the i/o units (refer to the specific i/o device publication for information). The operator's console, however, does not explicitly indicate i/o device conditions. In a basic card system (for example: a cpu, a printer, and a card read punch), indicators on the i/o units can be inspected with little difficulty. As the number of i/o units increases, however, it becomes increasingly difficult for the operator to see the indicators on all the i/o units.

A variety of methods can be used to determine when an i/o unit requires manual attention. Each depends on the operating procedures at the installation. Procedures that can be used are:

Main Storage Address Indication: A list of main storage addresses can be provided (with the program) for operator reference. The length of the list depends on the extent of operator intervention required. When the system enters the wait state, the operator can look at the main storage address indicators and compare the displayed address with the address list, and then determine the appropriate action to be taken (from details contained in the address list). For example, suppose that address 0111 (hexadecimal) is the main storage address displayed in sar (storage address register) when the program has been successfully completed. If the system enters the wait state with some other address displayed, operator intervention is called for (assume that errors have not occurred).

NOTE: The system should be programmed to enter wait state if it cannot proceed because data are unavailable from an i/o unit (card reader out of cards).

System Operator Communications: If an ibm 1052 Printer-Keyboard is used, the program can be written to type out messages to the operator when i/o units require attention. In this case, the programmer should supply information (to the operator) that describes what the typed messages signify.

Console Alarm: The program can be written to sound the alarm (special feature) whenever an i/o unit requires attention. One of the preceding procedures can then be used to provide more specific information.

End of Job Procedure

Under System/360 bps and bos, the operating systems under multiprogramming provide for eoj macro at end of job to activate job control, which processes the next job. In small installations, where System/360 bap or bps is in use, the operator may prefer setting up individual jobs, rather than processing them in a batch. In that case, sometime during a program, the operator sets up the next program on the desired i/o device, making that device ready, so that at eoj time he can quickly start the next program.

If the supervisor program desired and the required loader program are still in main storage, then, at eoj time, when the machine enters the wait state, press the interrupt key to resume processing. The program loader gains control and begins loading from the i/o device.

If the requirements of the preceding paragraph are not met, then the next job must be initiated by a manual ipl procedure.

Checkpoint/Restart Procedure

To restart a checkpointed job, a supervisor and loader program must be in main storage. (Manual ipl procedure can be used, if necessary.) Job control is loaded, and (after job control cards are read) the restart phase of the job control program is loaded. Checkpoint records are read and the initialization to rerun the job is complete. (The tape containing checkpoint records is positioned beyond the last record of the group of checkpoint records.) If the job requires additional phases, they must be available on the i/o device. (This procedure is established by the programmer.)

Process a Section of a Program

To examine the results caused by processing a section of a program, use the following procedure:

1. Set the desired stop address. See "Compare-Stop Procedures."

2. Load the program as described in "Program Loading."

3. The system stops at the conclusion of the instruction (and all pending interruptions) in which the address match occurred. Examine conditions produced by

the processing of the program segment; subsequent instructions can now be processed, one at a time, by using the procedure described in "Instruction Stepping."

The program may use the interval timer feature. If so, the interval timer may decrement through zero after the system has processed a program segment and then entered the stopped state. Therefore, when restarting the program, an interval timer interrupt occurs and the desired results may not be obtained. If the program depends on the interval timer but interval timer interrupts are not desired while checking out a program segment, set the interval timer switch to OFF.

Start at a Specific Instruction

1. Store a PSW in main storage address 0. This PSW is loaded with information that applies to the program segment. For example, the mode (problem or supervisor), system mask, and instruction address loaded indicate the system state at the starting point of the program segment.

2. Assuming the problem program is already in storage, and no loading is involved, press the PSW restart key. (A system reset takes place, the PSW is loaded from location 0 and the CPU goes into operating state, using the instruction at the location set in the instruction counter in the PSW.)

Compare-Stop Procedures

In contrast with the compare program instruction (which compares operands and sets the condition code), compare-stop procedures compare the instruction address with another specified address; when the two are the same, the CPU enters the stopped state. Three compare-stop procedures are discussed in the following text.

Stop on Address Compare (IAR)

1. Set address switches to instruction address desired.

2. Set address compare (IAR) switch to stop. The test light goes on.

3. When the instruction address (in the IAR) is equal to the set address, the CPU will stop at the completion of the addressed instruction.

4. To resume processing, restore the address compare (IAR) switch to PROC, and press the start key. The test light goes off.

Stop on Address Compare (SAR)
CPU Against Main Storage Location

1. Set data switches 8-31 (low-order 24 positions) to the desired storage address. (Note that this is the storage data register being set.)

2. Set data switch 0 in the down position for CPU comparison.

3. Set address compare (SAR) switch to STOP. The test light goes on.

4. When an instruction accesses the referenced storage location, the CPU will stop at the completion of that instruction.

5. To resume processing, restore the address compare (SAR) switch to the center position, and press the start key. The test light goes off.

Stop on Address Compare (SAR)
I/O Against Main Storage Location

1. Set data switches 8-31 (low-order 24 positions) to the desired storage address. (Note that this is the storage data register being set.)

2. Set data switch 1 in the down position for I/O comparison.

3. Set address compare (SAR) switch to STOP. The test light goes on.

4. When an I/O (channel) operation accesses the referenced storage location, the CPU will stop at the completion of that instruction. The manual light goes on.

5. To resume processing, restore the address compare (SAR) switch to the center position, and press the start key. The test light goes off.

NOTE: If data switches 0 and 1 are both set in the down position, the CPU will stop anytime the selection location is referenced.

Storage Dump Procedure

1. Place utility program 360P-UT-056 dump on the card reader.

2. Make card reader ready.

3. Set load switches to the address of the card reader.

4. Press load key, instituting IPL procedure. The load light goes on. The storage dump is printed out on the printer. The wait light goes on, indicating the system is now in the wait state. The load light goes off.

5. To resume processing, press the interrupt key. The wait light goes off. (Check that the dump lists the highest location of main storage to verify that the entire storage has been dumped.)

Error Log-Out Procedures

Most operating system programming provides for error log-out as part of error-correction routines. If it is necessary for the operator to provide a log-out, such as when the master check light is on, and no system technique is provided to handle the problem, a log-out can be manually instituted, using the SEREP deck. This

program lists on the printer all information that is stored in the diagnostic scan-out area in storage:

1. Set rate switch to SINGLE CYCLE.
2. Set check control switch to DISABLE.
3. Press log-out key.
4. Press start key.
5. Set rate switch back to PROCESS.
6. Press start key.
7. Place SEREP deck on card reader.
8. Make card reader ready.
9. Set load switches to address of card reader.

10. Press load key, instituting IPL procedure. At the completion of the loading, the program will print all error indications in readable format for CE's use.

11. Report the log-out data to the CE, to aid in localizing the malfunction.

Continuous Loop During Assembly with a 1052 (BPS Only)

If the program goes into a continuous loop (during an assembly program), this will be evidenced by console lights repeatedly flashing, and no indication of correct processing. The step of the assembly causing the loop can be by-passed, permitting the remainder of assembly to be completed, by the following procedure:

1. Initiate the procedure covered under "Making an Entry: Printer-Keyboard."
2. For the entry, type 2.
3. Complete the termination and return control to the program. The control bit has been turned on, by-passing that particular instruction being assembled. The remainder of the assembly program should continue normally.

Continuous Loop During Assembly without a 1052 (BPS Only)

If the program goes into a continuous loop during an assembly program (and no 1052 is available), the loop-causing step of the assembly can be by-passed, permitting the remainder of assembly to be completed, by the following procedure:

1. Press stop key. Manual light goes on. Processing stops.
2. Store 02(hex) in main location 005.
3. Press start key. Processing continues. The control bit has been turned on, by-passing that particular instruction being assembled. The remainder of the assembly program should continue normally. If processing does not resume, press interrupt key.

Continuous Looping

When a program is continuously looping in execution (indicated by console lights repeatedly flashing, and no indication of correct processing) and it is desired to trace the loop:

1. Press stop key.
2. Record the current PSW. (See "PSW Procedures" for displaying the current PSW.)
3. Record the CAW if the loop involves an I/O function.
4. Set the rate switch to INSN STEP.
5. Press the start key. (The machine now executes one instruction step, displaying the address of the next sequential instruction in the IAR.)
6. Record the displayed address.
7. Repeat Step 5; continue pressing the start key until the displayed address is the same as that recorded in Step 6. At that time one loop has been completed.
8. Set the rate switch to PROCESS.
9. Effect a storage dump.

Analyzing an Unexpected Wait State Condition (System/360 BAP)

If the CPU unexpectedly switches to the wait state as indicated by the wait light on the console, the contents of the current PSW should be examined, and a storage dump should be taken. Note that the PSW is an internal register that will be destroyed by any storage dump program.

If any of the System/360 BPS utility programs are being used, bits 40-63 of the current PSW, which normally contain the instruction address, will contain a three-byte BCD message indicating the type of error. For example, if the instruction address field of the current PSW contains D3D7C1, decoded LPA, this signifies that a program check has occurred; a storage dump helps to determine the cause. In this example, examine the old program PSW starting in location 28 (hex). This action helps to isolate the cause of the program check and where it occurred. The instruction address (which caused the wait state) minus the instruction length code is found at hexidecimal location 2E.

Under the BPS packages, an I/O interruption also switches the CPU to the wait state. In this case, the above procedure should be followed, except that the old I/O PSW (starting in hexadecimal location 38) should be examined instead of the old program PSW.

Refer to *Operating Guide for Basic Assembler and Utilities,* Form C28-6557 for the list of codes (and cor-

responding descriptions) that replace the instruction address in the current program psw following an unexpected switch by the cpu to the wait state. Appendix C contains a reference list.

Analyzing Input/Output Commands

For analyzing i/o commands for any reason whatever, the procedure for using either the console or a storage dump to determine the last i/o command issued, the device associated with that command, and the status or result of the execution of that command, is:

Examine the Channel Address Word (CAW): A full-word at location 48 (hex), which contains the address of the channel command word (ccw). (Refer to Appendix B for formats.) Note that if i/o command chaining was employed, the caw contains the address of the first ccw in the chain.

Analyze the Channel Status Word (CSW): A double word starting at location 40 (hex). See csw format in Appendix B. The csw has three significant parts:

1. The command address portion of the csw always contains the address of the last ccw executed plus eight bytes.

2. The status portion (bits 32-47) of the csw half-word at location 44 (hex) contains the status of the channel control unit or subchannel, and the status of the device to which the i/o command was issued. Each i/o device that can be attached to the system has its own characteristics as far as status bits are concerned. Refer to the individual srl for each i/o device status bit meaning, as they vary. The address of the particular device to which the i/o command was directed can always be found in the interruption code portion (bits 16-31) of the i/o psw at location 3A (hex).

3. The residual byte count should be zero at the completion of the i/o command. Otherwise, one of three things is indicated:
   a. A wrong-length record was encountered.
   b. A command reject was issued from the channel for the last i/o command received—in either of these two cases, something may be wrong with the user's channel program.
   c. A data check occurs during a read or write operation causing data transfer to stop at the point where the error occurred and device motion to stop at the end of the affected record. Channel end, device end, unit check and incorrect length indications are posted in the csw, and the residual byte count may indicate the amount of data not stored.

When working with variable-length records, the wrong-length record indication in the ccw bit 34 should be on; otherwise, every time a record with a count different from that specified in the ccw is encountered, bit 41 in the csw (incorrect length) will be turned on, causing an i/o interruption. (If the basic i/o subroutines are used, the cpu will enter the wait state).

Check the Channel Command Word (CCW): A double word location on any double word boundary in storage. The ccw contains the data address, a byte count indicating the number of bytes involved in the operation, the command code defining the actual i/o operation, and the flag bits (if any) for command and data chaining, etc. Note that, initially, there must be a byte count of one or more for any i/o operation, except transfer in channel (tic). (For the definitions of i/o device command codes, refer to the individual srl's; Appendix B contains a reference list.)

Standardized symbolic addresses for i/o devices using these operating systems include:

SYSIPT   Source program input device. (May be the same device as SYSRDR.) Generally IBM 1442, 2520, or 2540 Card Read Punch, or 2501 Card Reader, or 2400-series tape unit.

SYSLOG   Operator-message logging device. Generally IBM 1052 Printer-Keyboard or 1403, 1404, or 1443 Printer (if 1052 is not available).

SYSLST   Program listing device; IBM 1403, 1404, or 1443 Printer or 2400-series tape unit.

SYSOPT   Object program output device (disk drive, card punch, tape unit, or display unit).

SYSRDR   Job-control input device. (May be the same device as SYSIPT.) Same type read-punch, card reader, or tape unit.

SYS000   Used for temporary work area during assembly; disk storage drive or equivalent device. (For more storage devices, SYS--- is symbolically assigned to units 001-003 or 004, as required.)

While the operator can assign any i/o device address to any symbolic address, general convention has established the following functions by symbolic name:

1. Card input is always read from SYSRDR. (SYSRDR, however, may be assigned an address other than card input.)

2. Card output is always punched on SYSOPT. (SYSOPT, however, may be assigned an address other than card output.)

3. Printed output is always on SYS000. (SYS000, however, may be assigned an address other than a printer.)

4. The 1052 Printer-Keyboard is always SYSLOG.

5. SYSRES (if used) is the symbolic name of the location of the system residence unit. (This is generally a disk drive.)

In the operating system, i/o devices (program-referenced by symbolic names) are assigned physical 3-digit addresses by job control at job execution time. These physical 3-digit addresses are communicated to job control by the operator via ASSGN cards (part of the control cards inserted in the program). The SYSRES physical address cannot be assigned by an ASSGN card; this is to protect SYSRES from accidentally being addressed as an output unit, resulting in overwrite of SYSRES control programs.

Example—Assigning Physical Address: In the job instruction sheet, assume the programmer writes: "mount a scratch tape on SYS000." From the preceding table this indicates that SYS000 will be used as a temporary work area during assembly. The operator selects an available tape unit, mounts a scratch tape on it, readies the unit, and prepares an ASSGN control card containing the symbolic address SYS000 and the physical address assigned to the particular tape unit. When loading the program, insert the ASSGN card (with the other necessary control cards). The system control makes the necessary translation as required.

Appendix B: Reference Tables For the System/360 Units

Operation Codes

RR FORMAT INSTRUCTIONS

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)
0	00					12-0-9-8-1	0000 0000	CCW
1	01					12-9-1	0000 0001	
2	02					12-9-2	0000 0010	
3	03					12-9-3	0000 0011	
4	04	SPM		PF		12-9-4	0000 0100	
5	05	BALR		HT		12-9-5	0000 0101	
6	06	BCTR		LC		12-9-6	0000 0110	
7	07	BCR		DEL		12-9-7	0000 0111	
8	08	SSK				12-9-8	0000 1000	CCW
9	09	ISK				12-9-8-1	0000 1001	
10	0A	SVC				12-9-8-2	0000 1010	
11	0B					12-9-8-3	0000 1011	
12	0C	(EBCDIC +)				12-9-8-4	0000 1100	
13	0D	(EBCDIC −)				12-9-8-5	0000 1101	
14	0E					12-9-8-6	0000 1110	
15	0F					12-9-8-7	0000 1111	
16	10	LPR				12-11-9-8-1	0001 0000	CCW
17	11	LNR				11-9-1	0001 0001	
18	12	LTR				11-9-2	0001 0010	
19	13	LCR				11-9-3	0001 0011	
20	14	NR		RES		11-9-4	0001 0100	
21	15	CLR		NL		11-9-5	0001 0101	
22	16	OR		BS		11-9-6	0001 0110	
23	17	XR		IL		11-9-7	0001 0111	
24	18	LR				11-9-8	0001 1000	CCW
25	19	CR				11-9-8-1	0001 1001	
26	1A	AR				11-9-8-2	0001 1010	
27	1B	SR				11-9-8-3	0001 1011	
28	1C	MR				11-9-8-4	0001 1100	
29	1D	DR				11-9-8-5	0001 1101	
30	1E	ALR				11-9-8-6	0001 1110	
31	1F	SLR				11-9-8-7	0001 1111	
32	20	LPDR				11-0-9-8-1	0010 0000	CCW
33	21	LNDR				0-9-1	0010 0001	
34	22	LTDR				0-9-2	0010 0010	
35	23	LCDR				0-9-3	0010 0011	
36	24	HDR		BYP		0-9-4	0010 0100	
37	25			LF		0-9-5	0010 0101	
38	26			EOB		0-9-6	0010 0110	
39	27			PRE		0-9-7	0010 0111	
40	28	LDR				0-9-8	0010 1000	CCW
41	29	CDR				0-9-8-1	0010 1001	
42	2A	N ADR		SM		0-9-8-2	0010 1010	
43	2B	N SDR				0-9-8-3	0010 1011	
44	2C	N MDR				0-9-8-4	0010 1100	
45	2D	N DDR				0-9-8-5	0010 1101	
46	2E	AWR				0-9-8-6	0010 1110	
47	2F	SWR				0-9-8-7	0010 1111	
48	30	LPER				12-11-0-9-8-1	0011 0000	CCW
49	31	LNER				9-1	0011 0001	
50	32	LTER				9-2	0011 0010	
51	33	LCER				9-3	0011 0011	
52	34	HER		PN		9-4	0011 0100	
53	35			RS		9-5	0011 0101	
54	36			UC		9-6	0011 0110	
55	37			EOT		9-7	0011 0111	
56	38	LER				9-8	0011 1000	CCW
57	39	CER				9-8-1	0011 1001	
58	3A	N AER				9-8-2	0011 1010	
59	3B	N SER				9-8-3	0011 1011	
60	3C	N MER				9-8-4	0011 1100	
61	3D	N DER				9-8-5	0011 1101	
62	3E	AUR				9-8-6	0011 1110	
63	3F	SUR				9-8-7	0011 1111	

(2) Note that check bit (C) is not shown; add C bit for odd or even parity as needed except for even parity, decimal 64 is CA, the same as decimal 122
(3) CCW flag bit assignments
(4) Decimal feature instructions
(5) System/360 assembler programs require these codes

Standard Instruction Set
Floating-Point Feature Instructions

RX FORMAT INSTRUCTIONS

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	(2) 7-Track Tape BCDIC	Punched Card Code	System/360 8-bit Code	(3)	(5)
64	40	STH		SP	(2)	no punches	0100 0000	CCW	
65	41	LA				12-0-9-1	0100 0001		
66	42	STC				12-0-9-2	0100 0010		
67	43	IC				12-0-9-3	0100 0011		
68	44	EX				12-0-9-4	0100 0100		
69	45	BAL				12-0-9-5	0100 0101		
70	46	BCT				12-0-9-6	0100 0110		
71	47	BC				12-0-9-7	0100 0111		
72	48	LH				12-0-9-8	0100 1000	CCW	
73	49	CH				12-8-1	0100 1001		
74	4A	AH		¢		12-8-2	0100 1010		
75	4B	SH	.	.	B A 8 2 1	12-8-3	0100 1011		
76	4C	MH	⌑)	<	B A 8 4	12-8-4	0100 1100		
77	4D		[	(	B A 8 4 1	12-8-5	0100 1101		(
78	4E	CVD	<	+	B A 8 4 2	12-8-6	0100 1110		+
79	4F	CVB	⌑	!	B A 8 4 2 1	12-8-7	0100 1111		
80	50	ST	& +	&	B A	12	0101 0000	CCW	
81	51					12-11-9-1	0101 0001		
82	52					12-11-9-2	0101 0010		
83	53					12-11-9-3	0101 0011		
84	54	N				12-11-9-4	0101 0100		
85	55	CL				12-11-9-5	0101 0101		
86	56	O				12-11-9-6	0101 0110		
87	57	X				12-11-9-7	0101 0111		
88	58	L				12-11-9-8	0101 1000	CCW	
89	59	C				11-8-1	0101 1001		
90	5A	A		!		11-8-2	0101 1010		
91	5B	S	$	$	B 8 2 1	11-8-3	0101 1011		
92	5C	M	.	.	B 8 4	11-8-4	0101 1100		
93	5D	D	]	)	B 8 4 1	11-8-5	0101 1101		)
94	5E	AL	;	;	B 8 4 2	11-8-6	0101 1110		
95	5F	SL	∆	¬	B 8 4 2 1	11-8-7	0101 1111		
96	60	STD	-	-	B	11	0110 0000	CCW	
97	61		/	/	A 1	0-1	0110 0001		
98	62					11-0-9-2	0110 0010		
99	63					11-0-9-3	0110 0011		
100	64					11-0-9-4	0110 0100		
101	65					11-0-9-5	0110 0101		
102	66					11-0-9-6	0110 0110		
103	67					11-0-9-7	0110 0111		
104	68	LD				11-0-9-8	0110 1000	CCW	
105	69	CD				0-8-1	0110 1001		
106	6A	N AD				12-11	0110 1010		
107	6B	N SD	,	,	A 8 2 1	0-8-3	0110 1011		
108	6C	N MD	%(	%	A 8 4	0-8-4	0110 1100		
109	6D	N DD	⋎	—	A 8 4 1	0-8-5	0110 1101		
110	6E	AW	\	>	A 8 4 2	0-8-6	0110 1110		
111	6F	SW	⋈	?	A 8 4 2 1	0-8-7	0110 1111		
112	70	STE				12-11-0	0111 0000	CCW	
113	71					12-11-0-9-1	0111 0001		
114	72					12-11-0-9-2	0111 0010		
115	73					12-11-0-9-3	0111 0011		
116	74					12-11-0-9-4	0111 0100		
117	75					12-11-0-9-5	0111 0101		
118	76					12-11-0-9-6	0111 0110		
119	77					12-11-0-9-7	0111 0111		
120	78	LE				12-11-0-9-8	0111 1000	CCW	
121	79	CE				8-1	0111 1001		
122	7A	N AE	⧠	:	A	8-2	0111 1010		
123	7B	N SE	⧠ .	#	⧠ 8 21	8-3	0111 1011		
124	7C	N ME	@	@	8 4	8-4	0111 1100		
125	7D	N DE	:	'	8 4 1	8-5	0111 1101		
126	7E	AU	>	=	8 4 2	8-6	0111 1110		.
127	7F	SU	⋎	"	8 4 2 1	8-7	0111 1111		

Standard Instruction Set
Floating-Point Feature Instructions

PROGRAM STATUS WORD

System Mask*	Key	AMWP*	Interruption Code	
0	7 8	11 12	15 16	31

ILC	CC	Program Mask*	Instruction Address	
32	33 34 35 36	39 40		63

0-7 System mask
  0 Multiplexer channel mask
  1 Selector channel 1 mask
  2 Selector channel 2 mask
  3 Selector channel 3 mask
  4 Selector channel 4 mask
  5 Selector channel 5 mask
  6 Selector channel 6 mask
  7 External mask
8-11 Protection key
  12 ASCII mode (A)
  13 Machine check mask (M)

  14 Wait state (W)
  15 Problem state (P)
16-31 Interruption code
32-33 Instruction Length code (ILC)
34-35 Condition code (CC)
36-39 Program mask
  36 Fixed-point overflow mask
  37 Decimal overflow mask
  38 Exponent underflow mask
  39 Significance mask
40-63 Instruction address

*A one-bit equals on, and permits an interrupt.

PERMANENT STORAGE ASSIGNMENT

ADDRESS DEC	ADDRESS HEX	ADDRESS BINARY	LENGTH	PURPOSE
0	0	0000 0000	double-word	Initial program loading PSW
8	8	0000 1000	double-word	Initial program loading CCW1
16	10	0001 0000	double-word	Initial program loading CCW2
24	18	0001 1000	double-word	External old PSW
32	20	0010 0000	double-word	Supervisor call old PSW
40	28	0010 1000	double-word	Program old PSW
48	30	0011 0000	double-word	Machine-check old PSW
56	38	0011 1000	double-word	Input/output old PSW
64	40	0100 0000	double-word	Channel status word
72	48	0100 1000	word	Channel address word
76	4C	0100 1100	word	Unused
80	50	0101 0000	word	Timer (uses bytes 50,51 & 52)
84	54	0101 0100	word	Unused
88	58	0101 1000	double-word	External new PSW
96	60	0110 0000	double-word	Supervisor call new PSW
104	68	0110 1000	double-word	Program new PSW
112	70	0111 0000	double-word	Machine-check new PSW
120	78	0111 1000	double-word	Input/output new PSW
128	80	1000 0000	(1)	Diagnostic scan-out area

(1) The size of the diagnostic scan-out area depends on the particular model and I/O channels; for models 30 through 75, maximum size is 256 bytes.

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	7-Track Tape BCDIC (2)	Punched Card Code	System/360 8-bit Code	(3)
128	80	SSM				12-0-8-1	1000 0000	ccw
129	81			a		12-0-1	1000 0001	
130	82	LPSW		b		12-0-2	1000 0010	
131	83	(Diagnose)		c		12-0-3	1000 0011	
132	84	WRD		d		12-0-4	1000 0100	
133	85	RDD		e		12-0-5	1000 0101	
134	86	BXH		f		12-0-6	1000 0110	
135	87	BXLE		g		12-0-7	1000 0111	
136	88	SRL		h		12-0-8	1000 1000	ccw
137	89	SLL		i		12-0-9	1000 1001	
138	8A	SRA				12-0-8-2	1000 1010	
139	8B	SLA				12-0-8-3	1000 1011	
140	8C	SRDL				12-0-8-4	1000 1100	
141	8D	SLDL				12-0-8-5	1000 1101	
142	8E	SRDA				12-0-8-6	1000 1110	
143	8F	SLDA				12-0-8-7	1000 1111	
144	90	STM				12-11-8-1	1001 0000	ccw
145	91	TM		j		12-11-1	1001 0001	
146	92	MVI		k		12-11-2	1001 0010	
147	93	TS		l		12-11-3	1001 0011	
148	94	NI		m		12-11-4	1001 0100	
149	95	CLI		n		12-11-5	1001 0101	
150	96	OI		o		12-11-6	1001 0110	
151	97	XI		p		12-11-7	1001 0111	
152	98	LM		q		12-11-8	1001 1000	ccw
153	99			r		12-11-9	1001 1001	
154	9A					12-11-8-2	1001 1010	
155	9B					12-11-8-3	1001 1011	
156	9C	S10				12-11-8-4	1001 1100	
157	9D	T10				12-11-8-5	1001 1101	
158	9E	H10				12-11-8-6	1001 1110	
159	9F	TCH				12-11-8-7	1001 1111	
160	A0					11-0-8-1	1010 0000	ccw
161	A1					11-0-1	1010 0001	
162	A2			s		11-0-2	1010 0010	
163	A3			t		11-0-3	1010 0011	
164	A4			u		11-0-4	1010 0100	
165	A5			v		11-0-5	1010 0101	
166	A6			w		11-0-6	1010 0110	
167	A7			x		11-0-7	1010 0111	
168	A8			y		11-0-8	1010 1000	ccw
169	A9			z		11-0-9	1010 1001	
170	AA					11-0-8-2	1010 1010	
171	AB					11-0-8-3	1010 1011	
172	AC					11-0-8-4	1010 1100	
173	AD					11-0-8-5	1010 1101	
174	AE					11-0-8-6	1010 1110	
175	AF					11-0-8-7	1010 1111	
176	B0					12-11-0-8-1	1011 0000	ccw
177	B1					12-11-0-1	1011 0001	
178	B2					12-11-0-2	1011 0010	
179	B3					12-11-0-3	1011 0011	
180	B4					12-11-0-4	1011 0100	
181	B5					12-11-0-5	1011 0101	
182	B6					12-11-0-6	1011 0110	
183	B7					12-11-0-7	1011 0111	
184	B8					12-11-0-8	1011 1000	ccw
185	B9					12-11-0-9	1011 1001	
186	BA					12-11-0-8-2	1011 1010	
187	BB					12-11-0-8-3	1011 1011	
188	BC					12-11-0-8-4	1011 1100	
189	BD					12-11-0-8-5	1011 1101	
190	BE					12-11-0-8-6	1011 1110	
191	BF					12-11-0-8-7	1011 1111	

Decimal	Hexadecimal	Mnemonic	Graphic & Control Symbols BCDIC	Graphic & Control Symbols EBCDIC	7-Track Tape BCDIC (2)	Punched Card Code	System/360 8-bit Code	(3)
192	C0		?		B A 8 2	12-0	1100 0000	ccw
193	C1		A	A	B A 1	12-1	1100 0001	
194	C2		B	B	B A 2	12-2	1100 0010	
195	C3		C	C	B A 21	12-3	1100 0011	
196	C4		D	D	B A 4	12-4	1100 0100	
197	C5		E	E	B A 4 1	12-5	1100 0101	
198	C6		F	F	B A 42	12-6	1100 0110	
199	C7		G	G	B A 421	12-7	1100 0111	
200	C8		H	H	B A 8	12-8	1100 1000	ccw
201	C9		I	I	B A 8 1	12-9	1100 1001	
202	CA					12-0-9-8-2	1100 1010	
203	CB					12-0-9-8-3	1100 1011	
204	CC					12-0-9-8-4	1100 1100	
205	CD					12-0-9-8-5	1100 1101	
206	CE					12-0-9-8-6	1100 1110	
207	CF			.		12-0-9-8-7	1100 1111	
208	D0		!		B 8 2	11-0	1101 0000	ccw
209	D1	MVN	J	J	B 1	11-1	1101 0001	
210	D2	MVC	K	K	B 2	11-2	1101 0010	
211	D3	MVZ	L	L	B 21	11-3	1101 0011	
212	D4	NC	M	M	B 4	11-4	1101 0100	
213	D5	CLC	N	N	B 4 1	11-5	1101 0101	
214	D6	OC	O	O	B 42	11-6	1101 0110	
215	D7	XC	P	P	B 421	11-7	1101 0111	
216	D8		Q	Q	B 8	11-8	1101 1000	ccw
217	D9		R	R	B 8 1	11-9	1101 1001	
218	DA					12-11-9-8-2	1101 1010	
219	DB					12-11-9-8-3	1101 1011	
220	DC	TR				12-11-9-8-4	1101 1100	
221	DD	TRT				12-11-9-8-5	1101 1101	
222	DE	ED (4)				12-11-9-8-6	1101 1110	
223	DF	EDMK (4)				12-11-9-8-7	1101 1111	
224	E0		+		A 8 2	0-8-2	1110 0000	ccw
225	E1					11-0-9-1	1110 0001	
226	E2		S	S	A 2	0-3	1110 0010	
227	E3		T	T	A 21	0-3	1110 0011	
228	E4		U	U	A 4	0-4	1110 0100	
229	E5		V	V	A 4 1	0-5	1110 0101	
230	E6		W	W	A 42	0-6	1110 0110	
231	E7		X	X	A 421	0-7	1110 0111	
232	E8		Y	Y	A 8	0-8	1110 1000	ccw
233	E9		Z	Z	A 8 1	0-9	1110 1001	
234	EA					11-0-9-8-2	1110 1010	
235	EB					11-0-9-8-3	1110 1011	
236	EC					11-0-9-8-4	1110 1100	
237	ED					11-0-9-8-5	1110 1101	
238	EE					11-0-9-8-6	1110 1110	
239	EF					11-0-9-8-7	1110 1111	
240	F0		0	0	8 2	0	1111 0000	ccw
241	F1	MVO	1	1	1	1	1111 0001	
242	F2	PACK	2	2	2	2	1111 0010	
243	F3	UNPK	3	3	21	3	1111 0011	
244	F4		4	4	4	4	1111 0100	
245	F5		5	5	4 1	5	1111 0101	
246	F6		6	6	42	6	1111 0110	
247	F7		7	7	421	7	1111 0111	
248	F8	ZAP (4)	8	8	8	8	1111 1000	ccw
249	F9	CP (4)	9	9	8 1	9	1111 1001	
250	FA	AP (4)				12-11-0-9-8-2	1111 1010	
251	FB	SP (4)				12-11-0-9-8-3	1111 1011	
252	FC	MP (4)				12-11-0-9-8-4	1111 1100	
253	FD	DP (4)				12-11-0-9-8-5	1111 1101	
254	FE					12-11-0-9-8-6	1111 1110	
255	FF					12-11-0-9-8-7	1111 1111	

CODE FOR PROGRAM INTERRUPTION

Interruption Code DEC	Interruption Code HEX	Interruption Code BINARY	Program Interruption Cause
1	01	0000 0001	Operation
2	02	0000 0010	Privileged operation
3	03	0000 0011	Execute
4	04	0000 0100	Protection
5	05	0000 0101	Addressing
6	06	0000 0110	Specification
7	07	0000 0111	Data
8	08	0000 1000	Fixed-point overflow
9	09	0000 1001	Fixed-point divide
10	0A	0000 1010	Decimal overflow
11	0B	0000 1011	Decimal divide
12	0C	0000 1100	Exponent overflow
13	0D	0000 1101	Exponent underflow
14	0E	0000 1110	Significance
15	0F	0000 1111	Floating-point divide

SI Format

Op Code	//////////	B₁	D₁
0 7 8 15 16 19 20			31

//////////////////////	Chan Addr	Device Address
0 20 21 23 24		31

$$\left.\begin{array}{l} D1(B1) \\ S1 \end{array}\right\} \text{ HIO, SIO, TCH, TIO}$$

CHANNEL ADDRESS WORD

Key	0000	Command Address
0 3 4 7 8		31
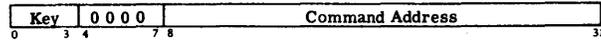
CHANNEL COMMAND WORD

Command Code	Data Address
0 7 8	31

Flags	0 0 0 /////////	Count
32 36 37 39 40 47 48		63
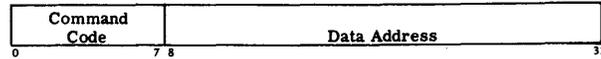
Command Code assignments are listed in the following table. The symbol X indicates that the bit position is ignored; M identifies a modifier bit.

CODE	COMMAND
MMMM 0 1 0 0	Sense
XXXX 1 0 0 0	Transfer in channel
MMMM 1 1 0 0	Read backward
MMMM MM0 1	Write
MMMM MM1 0	Read
MMMM MM1 1	Control

Bits 0-7 specify the command code.
Bits 8-31 specify the location of a byte in main storage.
Bits 32-36 are flag bits; refer to OPERATION CODE tables for flag bit assignments.
  Bit 32 causes the address portion of the next CCW to be used.
  Bit 33 causes the command code and data address in the next CCW to be used.
  Bit 34 causes a possible incorrect length indication to be suppressed.
  Bit 35 suppresses the transfer of information to main storage.
  Bit 36 causes an interruption as Program Control Interrupt
Bits 37-39 must contain zeros.
Bits 40-47 are ignored.
Bits 48-63 specify the number of bytes in the operation.

CHANNEL STATUS WORD

Key	0000	Command Address
0 3 4 7 8		31

Status	Count
32 47 48	63
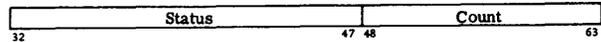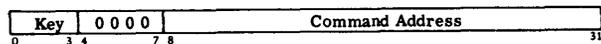
32	Attention	40	Program-controlled interruption
33	Status modifier	41	Incorrect length
34	Control unit end	42	Program check
35	Busy	43	Protection check
36	Channel end	44	Channel data check
37	Device end	45	Channel control check
38	Unit check	46	Interface control check
39	Unit exception	47	Chaining check

Count: Bits 48-63 form the residual count for the last CCW used.

CHANNEL COMMAND CODES

Device	Command for CCW	0	1	2	3	4	5	6	7	Hex	Dec
1050	Read Inquiry BCD	0	0	0	0	1	0	1	0	0A	10
	Read Reader 2 BCD	0	0	0	0	0	0	1	0	02	02
	Write BCD, Auto Carriage Return	0	0	0	0	1	0	0	1	09	09
	Write BCD, No Auto Carriage Return	0	0	0	0	0	0	0	1	01	01
	No Op	0	0	0	0	0	0	1	1	03	03
	Sense	0	0	0	0	0	1	0	0	04	04
2540	Read, Feed, Select Stacker SS Type AA	S	S	D	0	0	0	1	0		
	Read Type AB	1	1	D	0	0	0	1	0		
	Read, Feed (1400 compatibility mode only)	1	1	D	1	0	0	1	0		
	Feed, Select Stacker SS Type BA	S	S	1	0	0	0	1	1		
	PFR Punch, Feed, Select Stacker SS Type BA	S	S	D	1	0	0	0	1		
	Punch, Feed, Select Stacker SS Type BB	S	S	D	0	0	0	0	1		

SS	Stacker
00	R1
01	R2
10	RP3

D	Data Mode
0	EBCDIC
1	Column Binary

Device	Command for CCW	0	1	2	3	4	5	6	7	Hex	Dec
1442 N1	Read	M	M	M	0	0	0	1	0		
	Write	M	M	M	0	0	0	0	1		
	Control	M	M	M	0	0	0	1	1		
	No Op	0	0	0	0	0	0	1	1		
	Sense	0	0	M	M	0	1	0	0		

	M M M			Read/Write/Control/No Op/Sense
Read	0	0	X	Eject and SS1
Read	1	0	X	Eject and SS1
Read	0	1	X	Eject and SS2
Read	1	1	X	Eject and SS2
Write	0	0	X	SS1
Write	1	0	X	Eject and SS1
Write	0	1	X	SS2
Write	1	1	X	Eject and SS2
Control	1	0		Eject and SS1
Control	0	1		SS2
Control	1	1		Eject and SS2
Sense			1 1	Punch diagnostic
Sense			0 1	Read diagnostic

X = 0 means EBCDIC mode
X = 1 means Column Binary Mode

Device	Command for CCW	0	1	2	3	4	5	6	7	Hex	Dec
1403 or 1443	Write, No Space	0	0	0	0	0	0	0	1	01	01
	Write, Space 1 After Print	0	0	0	0	1	0	0	1	09	09
	Write, Space 2 After Print	0	0	0	1	0	0	0	1	11	17
	Write, Space 3 After Print	0	0	0	1	1	0	0	1	19	25
	Write, Skip To Channel N After Print	1	C	H	A	N	0	0	1		
	Diagnostic Read	0	0	0	0	0	0	1	0	02	02
	Test I/O	0	0	0	0	0	0	0	0	00	00
	Sense	0	0	0	0	0	1	0	0	04	04
Carriage Control	Space 1 Line Immediately	0	0	0	0	1	0	1	1	0B	11
	Space 2 Line Immediately	0	0	0	1	0	0	1	1	13	19
	Space 3 Line Immediately	0	0	0	1	1	0	1	1	1B	27
	Skip To Channel N Immediately	1	C	H	A	N	0	1	1		
	No Op	0	0	0	0	0	0	1	1	03	03

C	H	A	N	Channel		C	H	A	N	Channel
0	0	0	1	1		0	1	1	1	7
0	0	1	0	2		1	0	0	0	8
0	0	1	1	3		1	0	0	1	9
0	1	0	0	4		1	0	1	0	10
0	1	0	1	5		1	0	1	1	11
0	1	1	0	6		1	1	0	0	12

Device	Command for CCW	0	1	2	3	4	5	6	7	Hex	Dec
2400 Tape*	Transfer in Channel	0	0	0	0	1	0	0	0	08	08
	Sense	0	0	0	0	0	1	0	0	04	04
	Read Backward**	0	0	0	0	1	1	0	0	0C	12
	Write	0	0	0	0	0	0	0	1	01	01
	Read	0	0	0	0	0	0	1	0	02	02
	Control	0	0	C	C	C	1	1	1		
	Mode Set	D	D	M	M	M	0	1	1		

* 9 track op. forces 800 RPI and odd parity; also, it overrides
  7 track but does not reset 7 track. Load/Sys Reset forces
  7 track to 800 RPI, odd parity, data converter on, translator off.

	C	C	C	Control Codes	Hex	Dec
	0	0	0	REW	7	7
	0	0	1	RUN	0F	15
	0	1	0	ERG	17	23
	0	1	1	WTM	1F	31
	1	0	0	BSR	27	39
	1	0	1	BSF	2F	47
	1	1	0	FSR	37	55
	1	1	1	FSF	3F	63

D	D	7 Track Density
0	0	200
0	1	556
1	0	800
1	1	800

M M M (Mode Modifiers)

			Set Density	Set Odd Parity	Set Even Parity	Data Converter On	Data Converter Off	Translator On	Translator Off	Request TIE (Track In Error)
0 0 0	No Op									
0 0 1	Not Used									
0 1 0	Reset Condition		X	X					X	
0 1 1	Nine-track only						X		X	
1 0 0				X		X			X	
1 0 1			X	X			X	X	X	
1 1 0	Reset Condition		X	X				X	X	
1 1 1			X	X			X	X		

**Overrides Data Converter On

HEXADECIMAL AND DECIMAL INTEGER CONVERSION TABLE

	HALF WORD								HALF WORD						
	BYTE				BYTE				BYTE				BYTE		
	0123		4567		0123		4567		0123		4567		0123		4567
Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	268,435,456	1	16,777,216	1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	536,870,912	2	33,554,432	2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	805,306,368	3	50,331,648	3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	1,073,741,824	4	67,108,864	4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	1,342,177,280	5	83,886,080	5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	1,610,612,736	6	100,663,296	6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	1,879,048,192	7	117,440,512	7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	2,147,483,648	8	134,217,728	8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	2,415,919,104	9	150,994,944	9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	2,684,354,560	A	167,772,160	A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	2,952,790,016	B	184,549,376	B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	3,221,225,472	C	201,326,592	C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	3,489,660,928	D	218,103,808	D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	3,758,096,384	E	234,881,024	E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	4,026,531,840	F	251,658,240	F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
	8		7		6		5		4		3		2		1

TO CONVERT HEXADECIMAL TO DECIMAL

1. Locate the column of decimal numbers corresponding to the left-most digit or letter of the hexadecimal; select from this column and record on a scratch sheet the number that corresponds to the position of the hexadecimal digit or letter.
2. Repeat step 1 for the next (second from the left) position.
3. Repeat step 1 for the units (third from the left) position.
4. Add the numbers selected from the table to form the decimal number.

TO CONVERT DECIMAL TO HEXADECIMAL

1. (a) Select from the table the highest decimal number that is equal to or less than the number to be converted.
   (b) Record the hexadecimal of the column containing the selected number.
   (c) Subtract the selected decimal from the number to be converted.
2. Using the remainder from step 1 (c) repeat all of step 1 to develop the second position of the hexadecimal (and a remainder).
3. Using the remainder from step 2 repeat all of step 1 to develop the units position of the hexadecimal.
4. Combine terms to form the hexadecimal number.

SAMPLE

Conversion of
Hexadecimal   D34

1. D   3328
2. 3   48
3. 4   4
4. Decimal   3380

SAMPLE

Conversion of
Decimal   3380

1. D   - 3328
                               52
2. 3   - 48
                                4
3. 4   - 4
4. Hexadecimal   D34

To convert integer numbers greater than the capacity of the table, use the techniques below:

● HEXADECIMAL TO DECIMAL

Successive cumulative multiplication from left to right, adding units position.

Example: $D34_{16} = 3380_{10}$

$$D = \begin{array}{r} 13 \\ \times\ 16 \\ \hline 208 \end{array}$$
$$3 = +\ 3 \\ \hline 211$$
$$\times\ 16 \\ \hline 3376$$
$$4 = +\ 4 \\ \hline 3380$$

● DECIMAL TO HEXADECIMAL

Divide and collect the remainder in reverse order.

Example: $3380_{10} = X_{16}$

16 ⌊ 3380   remainder
16 ⌊ 211   4
16 ⌊ 13   3
                      D $3380_{10} = D34_{16}$

HEXADECIMAL AND DECIMAL FRACTION CONVERSION TABLE

			HALF WORD									
	BYTE						BYTE					
	0123		4567		0123				4567			
Hex	Decimal	Hex	Decimal	Hex	Decimal			Hex	Decimal Equivalent			
.0	.0000	.00	.0000 0000	.000	.0000	0000	0000	.0000	.0000	0000	0000	0000
.1	.0625	.01	.0039 0625	.001	.0002	4414	0625	.0001	.0000	1525	8789	0625
.2	.1250	.02	.0078 1250	.002	.0004	8828	1250	.0002	.0000	3051	7578	1250
.3	.1875	.03	.0117 1875	.003	.0007	3242	1875	.0003	.0000	4577	6367	1875
.4	.2500	.04	.0156 2500	.004	.0009	7656	2500	.0004	.0000	6103	5156	2500
.5	.3125	.05	.0195 3125	.005	.0012	2070	3125	.0005	.0000	7629	3945	3125
.6	.3750	.06	.0234 3750	.006	.0014	6484	3750	.0006	.0000	9155	2734	3750
.7	.4375	.07	.0273 4375	.007	.0017	0898	4375	.0007	.0001	0681	1523	4375
.8	.5000	.08	.0312 5000	.008	.0019	5312	5000	.0008	.0001	2207	0312	5000
.9	.5625	.09	.0351 5625	.009	.0021	9726	5625	.0009	.0001	3732	9101	5625
.A	.6250	.0A	.0390 6250	.00A	.0024	4140	6250	.000A	.0001	5258	7890	6250
.B	.6875	.0B	.0429 6875	.00B	.0026	8554	6875	.000B	.0001	6784	6679	6875
.C	.7500	.0C	.0468 7500	.00C	.0029	2968	7500	.000C	.0001	8310	5468	7500
.D	.8125	.0D	.0507 8125	.00D	.0031	7382	8125	.000D	.0001	9836	4257	8125
.E	.8750	.0E	.0546 8750	.00E	.0034	1796	8750	.000E	.0002	1362	3046	8750
.F	.9375	.0F	.0585 9375	.00F	.0036	6210	9375	.000F	.0002	2888	1835	9375
	1		2		3				4			

POWERS OF 16 TABLE

16^n	n
1	0
16	1
256	2
4 096	3
65 536	4
1 048 576	5
16 777 216	6
268 435 456	7
4 294 967 296	8
68 719 476 736	9
1 099 511 627 776	10
17 592 186 044 416	11
281 474 976 710 656	12
4 503 599 627 370 496	13
72 057 594 037 927 936	14
1 152 921 504 606 846 976	15

TO CONVERT .ABC HEXADECIMAL TO DECIMAL

Find .A in position 1 .6250

Find .0B in position 2 .0429 6875

Find .00C in position 3 .0029 2968 7500

.ABC Hex is equal to .6708 9843 7500

TO CONVERT .13 DECIMAL TO HEXADECIMAL

1. Find .1250 next lowest to .1300 = .2 Hex
   subtract − .1250

2. Find .0039 0625 next lowest to .0050 0000 = .01
   − .0039 0625

3. Find .0009 7656 2500 .0010 9375 0000 = .004
   − .0009 7656 2500

4. Find .0001 0681 1523 4375 .0001 1718 7500 0000 = .0007
   − .0001 0681 1523 4375

   .0000 1037 5976 5625 = .2147 Hex

5. .13 Decimal is approximately equal to

To convert fractions beyond the capacity of the table, use techniques below:

● HEXADECIMAL FRACTION TO DECIMAL

Convert the hexadecimal fraction to its decimal equivalent using the same technique as for integer numbers. Divide the results by 16^n (n is the number of fraction positions).

Example: $.8A7 = .540771_{10}$

$8A7_{16} = 2215_{10}$

$16^3 = 4096$

$$4096 \overline{\smash{\big)}\,2215.000000} \quad .540771$$

● DECIMAL FRACTION TO HEXADECIMAL

Collect integer parts of product in the order of calculation.

Example: $.5408_{10} = .8A7_{16}$

```
        .5408
        x16
8 ← [8].6528
        x16
A ← [10].4448
        x16
7 ← [7].1168
```

(Use in conjunction with section, "Analyzing an Unexpected Wait.")

Program Waits and Operator Messages

The first character of the code identifies the program being executed when the program wait occurred. The characters and the programs with which they are associated are:

CHARACTER	PROGRAM
A	Assembler (both phases)
1	Assembler (phase 1 only)
2	Assembler (phase 2 only)
D	Dump Programs
G	Loader Generator
I	I/O Support Package
L	Loaders

The second character of the code is concerned with the reason for the program wait. For example, the letter E appears on end-of-file or end-of-job conditions; the letter P, on program checks.

The third character of the code can be one of the following:

A   Operator action is necessary. No decision on the part of the operator is required.

D   Operator action is necessary. The operator must, however, make a decision on the course of action to be taken.

W   A program wait has occurred because of a program or machine check. The job cannot continue.

CODE	HEX	CODE	HEX
AID	C1C9C4	I3A	C9F3C1
AMW	C1D4E7	LAD	D3C1C4
APW	C1D7E7	LDD	D3C4C4
DEA	C4C5C1	LED	D3C5C5
DRA	C4D9C1	LKD	D3D2C4
DTA	C4E3C1	LOD	D3D6C4
GCA	C7C3C1	LPA	D3D7C1
GDD	C7C4C4	LUD	D3E4C4
GEA	C7C5C1	1EA	F1C5C1
GIA	C7C9C1	1TA	F1E3C1
IMW	C9D4E7	2EA	F2C5C1
I0D	C9F0C4	2HA	F2C8C1
I1D	C9F1C4	2SA	F2E2C1

Codes are displayed in bits 40 to 63 of the current PSW.

	Tape to Tape	Tape to Disk	Tape to Card	Tape to Printer	Disk to Tape	Disk to Disk	Disk to Card	Disk to Printer	Card to Tape	Card to Disk	Card to Printer Punch	Clear Disk	Initialize Disk	Storage Print	Multiple Utility	Multiple Disk to Printer	Initialize Tape	Tape Compare	Alternate Track Assignment
JOB Card	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Not Used	Required	Required	Required	Required	Required
ASSGN Cards	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Not Used	Required	Required	Required	Required	Required
UPSI Card	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
CONFG Card	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional
DATE	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Not Used	Required	Required	Required	Required	Required
VOL Card(s)	Required If Label Checking	Required If Label Checking	Required If Label Checking	Required If Label Checking	Required If Label Checking	Required	Required	Required	Required If Label Checking	Required	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
TPLAB Card(s)	Required If Tape Label Checking	Required If Tape Label Checking	Required If Tape Label Checking	Required If Tape Label Checking	Required If Tape Label Checking	Not Used	Not Used	Not Used	Required if Tape Label Checking	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
DLAB Card(s)	Not Used	Required	Not Used	Not Used	Required	Required	Required	Required	Not Used	Required	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
XTENT Card(s) (Up to 5)	Not Used	Required	Not Used	Not Used	Required	Required	Required	Required	Not Used	Required	Not Used	Required	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
LOG Card	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Not Used	Optional	Optional	Optional	Optional	Optional
NOLOG Card	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Optional	Not Used	Optional	Optional	Optional	Optional	Optional
EXEC	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Required	Not Used	Required	Required	Required	Required	Required

	Tape to Tape	Tape to Disk	Tape to Card	Tape to Printer	Disk to Tape	Disk to Disk	Disk to Card	Disk to Printer	Card to Tape	Card to Disk	Card to Printer Punch	Clear Disk	Initialize Disk	Storage Print	Multiple Utility	Multiple Disk to Printer	Initialize Tape	Tape Compare	Alternate Track Assignment
JOB	TAPTAP	TAPDSK	TAPCAR	TAPPRT	DSKTAP	DSKDSK	DSKCAR	DSKPRI	CARTAP	CARDSK	CDPRPN	CLRDSK	INTDSK	NOT USED	MUT8K	MDKPRN	INITTP	TPCP	ATASGN
VOL (File name)	UIN UOUT	UIN UOUT	UIN	UIN	UIN UOUT	UIN UOUT	UIN	UIN	UOUT	UOUT	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED
ASSGN Primary Input	SYSIPT	SYSIPT	SYSIPT	SYSIPT	SYSIPT	SYSIPT	SYSIPT	SYSIPT	SYSIPT	SYSIPT	SYSIPT	NOT USED	NOT USED	NOT USED	**	(A)SYSIPT (B)SYS000 (C)SYS002	NOT USED	SYSIPT SYS000	NOT USED
ASSGN Primary Output	SYSOPT	SYSOPT	SYSOPT	SYSOPT	SYSOPT	SYSOPT	SYSOPT	SYSOPT	SYSOPT	SYSOPT	* SYSOPT	SYSOPT	SYSOPT	NOT USED	**	(A)SYSOPT (B)SYS001 (C)SYS003	SYS000	SYSOPT (To Print Unmatched Records)	SYSOPT
ASSGN Alternate Tape Input	SYS000	SYS000	SYS000	SYS000	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	**	NOT USED	NOT USED	SYS001 SYS002	NOT USED
ASSGN Alternate Tape Output	SYS001	NOT USED	NOT USED	NOT USED	SYS001	NOT USED	NOT USED	NOT USED	SYS001	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	SYS001- SYS015	NOT USED	NOT USED
ASSGN Additional Input & Output Disk Drives	NOT USED	SYS002 SYS003 SYS004 SYS005	NOT USED	NOT USED	SYS002 SYS003 SYS004 SYS005	SYS002 SYS003 SYS004 SYS005	SYS002 SYS003 SYS004 SYS005	SYS002 SYS003 SYS004 SYS005	NOT USED	SYS002 SYS003 SYS004 SYS005	NOT USED	SYS002 SYS003 SYS004 SYS005	SYS002 SYS003 SYS004 SYS005	NOT USED	NOT USED	(A)SYS004 (B)SYS005 (C)SYS006	NOT USED	NOT USED	NOT USED
ASSGN Printer for Card to Printer and/or Punch	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	SYSLST	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED
ASSGN Device for Logging	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG	NOT USED	SYSLOG	SYSLOG	SYSLOG	SYSLOG	SYSLOG

* Always the punch unit
** The assignment of I/O devices for this program is:

Primary Tapes	Alternate Tapes	Unit Record Devices
(A)SYS000	(A)SYS001	(A)SYS006
(B)SYS002	(B)SYS003	(B)SYS007
(C)SYS004	(C)SYS005	(C)SYS008

Appendix E: Bit Meanings of Displays

A detailed description of the bit meanings of status indicator displays is given in this appendix. (Refer to "Status Indicator" for usage of these displays.)

Switch 1, Position 1: Common Channel Instruction Status

INDICATOR	BIT POSITION	DESCRIPTION
I/O INSTRUCTION	0-3	The CPU generated I/O instruction turns on the appropriate indicator—start I/O, test I/O, halt I/O, or test chan. The indicator is on until the channel responds.
CHAN NUMBER	4-6	Selected channel number in binary.
INSTRUCTION REPLY	7-10	Indicates the condition code with which the channel responded to an I/O instruction.
REPLY	11	Reply is on when a reply to an instruction is received from a channel.
BCHI	12	Branch on channel interrupt is on whenever an unmasked channel wants to interrupt. The latch is checked by the microprogram during I-fetch.
PRCD ON IRPT	13	Proceed on interrupt is turned on by a signal from CPU in reply to BCHI.
TIME OUT	14	Time out is on after an I/O instruction or proceed on interrupt is given to the channel and CPU has not received a reply for 74 μs.
TIME OUT CHK	15	Time out check is on if an answer is not received from the channel after time out.
FOUL	16	Foul is on if there is a program check on a start I/O instruction that is detected by CPU microprogram.

Switch 1, Position 2: Common Channel I/O Routine Status

INDICATOR	BIT POSITION	DESCRIPTION
RTNE RCVD	0	Routine received is on when a request to break into CPU is granted.
PCI ENABL	1	PCI enable is on during a PCI routine.
BREAK IN	2	Break in is on after a routine received signal has been received and break in is occurring.
I/O RTNE	3	I/O routine is on whenever an I/O routine is being processed.
EARLY FIRST CYCLE	4	Early first cycle is on early in the first cycle of an I/O routine.
FIRST CYCLE	5	First cycle is on during the first cycle of an I/O routine.

INDICATOR	BIT POSITION	DESCRIPTION
CHAIN FIRST CYCLE	6	Chain first cycle is on during the first cycle of a chained routine. (One routine is finished and the next started without CPU breaking in.)
LS RD	7	Local store read is on during a local store read routine when data are transferred from the B register to the local store buffer.
LS WR	8	Local store write is on during a local store write routine when data are transferred from the local store buffer to the B register.
CHAL DTC	9	Channel to adder latch data transfer and control is on when the microorder is given telling a selector channel to transfer information from the channel to the adder latch.
ALCH DTC	10	Adder latch to channel data transfer and control is on when the microorder is given telling a selector channel to transfer information from the adder latch to the channel.
CHAIN	11	Chain is on during the last cycle of a routine and indicates that another routine is to be chained into.
LAST CYCLE	12	Last cycle is on during the last cycle of a routine and indicates that chaining to another routine will not occur.
BREAK OUT	13	Break out is on when a routine is completed and CPU and ROS are restored to the point they were at before break in.
SBCR	14-17	Storage byte control register is used by the selector channel to designate the bytes that are to be placed in storage during a read store.
——	18	Spare position.
ROS BITS 33, 34	19-20	ROS bits 33 and 34 represent timing signals to the channel (I/O mode).
ROS BITS 47, 48	21-22	ROS bits 47 and 48 represent control signals to the channel (I/O mode).
FIRST CYCLE CHK	23	First cycle check is made during the first cycle to make sure that ROS is really in the first cycle of an I/O routine.

Switch 1, Position 3: Common Channel Control Registers

INDICATOR	BIT POSITION	DESCRIPTION
BUFFER 1, 2, 3	0-11	The buffer registers indicate the channels using the CPU. They are used to gate control information and errors to the channel.

INDICATOR	BIT POSITION	DESCRIPTION
I/O STATS	12-16	I/O stats indicate the condition of the five I/O stats that set conditions for microprogram branching. They are set by the selector channel on break in.
—	17	Spare position.
I/O CHECK MODE	18	I/O check mode is on to indicate that the channel is using CPU and any errors detected in the CPU could be caused by the channel.
LOGS 1, 2, 3	19-21	Log 1, 2, or 3 indicates the number of the selector channel that is being logged.
LOG GATE STATUS	22	Log gate status is on after a log-out allowing the channel that was logged to gate its status to CPU.
LOG RESET	23	Log reset is on after the gate stat has been turned off to provide a reset to the channel that was logged.

Switch 1, Position 4: Multiplexor Channel, Data Buffers

INDICATOR	BIT POSITION	DESCRIPTION
BUFFER 1	0-8	Contents of buffer 1 plus parity.
BUFFER 2	9-17	Contents of buffer 2 plus parity.
REQ LOG-OUT	23	Request log-out indicates an error in the multiplexor channel is conditioning a log-out request.

Switch 1, Position 5: Multiplexor Channel, Interface and Control

INDICATOR	BIT POSITION	DESCRIPTION
SEL OUT	0	Indicates when select out is up on the interface.
SEL IN	1	Indicates when select in is up on the interface.
OP IN	2	Indicates when op in is up on the interface.
SUP OUT	3	Indicates when suppress out is up on the interface.
REQ IN	4	Indicates when request in is up on the interface.
SVC OUT	5	Indicates when service out is up on the interface.
ADR OUT	6	Indicates when address out is up on the interface.
CMND OUT	7	Indicates when command out is up on the interface.
SVC IN	8	Indicates when service in is up on the interface.
ADR IN	9	Indicates when address in is up on the interface.
STAT IN	10	Indicates when status in is up on the interface.
—	11-12	Spare positions.
BUS OUT	13-21	Displays the information that is on bus out plus parity.
PRGM CHK	22	Indicates a boundary violation in storage.
STOR PROT CHK	23	Indicates that data are trying to be stored in a protected storage location and the keys do not match.

Switch 1, Position 6: Multiplexor Channel, Control Triggers

INDICATOR	BIT POSITION	DESCRIPTION
CONTROLLED EMIT	0-3	Indicates the contents of the ROS Emit Field at the time a DTC is issued.
ROUTINE REQUEST TGRS	4-8	Indicates the address of the first microinstruction of the routine requested or of the routine presently being run.
PRIORITY	9-10	Indicates the priority of the routine requested.
PCI	11	Indicates a request for a PCI routine.
CC	12	Indicates that the UCW the channel is working with contains a CC flag.
DTC	13	Indicates when a microorder DTC timing signal is given to request the next routine.
UCW	14	Indicates when a device disconnects from the interface that a new count word and data address word are to be stored in the UCW in bump.
IB FULL	15	Indicates whenever there is an interrupt pending in the channel.
POLL	16	Indicates whenever the channel is idle (Poll State).
BURST MODE	17	Indicates the multiplexor channel interface is operating in the burst mode.
MPX I/O STAT	18-21	Indicates the condition of the multiplexor I/O stats used for microprogram branching.
DATA XFR CTRL	22	Indicates a byte of data is being transferred in either direction over the interface.
CC RESET CTRL	23	Indicates the presence of a signal to reset the command chain flag because of an error condition.

Switch 2, Position 1: Selector Channel B Register

Bit positions 0, 9, 18, and 27 display the parity of the associated byte. The B register is connected on one side to the CPU adder latch and on the other to the C register.

Switch 2, Position 2: Selector Channel C Register

Bit positions 0, 9, 18, and 27 display the parity of the associated byte. The C register ties directly to the interface for byte assembly and disassembly.

Switch 2, Position 3: Selector Channel Byte Counter

INDICATOR	BIT POSITION	DESCRIPTION
BYTE COUNTER A	0-2	Byte counter phase A and parity.
BYTE COUNTER B	3-5	Byte counter phase B and parity.

INDICATOR	BIT POSITION	DESCRIPTION
END REG	6-7	The end register points to the last byte plus one to be transferred.
LAST WORDS	8-10	The last word latches control the last three words in a read or write routine.
EOR COUNT INTLK	11	Indicates when the channel has stored the fourth from the last word in a read operation or has fetched the last word in a write operation.
EOR 1	12	Indicates when the interface is using the last word latches.
EOR 2	13	Indicates when the external channel controls are using the last word latches.
EOR READ INTLK	14	Indicates when the interface logic has finished using the last word latches and is requesting the external channel control to take over.
B AC	15	B register almost changed indicates that local store is being bypassed in the data transfer path.
LS ENABL	16	Local store enable indicates that data will be transferred between local store and the B register.
REGS FULL	17-19	Indicate when local store, the B register, or the C register contain data.
READ BACKWARD	20	Read backward indicates a read backward op has been decoded.
READ OP	21	Read op indicates a read type op has been decoded.
READ RDY	22	Read ready indicates that the channel is performing a read type op and is permitted to make data store requests.
READ IF	23	Read interface indicates that the interface is now ready to read.
WRITE OP	24	Write op indicates a write type op has been decoded.
WRITE RDY	25	Write ready indicates that the channel is performing a write type op and is permitted to make data fetch requests.
WRITE IF	26	Write interface indicates that the interface is now ready to write.
CD=PC TYPE CHK	27	CD=PC type check indicates a program check during a write data chaining CCW fetch sequence.
SIM CHK	28	Simulated check indicates that the channel will interrupt without the unit's status.
ILI CHK	29	Incorrect length indicates that the number of bytes contained in the storage areas assigned is not equal to the number requested or offered.
PRGM CHK	30	Program check indicates that the channel has detected a program error.
STOR PROT CHK	31	Storage protect check indicates that the associated protect keys do not match.
CHAN DATA CHK	32	Channel data check indicates when an error is detected on any data transfer to or from an I/O device.

INDICATOR	BIT POSITION	DESCRIPTION
CHAN CTRL CHK	33	Channel control check indicates when there is any machine malfunction that affects channel controls.
IF CTRL CHK	34	Interface control check indicates when there was an invalid signal combination or sequence on the interface.
CHAIN 1 CHK	35	Chaining check indicates when there is a channel overrun. (Channel assumed a wrong starting address or count while waiting for the information—during input chaining operations only.)

Switch 2, Position 4: Selector Channel Position Register

INDICATOR	BIT POSITION	DESCRIPTION
POSITION REGISTER	0-8	The position register indicates the routine that the channel is processing or has processed last. The nine indicators are: UA fetch, CCW 1 type, CCW 2 type, unit sel, rd store, wr fetch, end up, comp, and irpt.
CYCLE COUNTER	9-12	The cycle counter indicates the number of times the A clock has cycled through in a particular routine.
CLOCK	13-15	Indicates the position the A clock is presently in.
LS REQ	16	Local store request indicates when local store data are requested.
PCI REQ	17	Program controlled interrupt request indicates that a maskable type of interrupt is being requested.
PRIORITY	18-20	Indicates the priority of the routine requested.
REQUEST REGISTER	21-26	The request register, in conjunction with the selected priority, identifies the routine being requested by the channel.
STAT	27-30	Indicates the I/O stats used for microprogram branching in the requested routine.
COM CHAN DETECT	31-34	Indicates that the common channel has detected a routine request from the channel.
CCD INH RTNE	35	Indicates that the detect registers (Pri 1, 2, 3, PCI) are inhibited from being set.

Switch 2, Position 5: Selector Channel Control Registers

INDICATOR	BIT POSITION	DESCRIPTION
POS REG TRF	0	Position register transfer indicates that a routine was transferred from the request to the position register but has not yet been serviced.
INH RD STOR	1	Inhibit read store indicates that the channel will inhibit storing of extra data on an overrun when chaining.

INDICATOR	BIT POSITION	DESCRIPTION
A CLOCK	2-5	Displays the A clock latches that control the A clock.
SP D1	6	Selector channel D1 special purpose latch is used to set program check if a CCW specifying a TIC addresses another CCW that also specifies a TIC.
SP D2	7	Selector channel D2 special purpose latch is used for request compare routine in a test I/O operation.
INSN SCAN	8	Instruction scan indicates that the channel is idle and ready to perform an operation.
CHAN IN USE	9	Channel in use indicates the channel is performing an operation.
POLL	10	Poll indicates the channel is polling the interface due to a request in.
POLL IRPT END	11	Poll interrupt end indicates that everything needed from the selected unit has been received and the CPU is now to be interrupted.
INSN INH	12	Instruction inhibit is on when the channel is fetching a CCW (other than initial) and is used to prevent any instruction line from affecting a unit selection.
BC RDY	13	Byte counter ready indicates that the new byte counter value has been obtained from a CCW.
UA TO BUS O	14	Unit address to bus out indicates when, in the unit select routine, bus out contains the unit address.
U SEL ADR OUT	15	Unit select address out indicates when the address out line is active on the interface during the unit select routine.
COMPARE	16-17	Compare equal or not equal indicates the compare result between the address sent out on the interface and the address received back during unit selection.
STOP	18	Stop indicates when the interface stop trigger is on.
IF CDA FIRST BYTE	19	Interface CDA first byte places the first byte of the new record into all bytes of the C register if it has been received before a new value for the byte counter has been obtained from the CCW.
CD	20	The chain data latch is used during data chaining to differentiate between a CCW requiring a unit selection and one that does not.
BC MOD ENABL	21	Byte counter mod enable indicates when the interface controls permit the channel to modify the byte counter.
WR CHAIN RDY	22	Write chain ready indicates when a new CCW is completely fetched during data chaining.
REC END	23	Record end indicates the end of any operation.
OP IN TEST	24	Operational in test indicates if op in falls during the period that select out is up.

INDICATOR	BIT POSITION	DESCRIPTION
CHAN STOP	25	Channel stop condition indicates the channel is unable to continue operation.
SEL OUT	26	Indicates when select out is up on the interface.
STOP RTNE	27	Stop routine indicates an interface stop sequence.
SEL IN	28	Indicates when select in is up on the interface.
OP IN	29	Indicates when operational in is up on the interface.
SVC OUT	30	Indicates when service out is up on the interface.
ADR OUT	31	Indicates when address out is up on the interface.
CMND OUT	32	Indicates when command out is up on the interface.
SVC IN	33	Indicates when service in is up on the interface.
ADR IN	34	Indicates when address in is up on the interface.
STAT IN	35	Indicates when status in is up on the interface.

Switch 2, Position 6: Selector Channel Registers

INDICATOR	BIT POSITION	DESCRIPTION
——	0	Spare position.
GENERAL PURPOSE REGISTER	1-7	The general purpose register is used as a buffer for prefetched control information and for byte control on input data.
——	8-10	Spare position.
FLAG REG	11-15	The flag register indicates when the associated flag bit in the CSW is active.
FIN	16	Finish indicates the end of each routine.
FIRST WORD	17	First word remains on until the first word in the record is stored or fetched.
——	18	Spare position.
FIRST BYTE	19	First byte remains on until the first byte is received on the interface.
TOTAL REC FETCH	20	Total record fetch indicates that a CCW and its data have been completely prefetched on a write data chain operation.
WR CHAIN PRCD	21	Write chain proceed indicates when the data under control of the previous CCW have been completely transmitted.
STOP REL	22	Stop release drops select out and ends an interface sequence.
——	23-25	Spare positions.
STAT NEXT	26	The status next latch represents special program check conditions that should block the setting of incorrect length.
——	27	Spare position.
MP	28-31	The multipurpose latches (C1, C2, C3, C4) indicate specific conditions during execution of an I/O routine.

INDICATOR	BIT POSITION	DESCRIPTION
SUP OUT	32	Suppress out indicates the suppress out line is up on the interface.
REQ IN	33	Indicates request in is up on the interface.
SVC OUT HOLD	34	Service out hold indicates the channel is holding service out up until it has the first word ready to send over the interface.
BLOCK STAT IN	35	Block status in indicates the channel is blocked from receiving status in.

Switch 3, Position 1: CPU L Register

Indicators (0-35) display the contents of the L register. The L register is a primary source of data for adder XG input and buffer for local store. The L register can also gate a byte of data at a time to the mover. Bit positions 0, 9, 18, and 27 display the parity of the associated byte.

Switch 3, Position 2: CPU R Register

Indicators (0-35) display the contents of the R register. The R register is a primary source of data for adder Y input and buffer for local store. The R register can also gate a byte of data to the mover. Parity is displayed in bit positions 0, 9, 18, and 27.

Switch 3, Position 3: CPU M Register

Indicators (0-35) display the contents of the M register. The M register is an alternate source of data for adder Y input and can gate its four bytes to the mover V input. Parity is displayed in bit positions 0, 9, 18, and 27.

Switch 3, Position 4: CPU H Register

Indicators (0-35) display the contents of the H register. The H register is an alternate source of data for adder Y input. Parity is displayed in bit positions 0, 9, 18, and 27.

Switch 3, Position 5: CPU SAR and Byte Stats

INDICATOR	BIT POSITION	DESCRIPTION
SAR	0-26	The storage address register is used for addressing main and bump storage. Bit positions 0, 9, and 18 display the parity of the associated byte.
BYTE STATS	28-31	Indicates byte stats 0, 1, 2, and 3.
BYTE STORE STATS	32-35	Indicates byte store stats 0, 1, 2, and 3.

Switch 3, Position 6: CPU ROSDR (56-89)

INDICATOR	BIT POSITION	ROSDR POSITION	DESCRIPTION
P	0	56	Parity of bits 57-89.
CE	1-4	57-60	Emit field.
LX	5-7	61-63	Left input to adder (XG).
TC	8	64	True or complement to left adder input (XG).
RY	9-11	65-67	Right input to adder (Y).
AD	12-15	68-71	Adder function (CPU mode).
CL	12-14	68-70	Selector channel adder latch tests (I/O mode).
—	15	71	Spare position (I/O mode).
AB	16-21	72-77	Condition branch test A (furnishes bit 11 of next ROS address).
BB	22-26	78-82	Condition branch test B (furnishes bit 12 of next ROS address).
—	27	83	Spare position.
SS	28-33	84-89	Stat setting and miscellaneous control.

Switch 4, Position 1: CPU ROSDR (0-30)

INDICATOR	BIT POSITION	ROSDR POSITION	DESCRIPTION
P	0	0	Parity of bits 1-30.
LU	1-3	1-3	Left input to mover (U).
MV	4-5	4-5	Right input to mover (V).
ZP	6-11	6-11	Bits 1-6 of next ROS address.
ZF	12-15	12-15	Source of bits 7-10 of next ROS address.
ZN	16-18	16-18	ROS addressing mode.
—	19		Spare position.
TR	20-24	19-23	Destination of adder latch contents.
—	25	24	Spare position.
WS	26-28	25-27	Local store address control.
CS	26	25	Local store address sector (I/O mode).
SA	27-28	26-27	Local store address (I/O mode).
SF	29-31	28-30	Local store function.

Switch 4, Position 2: CPU ROSDR (31-55) and Mover Function

INDICATOR	BIT POSITION	ROSDR POSITION	DESCRIPTION
P	0	31	Parity of bits 32-55.
IV	1-3	32-34	Invalid digit test and instruction address control (CPU mode).
CT	1-3	32-34	Timing signals to external channel (I/O mode).
AL	4-8	35-39	Shift control and gating into adder latch.
WM	9-12	40-43	Mover destination (CPU mode).
WL	9-11	40-42	Mover destination (I/O mode).
HC	12	43	Insert carry control (I/O mode).
UP	13-14	44-45	Byte counter function control (CPU mode).
MD	15	46	MD counter control (CPU mode).
MS	13-15	44-46	Multiplex stat setting (I/O mode).

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INDICATOR	BIT POSITION	ROSDR POSITION	DESCRIPTION
LB	16	47	LB counter control (CPU mode).
MB	17	48	MB counter control (CPU mode).
CG	16-17	47-48	Control signal gating to channel (I/O mode).
DG	18-20	49-51	Length counter and carry insertion control (CPU mode).
MG	18-20	49-51	Multiplex channel gate control (I/O mode).
UL	21-22	52-53	Mover function left digit.
UR	23-24	54-55	Mover function right digit.
—		25	Spare position.
MOVER FUNCTION CPU	26-28		CPU mover function register.
MOVER FUNCTION I/O	29-31		I/O mover function register.

Switch 4, Position 3: CPU ROAR

INDICATOR	BIT POSITION	DESCRIPTION
ONE SYL OP	0	One syl op trigger indicates a half word instruction.
REFETCH	1	Refetch stat indicates that the instruction buffer should not be used as the source of the next instruction.
ROS BASE ADR	6-11	ROS base address (bits 0-5 of ROAR).
FUNCTION BIT	12-15	ROS address function field (bits 6-9 of ROAR).
BRANCH A	16	A branch (bit 10 of ROAR).
BRANCH B	17	B branch (bit 11 of ROAR).
EXT IRPT REG	18-23	External interrupt register.
PSW	24-31	PSW 32-39.

Switch 4, Position 4: CPU Byte Counters

INDICATOR	BIT POSITION	DESCRIPTION
I/O MODE	0	I/O mode trigger is on during I/O routines.
I/O REG	1-3	I/O register and parity (used for byte addressing in I/O mode).
TIMER IRPT	4	Timer interrupt stat (set by timer counting to zero).
CONS IRPT	5	Console interrupt stat (set by console interrupt switch).
L BYTE CNTR	6-8	L byte counter and parity (L register byte selection).
M BYTE CNTR	9-11	M byte counter and parity (M register byte selection).
F REG	12-16	F register and parity (4 bit shift spill and enter).
Q REG	17	Q register (1 bit shift spill and enter).
EDIT STATS	18-19	Edit stats control operation during edit instruction.

INDICATOR	BIT POSITION	DESCRIPTION
GP STATS	20-27	General purpose stats 0-7 (multi-purpose stats).
L SIGN	28	L register sign stat (on for positive).
R SIGN	29	R register sign stat (on for positive).
CARRY	30	Carry stat (on for carry insert).
RTL	31	Retry threshold latch indicates whether instruction retry is possible (tested by SERR program).
STORAGE RING	32-35	Storage ring positions R1, R2, R3, and W1.

Switch 4, Position 5: CPU LSAR

INDICATOR	BIT POSITION	DESCRIPTION
LSAR	0-6	Local store address register plus parity.
FN LS	7-8	Local store function register (local store addressing).
J REG	9-13	J register plus parity (local store addressing).
MD	14-18	MD counter plus parity (local store addressing and decimal multiplication and division).
—	19	Spare position.
G1	20-25	Length counter 1 plus sign and parity (G1 storage field length counter).
G2	26-31	Length counter 2 plus sign and parity (G2 storage field length counter).

Switch 4, Position 6: CPU Error Register

BIT POSITION	DESCRIPTION	BIT POSITION	DESCRIPTION
0	Half sum 0-7	14	Mover left input
1	Half sum 8-15	15	Mover right input
2	Half sum 16-23	16	Mover output
3	Half sum 24-31	17	Local store address
4	Sum 0-7	18	Storage address register 8-15
5	Sum 8-15	19	Storage address register 16-23
6	Sum 16-23	20	Storage address register 24-31
7	Sum 24-31	21	ROS 1-30
8	Carry	22	ROS 32-55
9	L byte counter	23	ROS 57-89
10	M byte counter	24	Storage protect
11	MD counter	25	LCS summary check
12	G1 length counter	26	Log request (Turned on by log-out switch or common chan log-out request)
13	G2 length counter	27-31	Spare positions

Switch 4, Position 7: CPU Current ROS Address (Bit Positions 6-17)

Switch 4, Position 8: CPU Previous ROS Address (Bit Positions 6-17)

Appendix F: Input/Output Operation

This section describes the operation of typical i/o devices that may be attached to IBM System/360. In addition to the information about operation of keys and lights, general information about magnetic tape and basic card machine features is included.

These devices are inherently mechanical and, once started in motion, will continue to move for a predetermined time. The tape unit moves tape from interblock gap (IBG) to IBG. The card equipment (card reader and card punch) motion is from card to card. Printer motion is from line to line. This motion, once started, cannot normally be stopped.

Magnetic Tape Unit

Magnetic Tape Handling

Dust Prevention

Foreign particles on tape can reduce the intensity of reading and recording pulses by increasing the distance between the tape and the read/write head. Be extremely careful to protect magnetic tape from dust and dirt.

Keep the tape in a dust proof container whenever it is not in use on a tape unit. When a reel of tape is removed from a tape unit, immediately place it in a container. Always place appropriate grommets or special clips on the reels as they are stored, to prevent the free end from unwinding in the container.

While the tape is on the machine, close the container; put it in some location where it is not exposed to dust and dirt.

Store tapes in some type of cabinet elevated from the floor and away from sources of paper or card dust. This should minimize the transfer of dust from the outside of the container to the reel during loading or unloading operations.

Never use the top of a tape unit as a working area. Placing materials on top of the units exposes them to heat and dust from the blowers in the unit. It might also interfere with the cooling of the tape unit.

To label a reel of tape for identification, other than by means of the provided card holder, use a material that can be removed without leaving a residue. Adhesive stickers that can be applied and removed easily are satisfactory. Never use an eraser to alter the identification on a label.

Damage Prevention

Information is recorded within 0.020 inch of the edge of the tape. Proper operation requires that the edge of the tape be free from nicks and kinks.

Handle reels near the hub whenever possible. In picking up reels, grip the reel between the center hole and the outer edge. Gripping the reel so as to compress its outer edges pinches the few turns of the tape near the outer edge of the reel. Persons handling tape reels inside and outside the machine room should be instructed to avoid pinching the reels or having contact with the exposed edges of the tape.

Dropping a reel of tape can easily damage both the reel and the tape. Never throw or mishandle reels even while they are protected in their containers.

Cleaning Tape and Tape Container

To clean a tape, gently wipe the tape with a clean, lint-free cloth moistened with an IBM recommended tape transport cleaner.

Inspect containers periodically. Remove any accumulation of dust by washing with a regular household detergent.

Tape Break

If a tape break occurs, divide the reel into two smaller reels. It may be necessary to make a temporary splice in order to recover information; however, splicing is not recommended as a permanent correction procedure. In making a temporary splice, be sure to use the special low-cold-flowing splicing tape.

Dropped-Tape Inspection

If a reel of tape has been dropped, the reel may be broken or bent (bending is less likely, as a strain sufficient to bend a reel usually breaks it), the edge of the tape may be crimped, and the tape may be soiled. To test for and remedy these defects:

1. Inspect the tape reel immediately. Breaking or bending of the reel can usually be found by visual inspection. In addition, check the reel for bending by mounting it on the hub of a tape unit. If the reel has been bent or broken, it obviously should not be used again but the tape may be serviceable.

2. Inspect the tape itself:
   a. If there is no evidence of crimping or other tape damage, and the reel is undamaged, thoroughly clean the tape (exposed or unwound) and reel. The tape is then in good operating condition. If at all possible, test to verify that the tape operates properly before using it on subsequent runs.
   b. If there is no evidence of tape damage, but the reel is damaged, thoroughly clean the tape (exposed or unwaged) and rewind it on another reel. If possible, test to verify that the tape operates properly.
   c. If the edge of the tape is crimped, the action to be taken depends on whether the tape contains essential information. If the tape does not contain essential information, discard the crimped footage. If the tape contains essential information, thoroughly clean the tape and attempt to reconstruct this information through a tape-to-printer or other machine operation. Should reconstruction fail, the records in question must be rewritten from cards or from another source.

Tape Unit

The IBM 2400-series tape unit is a typical tape unit. For detailed information on this device see *IBM 2400 and 2816 Model 1 Component Description*, Form A22-6866. The 2400 tape unit is briefly described here. The operator panel is shown in Figure 7. The lights are on the upper row; the keys are on the lower row. The reel door interlock and the reel release are accessible only when the reel door is open.

Operator Keys—2401-2404 All Models

Load Rewind: Pressing this key initiates a tape loading or a rewind operation. The load-rewind key is operative only when the reel door is closed and the ready light is off. Use of this key after tape is properly mounted in the magnetic tape unit lowers tape into the columns, lowers the head assembly, and moves tape in the rewind direction until the load point reflective marker is sensed. The purpose of this key is to set the tape into the machine at the starting point (load point), ready for either reading or writing.

Use of the load-rewind key with tape loaded and the machine reel containing more than $\frac{1}{2}$ inch of wound tape initiates a high-speed rewind operation. The amount of tape to be rewound is measured automatically by a light-beam and photocell mechanism in the tape unit. Tape is removed from the columns, the head assembly is raised, and tape is rewound at high speed until less than $\frac{1}{8}$ inch of wound tape remains on the machine reel. Tape is then lowered into the columns, the head assembly is lowered, and a low-speed rewind continues until the load point marker is sensed.

Use of the load-rewind key with tape loaded and the machine reel containing less than $\frac{1}{2}$ inch of wound tape initiates a low-speed rewind until the load point marker is sensed. *Caution—do not open the reel door during rewind or load point searching. This could cause breaking or damaging of the magnetic tape.*

Start: This key places the tape unit in ready status and turns on the ready light if:
   1. Reel door is closed.
   2. Tape is loaded into the columns.
   3. Tape unit is not in the process of rewinding.
Pressing the start key disables all manual controls.

Unload: This key initiates a tape unload operation. The unload key is operative only when:
   1. Ready light is off.
   2. Tape is in columns.
   3. Reel door is closed.
Use of this key raises the head assembly and removes tape from the columns, regardless of the distribution of
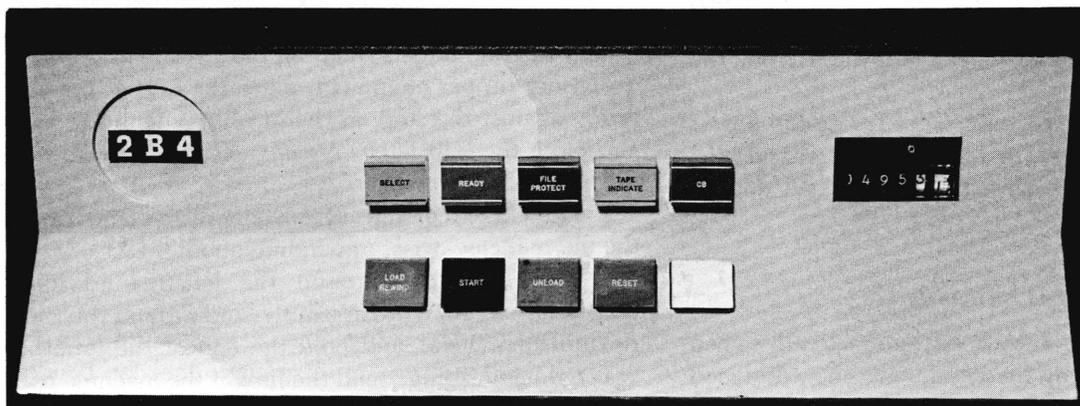
Figure 7. IBM 2401-2404 Operator Panel

the tape on the two reels. If the tape is not at load point when the operator wishes to change tape reels, a load point search should be initiated first by pressing the load-rewind key. Pressing the unload key also turns off the tape indicate light, if on.

Reset: This key resets the tape unit from ready status. In this condition, no operations can be performed through the tape control. The reset key is used to return the tape unit to manual control. Pressing the key removes the machine from ready status, if it has not already been removed, and stops whatever machine operation is in progress, except for unload. The unload operation is always completed, once started; the high-speed rewind operation is shifted into low-speed rewind. After the tape is loaded into the vacuum columns and low-speed rewind is in progress, press the reset key again to stop the low-speed rewind.

Reel Door Interlock: This interlock automatically prevents any normal operation of the tape unit when the door is open. The reel door should never be opened when the ready light is on or during any load-rewind operation.

Reel Release: This key may be pressed to permit the reels to be turned manually for threading tape when the reel door or power window is open.

Power Window

The reel door for the 2401-2404 Models 1-6 includes a tape access window that automatically opens following a tape unload and closes prior to a tape load operation. In addition to the operator key functions (previously described), key functions related to the power window are:

Load Rewind: Pressing this key causes the power window to raise and close before starting the load rewind operation. If any object prevents the power window from closing, it will operate the safety bail at the top of the reel door causing the window to reverse direction and lower until fully open.

Unload: When the tape unit is loaded and not ready, pressing the unload key causes the power window to open after the tape has been unloaded from the columns.

Reset: This key may be used just to close the power window, e.g., when the tape unit is unloaded and idle. The window cannot be closed while the reel door is open.

Operator Lights—2401-2404 All Models

Select: This light is turned on automatically when the unit is addressed by the computer. The addressed tape unit must be ready before it can be instructed by the program.

Ready: When this light is on, it indicates that the tape unit is properly loaded, the start key has been pressed, and the tape unit can now be activated through the tape control. The ready light is turned on by pressing the start key if:

1. Tape unit is loaded—tape in columns.
2. Reel door interlock is closed.
3. Tape unit is not in the process of finding load point.

Pressing the start key while the tape is in motion, as in a load-rewind operation, does not light the ready light until the load rewind is completed. The reel door should not be opened when the ready light is on. Manual control is indicated when the ready light is off, if the tape unit is not rewinding or loading and the reel door is closed.

File Protect: When this light is on, it indicates that the loaded tape unit is file protected, that is, neither writing nor erasing can take place on this tape unit. The file protect light is on when:

1. No file reel is mounted.
2. A file-protect tape reel is mounted.
3. A load-rewind operation is in progress.
4. An unload operation is in process.

The indicator is turned off by mounting a tape reel that is not file protected. If the file protection ring has been removed and this light fails to go on, notify the customer engineer.

CB: When the light is on, it indicates that a circuit breaker has been tripped. The tape unit cannot operate until the circuit breaker has been reset by a customer engineer.

Tape Indicate: When this light is on, it signifies that an end-of-tape marker has been sensed during a forward tape operation. The tape indicate light is turned off by pressing the unload key or when the tape unit receives a rewind, rewind-unload or backward command.

Tape Load Procedure—2401-2404

To load tape (see Figure 8) proceed as follows:

1. Open the left hub latch by pulling tab toward you. Mount the reel to be loaded on the left mounting hub. To ensure proper alignment, place the hub of the reel firmly against the stop on the machine mounting hub, and close the hub latch. *Always check to ensure that the hub latch is closed.*

2. Hold the reel release key depressed and rotate the file reel clockwise, unwinding about 4 feet of tape.

3. Place the tape around the left rewind idler, through the read/write assembly, and around the right rewind idler. Place and hold the end of the tape between the index finger and the hub of the machine reel. Press the reel release key and wind tape on the machine reel clockwise for at least two turns beyond the
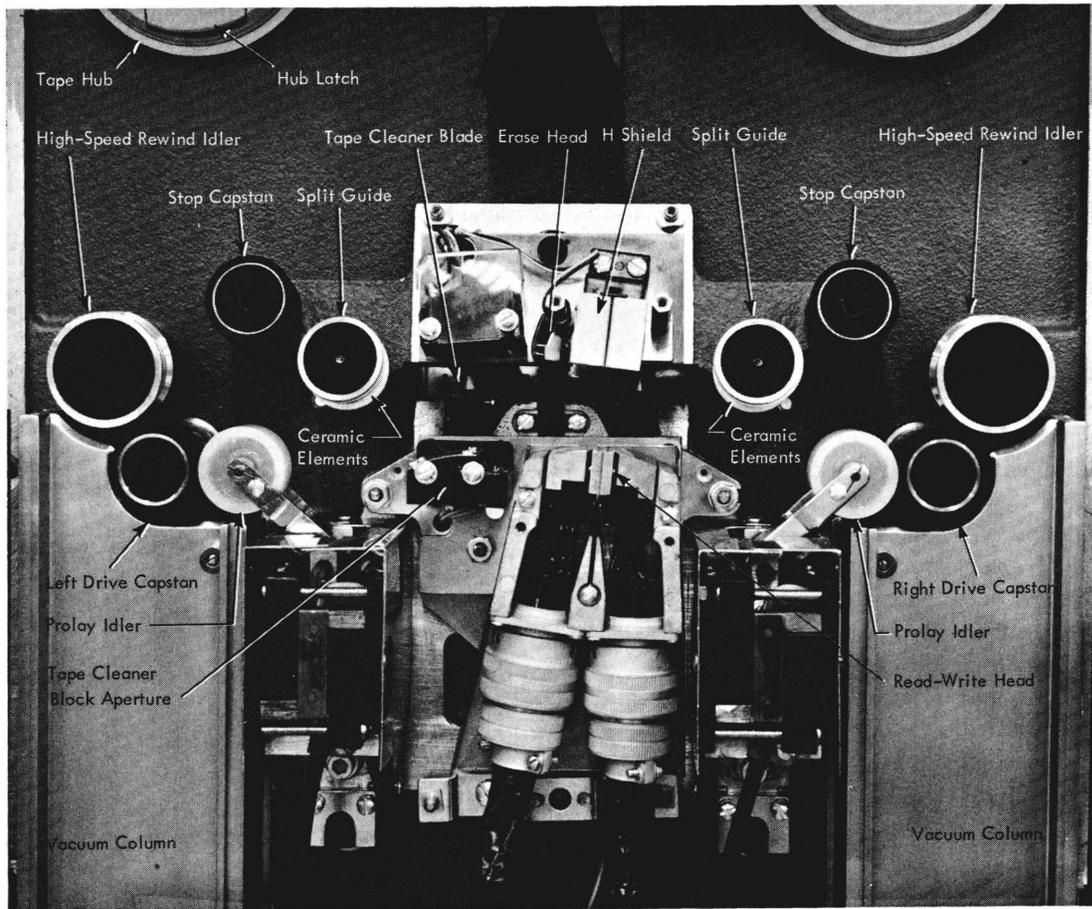
Figure 8. IBM 2401-2404 Transport, Models 2, 3, 5, or 6

load point marker. Align the tape carefully on the machine reel to prevent damage to the edge on the first few turns. Use the reel finger hold when winding the tape. Rotating the reel using the cut out area can result in damage to the edge of the tape.

4. Close the reel door, if open.

5. Press the load-rewind key. This closes the power window, loads tape into the vacuum columns, lowers the head assembly, and rewinds tape to load point.

6. Press the start key. This places the tape unit under automatic control and turns on the ready light.

Tape Unload Procedure—2401-2404

1. If the ready light is on, press the reset key to return the unit to manual control.

2. Press the load-rewind key to rewind the tape.

3. When the load point is reached, press the unload key. This raises the head, unloads tape, and lowers the power window.

4. Hold the reel release key depressed and manually rewind the file reel by turning it counterclockwise with the finger pressed in the finger hold of the tape reel.

5. When the tape is completely rewound, open the hub latch and remove the reel. If resistance is encountered in removing a reel, exert pressure from the rear of the reel with the hands as near the hub as possible. Never rock a reel by grasping it near the outer edge in a way that pinches the edges of the outer turns of the tape.

NOTE: Do not turn power off with the tape unit in a load status, because the head assembly must be up for removal of the tape.

Direct-Access Device

A typical direct-access storage device is the 2311 Disk Storage Drive. For complete description, see *IBM System/360 Component Descriptions*, Form A26-5988.

Operator Controls and Indicators

Start-Stop Key: This key is lighted when it is set to START.

With the 2311 properly connected in a processing system, set this key to START to supply power to the disk drive motor and other 2311 components. When the disk drive motor has come to speed, and other components are ready for operation, the read/write heads are moved into position and the access mechanism performs an automatic seek cycle.

Pressing the start-stop key when it is set to START changes it to STOP. This action causes the access mechanism to retract from the disk pack and removes power from the disk drive motor. Automatic braking stops disk pack rotation in a few seconds.

Select Lock Indicator: When on, this indicates a machine condition that requires customer engineering attention. This condition causes the disk storage drive to be disabled and stops the usage meter.

Enable/Disable Switch: When the CPU is in the stopped state, this switch enables or disables the communication of the storage drive with the CPU. It also enables or disables the equipment usage meter.

If the CPU is running when the switch setting is changed, the storage drive and usage meter operating status are not changed until the CPU is placed in the stopped state. (See also "Select Lock Indicator.")

Operating Procedures

Disk Pack Handling

Each disk pack is protected in transit by special carton inserts and special protective material.

When received, examine the carton closely. If its condition is acceptable, remove the disk pack and store it. Keep the carton and inserts; you may need them later.

If the carton or its contents show any unusual shipping damage, do not use the disk pack. Retain the damaged carton and disk pack in its "as received" condition and notify the IBM Customer Engineer immediately.

Disk packs have been designed for ease of transport from location to location.

For best shipping results:

1. Be sure the pack is secure in its two-piece cover.
2. Use only the specially designed IBM shipping carton with its special protective padding properly inserted. If the original carton is worn or damaged, a new carton may be ordered from your local IBM office.

Handle a disk pack only with its cover on.

If the disk pack is accidentally dropped, or receives a sharp impact of any kind, call an IBM Customer Engineer before using it.

Disk Pack Labeling: For positive identification, small adhesive-backed labels can be placed on the disk pack center hub. Labels in this location can be read through the transparent disk pack cover.

The following operating procedures should be followed when labeling disk packs:

1. Use adhesive-backed labels that can be applied and removed easily.
2. Use a writing implement, like a pen or felt-tip marker, which does not produce loose residue. Do not use a lead pencil.
3. Write on the label before it is applied to the disk pack.
4. Place the label only on the center hub, not on the disk pack cover or top disk surface.
5. Use a new label if changes are necessary. Never use an eraser because microscopic eraser particles can damage disk surfaces and read/write heads.

Disk Pack Loading:

1. Open the 2311 cover.
2. Remove the bottom disk pack cover by turning the bottom locking knob.
3. Place the 1316 Disk Pack (still contained in top cover) on the 2311 spindle.
4. Turn the top cover in direction of ON arrow until firm resistance is met.
5. Lift the top cover from the disk pack.
6. Close the 2311 cover.
7. Press the 2311 start key.
8. Reassemble the top and bottom covers of the disk pack.
9. Store the covers in a clean cabinet or on a clean shelf.

CAUTION:
Do not leave disk pack cover inside disk drive.

Disk Pack Unloading:

1. Press the 2311 stop key.
2. Wait for the disk pack to stop rotating.
3. Separate the top and bottom disk pack covers.
4. Open the 2311 cover.
5. Place the disk pack top cover over disk pack.
6. Turn the top cover in direction of OFF arrow at least two full turns.
7. Lift the top cover, now containing the disk pack, from the spindle.
8. Fasten the bottom cover to disk pack (firmly).
9. Close the 2311 cover.
10. Store the disk pack in a clean cabinet or on a clean shelf.

Disk Pack Storage: To assure maximum disk pack life and reliability:

1. Store the disk packs flat, not on edge.
2. Each pack should rest on a shelf, not on another disk pack.
3. Store in a clean, enclosed metal cabinet or a similar fire-resistant container; never in direct sunlight.
4. Store disk packs in a machine-room atmosphere (60° to 90° F, 10% to 80% humidity).

5. If disk packs must be stored in a different environment, allow two hours for adjustment to machine room atmosphere before use.

Punched Cards

Although certain special characters may vary slightly from one model key punch to another, the punched card shown in Figure 9 is typical throughout IBM System/360 usage. In Figure 9, all characters conform to the EBCDIC code.

Card Read Punch

A typical card read punch is the IBM 2540. For complete description, see *IBM 2540 Component Description and Operating Procedures,* Form A21-9033.

Reader Controls (Figure 10)

Start Key: The reader start key has three functions:

1. Pressing the start key feeds cards to all stations in the read feed, enters the data from the first card into the read buffer in the 2821 Control Unit, and places the reader in ready status if the read feed is clear of cards, cards are in the hopper or the file feed magazine, power is on, and all interlocks are satisfied.

2. Pressing the start key causes a non-process run out (NPRO) of any cards in the read feed into stacker R1 when the hopper is empty, the reader end-of-file light is off, and the hopper joggler gate is open.

3. Pressing the start key after the clearing of an error that required operator intervention initiates any necessary feed cycles and places the reader in ready status.

Stop Key: Pressing the reader stop key halts card movement at the completion of the current operation, turns off the reader end-of-file light, and places the reader in not ready status.

End-of-File Key: Pressing the reader end-of-file key conditions the 2540 circuits so that card feeding and reading will continue after the read hopper is empty until the last card has been read and stacked.

Lights

Feed Stop: This light comes on when the reader motor stops because of a card jam, a misfeed, a read clutch failure, or failure to get a read complete signal on a read cycle.

Ready: This light indicates that the reader is in ready status.

Read Check: This light signals the detection of a hole count check, parity check, buffer address error or translate check in the 2821 read buffer.

Validity Check: This light indicates that an invalid punch configuration was recognized in a data mode 1 read or PFR read operation.

End-of-File: This light indicates that the end-of-file key has been pressed, and that the end-of-file circuits are active. The end-of-file light goes out and the circuits are deactivated if the stop key is pressed or the last card has been stacked and an additional feed instruction, or read and feed instruction, has been given to the reader.

Figure 9. Standard IBM System/360 Card Code

Figure 10. Reader Controls and Common Indicator Lights

Punch Controls (Figure 11)

Start Key: The punch start key has three functions:

1. Pressing the punch start key feeds cards to the punch and blank stations, if the punch feed is clear of cards, cards are in the hopper, power is on and all interlocks are satisfied. If punch feed read (PFR) is installed, the contents of the first card enter the punch buffer in the 2821.

2. Pressing the punch start key causes a non-process run out (NPRO) of all cards in the punch feed into stacker P1 if the hopper is empty. If PFR is installed, the punch end-of-file light must be off for a non-process run out (NPRO) operation.

3. Pressing the punch start key initiates any necessary feed cycles and restores the punch feed to ready status after an error condition requiring operator intervention has been cleared.

Stop Key: Pressing the punch stop key halts card movement at the completion of the current operation and places the punch in not ready status. If PFR is installed, pressing the punch stop key turns off the punch end-of-file light.

End-of-File Key: The end-of-file key is installed in the punch feed when the PFR special feature is on the 2540. Pressing the punch end-of-file key causes the 2540 to continue feeding and processing cards after the punch hopper is empty until the last card is read and/or punched and stacked.

Lights

Chips: This light indicates that the chip box is either full or improperly positioned.

Ready: This light indicates that the punch is in ready status.
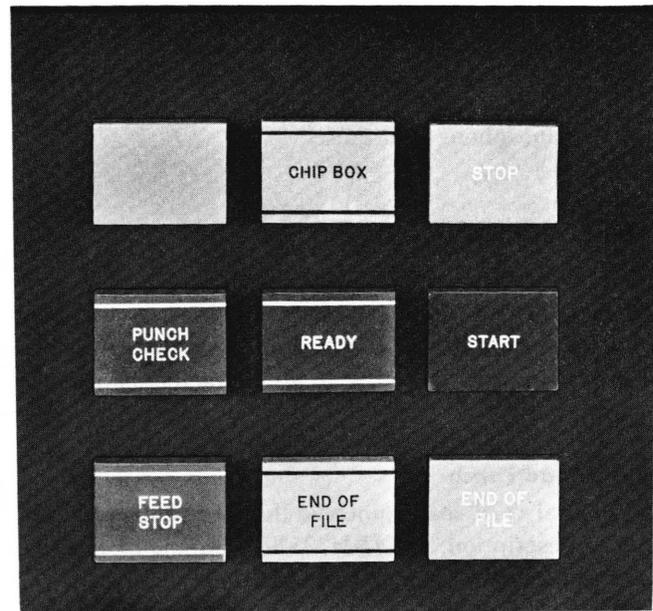
Figure 11. Punch Controls

Punch Check: This light indicates the detection of a hole count check, parity check, buffer address error or translate check in the 2821 punch buffer.

Feed Stop: This light comes on when the punch motor is stopped by a card jam or a misfeed or a punch clutch failure.

End-of-File: This light is installed in the punch feed when PFR is on the 2540, and indicates that the punch end-of-file key has been pressed, activating the punch feed end-of-file circuits. If the punch stop key is pressed, the punch end-of-file light will go out and the circuits will be deactivated.

Common Indicator Lights

Transport: This light indicates a card jam in the transport area of the 2540.

Power: This light indicates that the 2540 is being supplied with DC power.

Stacker: This light indicates that any one of the five stackers is filled.

Fuse: This light indicates that a signal fuse in the 2540 has blown. A blown fuse must be replaced by a fuse of the same size. An IBM Customer Engineer should be notified, because this could indicate some malfunction in the 2540 circuitry.

Operating and Restart Procedures

Initial Start: To begin operation with the 2540 reader:

1. Perform a NPRO operation by opening the joggler gate, emptying the hopper, and pressing the reader start key to ensure that no cards are left in the feed.

2. Load the desired cards into the hopper of the file feed magazine and close the joggler gate. Card decks

less than 1 inch thick should be placed directly in the hopper with the card weight; larger decks can be placed in the file feed magazine.

3. Press the reader start key.

To begin operation with the 2540 punch:

1. Perform a NPRO operation by emptying the hopper and pressing the punch start key.

2. Load the desired cards into the punch hopper.

3. Press the punch start key.

Restart from Error Conditions

Because the 2540 uses the flexible System/360 instruction set, the different external error indications can each require several different restart procedures, depending on the instruction during which the error occurs. The operator should be provided with some programmed message, such as a type-out or print-out, to aid him in finding a suitable restart procedure.

The programmer uses the sense information to write in which error message should be given to the operator. Programming automatically provides the proper operator message.

Specific restart procedures are provided in the referenced manual, Form A21-9033. Action required for specific operator messages is provided in the applicable operating guide for the operating system in use. See "Program-Oriented Procedures" for a listing of referenced publications.

Printer

The IBM 1403 Models 1-7, comprise printers that may be used in this installation. For complete description see *IBM 1403 Printer*, Form A24-3073. The 1403 is briefly described here.

Keys and Lights (Figure 12)

Print Start (front and back): This key starts the machine and turns on ready light.

Check Reset: This key resets a printer error indication. Print start key is used to restart the operation.

Print Stop (front and back): This key stops the printer at the completion of the instruction in process. The ready light turns off.

End-of-Forms: This light shows an end-of-form condition; the machine stops.

Forms Check: This light indicates form-feed trouble in the forms tractors. This light turns off when corrective action is taken, and the check-reset key is pressed.

Print Ready: This light turns on when the printer is ready to print.

Print Check: This light indicates a print error.

Sync Check: This light turns on when the chain or train is not in synchronization with the compare
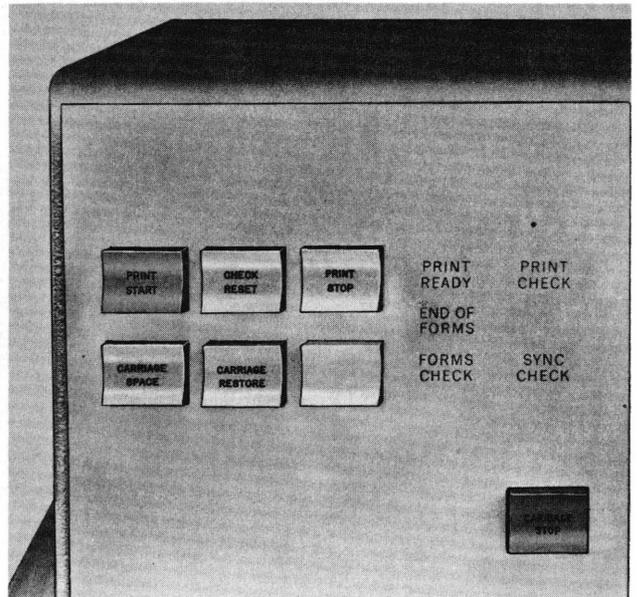
Figure 12. IBM 1403 Operating Keys and Lights

counter for the printer. The timing is automatically corrected and the light is extinguished by pressing the check-reset key.

Carriage Controls

Carriage Restore: Pressing this key positions the carriage at channel 1 (home position). If the carriage-feed clutch is disengaged, the form does not move. If it is engaged, the form moves with the control tape.

NOTE: This key must not be pressed when the printer is printing.

Carriage Stop: Pressing this key stops the carriage operation, and turns on the forms check light.

Carriage Space: Pressing this key causes the carriage to advance the form one space if the clutch is engaged.

Manual Controls

The manual controls are shown in Figure 13.

Feed Clutch: The feed clutch controls the carriage-tape drive and form-feeding mechanism and selects 6- or 8-lines-per-inch spacing. When set to neutral, automatic form feeding cannot take place.

Paper-Advance Knob: This knob positions the form vertically. It can be used only when the feed clutch is disengaged.

Vertical Print Adjustment: This knob controls fine spacing adjustment of forms at the print line. The carriage tape is not affected by this knob.

Horizontal Adjustment: This device positions the printing mechanism horizontally. When the lever is raised, the print mechanism unlocks, and can be positioned horizontally within its 2.4-inch travel limit.
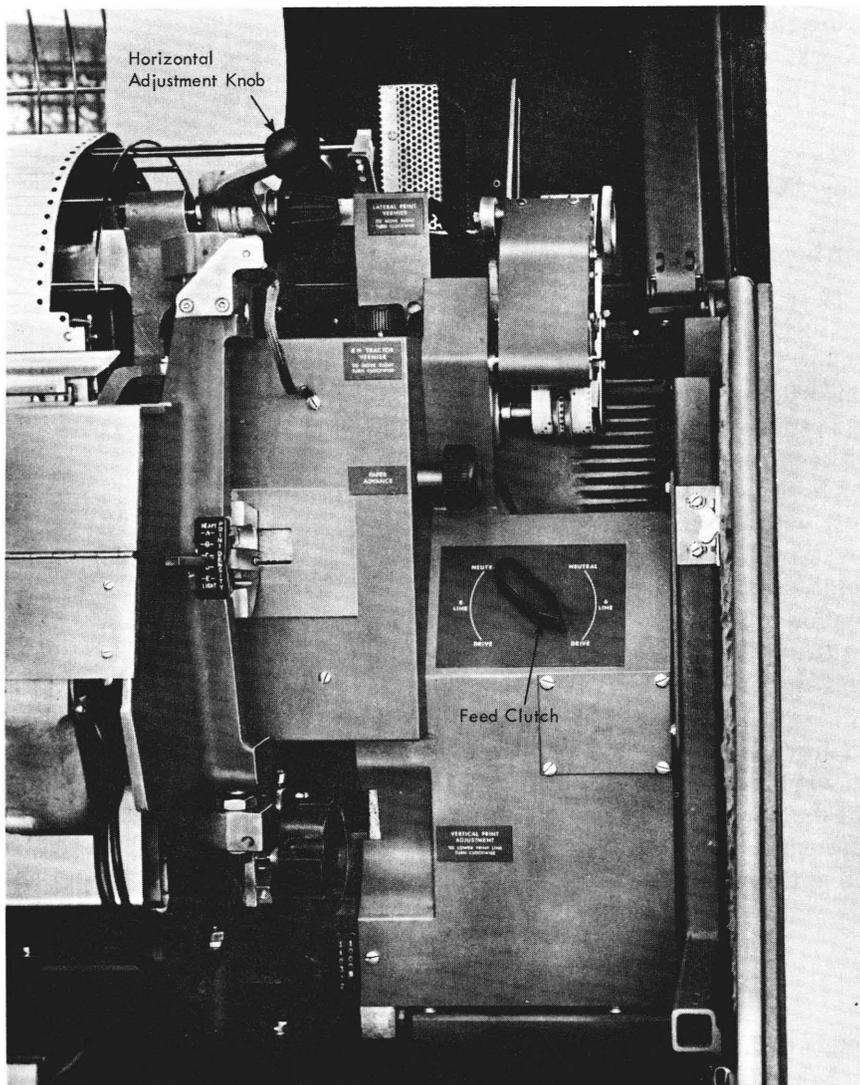
Figure 13. Carriage Controls

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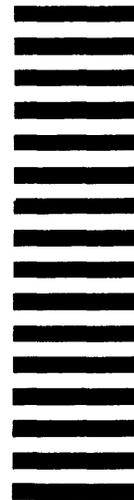
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