IBM 1620

DATA PROCESSING SYSTEM

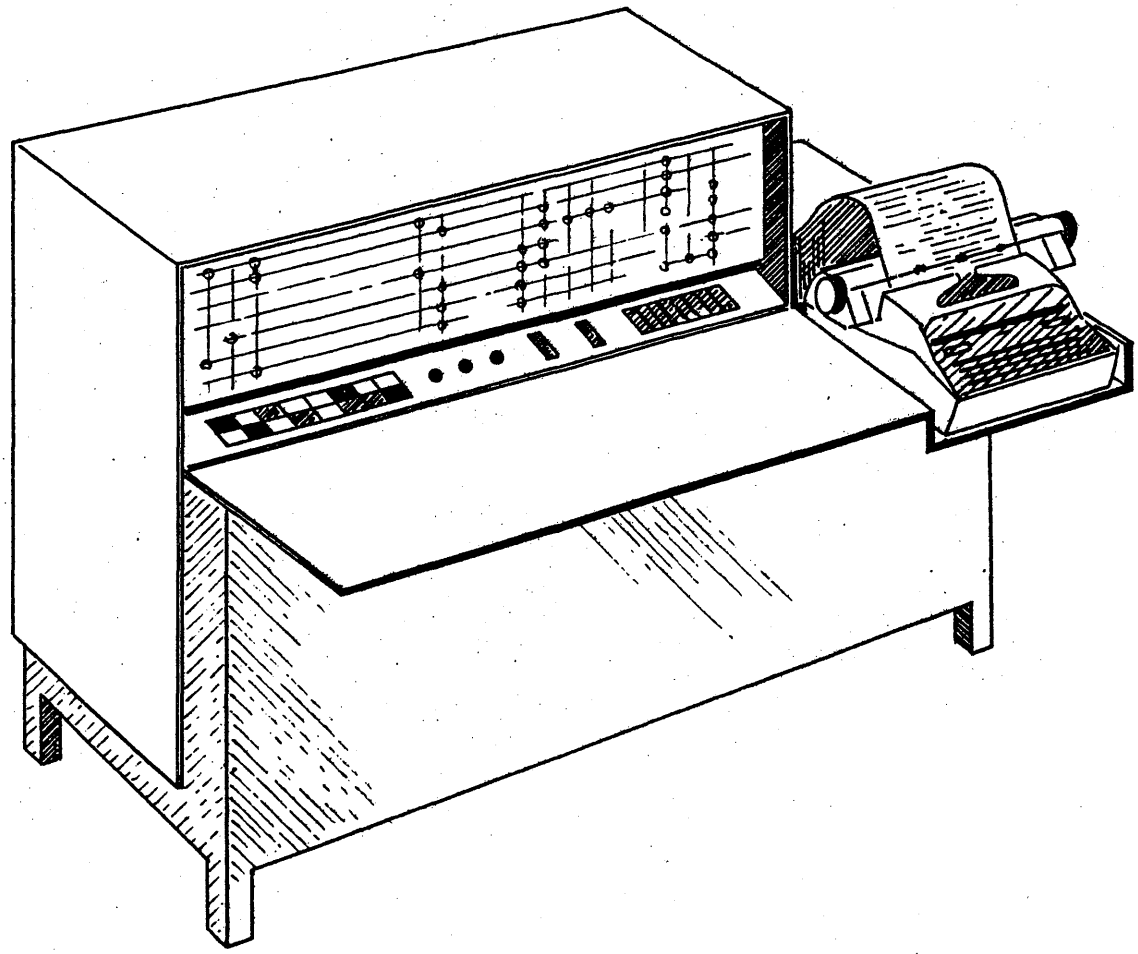
PRODUCT SPECIFICATIONS

January 6, 1960

PROCESSING SYSTEMS
SAN JOSE

COMPANY CONFIDENTIAL

CADET COMPUTER
PRELIMINARY FUNCTIONAL SPECIFICATIONS



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PRELIMINARY

FUNCTIONAL SPECIFICATIONS

CADET COMPUTER

July 31, 1959

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The machine description contained herein should not be interpreted as final in all respects. Certain changes may become necessary for hardware reasons as the implementation proceeds.

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1. INTRODUCTION

1.1 General Description

The dataflow schematic of the system is shown in Figure 1.1. A core memory of twenty-thousand (20,000) numeric digits is the main storage medium. Memory is addressed serially by digit from the five digit Memory Address Register (MAR). This register is shared by the Instruction Address Registers (IR-1 and IR-2), the Operand Address Registers (OR-1, OR-2, and OR-3), and the Product Address Registers (PR-1, PR-2, and PR-3) all of which are located in a core array. The data bus is primarily serial by digit and parallel by six bits. All operations are performed serially (i.e., read, write, compute). No provision is included for simultaneous, time-shared, or overlapped operations. (See Section 2 for a detailed functional description.)

1.2 Machine Code

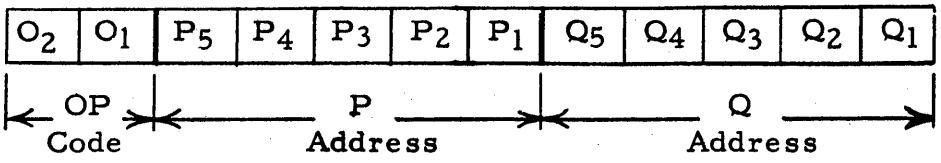
1.2.1 The memory data bus, and register storage sections of the machine are in BCD numeric notation; specifically, four bits for numeric, one bit for odd parity, and one bit for flag notation. A vertical redundancy (parity) check is provided on all data read to or from memory, on all data read to or from an input-output device. and on all memory addresses used by the Memory Address Register (MAR). Illegal characters (i.e., correct parity but invalid bit combinations exceeding ten) are not detected.

1.2.2 The machine is primarily a numeric computer; however alphabetic and special characters are handled internally by two decimal machine digits. The only non-decimal machine digit allowed is the record mark, ≠, with C-8-2 bit coding. The record mark is primarily used in input/output operations and in record transmission within the machine. It may, however, be used as a digit in arithmetic field or in collating operations where it will be interpreted as a zero. It is not usable as a digit in an instruction.

1.3 Instruction Format

1.3.1 All instructions are a fixed length of twelve digits, a two digit operation code, a five digit P-address and a five digit Q-address.

The figure below shows the format of an instruction as it appears in memory.

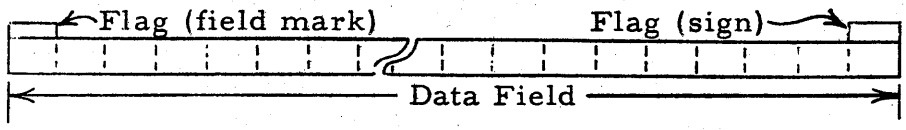


During instruction time the five digit P-address is placed in Operand Address Register-2 (OR-2) in the form PPPPP and the five digit Q-address is placed in Operand Address Register-1 (OR-1) in the form QQQQQ.

1.3.2 The first operation code digit, O_2, of each instruction is located at an address having the form XXXXN (where N is an even integer) with the remaining digits of the instruction falling in succeedingly higher order memory addresses. (See Figure 4.1 for instruction summary.) Flag bits are ignored during instruction interpretation; however, these flags may be placed on digits within an instruction so that the instruction can be operated on as data whenever program modification is necessary.

1.4 Data Format

Data words are variable in length and may contain any desired number of digits. The units position of a numeric field is signed by using a flag bit and the high order position is also indicated by using a flag bit



It should be noted that a flag bit can indicate the sign of the field or the end of the field depending upon its relative location in the field. Alphabetic and special characters are represented as two decimal machine digits. Alphabetic and numeric information may be randomly mixed within memory.

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CADET DATAFLOW SCHEMATIC

FIGURE 1.1

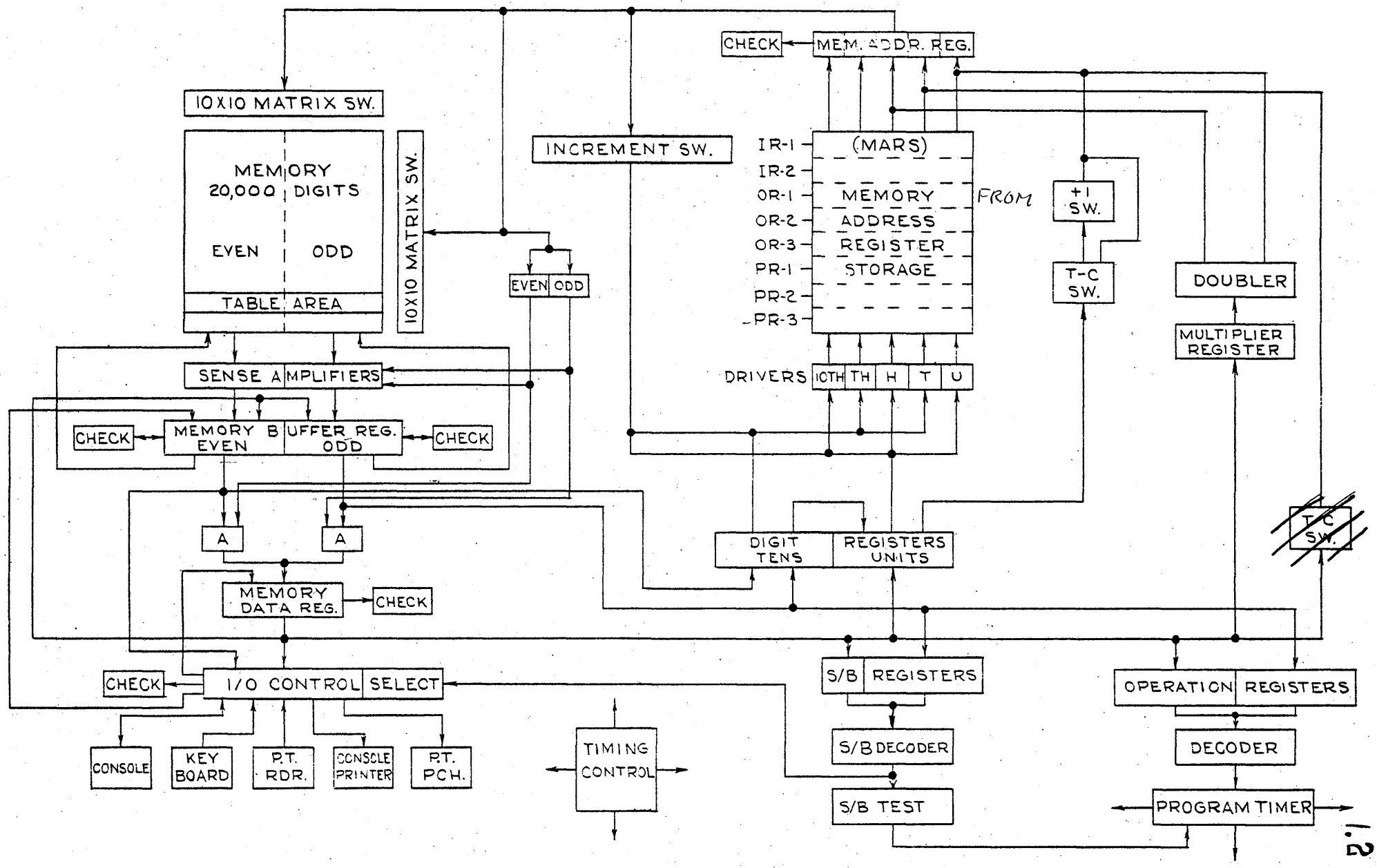

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Figure 1.2

CADET CHARACTER CODE CHART

← Alphanumeric Mode →								→ Numeric Mode ←
Zone Digit								Numeric Digit
8421	8421	8421	8421	8421	8421	8421	8421	8421
0000	0001	0010	0011	0100	0101	0110	0111	
				I	R	Z	9	1001
				H	Q	Y	8	1000
				G	P	X	7	0111
				F	O	W	6	0110
				E	N	V	5	0101
)	*	(	@	D	M	U	4	0100
.	$	,	=	C	L	T	3	0011
				B	K	S	2	0010
				A	J	/	1	0001
+	-		b				0	0000

Numeric Mode (I/O): Digits are represented within the machine by one BCD position.

Example:

	8421
6	0110

Alphanumeric Mode (I/O): Alphanumeric (and special) Characters are represented within the machine by two BCD character positions.

Example:

	8421	8421
6	0111	0110
P	0101	0111

2. DETAILED FUNCTIONAL DESCRIPTION

2.1 Memory

2.1.1 The basic CADET system has twenty-thousand (20,000) numeric digits of core memory comprising one module. Additional memory may be added in modular increments (20,000) to a maximum of five modules (100,000 digits). The module is a three dimensional array 12 planes deep with 100 x 100 positions per plane. Addressing is from a single register, the Memory Address Register (MAR), which is 22 bits in the basic machine (four full decimal digit positions, one bit for the ten-thousand position, and a parity bit for each of the five positions).

The array is driven from two 10 x 10 matrix switches which select one "column" of 12 cores (one core in the same position in each plane) to be read from memory to the transistor register called the Memory Buffer Register (MBR). Since characters in CADET code consist of 6 bits (4 data bits, 1 parity check bit, and 1 flag bit) the state of these 12 cores read from memory by one read command is placed in MBR as two characters (digits). (If the digit at memory location XXXXN, where N is an even number, is addressed for read out, the digit at memory location XXXXN + 1 will be read out as well; if the digit at memory location XXXXN + 1 is addressed for read out, the digit at memory location XXXXN will be read out as well.)

When the two digits have been received by the MBR, further selection of the digit is made based on the units position of the address in MAR and it is ascertained which of these digits is to be sent to the one digit transistor Memory Data Register (MDR). The digit may then be sent from the MDR to other machine locations.

Memory is addressed cyclically in that address 00000 follows, in sequence, the largest allowable address. In the basic machine (20,000 digits) address 00000 follows 19,999. If the high order position of either address (P_5 or Q_5) is specified to be greater than "1" in the basic machine, a parity check error will be detected in MAR and the MAR Check Indicator will be turned ON.

The CADET memory has been designed for a basic cycle of 20 u sec. At this time, there is every indication that the speed can be increased; however, the final memory cycle will be decided upon as a result of model test.

2.1.2 Three hundred-twenty (320) memory locations have been assigned as a "Table Area"; a twenty (20) digit area from memory locations 00080 through 00099 to receive the product in multiplication, a two-hundred (200) digit area from memory locations 00100 through 00299 for storage of a multiplication table for use by the computer during the execution of the MULTIPLY instruction, and a one-hundred (100) digit area from memory locations 00300 through 00399 for storage of an addition table for use by the computer during the execution of all arithmetic instructions. All of these "Table Area" locations are in addressable memory.

2.2 Memory Address Register Storage (MARS)

The Memory Address Register (MAR) is shared by eight - 5 digit registers: Instruction Address Registers 1 and 2 (IR-1 and IR-2), Operand Address Registers 1, 2 and 3 (OR-1, OR-2 and OR-3) and Product Address Registers 1, 2 and 3 (PR-1, PR-2 and PR-3) all of which are located within a core array called Memory Address Register Storage (MARS). Since none of these registers are located in memory, however, they are not available to the programmer as addressable locations. All MARS Registers are cyclic in addressing memory in that address 00000 follows, in sequence, the largest allowable address. Thus, in the basic machine address 00000 follows 19999. Individual register operation is described below.

2.2.1 Instruction Address Register 1 (IR-1)

This register and MAR are both involved in the reading of an instruction. At the beginning of Instruction-time (I-time), IR-1 contains the memory address of the first operation code digit, O_2, of the instruction. During the first cycle of instruction time the address contained in IR-1 is read out to MAR. The two digit operation code of the instruction is then read out of memory to MBR-Even and MBR-Odd (per IR-1) and thence is transmitted to the two digit Operation Register. Simultaneously the content of MAR is routed through the Increment Switch, stepped by two, and placed back in IR-1. During the next memory cycle the first two digits of the

P-address, P_5 and P_4, are read out of memory (per IR-1) to the MBR and are then placed in the ten-thousands and thousands positions of OR-2; in this manner P_3 and P_2 are placed in the hundreds and tens positions of OR-2. One cycle is then used to place P_1 into the units position of OR-2 and the address routed through the Increment Switch, stepped by one and placed back in IR-1. The first digit of the Q-address, Q_5, is read out in the next memory cycle to MDR (per IR-1) and thence to the ten-thousands position of OR-1. During the next two memory cycles the remaining digits of the Q-address are placed in OR-1. By the end of instruction time IR-1 has stepped twelve addresses higher to the high-order digit of the next instruction in the program. It remains in this position during Execution-time (E-time). Eight memory cycles are required to complete the I-time.

2.2.2 Instruction Address Register 2 (IR-2)

This register is used to store the contents of IR-1 during the execution of the BRANCH AND TRANSMIT or BRANCH AND TRANSMIT (IMMEDIATE) instructions. If, during the execution of the BRANCH BACK instruction, the Save Light is not ON, the contents of IR-2 are returned to IR-1 for immediate use by the program. (See Sections 2.5.5.6 and 4.24)

2.2.3 Operand Address Registers

2.2.3.1 The first two Operand Address Registers, OR-2 and OR-1 are loaded with the P and Q address part of an instruction during I-time as described in 2.2.1. During E-time, these registers share MAR in providing locations of data in memory for the performing of the operation specified.

2.2.3.2 Operand Address Register 3 is used only during the execution of the MULTIPLY and MULTIPLY (IMMEDIATE) instructions as the reset address of the units position of the multiplicand. At the beginning of E-time in these instructions, OR-3 is set to the memory location of the units position of the multiplicand as specified by OR-2. OR-2 is then decremen-

ted once each time a digit of the multiplicand is multiplied by a digit of the multiplier (specified by OR-1). When a flag (field mark) is detected in the multiplicand, a new digit of the multiplier is obtained per OR-1 and OR-2 is reset to the content of OR-3 to begin the cycle again.

2.2.4 Product Address Register 1 (PR-1)

2.2.4.1 At the beginning of E-time in the MULTIPLY or MULTIPLY (IMMEDIATE) instructions, PR-1 is reset to memory position 00099 (the units position of the Product Area in memory). Its address is decremented one position at the beginning of the development of the partial product associated with each new multiplier digit. The decremented address of PR-1 is also placed in PR-2 from which all successive additions of that partial product are executed.

2.2.4.2 If the computer is in "manual" mode and the Save Key on the Console is depressed, the content of IR-1 will be placed into PR-1 for future reference. The next BRANCH BACK instruction encountered in the "automatic" mode will cause the content of PR-1 to be placed into IR-1. (See Section 2.5.5.6.)

2.2.5 Product Address Register 2 (PR-2)

This register is used only in the execution of the MULTIPLY and MULTIPLY (IMMEDIATE) instructions. Each time a new multiplier digit is obtained, PR-2 is set equal to PR-1 so that the new partial product may be developed in the proper digit position of the Product Area in memory. As each new multiplicand digit is used, PR-2 is decremented by one so that it addresses the next higher order digit of the Product Area in memory; addition to obtain a new digit of the partial product is then carried out.

2.2.6 Product Address Register 3 (PR-3)

This register is used only in the execution of the MULTIPLY or MULTIPLY (IMMEDIATE) instruction. Near the end of each

basic multiplication cycle PR-3 is set equal to PR-2. PR-3 is then used to address the proper digit positions of the partial product so that carries resulting from the development of a new partial product digit can be propagated.

2.3 Sense and Branch Register (S/B Reg.)

This is a two digit transistor register used for storing Q-address digits Q_4 and Q_3 encountered during I-time in the:

2.3.1 BRANCH INDICATOR (BI) and BRANCH NO INDICATOR (BNI) instructions. Program interrogation of the status of Console Sense Switches, Machine Status Indicators and other Machine Check Indicators is made possible through these instructions.

The coding of the Q-address in the BI and BNI instructions determines which machine indicator will be interrogated (see the description of these instructions in Section 4.28 and 4.29 for addresses assigned). Digits Q_4 and Q_3 will be sent to the S/B Registers for decoding and test of the specified indicator during I-time. If the test is positive, the branch trigger will be turned ON for use during E-time; if the test is negative, the branch trigger will not be turned ON. (Note: The indicator interrogated may be turned OFF by the test. Section 4.28 defines the indicator status after test.)

2.3.2 Read, Write, and Control Operations

During the execution of these instructions, the S/B Registers serve as Select Registers for the addressed input-output device; however, only digits Q_4 and Q_3 will be stored in the S/B Register for decoding into the input-output control. (See Section 4.16-4.21 for addresses assigned.)

2.4 Input/Output

No provision is made for simultaneous or overlapped operation with the serial, unbuffered CADET input/output devices. Each machine must be equipped with at least a Keyboard/Printer in the form of an IBM Model 35 Input/Output Writer so that manual operation of the machine from the Console can be performed. The IBM Type 961

Paper Tape Punch will be available as well, and it is also expected that an as yet unannounced 150 cps Paper Tape Reader will be available.

2.4.1 Keyboard/Printer

2.4.1.1 Function

This device is housed in the form of an I/O typewriter; however, it cannot be used as an off-line typewriter since the Keyboard locks-up when it is not being used to enter data to memory. When the Keyboard is used for direct input of data to memory. a hard copy record of this data is obtained as a byproduct. The Printer portion is used for automatic print-out of memory data at the rate of 10 characters per second.

2.4.1.2 Control Operations

Tabulate, space, and carriage return are functions applicable to the Printer which are specified by the CONTROL instruction.

2.4.1.3 Error Checking

A parity check is made on all data used by the Keyboard/Printer.

2.4.1.3.1 If a redundant character is presented by the Keyboard to the I/O translator (in the I/O Control section of the machine), the Read Check Indicator is turned ON. The machine will remain in "automatic" mode, however, and will accept additional data from the Keyboard until the Release Key on the Console is depressed. The machine will then enter "manual" mode.

2.4.1.3.2 If a redundant character is presented to the Printer from the translator, the

Write Check Indicator is turned ON. The Printer will continue operating until the end of the record is reached before the indicator will be interrogated. Whether or not the computer stops will then depend upon the setting of the Data Check Switch on the Console.

2.4.2 Type 961 Paper Tape Punch

2.4.2.1 Function

CADET characters are translated to the 884 eight-channel paper tape code* in the Input/Output control section of the machine and are punched in paper tape at the rate of 15 characters per second by this device.

2.4.2.2 Control Operations

None of the functions specified by the CONTROL instruction are applicable to this device.

2.4.2.3 Error Checking

2.4.2.3.1 If a redundant character is presented by the I/O translator to the 961 Punch, the character is punched in the tape but the feed will not advance the tape. With the incorrect character still under the punches, the machine will hang-up in "automatic" mode regardless of the setting of the Data Check Switch. The No Feed Light and the Write Check Indicator on the Console are turned ON and the Reset Key will have to be depressed to return the machine to "manual" mode. Manual restart procedures are required to lace the

*The & % ¤ and # in standard 884 eight-channel code have been replaced by the + ( ) and = respectively, for use in Fortran language. (See Figure 2.1.)

incorrect character and re-punch the correct one.

2.4.2.3.2 Should the 961 Punch exhaust its supply of paper tape, the machine will hang-up in "automatic" mode and the No Feed Light on the Console is turned ON. Manual restart procedures are required.

2.4.3 150 cps Paper Tape Reader

2.4.3.1 Function

Standard eight channel paper tape alphanumeric characters are read by this device at 150 characters per second to the Input/Output Control section of the machine where they are translated into CADET code. Reel and center reel feed will both be available.

2.4.3.2 Control Operations

None of the functions specified by the CONTROL instruction are applicable to this device.

2.4.3.3 Error Checking

If a redundant character is presented by the Reader to the I/O translator (in the I/O Control section of the machine), the Read Check Indicator is turned ON. The machine will remain in "automatic" mode and the indicator is not interrogated until the complete record is read. Whether or not the computer stops will then depend upon the setting of the Data Check Switch on the Console.

2.5 Console

2.5.1 General

The keys, lights, switches and displays provided on the CADET

Operator's Console are used to:

a) Provide manual machine control.

b) Correct errors.

c) Display the contents of memory and the registers in the Memory Address Register Storage (MARS).

d) Revise the contents of memory.

2.5.1.1 Emphasis has been placed on automatic computer operation; therefore, most of the control from the Console consists of the execution of CADET instructions which have been placed in memory via the Console Keyboard.

2.5.1.2 See Figure 2.2 for the CADET Console Component Chart.

2.5.2 Indicator Displays

2.5.2.1 Machine Check Indicators

These incandescent lamps display various error conditions in the computer. A specific Machine Check Indicator is turned ON when the error condition associated with that indicator occurs during operation of the computer.

The computer will continue in "automatic" mode or will halt, depending on the setting of a Modifier Switch associated with the indicator. The detailed functions of the Modifier Switches are explained in Section 2.5.4.

The status of each of these indicators may be interrogated by a BRANCH INDICATOR (Section 4.28) or BRANCH NO INDICATOR (Section 4.29) instruction addressing the specific indicator. The indicator is turned OFF by the interrogation.

Depression of the Reset Key will cause all these indicators to be reset to the OFF condition.

2.5.2.1.1 Data Check Indicators

Each of the 5 indicators in this group is associated with a parity check at a specific point in the dataflow of the system. (The Any Latch is turned ON if any of the indicators in this group are turned ON and will turn OFF only when the Data Check Indicator(s) which turned it ON is turned OFF.) One Modifier Switch is associated with this group of indicators.

2.5.2.1.1.1 Memory Buffer Register - Even (MBR-E) Check Indicator

This indicator is turned ON when a parity check error is detected on a digit in the Even address portion of the two digit MBR.

2.5.2.1.1.2 Memory Buffer Register - Odd (MBR-O) Check Indicator

This indicator is turned ON when a parity check

error is detected on a digit in the Odd address portion of the two digit MBR.

2.5.2.1.1.3 Memory Data Register (MDR) Check Indicator

This indicator is turned ON when a parity check error is detected on a digit in the MDR.

2.5.2.1.1.4 Read (RD) Check Indicator

This indicator is turned ON when a parity check error is detected in reading from an input device. One or more of the other Data Check Indicators may also be turned ON.

2.5.2.1.1.5 Write (WR) Check Indicator

This indicator is turned ON when a parity check error is detected during a write operation. If the parity check error was present when the digit to be written was received by the output control, one or more of the other Data Check Indicators may also be ON.

2.5.2.1.2 Overflow Check Indicator

This indicator is turned ON when the overflow condition occurs as the result

of an add, subtract or compare operation executed by the computer. One Modifier Switch is associated with this indicator.

2.5.2.1.3 Memory Address Register (MAR) Check Indicator

This indicator is turned ON when a parity check error is detected in the addressing of memory by MAR. One Modifier Switch is associated with the indicator.

2.5.2.2 Register Display Indicators

2.5.2.2.1 Memory Data Register (MDR) Display

The 6 incandescent lamps in this section display in CADET BCD code the digit in memory presently being addressed. The flag-bit and the check-bit, as well as the BCD numerical notation, are displayed. See Section 2.5.5.5 for addressing procedure.

2.5.2.2.2 Memory Buffer Register (MBR) Display

The 12 incandescent lamps in this section display two digits in memory including flag bits and check bits, for any given location addressed. If the memory location addressed for display is an "even" memory location, the digit at this location is placed in the MBR Display in the Even column; the Odd column will contain the display of the next higher order digit. If the memory location addressed for display is an "odd" memory location, the digit at this location is placed in the MBR

Display in the Odd column; the Even column will contain the display of the next lower order digit. (In this way the complete two digit representation of an alphanumeric character within CADET may be viewed at one time.) The character displayed in the MDR Display is duplicated in MBR Even or MBR Odd depending on whether the digit addressed is at an "even" or "odd" memory location.

2.5.2.2.3 Operation Register Display

The two-decimal digit representation of the operation code part of the instruction last executed is displayed in CADET code by the 10 incandescent lamps in this section. Flag bits, which may be stored over the operation code digits in memory, are not displayed.

2.5.2.2.4 Memory Address Register (MAR) Display

The 25 incandescent lamps in this section permit display of the five digit address in any of the eight MARS registers. The specific register to be displayed is selected by the MARS Display Selector Switch and the display is activated by depression of the Display MAR Key.

2.5.2.3 Machine Status Indicators

These incandescent lamps display the status of the various triggers within the computer. There are approximately 110 indicators in this group; they are labeled for identification and are primarily intended for use by the Customer Engineer. However, this group includes the High/Positive and Equal/Zero

Indicators, and the Sense and Branch , Multiply, and Digit Registers which may be used by the Console Operator.

2.5.2.3.1 Instantaneous Stop Indicator

This incandescent lamp is turned ON when the Instantaneous Stop Key and the Stop Key are depressed simultaneously.

This indicator is primarily a reminder to the operator that when a Stop of this type has occurred additional corrective procedure is required before depression of the Start Key. The Instantaneous Stop Indicator is turned OFF when the Reset Key is depressed.

2.5.3 Memory Address Register Storage (MARS) Display Selection Switch

This eight-position rotary switch permits selection of any of the eight MARS Registers for display in MAR Display.

Depressing the Display MAR Key will cause the contents of the selected register to appear in the MAR Display. After the Display MAR Key has been depressed, the position of the rotary can be changed without altering the display.

Before displaying a second MARS Register, the operator must depress the Release Key to initiate the "manual" mode; when in "manual" mode he may change the position of the rotary, depress the Display MAR Key and the content of this next register will appear in MAR Display.

2.5.4 Modifier Switches

These single pole, double throw, toggles are provided as a means of externally controlling the execution of certain mach-

ine functions for which two alternative logic paths are provided; one or the other of the paths is selected, dependent upon the setting of the appropriate Modifier Switch on the Console.

The details of the functions controlled by each of the Modifier Switches are described in the following sections.

2.5 4.1 This group of Modifier Switches is associated with the Machine Check Indicators (described in Section 2.5.2.1) which can be interrogated by a BRANCH INDICATOR (Section 4.28) or BRANCH NO INDICATOR (Section 4.29) instruction.

2.5.4.1.1 Data Check Switch

This Modifier Switch controls the group of 5 Data Check Indicators (MDR, MBR-E, MBR-O, RD, WR).

When this Modifier Switch is set to "Stop" and any one of the 5 Data Checks is turned ON, the machine will halt at the end of the memory cycle during which the data check is detected. Because a data check can occur during any memory cycle in I-time or E-time, and the halt occurs at the end of the memory cycle, it will be necessary for the operator to take additional corrective procedures before depressing the Start Key.

When this Modifier Switch is set to "Program", the computer will continue operating in the "automatic" mode when one or more of the data checks is turned ON (except in the case of punching paper tape, in which the computer will halt on any character when a parity error is detected).

2.5.4.1.2 Overflow Check Switch

When this Modifier Switch is set to "Stop" and the Overflow Check Indicator is turned ON, the computer will halt at the end of execution of the instruction which causes the indicator to be turned ON. If the Start Key is depressed the computer will begin executing instructions per IR-1. The Overflow Check Indicator will remain ON, but the computer continues in the "automatic" mode until another overflow occurs.

When the Overflow Check Switch is set to "Program", and the Overflow Check Indicator is turned ON, the machine will continue to operate in the "automatic" mode and the indicator can be interrogated and turned OFF by the running program.

2.5.4.1.3 MAR Check Switch

When this Modifier Switch is set to "Stop" and the MAR Check Indicator is turned ON, the computer will halt at the end of the memory cycle which causes the indicator to be turned ON.

When this Modifier Switch is set to "Program" and the MAR Check Indicator is turned ON, the computer will continue to operate in the "automatic" mode. The indicator may be interrogated and turned OFF by the running program. It is possible with the switch set to "Program", that the machine will "hang up" in the "automatic" mode because of the inability to address memory correctly and, therefore, be unable to complete execution of the instruction.

2.5.4.2 Console Sense Switches

There are four Modifier Switches in this group, numbered 1 through 4. When a switch is set to "On" and a BRANCH INDICATOR (Section 4.28) instruction specifying that switch is executed, the branch will occur.

When the Modifier Switch specified is set to "Off", the operation will be terminated and the next instruction in sequence will be executed.

When a BRANCH NO INDICATOR (Section 4.29) instruction is used to interrogate one of these switches, the branch will occur when the switch is set to "Off".

2.5 5 Control Keys

Emphasis has been placed upon "automatic" operation of the machine wherever possible so that most of the frequently used Control Keys (i.e., Save, Insert, Release, etc.) are functionally designed for convenient instruction entry. Once instructions have been manually entered at locations beginning with memory address 00000, the Start Key is depressed and the instructions are executed as stored program instructions with the computer in the "automatic" mode.

The computer is in the "manual" mode whenever the Signal Light labeled Manual is ON. This light is turned ON by depression of the Reset Key, Stop Key, or Release Key or by the execution of a HALT instruction. Whenever the Manual Signal Light is ON, the computer has terminated all operation, is in a halted status and is prepared to accept operator intervention. Whenever the Manual Light is OFF, the computer is in the "automatic" mode, (i.e., while executing a stored program, while displaying MAR, or while entering data into memory via the Console Keyboard). The functional details of each of the Control Keys is described in the following sections.

2.5.5.1 Power Key

This Key is a double pole, single throw toggle. Placing the Power Key in the ON position will cause

a-c voltages to be applied to the Power supplies and d-c voltages to be properly sequenced on the machine.

Placing the Power Key in the OFF position will cause d-c voltages to be sequenced off the machine and a-c voltages to be removed from the power supplies.

2.5.5.2 Display MAR Key

This key is operative only when the Manual Light is ON. For display of a particular MARS register, the MARS Display Selector Switch is set to the desired register. When the Display MAR Key is depressed, the content of that register is placed in MAR and displayed in the MAR Display.

Depression of the Display MAR Key turns OFF the Manual Light. To display a second MARS register the "manual" mode must be reinitiated by depressing the Release Key and then the procedure for displaying a MARS register may be repeated.

2.5.5.3 Instruction Step Key

This key is operative only when the computer is in the "manual" mode. Depression of this key causes the machine to execute the Instruction-time (8 cycles) and the Execution-time of one instruction step of the stored program. Instructions are executed per IR.

The "manual" mode is retained; depression of the Start Key will cause the execution of the program at high speed in the "automatic" mode.

2.5.5.4 Reset Key

Depression of the Reset Key restores all Machine Status Indicators and Machine Check Indicators and Signal Lights to their initial or "reset" condition.

The Manual Signal Light remains ON.

2.5.5.5 Increment Display Key

This Key is used to display sequentially the digits of any memory area in the MDR Display and the MBR Display. The display procedure is as follows:

2.5.5.5.1 While in the "automatic" mode the computer executes the full eight Instruction cycles of a write operation in which the Q-address of the instruction is specified to be zero (i.e., Q00QQ) and the P-address specifies the high order digit of the field to be displayed.

(Note: This write operation could be entered as part of the main program or could be entered into memory via the Console Keyboard.)

2.5.5.5.2 A Q-address of zero selects the Console as the output device and the P-address is placed in OR-2.

2.5.5.5.3 At the end of I-time the computer halts but remains in the "automatic" mode.

2.5.5.5.4 Depression of the Increment Display Key causes a memory read out cycle per OR-2. The digit addressed is placed in the MDR Display and the P-address from OR-2 is incremented and replaced in OR-2.

2.5.5.5.5 In this manner, successive depressions of the Increment Display Key display the specified memory area from low order to high order memory address one digit at a time in the MDR Display. (Note: If a record mark is encountered, the display is terminated - except when the display instruction is DUMP NUMERICALLY - and the next instruction in the sequence is executed.)

2.5.5.5.6 In addition to appearing in the MDR Display the digit addressed will appear

with the digit from the adjacent memory position in the two-digit MBR Display. In this way, for each two depressions of the Increment Display Key one CADET alphanumeric character is displayed in the MBR Display.

2.5.5.5.7 To terminate the display operation, depression of the Release Key places the computer in the "manual" mode.

2.5.5.6 Save Key

This Key is operative only when the machine is in the "manual" mode.

Depression of the Save Key will turn ON the Save Light; the Manual Signal Light will remain ON.

The address from IR-1 is stored in PR-1; the next BRANCH BACK (Section 4.24) instruction executed will cause PR-1 (rather than IR-2) to be loaded into IR-1. The BRANCH BACK instruction, when executed, will turn OFF the Save Light so that subsequent BRANCH BACK Instructions will use IR-2.

Depression of the Reset Key will turn OFF the Save Light; therefore, if the Reset Key is depressed after depression of the Save Key and prior to execution of the first BRANCH BACK instruction, the content of PR-1 will not be used.

Depression of the Save Key causes all bits in IR-1 to be set to zero (not usable as an address). The Start Key cannot be depressed without obtaining a MAR Check (Section 2.5.2.1.3); therefore, the Insert Key must be depressed to effect the loading of zero digits (C bits) in IR-1 before the computer will operate in the "automatic" mode.

When the Save Key is used, the routine entered and executed at location 00000 should not contain a

MULTIPLY or MULTIPLY (IMMEDIATE) instruction, which would destroy the content of PR-1.

2.5.5.7 Insert Key

This key is operative only when the computer is in the "manual" mode; depression of this key turns OFF the Manual Light.

Depression of the Insert Key causes zeros to be loaded into IR-1 and OR-2, and the Console Keyboard is activated so that direct entry of instructions may be made starting with location 00000 (per OR-2). Up to eight consecutive instructions may be keyed in depending upon space available. (Note: The ninth consecutive instruction, if keyed in, would destroy a portion of the multiply table stored beginning at 00100.) The last instruction in the sequence should be either a BRANCH BACK or BRANCH (unconditional) depending upon whether or not the Save Key was used. (Note: Entry of only the 2-digit operation code portion of BRANCH BACK is required since the P and Q-addresses are not used.)

The Console Keyboard will remain activated until the Release Key is depressed.

Depression of the Start Key will cause the computer to execute the instruction stored at location 00000.

2.5.5.8 Release Key

This key is operative only when the computer is in the "automatic" mode.

Depression of this key will terminate any I/O operation by issuing a "disconnect" to the device. The "manual" mode is initiated and the Manual Light is turned ON. If the Insert Light is ON, it is turned OFF.

2.5.5.8.1 The Release Key is used to initiate the "manual" mode after the display of each MARS register (see Display MAR Key, Section 2.5.5.2).

2.5.5.8.2 The Release Key is used to terminate the operation when the Increment Display Key is used to display a memory area (Section 2.5.5. 5.).

2.5.5.8.3 The Release Key is used to restore the "manual" mode after entering data into memory via the Console Keyboard (Section 2.5.5.7).

2.5.5.9 Start Key

This key is operative only when the computer is in the "manual" mode.

Depression of this Key continues execution of instructions at high speed if the computer has halted at a program stop, a machine check, or if it is being returned to "automatic" operation after having been in "manual" operation. The address of the first instruction to be executed is contained in IR-1.

Depression of the Start Key turns ON the Start Light and turns OFF the Manual Light.

2.5.5.10 Stop Key

Depression of this key causes the machine to halt and it operates in two modes depending on whether or not the Instantaneous Stop Key is depressed simultaneously. If the Stop Key only is depressed, the machine halts at the end of E-time of the instruction the machine is then executing. If the Stop Key is depressed simultaneously with the Instantaneous Stop Key, the machine halts at the end of the memory cycle which the machine is then executing; the Instantaneous Stop Indicator is turned ON.

Depression of the Stop Key terminates the "automatic" mode and initiates the "manual" mode. The Manual Light is turned ON; if the Start Light is ON, it is turned OFF.

2.5.5.11 Instantaneous Stop Key

Depression of this key only has no effect on machine operation; if the Stop Key is simultaneously depressed, the machine halts at the end of the memory cycle which the machine is then executing. The Instantaneous Stop Indicator is turned ON.

2.5.6 Signal Lights

These lights are provided as an aid to the operator; the ON/OFF condition of these lights and combinations of these lights and the Indicator Displays (Section 2.5.2) make it possible to analyze easily the mode and type of operation occuring at any time. Error conditions and "hung" conditions are readily detectable. In console procedures where several keying operations are required (such as entering and executing a number of instructions), these lights retain a setting which indicates clearly which step of the keying procedure was last completed.

A description of the conditions which control the set and reset of each of these lights is described in the following sections.

2.5.6.1 Power On Light

This light is turned ON when the Power On Key is thrown. It will remain on as long as power is applied to the machine and will be turned OFF only when the power is turned off.

2.5.6.2 No Feed Light

This light is turned ON when the computer executes a write operation specifying the Paper Tape Punch as the output device and there is no paper on the feed roll of this device.

This light is also turned ON when a parity check error occurs while punching paper tape.

When either of these conditions occurs the computer will be "hung up" in the "automatic" mode; manual corrective procedure is required. These conditions are readily detectable because the Start Light will remain ON and the No Feed Light is turned ON. The Write Check Indicator (and possibly one or more of the other Data Check Indicators) is also ON. Depression of the Release Key will disconnect the output device and put the computer in the "manual" mode. While in the "manual" mode, depression of the Reset Key will turn OFF the No Feed Light and the other Data Check Indicators. The operator can then take the necessary corrective procedures, re-issue the write operation, depress the Start Key and the computer will resume high speed execution of the stored program.

2.5.6.3 Save Light

The Save Light is turned ON when the Save Key is depressed; it is turned OFF by the execution of a BRANCH BACK instruction while in "automatic" mode or by depression of the Reset Key while in "manual" mode.

When the Save Light is ON, either the Manual Light or the Start Light or the Insert Light is also ON.

2.5.6.4 Insert Light

This light is turned ON when the Insert Key is depressed; it is turned OFF by depression of the Release Key or the Reset Key.

When the Insert Light is ON, neither the Manual Light nor the Start Light is ON.

2.5.6.5 Start Light

This light is turned ON when the Start Key is

depressed; it is turned OFF by the execution of a HALT instruction or by depression of the Release Key or the Stop Key.

Whenever the Start Light is ON the computer is in the "automatic" mode; the other condition under which the computer is in the "automatic" mode is when neither the Manual Light nor the Start Light is ON.

The Save Light and/or the No Feed Light can be ON while the Start Light is ON.

2.5.6.6 Manual Light

Whenever this light is ON, the computer is in the "manual" mode; whenever this light is OFF the computer is in the "automatic" mode.

The manual Light is turned ON by the execution of a HALT instruction or by depression of the Release Key or the Stop Key. Depression of any of the following Control Keys will turn the Manual Light OFF: Start Key, Insert Key, Display MAR Key.

The Save Light and/or the No Feed Light can be ON when the Manual Light is ON.

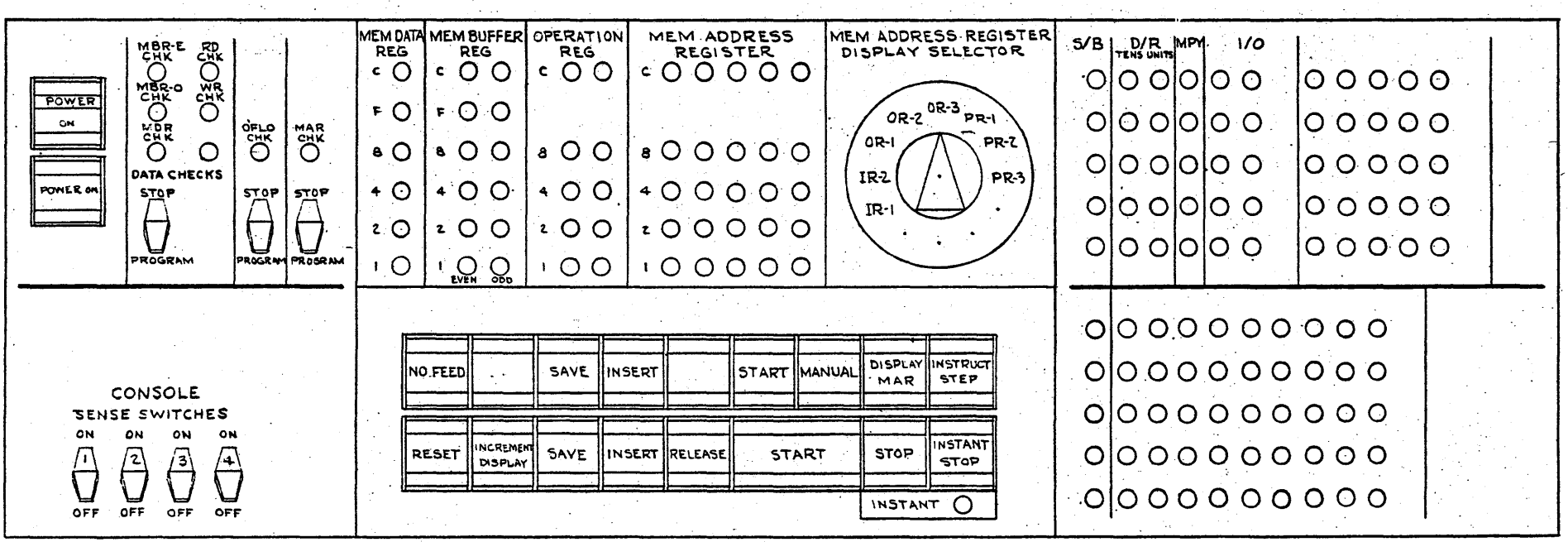
FIGURE 2.1
CADET PAPER TAPE CODE

X	0	X	0	X	0	X	0				
1	1	1	0	0	1	0	0	8	4	2	1
								1	1	1	1
								1	1	1	0
								1	1	0	1
)		*		(		@		1	1	0	0
.		$		,		=		1	0	1	1
				‡				1	0	1	0
I		R		Z		9		1	0	0	1
H		Q		Y		8		1	0	0	0
G		P		X		7		0	1	1	1
F		⊙		W		6		0	1	1	0
E		N		V		5		0	1	0	1
D		M		U		4		0	1	0	0
C		L		T		3		0	0	1	1
B		K		S		2		0	0	1	0
A		J		/		1		0	0	0	1
+		−		0		b		0	0	0	0

COMPANY CONFIDENTIAL

CADET OPERATOR'S CONSOLE

FIGURE 2.2



7-31-59

3.0 ARITHMETIC OPERATIONS

All arithmetic operations are performed using an assigned "Table Area" in memory in which is stored all possible two digit sums and two digit products. (See Figure 3.1 and 3.2) No adder circuitry exists. (Subtraction uses the add table also through complement additions.)

3.1 Addition

3.1.1 Four memory references are required for the development of each digit in the algebraic sum in the following manner:

3.1.1.1 One digit of the addend is read from memory per OR-1 to the units position of the two digit Digit Registers serving MARS.

3.1.1.2 The corresponding digit of the augend per OR-2 is read from memory to the tens position of MAR.

3.1.1.3 Simultaneously with 3.1.1.2 the addend digit stored in the Digit Registers is read to the units position of MAR and this manufactured address (with a "3" forced into the hundreds position of MAR) is used to read the one digit sum from the addition table stored in memory (from locations 00300 to 00399) to the MDR. (See Figure 3.1)

3.1.1.4 The one digit sum is then read from the MDR into memory to the correct digit position of the sum (per OR-2) replacing the augend digit.

3.1.2 Carries resulting from the addition of two digits are noted by flags over the appropriate one digit sums in the addition table. Detection of these sets a logical path for the next addend digit so that the addend digit is increased by one before it is used to address the addition table in the next add cycle.

3.1.3 Recomplement is required in any add operation where the signs of the addend and augend are initially different and the sign of the sum is positive.

3.2 Subtraction

3.2.1 Four memory references are required for the development of each digit in the algebraic difference in the following manner:

3.2.1.1 One digit of the subtrahend is read from memory per OR-1 to the units position of the two digit Digit Registers serving MARS.

3.2.1.2 The corresponding digit of the minuend per OR-2 is read from memory to the tens position of MAR.

(Note: The minuend digit may be complemented before it is placed in MAR, depending upon the relative difference in signs of the minuend and subtrahend, so that the addition table can be used.)

3.2.1.3 Simultaneously with 3.2.1.2 the subtrahend digit stored in the Digit Registers is read to the units position of MAR. (Note: The subtrahend digit may be complemented before it is placed in MAR, depending upon the relative difference in signs of the minuend and subtrahend, so that the addition table can be used.) This manufactured address (with a "3" forced into the hundreds position of MAR) is used to read the one digit difference (or complement sum)from the addition table stored in memory (from locations 00300 to 00399) to the MDR. (See Figure 3.1)

3.2.1.4 The one digit difference is then read from the MDR into memory to the correct digit position of the difference (per OR-2) replacing the minuend digit.

3.2.2 Carries resulting from the subtraction are noted by flags over the appropriate one digit differences in the addition table. Detection of these sets a logical path for the next subtrahend digit so that the subtrahend digit is increased by one before it is used to address the addition table in the next subtract cycle.

3.2.3 Recomplement is required for any subtract operation where the signs of the subtrahend and minuend are initially the same and the sign of the difference is positive.

3.3 Multiplication

3.3.1 Approximately eight memory references are required to develop each digit of a partial product in the Product Area in memory (locations 00080 - 00099) in the following manner:

3.3.1.1 One digit of the multiplier is read out from memory per OR-1 to a Multiplier Register where it is retained for use with each digit of the multiplicand.

3.3.1.2 The multiplicand digit is then read from memory per OR-2 and is placed in the tens position of MAR.

3.3.1.3 Simultaneously with 3.3.1.2 the multiplier digit is passed through a doubler circuit to form two digits which are entered into the hundreds and units position of MAR. (the digit entering the hundreds position is increased by one before being placed in MAR). This manufactured address is used to read the two digit product (whose digits are in reverse order) from the multiplication table stored in memory (from locations 00100 to 00299) to the MBR. See Figure 3.2. The two digit product is then stored (with digits in the correct order) in the two digit Digit Registers serving MARS.

3.3.1.4 The appropriate digit of the Product Area in memory is then read out per PR-2 (PR-1 on the first multiply cycle associated with a new multiplier digit) to the tens position of MAR. Simultaneously the units digit of the two digit product in the Digit Registers is read to the units position of MAR.

3.3.1.5 This manufactured address (with a "3" forced into the hundreds position of MAR) is used to read the one digit sum from the addition table to the MDR.

3.3.1.6 This one digit sum is placed back in the appropriate position of the Product Area per PR-2 and the address contained in PR-2 decremented by one.

3.3.1.7 The next low order digit of the Product Area per PR-2 is read out to the tens position of MAR. Simultaneously the tens digit of the two digit product in the Digit Registers is read to the units position of MAR.

3.3.1.8 This manufactured address (with a "3" forced into the hundreds position of MAR) is used to read the one digit sum from the addition table to the MDR.

3.3.1.9 This one digit sum is placed back in the appropriate position of the Product Area per PR-2.

3.3.1.10 Carries, if any, are propagated through the partial product using the addition table and addressing the appropriate positions of the partial product per PR-3 before the next multiplication cycle begins.

3.3.2 The number of digits in the product is limited only by available memory space. The twenty digit locations in the Product Area in memory will be cleared to zeros at the beginning of E-time in the MULTIPLY and MULTIPLY (IMMEDIATE) instructions. The length of the product may correctly exceed twenty digits if a program is written to clear to zero the appropriate number of locations in excess of twenty before multiplying. If the product exceeds 100 digits, the 101st digit (high order end of product) will be placed in location 19999 and remaining digits in succeeding lower memory locations.

FIGURE 3. 1

CADET ADDITION TABLE

(For Use in Execution of All Arithmetic Instructions)

Address ten-thousands, thousands, hundreds, tens digits

Address units digit

	0	1	2	3	4	5	6	7	8	9
0030	0	1	2	3	4	5	6	7	8	9
0031	1	2	3	4	5	6	7	8	9	$\overline{0}$
0032	2	3	4	5	6	7	8	9	$\overline{0}$	$\overline{1}$
0033	3	4	5	6	7	8	9	$\overline{0}$	$\overline{1}$	$\overline{2}$
0034	4	5	6	7	8	9	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
0035	5	6	7	8	9	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$
0036	6	7	8	9	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$
0037	7	8	9	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$
0038	8	9	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
0039	9	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$

FIGURE 3. 2

CADET MULTIPLICATION TABLE

(For Use in Execution of Multiply Instruction)

Address units digit

Address ten-thousands, thousands, hundreds, tens digits

	0	1	2	3	4	5	6	7	8	9
0010	0	0	0	0	0	0	0	0	0	0
0011	0	0	1	0	2	0	3	0	4	0
0012	0	0	2	0	4	0	6	0	8	0
0013	0	0	3	0	6	0	9	0	2	1
0014	0	0	4	0	8	0	2	1	6	1
0015	0	0	5	0	0	1	5	1	0	2
0016	0	0	6	0	2	1	8	1	4	2
0017	0	0	7	0	4	1	1	2	8	2
0018	0	0	8	0	6	1	4	2	2	3
0019	0	0	9	0	8	1	7	2	6	3
0020	0	0	0	0	0	0	0	0	0	0
0021	5	0	6	0	7	0	8	0	9	0
0022	0	1	2	1	4	1	6	1	8	1
0023	5	1	8	1	1	2	4	2	7	2
0024	0	2	4	2	8	2	2	3	6	3
0025	5	2	0	3	5	3	0	4	5	4
0026	0	3	6	3	2	4	8	4	4	5
0027	5	3	2	4	9	4	6	5	3	6
0028	0	4	8	4	6	5	4	6	2	7
0029	5	4	4	5	3	6	2	7	1	8

4.0 INSTRUCTION SET

The instructions described in the following pages are executed according to the rules for instructions and data fields presented in Sections 1.3 and 1.4. In addition to these, two additional points should be noted as follows:

4.0.1 The Q-address portion of an instruction can be an address or data depending on whether or not the instruction has an "Immediate" tag (operation codes 11 through 17). If tagged "Immediate", digit Q_1 becomes the units digit of one of the data fields used by the instruction. This data field is identical to any other data field and may be of any length of two digits or more as long as a flag bit defines its high order postion. In most practical cases it will be self contained in the Q-address with five digits the maximum length; however, this is not a restriction and the field may extend into the P-address (or beyond) if necessary. It must be remembered, however, that any data field extending into the P-address must have digits P_1 through P_5 usable as an address also.

In those instructions having an "Immediate" tag, the address of the units digit of the Q-address portion of the instruction itself (ie: Q_1) is derived from IR-1 during the last cycle of I-time and is placed in OR-1. The Q-address of an "Immediate" instruction is not, therefore, available for display from any of the MARS registers.

4.0.2 If digit O_2 of the operation code portion of the instruction is not at an even memory location, the instruction will not be properly executed. Similarly the P-address of a Branch Operation must specify the memory location of the first digit of the next instruction to be executed, and, therefore, refer to an even memory location.

4.1 Instruction: ADD

Mnemonic: A

Operation Code: 21

Summary: Add the field at QQQQQ to the field at PPPPP and store the result at PPPPP.

Function:

1. The location of the addend is specified by OR-1 (5 digits in the form of QQQQQ). The location of the augend is specified by OR-2 (5 digits in the form PPPPP). The algebraic sum is stored (replacing the augend) in the field specified by OR-2 (PPPPP). The addend will remain unchanged in the field specified by OR-1 (QQQQQ).

2. Addition proceeds serially, one digit at a time, building up partial sums from low order to high order digit of the sum field until the operation is terminated by a flag bit in the high order position of the augend. The high order digit of the sum is marked by storing a flag bit. The sign of the sum is marked by the presence or absence of a flag bit in the units position of the sum (-flag;+no flag). A zero sum is always stored as a negative field, except in the case of adding two positive zero fields.

3. The number of digits in the sum is equal to the number of digits in the augend. For a complete sum to be formed, the number of digits in the augend at PPPPP must be greater than or equal to the number of digits in the addend at QQQQQ. If this rule is violated, the Overflow Indicator is turned ON, and the addition is performed using only as many addend digits as there are positions in the augend (the extra digits in the addend are not used). The algebraic sum of the two equal length fields is then obtained.

4. Minimum field length for either the augend or the addend is two digits.

Resulting Indicator Conditions:

1. The High/Positive Indicator is turned ON if the sum is positive and is turned OFF if the sum is negative.

2. The Equal/Zero Indicator is turned ON if the sum is zero and is turned OFF if the sum is not zero.

3. The Overflow Indicator is turned ON if an overflow occurs; the overflow digit is lost. If the Overflow Indicator was turned ON as a result of a previous arithmetic operation, a no overflow condition on this ADD instruction will not turn it OFF.

Note: Once the High/Positive or Equal/Zero Indicators are turned ON (or OFF) by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed, (unless the Reset Key on the console is depressed which turns these indicators OFF). Testing them with a BI or BNI instruction has no effect upon their state. The Overflow Indicator will be turned OFF only by testing it with a BI or BNI instruction (or by depressing the Reset Key on the Console).

Execution Time:

1. Basic 8 + 4P memory cycles

2. Recomplement ~~4~~ 3 (1 + P) memory cycles

(Where P is the number of augend digits in the field addressed by OR-2 (PPPPP)

Recomplement time must be included when the signs of the two fields to be operated upon are initially different and the sign of the sum is ~~positive~~ opposite the augend

4.2 Instruction: ADD (IMMEDIATE)

Mnemonic: AM

Operation Code: 11

Summary: Add the Q-address to the field at PPPPP and store the result at PPPPP.

Function:

1. The location of the addend is specified by OR-1 (5 digits specifying the field beginning within the Q-address portion of the instruction itself). The units digit of the addend is digit Q_1. The location of the augend is specified by OR-2 (5 digits in the form PPPPP) The algebraic sum is stored (replacing the augend) in the field specified by OR-2 (PPPPP). The addend will remain unchanged in the Q-address field specified by OR-1.

2. Addition proceeds serially, one digit at a time, building up partial sums from low order to high order digit of the sum field until the operation is terminated by a flag bit in the high order position of the augend. The high order digit of the sum is marked by storing a flag bit. The sign of the sum is marked by the presence or absence of a flag bit in the units position of the sum (-flag; +no flag). A zero sum is always stored as a negative field, except in the case of adding two positive zero fields.

3. The number of digits in the sum is equal to the number of digits in the augend. For a complete sum to be formed the number of digits in the augend at PPPPP must be greater than or equal to the number of digits of the Q-address used as the addend. If this rule is violated, the Overflow Indicator is turned ON, and the addition is performed using only as many addend digits as there are positions in the augend (the extra digits in the addend are not used). The algebraic sum of the two equal length fields is then obtained.

4. Minimum field length for either the augend or the addend is two digits.

Resulting Indicator Conditions:

1. The High/Positive Indicator is turned ON if the sum is positive and is turned OFF if the sum is negative.

2. The Equal/Zero Indicator is turned ON if the sum is zero and is turned OFF if the sum is not zero.

3. The Overflow Indicator is turned ON if an overflow occurs; the overflow digit is lost. If the Overflow Indicator was turned ON as a result of a previous arithmetic operation, a no overflow condition on this ADD (IMMEDIATE) instruction will not turn it OFF.

Note: Once the High/Positive or Equal/Zero Indicators are turned ON (or OFF) by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed, (unless the Reset Key on the console is depressed which turns these indicators OFF). Testing them with a BI or BNI instruction has no effect upon their state. The Overflow Indicator will be turned OFF only by testing it with a BI or BNI instruction (or by depressing the Reset Key on the Console).

Execution Time:

1. Basic 8 + 4P memory cycles

2. Recomplement 3 (1 + P) memory cycles

(Where P is the number of augend digits in the field addressed by OR-2 (PPPPP).

Recomplement time must be included when the signs of the two fields to be operated upon are initially different and the sign of the sum is ~~positive~~. opposite the AUGEND

4.3 Instruction: SUBTRACT

Mnemonic: S

Operation Code: 22

Summary: Subtract the field at QQQQQ from the field at PPPPP and store the result at PPPPP.

Function:

1. The location of the subtrahend is specified by OR-1 (5 digits in the form of QQQQQ.) The location of the minuend is specified by OR-2 (5 digits in the form of PPPPP). The algebraic difference is stored (replacing the minuend) in the field specified by OR-2 (PPPPP). The subtrahend will remain unchanged in the field specified by OR-1 (QQQQQ).

2. Subtraction proceeds serially, one digit at a time, building up partial differences from the low order to the high order digit of the difference field until the operation is terminated by a flag bit in the high order position of the minuend at PPPPP. The high order digit of the difference is marked by storing a flag bit. The sign of the difference is marked by the presence or absence of a flag bit in the units position of the difference (-flag; + no flag). A zero difference is always stored as a negative field, except in the case of subtracting a negative zero field from a positive zero field.

3. The number of digits in the difference is equal to the number of digits in the minuend. For a complete difference to be formed, the number of digits in the minuend at PPPPP must be greater than or equal to the number of digits in the subtrahend at QQQQQ. If this rule is violated, the Overflow Indicator is turned ON and the subtraction is performed using only as many subtrahend digits as there are positions in the minuend (the extra digits in the subtrahend are not used). The algebraic difference of the two equal length fields is then obtained.

4. Minimum field length for either the minuend or the subtrahend is two digits.

Resulting Indicator Conditions:

1. The High/Positive Indicator is turned ON if the difference is positive and is turned OFF if the difference is negative.

2. The Equal/Zero Indicator is turned ON if the difference is zero and is turned OFF if the difference is not zero.

3. The Overflow Indicator is turned ON if an overflow occurs; the overflow digit is lost. If the Overflow Indicator was turned ON as a result of a previous arithmetic operation, a no overflow condition on this SUBTRACT instruction will not turn it OFF.

Note: Once the High/Positive or Equal/Zero Indicators are turned ON (or OFF) by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed, (unless the Reset Key on the Console is depressed which turns these indicators OFF). Testing them with a BI or BNI instruction has no effect upon their state. The Overflow Indicator will be turned OFF only by testing it with a BI or BNI instruction (or by depressing the Reset Key on the Console).

Execution Time:

1. Basic 8 + 4P memory cycles

2. Recomplement 3 (1 + P) memory cycles

(Where P is the number of minuend digits in the field addressed by OR-2 (PPPPP).

Recomplement time must be included when the signs of the two fields to be operated upon are initially the same and the sign of the difference is ~~positive~~. OPPOSITE THE MINUEND.

4.4 Instruction: SUBTRACT (IMMEDIATE)

Mnemonic: SM

Operation Code: 12

Summary: Subtract the Q-address from the field at PPPPP and store the result at PPPPP.

Function:

1. The location of the subtrahend is specified by OR-1 (5 digits specifying the field ~~within~~ beginning @ the Q-address portion of the instruction itself). The units digit of the subtrahend is digit Q_{11}. The location of the minuend is specified by OR-2 (5 digits in the form of PPPPP. The algebraic difference is stored (replacing the minuend) in the field specified by OR-2 (PPPPP). The subtrahend will remain unchanged in the Q-address field specified by OR-1.

2. Subtraction proceeds serially, one digit at a time, building up partial differences from the low order digit to the high order digit of the difference field until the operation is terminated by a flag bit in the high order position of the minuend at PPPPP. The high order digit of the difference is marked by storing a flag bit. The sign of the difference is marked by the presence or absence of a flag bit in the units position of the difference (-flag; + no flag). A zero difference is always stored as a negative field, except in the case of subtracting a negative zero field from a positive zero field.

3. The number of digits in the difference is equal to the number of digits in the minuend. For a complete difference to be formed the number of digits in the minuend at PPPPP must be greater than or equal to the number of digits of the Q-address used as the subtrahend. If this rule is violated, the Overflow Indicator is turned ON and the subtraction is performed using only as many subtrahend digits as there are positions in the minuend (the extra digits in the subtrahend are not used). The algebraic difference of the two equal length fields is then obtained.

4. Minimum field length for either the minuend or the subtrahend is two digits.

Resulting Indicator Conditions:

1. The High/Positive Indicator is turned ON if the difference is positive and is turned OFF if the difference is negative.

2. The Equal/Zero Indicator is turned ON if the difference is positive and is turned OFF if the difference is negative.

3. The Overflow Indicator is turned ON if an overflow occurs; the overflow digit is lost. If the Overflow Indicator was turned ON as a result of a previous arithmetic operation, a no overflow condition on this SUBTRACT (IMMEDIATE) instruction will not turn it OFF.

Note: Once the High/Positive or Equal/Zero Indicators are turned ON (or OFF) by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed, (unless the Reset Key on the Console is depressed which turns these indicators OFF). Testing them with a BI or BNI instruction has no effect upon their state. The Overflow Indicator will be turned OFF only by testing it with a BI or BNI instruction (or by depressing the Reset Key on the Console).

Execution Time:

1. Basic 8 + 4P memory cycles

2. Recomplement 3 (1 + P) memory cycles

(Where P is the number of minuend digits in the field addressed by OR-2 (PPPPP).

Recomplement time must be included when the signs of the two fields to be operated upon are initially the same and the sign of the difference is ~~positive~~. OPPOSITE THE MINUEND

4.5 Instruction: MULTIPLY

Mnemonic: M

Operation Code: 23

Summary: Multiply the field at PPPPP by the field at QQQQQ and place the result in the field at 00099.

Function:

1. The location of the multiplier is specified by OR-1 (5 digits in the form QQQQQ). The location of the multiplicand is specified by OR-2 (5 digits in the form (PPPPP). The algebraic product is placed at location 00099 and succeedingly lower memory locations. Both the multiplier and the multiplicand remain unchanged when the multiplication is completed.

2. Multiplication proceeds serially, one digit at a time, building up partial products from the low order to high order digit of the product field until the operation is terminated by a flag bit in the high order position of the multiplier field. The high order position of the product is marked by storing a flag bit. The sign of the product is marked by the presence or absence of a flag bit in the units position of the product (-flag;+ no flag). A zero product may be stored as a positive field or a negative field depending upon the signs of the multiplier and multiplicand.

3. The number of digits in the product is limited only by available memory space, and is equal to the sum of the number of digits in the multiplier and the number of digits in the multiplicand. Twenty digits of the Product Area in memory (locations 00080-00099) are cleared to zeros at the beginning of E-time in the execution of this instruction. The length of the product may correctly exceed 20 digits if a program is written to clear to zero the appropriate number of locations in excess of 20 before this instruction is executed. If the product exceeds 100 digits, the 101st digit (high order end of product) will be placed in location 19999 and remaining digits in succeedingly lower memory locations.

4. Minimum field length for either the multiplier or multiplicand is two digits.

Resulting Indicator Conditions:

1. The High/Positive Indicator is turned ON if the product is positive and is turned OFF if the product is negative.

2. The Equal/Zero Indicator is turned ON if the product is zero and is turned OFF if the product is not zero.

Note: Once the High/Positive or Equal/Zero Indicators are turned ON (or OFF) by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed, (unless the Reset Key on the Console is depressed which turns the indicators OFF). Testing them with a BI or BNI instruction has no effect upon their state.

Execution Time: 28 + Q (8.4P + 2) memory cycles

(Where Q is the number of multiplier digits in the field addressed by OR-1 (QQQQQ) and P is the number of multiplicand digits in the field addressed by OR-2 (PPPPP).

4.6 Instruction: MULTIPLY (IMMEDIATE)

Mnemonic: MM

Operation Code: 13

Summary: Multiply the field at PPPPP by the Q-address and place the result in the field at 00099.

Function:

1. The location of the multiplier is specified by OR-1 (5 digits specifying the field within the Q-address portion of the instruction itself). The units digit of the multiplier is digit Q_1. The location of the multiplicand is specified by OR-2 (5 digits in the form PPPPP). The algebraic product is placed at location 00099 and succeedingly lower memory locations. Both the multiplier and the multiplicand remain unchanged when the multiplication is completed.

2. Multiplication proceeds serially, one digit at a time, building up partial products from the low order to high order digit of the product field until the operation is terminated by a flag bit in the high order position of the multiplier field. The high order position of the product is marked by storing a flag bit. The sign of the product is marked by the presence or absence of a flag bit in the units position of the product (-flag; + no flag). A zero product may be stored as a positive field or a negative field depending upon the signs of the multiplier and multiplicand.

3. The number of digits in the product is limited only by available memory space, and is equal to the sum of the number of digits in the multiplier and the number of digits in the multiplicand. Twenty digits of the Product Area in memory (locations 00080-00099) are cleared to zeros at the beginning of E-time in the execution of this instruction. The length of the product may correctly exceed 20 digits if a program is written to clear to zero the appropriate number of locations in excess of 20 before this instruction is executed. If the product exceeds 100 digits, the 101st digit (high order end of product) will be placed in location 19999 and remaining digits in succeedingly lower memory locations.

4. Minimum field length for either the multiplier or multiplicand is two digits.

Resulting Indicator Conditions:

1. The High/Positive Indicator is turned ON if the product is positive and is turned OFF if the product is negative.

2. The Equal/Zero Indicator is turned ON if the product is zero and is turned OFF if the product is not zero.

Note: Once the High/Positive or Equal/Zero Indicators are turned ON (or OFF) by an arithmetic or compare operation, they will retain their state until the next arithmetic or compare operation is executed, (unless the Reset Key on the Console is depressed which turns the indicators OFF). Testing them with a BI or BNI instruction has no effect upon their state.

Execution Time: $28 + M(8.4P + 2)$ memory cycles

(Where M is the number of multiplier digits in the field whose low order digit is Q_1 and P is the number of multiplicand digits in the field addressed by OR-2 (PPPPP).)

4.7 Instruction: COMPARE

Mnemonic: C

Operation Code: 24

Summary: Compare the field at QQQQQ to the field at PPPPP and determine if the field at PPPPP is high or equal.

Function:

1. The high or equal condition algebraically of the field specified by OR-2 (5 digits in the form PPPPP) relative to the field specified by OR-1 (5 digits in the form QQQQQ) is established. Both fields remain unchanged after the comparison has been completed.

2. The comparison proceeds serially, one digit at a time, from low order to high order digits of the compared fields until the operation is terminated by a flag bit in the high order position of the field at PPPPP. The comparison is performed internally by subtracting the field at QQQQQ from field at PPPPP; however, the digits of the difference are lost.

3. If the signs of the two fields are initially different, the compare operation is terminated after the units digit in each field has been interrogated; the field whose sign is positive is declared high.

4. A true comparison may be executed on two fields containing a random mixture of alphanumeric and special characters (noting that one alphanumeric or special character is stored as two machine digits) or on two numeric fields. A true comparison may not be executed on an alphanumeric field and a numeric field without first expanding the numeric field to the alphanumeric format (or vice versa).

5. For a complete comparison to be performed, the number of digits in the field at PPPPP must be greater than or equal to the number of digits in the field at QQQQQ (unless their signs are not alike). If this rule is violated, the Overflow Indicator is turned ON and the extra digits in the field at QQQQQ are not used; however, the result of the comparison is correct to the point where comparison was terminated.

6. Minimum field length for either of the two fields being compared is two digits. (Note: One digit fields may be compared if their signs are not alike.)

Collating Sequence: The ascending collating sequence from which the results of comparisons are determined is:

1. Numeric sequence: 0 through 9

2. Alphanumeric sequence:

   + .) - $ * , (b = @ A through R / S through Z 0 through 9

The record mark, ≠ , with C-8-2 bit coding will be interpreted as a zero if used as a character in fields being compared. Flag bits have no effect on the collating sequence.

Resulting Indicator Conditions:

1. The High/Positive Indicator is turned ON if the field at PPPPP is algebraically higher than the field at QQQQQ and is turned OFF if not higher.

2. The Equal/Zero Indicator is turned ON if the field at PPPPP is algebraically equal to the field at QQQQQ and is turned OFF if not equal.

Note: Once the High / Positive or Equal/Zero Indicators are turned ON (or OFF) by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed, (unless the Reset Key on the Console is depressed which turns these Indicators OFF.) Testing them with a BI or BNI instruction has no effect upon their state. The Overflow Indicator will be turned OFF only by testing it with a BI or BNI instruction (or by depressing the Reset Key on the Console).

Execution Time:

1. Signs alike: 8 + 4P memory cycles

2. Signs different: 10 memory cycles

(Where P is the number of digits in the field addressed by OR-2 (PPPPP).)

4.8 Instruction: COMPARE (IMMEDIATE)

Mnemonic: CM

Operation Code: 14

Summary: Compare the Q-address to the field at PPPPP and determine if the field at PPPPP is high or equal.

Function:

1. The high or equal condition algebraically of the field specified by OR-2 (5 digits in the form PPPPP) relative to the field specified by OR-1 (5 digits specifying the field within the Q-address portion of the instruction itself) is established. The units digit of the field being compared is digit Q_1. Both fields remain unchanged after the comparison has been completed.

2. The comparison proceeds serially, one digit at a time, from low order to high order digits of the compared fields until the operation is terminated by a flag bit in the high order position of the field at PPPPP. The instruction is performed internally by subtracting the Q-address field from the field at PPPPP; however, the digits of the difference are lost.

3. If the signs of the two fields are initially different, the compare operation is terminated after the units digit in each field has been interrogated; the field whose sign is positive is declared high.

4. A true comparison may be executed on two fields containing a random mixture of alphanumeric and special characters (noting that one alphanumeric or special character is stored as two machine digits) or on two numeric fields. A true comparison may not be executed on an alphanumeric field and a numeric field without first expanding the numeric field to the alphanumeric format (or vice versa).

5. For a complete comparison to be performed, the number of digits in the field at PPPPP must be greater than or equal to the number of digits of the Q-address used (unless their signs are not alike). If this rule is violated, the Overflow Indicator is turned ON and the extra digits in the Q-address field are not used; however, the result of the comparison is correct to the point where comparison was terminated.

6. Minimum field length for either of the two fields being compared is two digits. (Note: One digit fields may be compared if their signs are not alike.)

Collating Sequence: The ascending collating sequence from which the results of comparisons are determined is:

1. Numeric sequence: 0 through 9
2. Alphanumeric sequence:
   + .) - $ * , (b = @ A through R/ S through Z
   0 through 9

The record mark, with C-8-2 bit coding, will be interpreted as a zero if used as a character in fields being compared. Flag bits have no effect on the collating sequence.

Resulting Indicator Conditions:

1. The High/Positive Indicator is turned ON if the field at PPPPP is algebraically higher than the Q-address field and is turned OFF if not higher.
2. The Equal/Zero Indicator is turned ON if the field at PPPPP is algebraically equal to the Q-address field and is turned OFF if not equal.

Note: Once the High/Positive or Equal/Zero Indicators are turned ON (or OFF) by an arithmetic or compare operation, they will retain that state until the next arithmetic or compare operation is executed, (unless the Reset Key on the Console is depressed which turns these indicators OFF.) Testing them with a BI or BNI instruction has no effect upon their state. The Overflow Indicator will be turned OFF only by testing it with a BI or BNI instruction (or by depressing the Reset Key on the Console).

Execution Time: 1. Signs alike: 8 + 4P memory cycles

2. Signs different: 10 memory cycles

(Where P is the number of digits in the field addressed by OR-2 (PPPPP).)

4.9 Instruction: TRANSMIT DIGIT

Mnemonic: TD

Operation Code: 25

Summary: Transmit the single digit at QQQQQ to PPPPP.

Function:

1. The location of the digit to be transmitted is specified by OR-1 (5 digits in the form QQQQQ). The location to which the digit is to be transmitted is specified by OR-2 (5 digits in the form PPPPP). A flag bit, if any, in the digit at QQQQQ is transmitted intact. The digit at PPPPP prior to the transmission is obliterated (including its flag bit, if any). The digit at QQQQQ remains unchanged when transmission is completed.

Execution Time: 10 memory cycles.

4.10 Instruction: TRANSMIT DIGIT (IMMEDIATE)

Mnemonic: TDM

Operation Code: 15

Summary: Transmit the single digit Q_1 to location PPPPP.

Function:

1. The location of the digit to be transmitted (Q_1) is specified by OR-1 (5 digits specifying the units digit of the instruction itself). The location to which digit Q_1 will be transmitted is specified by OR-2 (5 digits in the form PPPPP). A flag bit, if any, in digit Q_1 is transmitted intact. The digit at PPPPP prior to the transmission is obliterated (including its flag bit, if any). The digit Q_1 remains unchanged when transmission is completed.

Execution Time: 10 memory cycles.

4.11 Instruction: TRANSMIT FIELD

Mnemonic: TF

Operation Code: 26

Summary: Transmit the field at QQQQQ to PPPPP.

Function:

1. The location of the field to be transmitted is specified by OR-1 (5 digits in the form QQQQQ). The location to which the field is transmitted is specified by OR-2 (5 digits in the form PPPPP). The field at QQQQQ remains unchanged when transmission is completed.

2. Transmission proceeds serially, one digit at a time, from low order to high order digit of the transmitted field until the operation is terminated by a flag bit in the high order position of the field at QQQQQ. The flag bits in the high order and units positions of the field at QQQQQ are duplicated in the field at PPPPP. The digits in the field at PPPPP prior to the transmission are obliterated (including their flag bits, if any).

Execution Time: 8 + 2Q memory cycles

(Where Q is the number of digits in the field at QQQQQ.)

4.12 Instruction: TRANSMIT FIELD (IMMEDIATE)

Mnemonic: TFM

Operation Code: 16

Summary: Transmit the Q-address to location PPPPP.

Function:

1. The location of the field to be transmitted is specified by OR-1 (5 digits specifying the field within the Q-address portion of the instruction itself). The units digit of the transmitted field is digit Q_1. The location to which the field is transmitted is specified by OR-2 (5 digits in the form PPPPP). The Q-address field remains unchanged when transmission is completed.

2. Transmission proceeds serially, one digit at a time, from low order to high order digit of the transmitted field until the operation is terminated by a flag bit in the high order position of the transmitted field. The flag bits in the high order and units positions of the transmitted field are duplicated in the field at PPPPP. The digits in the field at PPPPP prior to the transmission are obliterated (including their flag bits, if any).

Execution Time: 8 + 2M

(Where M is the number of digits in the field whose low order digit is Q_1.)

4.13 Instruction: TRANSMIT RECORD

Mnemonic: TR

Operation Code: 31

Summary: Transmit the record at QQQQQ to PPPPP.

Function:

1. The location of the record to be transmitted is specified by OR-1 (5 digits in the form QQQQQ). The location to which the record is transmitted is specified by OR-2 (5 digits in the form PPPPP). The record at QQQQQ remains unchanged when transmission is completed.

2. Transmission proceeds serially, one digit at a time, from high order to low order digit of the transmitted record until the operation is terminated by a record mark in the low order position of the record at QQQQQ. All flag bits in the record at QQQQQ are duplicated in the record at PPPPP. The digits in the record at PPPPP prior to the transmission are obliterated (including their flag bits, if any). The record mark is duplicated in the low order position of the record at PPPPP.

Execution Time: 8 + 2Q memory cycles.

(Where Q is the number of digits in the record at QQQQQ.)

4.14 Instruction: SET FLAG

Mnemonic: SF

Operation Code: 32

Summary : Set the flag bit of the digit at PPPPP to one.

Function:

1. The flag bit of the digit at the location specified by OR-2 (5 digits in the form PPPPP) is set to one. The C-bit of the digit is adjusted for correct parity; all other bit positions remain unchanged.

2. The Q-address of the instruction is placed in OR-1 as QQQQQ; however, it is not used in the execution of the instruction.

Execution Time: 10 memory cycles.

4.15 Instruction: CLEAR FLAG

Mnemonic: CF

Operation Code: 33

Summary: Set the flag bit of the digit at PPPPP to zero.

Function:

1. The flag bit of the digit at the location specified by OR-2 (5 digits in the form PPPPP) is set to zero. The C-bit of the digit is adjusted for correct parity; all other bit positions remain unchanged.

2. The Q-address of the instruction is placed in OR-1 as QQQQQ; however, it is not used in the execution of the instruction.

Execution Time: 10 memory cycles.

4.16 Instruction: CONTROL

Mnemonic: K

Operation Code: 34

Summary: Execute the control function specified by Q_4 and Q_3 on the input/output device specified by Q_2.

Function:

1. Digits Q_4 and Q_3 of the instruction specify the selected device with addresses assigned as follows:

   Q01YQ - Keyboard/Printer
   Q02YQ - Paper Tape Punch
   Q03YQ - Paper Tape Reader
   (Note: Q may have any digital value.)

2. Digit Q_2 of the instruction specifies the control function with addresses assigned as follows:

   Q0X1Q - Space
   Q0X2Q - Return Carriage
   Q0X8Q - Tabulate
   (Note: Q may have any digital value.)

   The select address and control address are placed in OR-1 as Q0XYQ (X equal 1, 2, or 3; Y equal 1, 2, or 8). The 0X digits are sent to the sense and branch registers for decoding and for use by the I/O control. Only one device may be selected at any time and the device remains selected only until the execution of the instruction is completed. Selection using an invalid address or a device not on-line will cause the machine to hang-up in the "automatic " mode. The Y digit is placed in the MDR where it is available to the I/O Control. Control addresses are not exclusive. Specifying a control function for a device to which it does not apply or using an invalid control address will cause the machine to hang-up in the "automatic" mode.

Execution Time: Depends upon the control function and the speed of the device selected.

Note: Presently defined control functions are applicable only to the Printer.

4.17 Instruction: DUMP NUMERICALLY

Mnemonic: DN

Operation Code: 35

Summary: Transmit numeric data from PPPPP through location 19998 to the selected output device specified by the Q-address.

Function:

1. The Q-address of the instruction specifies the selected device with select addresses assigned as follows:

   Q01QQ - Printer
   Q02QQ - Paper Tape Punch
   (Note: Q may have any digital value.)

   The select address is placed in OR-1 as Q0XQQ (X equal 1 or 2) and the 0X digits are sent to the Sense and Branch Registers for decoding and for use by the I/O Control. Only one device may be selected at any time and the device remains selected only until the execution of the instruction is completed. Selection using an invalid address or a device not on-line will cause the machine to hangup in the "automatic" mode; a special case of this is a select address of Q00QQ which will cause a Console display of the character in memory specified by the Q-address, but the machine still hangs in the "automatic" mode. (See Section 2.5.5.5)

2. Data from the memory location specified by OR-2 (5 digits in the form PPPPP) and successively higher memory locations is transmitted serially, one digit at a time, to the selected output device. All data will remain unchanged in memory after the write-out is completed. All flag bits in the memory digits are duplicated in the characters of the output data.

   Each digit in memory is transmitted as a single character of output data; alphabetic and special characters (composed of 2 digits in memory) are written as two numeric characters.

3. The operation will continue per OR-2 until the character at memory location 19998 has been written; the operation will then terminate. Record marks in memory are duplicated as characters of output data. (Note: An End of Line punch will be placed in paper tape after the character at 19998 is written if the output device is the paper tape punch.)

   If 19999 is the initial P-address of the instruction the machine will continue writing out digits (with OR-2 looping from memory address 19999 to 00000) until all of memory has been written.

Resulting Indicator Conditions: The Write Check Indicator is turned ON if a parity error occurs in any character being written on an output device. If ON, correct parity in subsequent characters will not turn it OFF. (See Section 2.5.2.1)

Execution Time: Depends upon the speed of the output device.

4.18 Instruction: READ NUMERICALLY

Mnemonic: RN

Operation Code: 36

Summary: Transmit numeric data from the selected input device specified by QQQQQ to the memory location PPPPP and successively higher memory locations.

Function:

1. The Q-address of the instruction specifies the selected device with select addresses assigned as follows:

   Q01QQ - Keyboard
   Q03QQ - Paper Tape Reader
   (Note: Q may have any digital value.)

   The select address is placed in OR-1 as Q0XQQ (X equal 1 or 3) and the 0X digits are sent to the Sense and Branch Registers for decoding and for use by the I/O Control. Only one device may be selected at any time and the device remains selected only until the execution of the instruction is completed. Selection using an invalid address or a device not on-line will cause the machine to hang-up in the "automatic" mode; a select address of Q01QQ will cause the machine to appear to be hung since it awaits manual data entry from the Keyboard.

2. Data from the input device is serially transmitted, one digit at a time, to memory at the location specified by OR-2 (5 digits in the form PPPPP) and successively higher memory locations. All flag bits in the input data (except flag bits on record marks) are duplicated in the digits stored in memory; record marks with flag bits are placed in memory without the flag bit. Every character in the input data is stored in memory as a single digit. The alphanumeric characters - and J through R will be translated and stored in memory as numeric digits 0 through 9 with flag bits; no other alphanumeric or special characters are allowed (except the record mark).

3. The operation is terminated by the input device when it recognizes the end of record and a record mark is placed in memory directly following the last character read in.

   (Note: The Release Key on the Console performs this function if the selected device is the Keyboard but no record mark is entered into memory.)

Resulting Indicator Conditions: The Read Check Indicator is turned ON if a parity error occurs in any character being read from the input device. If ON, correct parity in subsequent characters will not turn it OFF. (See Section 2.5.2.1.)

Execution Time: Depends upon the speed of the input device.

4.19 Instruction: READ ALPHANUMERICALLY

Mnemonic: RA

Operation Code: 37

Summary: Transmit alphanumeric data from the selected input device specified by QQQQQ to memory location PPPPP and successively higher memory locations.

Function:

1. The Q-address of the instruction specifies the selected device with select addresses assigned as follows:

   Q01QQ - Keyboard
   Q03QQ - Paper Tape Reader
   (Note: Q may have any digital value.)

   The select address is placed in OR-1 as Q0XQQ (X equal 1 or 3) and the 0X digits are sent to the Sense and Branch Registers for decoding and for use by the I/O Control. Only one device may be selected at any time and the device remains selected only until the execution of the instruction is completed. Selection using an invalid address or a device not on-line will cause the machine to hang-up in the "automatic" mode; a select address of Q01QQ will cause the machine to appear to be hung since it awaits manual data entry from the Keyboard.

2. Data from the input device is serially transmitted to the memory location specified by OR-2 (5 digits in the form PPPPP) and successively higher memory locations. The units digit of the P-address must be an odd numbered memory location (i.e.: addressing the memory location to which the numeric portion of the first character is read); if even, data is not correctly placed in memory and parity check errors may occur. All flag bits in the memory field to which data is being read remain unchanged; flag bits on the input data are not allowed. Data from the input device may be a random mixture of numeric, alphabetic, and special characters; however, each input character is stored in memory as two numeric digits.

3. The operation is terminated by the input device when it recognizes the end of record and an alphanumeric record mark (zone digit, 0; numeric digit, ≠) will be placed in memory directly following the last character read in.

(Note: The Release Key on the Console performs this function if the selected device is the Keyboard but no alphanumeric record mark is entered into memory.)

Resulting Indicator Conditions: The Read Check Indicator is turned ON if a parity check error occurs in any character being read from the input device. If ON, a correct parity in subsequent characters will not turn it OFF. (See Section 2.5.2.1.)

Execution Time: Depends upon the speed of the input device.

4.20 Instruction: WRITE NUMERICALLY

Mnemonic: WN

Operation Code: 38

Summary: Transmit numeric data from memory location PPPPP and successively higher memory locations to the selected output device specified by QQQQQ.

Function:

1. The Q-address of the instruction specifies the selected device with select addresses assigned as follows:

   Q01QQ - Printer
   Q02QQ - Paper Tape Punch
   (Note: Q may have any digital value.)

   The select address is placed in OR-1 as Q0XQQ (X equal 1 or 2) and the 0X digits are sent to the Sense and Branch Registers for decoding and for use by the I/O Control. Only one device may be selected at any time and the device remains selected only until the execution of the instruction is completed. Selection using an invalid address or a device not on-line will cause the machine to hang up in the "automatic" mode; a special case of this is a select address Q00QQ which will cause a Console display of the character in memory specified by the P-address, but the machine still hangs in the "automatic" mode. (See Section 2.5.5.5)

2. Data from the memory location specified by OR-2 (5 digits in the form PPPPP) and successively higher memory locations is transmitted serially, one digit at a time, to the selected output device. All data will remain unchanged in memory after the write-out is completed. All flag bits in the memory digits are duplicated in the characters of the output data.

   Each digit in memory is transmitted as a single character of output data; alphabetic and special characters (composed of 2 digits in memory) are written as two numeric characters.

3. The operation is terminated by the recognition of a record mark in memory. The record mark is not written on the output device.* If no record mark exists in memory, the machine will continue writing out characters (with OR-2 looping from memory location 19999 to 00000) until the Stop Key and the Instantaneous Stop Key on the Console are simultaneously depressed.

Resulting Indicator Conditions: The Write Check Indicator is turned ON if a parity error occurs in any character being written on an output device. If ON, correct parity in subsequent characters will not turn it OFF. (See Section 2.5.2.1)

Execution Time: Depends upon the speed of the output device.

*Recognition of the record mark will, however, cause an End of Line Punch (8th channel) to be punched in paper tape when the Paper Tape Punch is used.

4.21 Instruction: WRITE ALPHANUMERICALLY

Mnemonic: WA

Operation Code: 39

Summary: Transmit alphanumeric data from memory location PPPPP and successively higher memory locations to the selected output device specified by QQQQQ.

Function:

1. The Q-address of the instruction specifies the selected device with select addresses assigned as follows:

   Q01QQ - Printer
   Q02QQ - Paper Tape Punch
   (Note: Q may have any digital value.)

   The select address is placed in OR-1 as Q0XQQ (X equal 1 or 2) and the 0X digits are sent to the Sense and Branch Registers for decoding and for use by the I/O Control. Only one device may be selected at any time and the device remains selected only until the execution of the instruction is completed. Selection using an invalid address or a device not on-line will cause the machine to hang-up in the "automatic" mode; a special case of this is a select address of Q00QQ which will cause a Console display of the character in memory specified by the P-address, but the machine still hangs up in the "automatic" mode. (See Section 2.5.5.5)

2. Data from the memory location specified by OR-2 (5 digits in the form PPPPP) and successively higher memory locations is transmitted serially to the selected output device. The units digit of the P-address must be an odd numbered memory location (i.e., addressing the numeric portion of the first two digit character of the record to be written); if even, data is not correct when sent to the output device and parity check errors may occur. All data will remain unchanged in memory after the write-out is completed.

Flag bits in the memory digits are not transmitted to the output device. Data in memory may be a random mixture of alphanumeric and special characters; however, two consecutive memory digits are combined as one alphanumeric character written on the output device. Single digit numeric characters in memory when written in this mode cause invalid combinations of numerics (in an attempt to form one alphanumeric output character from two independent memory digits) and parity errors may occur.

3. The operation is terminated by the recognition of an alphanumeric record mark (zone digit, 0; numeric digit, ≠). The record mark is not written on the output device.* If the alphanumeric record mark does not exist in memory the machine will continue writing out characters (with OR-2 looping from memory location 19999 to 00000) until the Stop Key and the Instantaneous Stop Key on the Console are simultaneously depressed. Unless alphanumeric characters exist throughout memory, however, illegal combinations of digits will occur with possible parity errors resulting.

Resulting Indicator Conditions: The Write Check Indicator is turned ON if a parity error occurs in any character being written on an output device. If ON, correct parity in subsequent characters will not turn it OFF. (See Section 2.5.2.1)

Execution Time: Depends upon the speed of the output device.

*Recognition of the record mark will, however, cause an End of Line punch (8th channel) to be punched in paper tape when the Paper Tape Punch is used.

4.22 Instruction: BRANCH AND TRANSMIT

Mnemonic: BT

Operation Code: 27

Summary: Save the content of IR-1 and branch unconditionally to PPPPP. Transmit the field at QQQQQ to PPPPP minus one.

Function:

1. The content of IR-1 is stored in IR-2. (IR-1 is stepped to the address of the next instruction in the sequence before being stored.) The content of OR-2 (5 digits in the form PPPPP) is stored in IR-1.
2. The next instruction to be executed is specified by IR-1.
3. The location of the field to be transmitted is specified by OR-1 (5 digits in the form QQQQQ). The location to which the field is transmitted is specified by OR-2 (PPPPP minus one; the content of OR-2 is decremented by one, prior to the transmission). The field at QQQQQ remains unchanged when transmission is completed.
4. Transmission proceeds serially, one digit at a time, from low order to high order digit of the transmitted field until the operation is terminated by a flag bit in the high order position of the field at QQQQQ. The flag bits in the high order and units positions of the field at QQQQQ are duplicated in the field at PPPPP minus one. The digits in the field at PPPPP minus one prior to the transmission are obliterated (including their flag bits, if any).

Execution Time: 10 + 2Q memory cycles
(Where Q is the number of digits in the field at QQQQQ.)

Note: This instruction must have a P-address whose units digit is an even integer and must be the memory location of the first digit, O_2, of the next instruction to be executed.

4.23 Instruction: BRANCH AND TRANSMIT (IMMEDIATE)

Mnemonic: BTM

Operation Code: 17

Summary: Save the content of IR-1 and branch unconditionally to PPPPP. Transmit the Q-address to PPPPP minus one.

Function:

1. The content of IR-1 is stored in IR-2. (IR-1 is stepped to the address of the next instruction in the sequence before being stored.) The content of OR-2 (5 digits in the form PPPPP) is stored in IR-1.
2. The next instruction to be executed is specified by IR-1.
3. The location of the field to be transmitted is specified by OR-1 (5 digits specifying the field within the Q-address portion of the instruction itself). The units digit of the field being transmitted is digit Q_1. The location to which the field is transmitted is specified by OR-2 (PPPPP minus one; the content of OR-2 is decremented by one, prior to the transmission). The Q-address field remains unchanged when transmission is completed.
4. Transmission proceeds serially, one digit at a time, from low order to high order digit of the transmitted field until the operation is terminated by a flag bit in the high order position of the transmitted field. The flag bits in the high order and units positions of the transmitted field are duplicated in the field at PPPPP minus one. The digits in the field at PPPPP minus one prior to the transmission are obliterated (including their flag bits, if any).

Execution Time: 10 + 2M memory cycles
(Where M is the number of digits in the field beginning at Q_1.)

Note: This instruction must have a P-address whose units digit is an even integer and must be the memory location of the first digit, O_2, of the next instruction to be executed.

4.24 Instruction: BRANCH BACK

Mnemonic: BB

Operation Code: 42

Summary: Branch unconditionally to the instruction specified by IR-2 or PR-1.

Function:

1. The state of the Save Light is interrogated. If the Save Light is OFF, the content of IR-2 is stored in IR-1. If the Save Light is ON, it is turned OFF and the content of PR-1 is stored in IR-1.

2. The next instruction to be executed is specified by IR-1.

3. The P-address of the instruction is placed in OR-2 as PPPPP and the Q-address is placed in OR-1 as QQQQQ; however, neither address is used in the execution of the instruction.

Execution Time: 10 memory cycles

4.25 Instruction: BRANCH ON DIGIT

Mnemonic: BD

Operation Code: 43

Summary: Test any digit in memory specified by QQQQQ and branch to PPPPP if the digit is not zero.

Function:

1. The digit at the location specified by OR-1 (5 digits in the form QQQQQ) is interrogated. If the digit is not a zero, the content of OR-2 (5 digits in the form PPPPP) is stored in IR-1. If the digit is a zero, the operation is terminated.

2. The next instruction to be executed is specified by IR-1.

Execution Time: 10 memory cycles if no branch is executed.
12 memory cycles if the branch is executed.

Note: This instruction must have a P-address whose units digit is an even integer and must be the memory location of the first digit, O_2, of the next instruction to be executed if the branch is taken.

4.26 Instruction: BRANCH NO FLAG

Mnemonic: BNF

Operation Code: 44

Summary: Test the flag bit of any digit in memory specified by QQQQQ and branch to PPPPP if the bit is not present.

Function:

1. The flag bit of the digit at the location specified by OR-1 (5 digits in the form QQQQQ) is interrogated. If the flag bit is a zero, the content of OR-2 (5 digits in the form PPPPP) is stored in IR-1. If the flag bit is a one, the operation is terminated.

2. The next instruction to be executed is specified by IR-1.

Execution Time: 10 memory cycles if no branch is executed.
12 memory cycles if the branch is executed.

Note: This instruction must have a P-address whose units digit is an even integer and must be the memory location of the first digit, O_2, of the next instruction to be executed if the branch is taken.

4.27 Instruction: BRANCH NO RECORD MARK

Mnemonic: BNR

Operation Code: 45

Summary: Test any digit in memory specified by QQQQQ and branch to PPPPP if the digit is not a record mark.

Function:

1. The digit at the location specified by OR-1 (5 digits in the form QQQQQ) is interrogated. If the digit is not a record mark, the content of OR-2 (5 digits in the form PPPPP) is stored in IR-1. If the digit is a record mark, the operation is terminated.

2. The next instruction to be executed is specified by IR-1.

Execution Time: 10 memory cycles if no branch is executed.
12 memory cycles if the branch is executed.

Note: This instruction must have a P-address whose units digit is an even integer and must be the memory location of the first digit, O_2, of the next instruction to be executed if the branch is taken.

4.28 Instruction: BRANCH INDICATOR

Mnemonic: BI

Operation Code: 46

Summary: If the Indicator or Console Sense Switch specified by QQQQQ is ON, branch to PPPPP.

Function:

1. The Q-address of the instruction specifies the Indicator or Console Sense Switch to be interrogated with indicator addresses assigned as follows:

   Q01QQ Console Sense SW #1
   Q02QQ Console Sense SW #2
   Q03QQ Console Sense SW #3
   Q04QQ Console Sense SW #4
   Q06QQ Read Check Indicator
   Q07QQ Write Check Indicator
   Q08QQ MAR Check Indicator
   Q11QQ High/Positive Indicator
   Q12QQ Equal/Zero Indicator
   Q13QQ High/Positive or Equal/Zero Indicators
   Q14QQ Overflow Check Indicator
   Q16QQ MBR— Even Check Indicator
   Q17QQ MBR-Odd Check Indicator
   Q18QQ MDR-Check Indicator
   Q19QQ Any Latch
   (Note: Q may have any digital value).

   The indicator addresses are placed in OR-1 as QQQQQ and digits Q_4 and Q_3 are sent to the Sense and Branch Registers for decoding and for use by the Sense and Branch test. Invalid addresses result in a negative test.

2. The state of the specified indicator is interrogated. If the indicator is ON, the content of OR-2 (5 digits in the form PPPPP) is stored in IR-1. If the indicator is OFF, the operation is terminated.

3. All indicators except the Any Latch, and High/Positive and Equal/Zero Indicators are turned OFF when interrogated regardless of their previous state. Interrogation of the High/Positive and Equal/Zero Indicators has no effect upon their state; they are reset OFF only at the beginning of arithmetic and compare operations. Interrogation of the Any Latch has no effect upon its state; it is turned OFF only when the Data Check Indicator which turned it ON is turned OFF. (See Section 2.5.2.1.1). Interrogation of the Console Sense Switches has no effect upon their state; they are set and reset manually only from the Console.

4. The next instruction to be executed is specified by IR-1.

Execution Time: 8 memory cycles if no branch is executed.
10 memory cycles if the branch is executed.

Note: This instruction must have a P-address whose units digit is an even integer and must be the memory location of the first digit, O_2, of the next instruction to be executed if the branch is taken.

4.29 Instruction: BRANCH NO INDICATOR

Mnemonic: BNI

Operation Code: 47

Summary: If the Indicator or Sense Switch specified by QQQQQ is OFF, branch to PPPPP.

Function:

1. The Q-address of the instruction specifies the Indicator or Console Sense Switch to be interrogated with indicator addresses assigned as follows:

   Q01QQ Console Sense SW #1
   Q02QQ Console Sense SW #2
   Q03QQ Console Sense SW #3
   Q04QQ Console Sense SW #4
   Q06QQ Read Check Indicator
   Q07QQ Write Check Indicator
   Q08QQ MAR Check Indicator
   Q11QQ High/Positive Indicator
   Q12QQ Equal/Zero Indicator
   Q13QQ High/Positive and Equal/Zero Indicators
   Q14QQ Overflow Check Indicator
   Q16QQ MBR-Even Check Indicator
   Q17QQ MBR-Odd Check Indicator
   Q18QQ MDR-Check Indicator
   Q19QQ Any Latch
   (Note: Q may have any digital value.)

   The indicator addresses are placed in OR-1 as QQQQQ and digits Q4 and Q3 are sent to the Sense and Branch Registers for decoding and for use by the Sense and Branch Test. Invalid addresses result in a positive test.

2. The state of the specified indicator is interrogated. If the indicator is OFF the content of OR-2 (5 digits in the form PPPPP) is stored in IR-1. If the indicator is ON, the operation is terminated.

3. All indicators except the Any Latch, and High/Positive and Equal/Zero Indicators are turned OFF when interrogated regardless of their previous state. Interrogation of the High/Positive and Equal/Zero Indicators has no effect upon their state; they are reset OFF only at the beginning of arithmetic and compare operations. Interrogation of the Any Latch has no effect upon its state; it is turned OFF only when the Data Check Indicator which turned it ON is turned OFF. (See Section 2.5.2.1.1.) Interrogation of the Console Sense Switches has no effect upon their state; they are set and reset manually only from the Console.

4. The next instruction to be executed is specified by IR-1.

Execution Time: 8 memory cycles if no branch is executed.
10 memory cycles if the branch is executed.

Note: This instruction must have a P-address whose units digit is an even integer and is the memory location of the first digit, O_2, of the next instruction to be executed if the branch is taken.

4.30 Instruction: HALT

Mnemonic: H

Operation Code: 48

Summary: Stop "automatic" operation.

Function:

1. The computer enters the "manual" mode of operation.

2. When the Start Key on the Console is depressed, the next instruction to be executed is specified by IR-1.

3. The P-address of the instruction is stored in OR-2 as PPPPP and the Q-address of the instruction is stored in OR-1 as QQQQQ; however, neither address is used in the execution of the instruction.

Execution Time: 8 memory cycles.

4.31 Instruction: BRANCH

Mnemonic: B

Operation Code: 49

Summary: Branch unconditionally to PPPPP.

Function:

1. The content of OR-2 (5 digits in the form PPPPP) is placed in IR-1.
2. The next instruction to be executed is specified by IR-1.
3. The Q-address of this instruction is placed in OR-1 as QQQQQ; however, the address is not used in the execution of the instruction.

Execution Time: 10 memory cycles.

Note: This instruction must have a P-address whose units digit is an even integer and is the memory location of the first digit, O_2, of the next instruction to be executed.

4.32 Instruction: NO OPERATION

Mnemonic: NOP

Operation Code: 50 through 99

Summary: Terminate this instruction and proceed to the next instruction in the sequence.

Function:

1. Terminate the operation of this instruction. The next instruction to be executed is specified by IR-1.

2. The P-address of the instruction is placed in OR-2 as PPPPP and the Q-address is placed in OR-1 as QQQQQ; however, neither address is used in the execution of the instruction.

Execution Time: 8 memory cycles.

Figure 4.1

CADET INSTRUCTION SET

P = Number of digits in the field addressed by PPPPP.
Q = Number of digits in the field addressed by QQQQQ.
M = Number of digits in the field whose low order digit is Q_1.

Mnemonic	Code	Operation	Execution Time (Memory Cycle)
A	21	Add	8 + 4P*
AM	11	Add (Immediate)	8 + 4P*
S	22	Subtract	8 + 4P*
SM	12	Subtract (Immediate)	8 + 4P*
M	23	Multiply	28 + Q (8.4P + 2)
MM	13	Multiply (Immediate)	28 + M (8.4P + 2)
C	24	Compare	8+4P (like signs) or 10 (unlike signs)
CM	14	Compare (Immediate)	8+4P (like signs) or 10 (unlike signs)
TD	25	Transmit Digit	10
TDM	15	Transmit Digit (Immediate)	10
TF	26	Transmit Field	8 + 2Q
TFM	16	Transmit Field (Immediate)	8 + 2M
TR	31	Transmit Record	8 + 2Q
SF	32	Set Flag	10
CF	33	Clear Flag	10
K	34	Control	**
DN	35	Dump Numerically	**
RN	36	Read Numerically	**
RA	37	Read Alphanumerically	**
WN	38	Write Numerically	**
WA	39	Write Alphanumerically	**
BT	27	Branch and Transmit	10 + 2Q
BTM	17	Branch and Transmit (Immediate)	10 + 2M
BB	42	Branch Back	10
BD	43	Branch on Digit	10 (no branch) or 12 (branch)
BNF	44	Branch No Flag	10(no branch)or 12(branch)
BNR	45	Branch No Record Mark	10(no branch)or 12(branch)

Mnemonic	Code	Operation	Execution Time (Memory Cycle)
BI	46	Branch Indicator	8(no branch)or 10(branch)
BNI	47	Branch No Indicator	8(no branch)or 10(branch)
H	48	Halt	8
B	49	Branch	10
NOP	50 - 99	No Operation	8

*Recomplement time should be added to these instructions under the following conditions:

1. ADD: add 4(P ± 1) memory cycles when signs are initially different and the sign of the sum is positive (+).

2. SUBTRACT: add 4 (P + 1) memory cycles when signs are initially alike and the sign of the difference is positive (+).

**The execution times of these instructions are dependent upon the speed of the input/output device addressed.

Indicator Codes (Specify in Q address)

Code	Indicator Name
Q01QQ	Console Sense SW #1
Q02QQ	Console Sense SW #2
Q03QQ	Console Sense SW #3
Q04QQ	Console Sense SW #4
Q06QQ	Read Check Indicator
Q07QQ	Write Check Indicator
Q08QQ	MAR Check Indicator
Q11QQ	High/Positive Indicator
Q12QQ	Equal/Zero Indicator
Q13QQ	High/Positive or Equal/Zero Indicator
Q14QQ	Overflow Check Indicator
Q16QQ	MBR-Even Check Indicator
Q17QQ	MBR-Odd Check Indicator
Q18QQ	MDR Check Indicator
Q19QQ	Any Latch

I/O Device Codes (Specify in Q - address)

Code	Device
Q00QQ	Console
Q01QQ	Keyboard/Printer
Q02QQ	Paper Tape Punch
Q03QQ	Paper Tape Reader

Control Codes (Specify in Q-address)

Code	Function
QQQ1Q	Space
QQQ2Q	Return Carriage
QQQ8Q	Tabulate