IBM® 1130 Reference Card

Form X26-3566-4
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Interrupt Level Status Words

Interrupt Level	Interrupt Vector Storage Location	Interrupt Level Status Word Bits 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	00008 (Hex 0008)	The 1442 is the only device that causes an interrupt to level 0. A sense interrupt command is not required to identify the device.															
1	00009 (Hex 0009)	1132 Printer	SCA														
2	00010 (Hex 000A)	Single Disk Storage: 1131 Disk Storage	2310 Drive 1	2310 Drive 2	2310 Drive 3	2310 Drive 4	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device
3	00011 (Hex 000B)	1627 Plotter	SAC Device	SAC Device	SAC Device	2250 Display	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device
4	00012 (Hex 000C)	1134 PTR and 1055 PTP	Console Printer/ Keyboard	1442 Card Read/ Punch	2501 Card Reader	1403 Printer	1231 OMPR	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device
5	00013 (Hex 000D)	Program Stop Key	Interrupt Run Mode	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device	SAC Device

Device Status Words

Device	Device Code	Device Status Word Bits 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Program Stop Key and Interrupt Run Mode	00111	Program Stop Key * (5)	Interrupt Run Mode * (5)														
Console Keyboard and Console Printer	00001	Printer Service Response * (4)	Keyboard Response * (4)	Interrupt Request * (4)	0-Keyboard 1-Console Entry	Printer Busy	Printer Not Ready	Keyboard Busy									
Synchronous Communications Adapter	01010	Read Response * (1)	Write Response * (1)	Check	Timeout * (1)	Auto Answer Request ** (1)	Busy	Enabled **	Ready	Receive Run							
Disk Storage 1131 Disk Storage 2310 Drive 1 2310 Drive 2 2310 Drive 3 2310 Drive 4	00100 10001 10010 10011 10100	Data Error	Operation Complete * (2)	Disk Not Ready	Disk Busy (R/W or Carriage)	Carriage Home										Sector Count	Sector Count
1132 Printer	00110	Read Emitter Response * (1)	Skip Response * (1)	Space Response * (1)	Carriage Busy	Print Scan Check	Not Ready	Printer Busy		Tape Channel 1	Tape Channel 2	Tape Channel 3	Tape Channel 4	Tape Channel 5	Tape Channel 6	Tape Channel 9	Tape Channel 12
Paper Tape Units 1055 Punch 1134 Reader	00011		Reader Response * (4)		Punch Response * (4)	Reader Busy	Reader Not Ready	Punch Busy	Punch Not Ready								

* Causes an interrupt to the interrupt level shown in the circle.
** Auto Answer Request causes an interrupt only if the SCA has been Enabled.

Device Status Words

Device	Device Code	Device Status Word Bits 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1231 Optical Mark Page Reader	01000	Read Response * (4)	Timing Mark Error * (4)	Read Error * (4)	Master Data	OP Complete Response * (4)	OK to Select	Feed Busy	Document Selected by OMPR	Test Timing Mark Chk. Busy	Hopper Empty				Read Busy	Busy	Not Ready
1442 Card Read Punch/Card Punch	00010	Read Response * (0)	Punch Response * (0)	Error Check	Last Card	Operation Complete * (4)			Feed Check (Read Station)							Busy	Not Ready or Busy
1403 Printer	10101	Parity Check	Transfer Complete Interrupt * (4)	Print Complete Interrupt * (4)	Carriage Interrupt * (4)		Print (Ring) Check	Sync Check					Carriage Channel 9	Carriage Channel 12	Carriage Busy	Printer Busy	1403 Not Ready
1627 Plotter	00101	Plotter Response * (3)														Busy	Not Ready
2250 Display Unit	11001	Order Controlled Interrupt * (3)	Keyboard Interrupt * (3)	Detect Interrupt * (3)	Cycle Steal Check * (3)	Detect Status	Reserved	Reserved	Light Pen Switch Status	Busy	Character Mode	Point Mode	Reserved	Reserved	Reserved	Address Displacement	Address Displacement
2501 Card Reader	01001			Error Check	Last Card	Operation Complete * (4)										Busy	Not Ready or Busy

* Causes an interrupt to the interrupt level shown in the circle.

Data Word Formats

Data Word	Data Word Bits															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Single Precision Word	Sign 0 = + 1 = -	Data Bits														
Double Precision Word Even Address (EA)	Sign 0 = + 1 = -	Data Bits														
Odd Address (EA+1)	Data Bits															
Console Keyboard	Character Code												End of Field (EOF)	Backspace (←)	Erase Field	
Console Printer	Character Code						U/L Case 1 = Upper 0 = Lower	0 = Control 1 = Print								
Synchronous Communications Adapter	Data Character for 6-bit Level															
	Data Character for 7-bit Level															
	Data Character for 8-bit Level															
Disk Storage Word 1131 or 2310	Data Bits															
1132 Printer	Character from Read Emitter															
Card Input (Load Mode)	Bit from Card Row 12	Bit from Card Row 11	Bit from Card Row 0	Bit from Card Row 1	Bit from Card Row 2				Bit from Card Row 3	Bit from Card Row 3	Bit from Card Row 4	Bit from Card Row 5	Bit from Card Row 6	Bit from Card Row 7	Bit from Card Row 8	Bit from Card Row 9
Card Input/Output (Normal)	Bit from Card Row 12	Bit from Card Row 11	Bit from Card Row 0	Bit from Card Row 1	Bit from Card Row 2	Bit from Card Row 3	Bit from Card Row 4	Bit from Card Row 5	Bit from Card Row 6	Bit from Card Row 7	Bit from Card Row 8	Bit from Card Row 9				

Data Word Formats and 2250 Display Order Formats

Data Word or 2250 Display Order Word	Data Word or Display Order Word Bits															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1627 Plotter	Pen Movement Code															
Paper Tape Input (Load Mode)	Bit from Channel 4	Bit from Channel 3	Bit from Channel 2	Bit from Channel 1	Bit from Channel 4	Bit from Channel 3	Bit from Channel 2	Bit from Channel 1	Bit from Channel 4	Bit from Channel 3	Bit from Channel 2	Bit from Channel 1	Bit from Channel 4	Bit from Channel 3	Bit from Channel 2	Bit from Channel 1
Paper Tape Input/Output (Normal Mode)	Bit from Channel 8	Bit from Channel 7	Bit from Channel 6	Bit from Channel 5	Bit from Channel 4	Bit from Channel 3	Bit from Channel 2	Bit from Channel 1								
1231 Input Word	Input Segment 1 (Odd)					Input Segment 2 (Even)									Parity Bit Segment 1	Parity Bit Segment 2
1403 Output Word		Parity Bit First Data Character	First Character Data Code							Parity Bit 2nd Data Character	Second Character Data Code					
Set Graphic Mode Vector (SGMV) Point (SGMP)	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	V/P 0 = Vector 1 = Point
Long Absolute XY, 1st Word Beam On (DBA) Beam Off (MBA)	0	1	0	Beam Bit 1 = On 0 = Off			X Coordinate									
2nd Word							Y Coordinate									
Short Absolute X/Y Beam On (DBAX or DBAY) Beam Off (MBAX or MBAY)	0	1	1	Beam Bit 1 = On 0 = Off	X/Y Bit 1 = Y 0 = X		X (0 in Bit 4) or Y (1 in Bit 4) Coordinate									
Incremental XY Beam On (DBI) Beam Off (MBI)	1	X Sign Bit 1 = Minus 0 = Plus	X Increment (ΔX)						Beam Bit 1 = On 0 = Off	Y Sign Bit 1 = Minus 0 = Plus			Y Increment (ΔY)			
Set Character Mode Basic (SCMB), Large (SCML)	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0 = Basic 1 = Large

2250 Stroke Data Word Format and 2250 Control Order Formats

2250 Stroke Data Word or Control Order Word	Stroke Data Word or Control Order Word Bits															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Stroke Data Word Beam On (DBS) Beam Off (MBS)	Length Bit	Stroke 1 X Coordinate			Beam Bit 1 = On 0 = Off	Stroke 1 Y Coordinate			Revert Bit	Stroke 2 X Coordinate			Beam Bit 1 = On 0 = Off	Stroke 2 Y Coordinate		
Character Control Word (CS) Subscript No-Operation Null Superscript New Line						Function Code 000 = Subscript 010 = No-Operation 010 = Null 100 = Superscript 111 = New Line			Revert Bit 0 0 1 0 1						
Short Branch (GSB)	0	0	0	Address												
Long Branch/Interrupt, 1st Wd Unconditional (GB) Unconditional, Ext.(GBE) Conditional (GBC) Conditional, Ext.(GBCE) Unconditional Int. (GI) Conditional Interrupt (GIC)	0	0	1	0	I/B Bit 0 = Int. 1 = Branch	N Bit 0 = Execute 1=2-Word No-Op	I/A Bit 0=Direct Addressing 1 = Indirect Addressing	0	0	0	0	0	0	0	Detect Bit 1 = Light Pen Detect Condition	Switch Bit 1 = Light Pen Switch Condition
2nd Word	Address or Program ID Data															
Set Pen Mode Set Pen Mode (SPM) 1-Word No-Op (GNOP)	0	0	1	1	0	0	0	1					1=Enable Light Pen Detects	1=Disable Light Pen Detects	1=Enable Light Pen Interrupts	1=Disable Light Pen Interrupts
Start Timer (STMR)	0	0	1	1	0	1	0	0								
Revert (RVT)	0	0	1	1	0	1	1	0								
Store Revert Register, 1st Wd	0	0	1	1	0	1	0	1								
2nd Word	Revert Register Storage															

IOCC Codes and Modifiers

Input/Output Control Command (IOCC)	Device Code	Function Code	Modifier Bits 8 9 10 11 12 13 14 15	Hexadecimal Value
Console Printer	00001			
Write		001		XXXX0900
Sense Device (DSW)				
Without Reset		111	0	0F00
With Reset		111	1	0F01
Console Keyboard	00001			
Read		010		XXXX0A00
Control (Interrupt)		100		XXXX0C00
Sense Device (DSW)				
Without Reset		111	0	0F00
With Reset		111	1	0F01
Console Entry Switches	00111			
Read		010		XXXX3A00
Single Disk Storage (1131)	00100			
Initiate Write		101	* * *	XXXX250*
Initiate Read		110	0 * * *	XXXX260*
Initiate Read Check		110	1 * * *	268*
Control				
Seek Forward		100	0	###2400
Seek Backward		100	1	###2404
Sense Device (DSW)				
Without Reset		111	0	2700
With Reset		111	1	2701
Synchronous Communications Adapter	01010			
Initiate Write				
Set to Transmit Condition		101	0	5500
Reset Communications Adapter		101	1	5540
Initiate Read				
Set to Receive Condition		110	0 0	5600
Set to Slave Mode		110	1 0	5602
Set to Master Mode		110	0 1	5601
Write				
Load Buffer from Core Storage		001	0 0 0	XXXX5100
Set Sync/Idle Register		001	1 0 0	XXXX5104
Turn on Audible Alarm		001	0 1 0	5102
Turn off Audible Alarm		001	0 0 1	5101
Read				
Load Core Storage from Buffer		010	0 0	XXXX5200
Diagnostic Read 1		010	0 1	5201
Diagnostic Read 2		010	1 0	5202
Control				
Enable		100	1 0 0 0 0 0 0 0	5480
Disable		100	0 1 0 0 0 0 0 0	5440
Start/Stop Timeout		100	0 0 1 0 0 0 0 0	5420
Synchronize		100	0 0 0 1 0 0 0 0	5410
Diagnostic Mode		100	0 0 0 0 1 0 0 0	5408
End Operation		100	0 0 0 0 0 1 0 0	5404
Set to 6-bit Level		100	0 0 0 0 0 0 1 0	5402
Set to 7-bit Level		100	0 0 0 0 0 0 0 1	5401
Sense Device (DSW)				
Without Reset		111	0	5700
With Reset		111	1	5701
Restart Timers		111	1	5702

Key for Symbols Used in Input/Output Control Commands

- Shaded areas are reserved. (The hexadecimal values were developed assuming all reserved modifiers to be zero.)
- X - Address word (not shown) contains the address of the first core storage location used by the command.
- * - Sector count can be any binary value 000-111 (hexadecimal 0-7).
- # - Address word (not shown) contains the number of cylinders of movement.
- & - Address word (not shown) contains the write (skip) command modifier.

IOCC Codes and Modifiers

Input/Output Control Command (IOCC)	Device Code	Function Code	Modifier Bits 8 9 10 11 12 13 14 15	Hexadecimal Value
Paper Tape Units	00011			
Read (1134)		010		XXXX1A00
Write (1055)		001		XXXX1900
Control (1134)		100		1C00
Sense Device (1134 or 1055 DSW)				
Without Reset		111	0	1F00
With Reset		111	1	1F01
1132 Printer	00110			
Read Emitter		010		XXXX3200
Control				
Start Printer		100	1 0 0 0 0	3480
Stop Printer		100	0 1 0 0 0	3440
Start Carriage		100	0 0 1 0 0	3404
Stop Carriage		100	0 0 0 1 0	3402
Space Carriage		100	0 0 0 0 0 1	3401
Sense Device (DSW)				
Without Reset		111	0	3700
With Reset		111	1	3701
1231 Optical Mark Page Reader	01000			
Read		010		XXXX4200
Control				
Start Read		100	0 1 0	4404
I/O Disconnect		100	0 0 1	4402
Stacker Select		100	1 0 0	4480
Sense Device (DSW)				
Without Reset		111	0	4700
With Reset		111	1	4701
1403 Printer	10101			
Initiate Write		101		XXXXAD00
Control (Single Space)		100		AC00
Write &				
Skip to Channel 1		001		800A900
Skip to Channel 2		001		400A900
Skip to Channel 3		001		200A900
Skip to Channel 4		001		100A900
Skip to Channel 5		001		080A900
Skip to Channel 6		001		040A900
Skip to Channel 7		001		020A900
Skip to Channel 8		001		010A900
Skip to Channel 9		001		008A900
Skip to Channel 10		001		004A900
Skip to Channel 11		001		002A900
Skip to Channel 12		001		001A900
Sense Device (DSW)				
Without Reset		111	0	AF00
With Reset		111	1	AF01
1442 Card Read Punch	00010			
Read		010		XXXX1200
Write		001		XXXX1100
Control				
Stacker Select		100	1 0 0 0	1480
Start Read		100	0 1 0 0	1404
Feed Cycle		100	0 1 0 0	1402
Start Punch		100	0 0 0 1	1401
Sense Device (DSW)				
Without Reset		111	0 0	1700
With Reset (DSW bits 0 and 1)		111	0 1	1701
With Reset (DSW bit 4)		111	1 0	1702
1627 Plotter	00101			
Write		001		XXXX2900
Sense Device (DSW)				
Without Reset		111	0	2F00
With Reset		111	1	2F01

IOCC Codes and Modifiers

Input/Output Control Command (IOCC)	Device Code	Function Code	Modifier Bits 8 9 10 11 12 13 14 15	Hexadecimal Value
2310 Disk Storage (Drive 1)	10001			
Initiate Write		101	* * *	XXXX8D0*
Initiate Read		110	0 * * *	XXXX8E0*
Initiate Read Check		110	1 * * *	8E8*
Control				
Seek Forward		100	0	###8C00
Seek Backward		100	1	###8C04
Sense Device (DSW)				
Without Reset		111	0	8F00
With Reset		111	1	8F01
2310 Disk Storage (Drive 2)	10010			
Initiate Write		101	* * *	XXXX950*
Initiate Read		110	0 * * *	XXXX960*
Initiate Read Check		110	1 * * *	968*
Control				
Seek Forward		100	0	###9400
Seek Backward		100	1	###9404
Sense Device (DSW)				
Without Reset		111	0	9700
With Reset		111	1	9701
2310 Disk Storage (Drive 3)	10011			
Initiate Write		101	* * *	XXXX9D0*
Initiate Read		110	0 * * *	XXXX9E0*
Initiate Read Check		110	1 * * *	9E8*
Control				
Seek Forward		100	0	###9C00
Seek Backward		100	1	###9C04
Sense Device (DSW)				
Without Reset		111	0	9F00
With Reset		111	1	9F01
2310 Disk Storage (Drive 4)	10100			
Initiate Write		101	* * *	XXXXA50*
Initiate Read		110	0 * * *	XXXXA60*
Initiate Read Check		110	1 * * *	A68*
Control				
Seek Forward		100	0	###A400
Seek Backward		100	1	###A404
Sense Device (DSW)				
Without Reset		111	0	A700
With Reset		111	1	A701
2250 Display Unit	11001			
Initiate Write				
Start Regeneration		101	0 0 0 0	XXXXCD00
Set Programmed Function Indicators		101	1 0 0 0	XXXXCD80
Initiate Read		110	0 0 0	XXXXCE00
Control				
No-Operation		100	0 0 0 0	CC00
Reset Display		100	1 0 0 0	CC80
Sense Device (DSW)				
Without Reset		111	0 0 0 0	CF00
With Reset		111	0 0 0 1	CF01
2501 Card Reader	01001			
Initiate Read		110		XXXX4E00
Sense Device (DSW)				
Without Reset		111	0	4F00
With Reset		111	1	4F01
Sense Interrupt (ILSW)--All Devices		111		0700

Instruction Set

Hexadecimal	Load and Store Instructions
	Load Accumulator (LD) 11000
C0XX	Contents of CSL at EA (I+DISP) are loaded into A
C1XX	Contents of CSL at EA (XR1+DISP) are loaded into A
C2XX	Contents of CSL at EA (XR2+DISP) are loaded into A
C3XX	Contents of CSL at EA (XR3+DISP) are loaded into A
C400XXXX	Contents of CSL at EA (Addr) are loaded into A
C500XXXX	Contents of CSL at EA (Addr +XR1) are loaded into A
C600XXXX	Contents of CSL at EA (Addr +XR2) are loaded into A
C700XXXX	Contents of CSL at EA (Addr +XR3) are loaded into A
C480XXXX	Contents of CSL at EA (V in CSL at Addr) are loaded into A
C580XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") are loaded into A
C680XXXX	Contents of CSL at EA (V in CSL at "Addr +XR2") are loaded into A
C780XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") are loaded into A
	Load Double (LDD) 11001
C8XX	Contents of CSL at EA (I + DISP) and EA+1 are loaded into A and Q
C9XX	Contents of CSL at EA(XR1 + DISP) and EA+1 are loaded into A and Q
CAXX	Contents of CSL at EA (XR2 + DISP) and EA+1 are loaded into A and Q
CBXX	Contents of CSL at EA (XR3 + DISP) and EA+1 are loaded into A and Q
CC00XXXX	Contents of CSL at EA (Addr) and EA+1 are loaded into A and Q
CD00XXXX	Contents of CSL at EA (Addr +XR1) and EA+1 are loaded into A and Q
CE00XXXX	Contents of CSL at EA (Addr +XR2) and EA+1 are loaded into A and Q
CF00XXXX	Contents of CSL at EA (Addr +XR3) and EA+1 are loaded into A and Q
CC80XXXX	Contents of CSL at EA (V in CSL at Addr) and EA+1 are loaded into A and Q
CD80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1 are loaded into A and Q
CE80XXXX	Contents of CSL at EA (V in CSL at "ADDR +XR2") and EA+1 are loaded into A and Q
CF80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") and EA+1 are loaded into A and Q
	Store Accumulator (STO) 11010
D0XX	Contents of A are stored in CSL at EA (I+DISP)
D1XX	Contents of A are stored in CSL at EA (XR1+DISP)
D2XX	Contents of A are stored in CSL at EA (XR2+DISP)
D3XX	Contents of A are stored in CSL at EA (XR3+DISP)
D400XXXX	Contents of A are stored in CSL at EA (Addr)
D500XXXX	Contents of A are stored in CSL at EA (Addr +XR1)
D600XXXX	Contents of A are stored in CSL at EA (Addr +XR2)
D700XXXX	Contents of A are stored in CSL at EA (Addr +XR3)
D480XXXX	Contents of A are stored in CSL at EA (V in CSL at Addr)
D580XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR1")
D680XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR2")
D780XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR3")
	Store Double (STD) 11011
D8XX	Contents of A and Q are stored in CSL at EA (I+DISP) and EA+1
D9XX	Contents of A and Q are stored in CSL at EA (XR1 +DISP) and EA+1
DAXX	Contents of A and Q are stored in CSL at EA (XR2 +DISP) and EA+1
DBXX	Contents of A and Q are stored in CSL at EA (XR3 +DISP) and EA+1
DC00XXXX	Contents of A and Q are stored in CSL at EA (Addr) and EA+1
DD00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR1) and EA+1
DE00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR2) and EA+1
DF00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR3) and EA+1
DC80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA+1
DD80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR1") and EA+1
DE80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR2") and EA+1
DF80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR3") and EA+1

Instruction Set

Hexadecimal	Load and Store Instructions
	Load Index (LDX) 01100
60XX	Load DISP into the Instruction Register
61XX	Load DISP into Index Register 1
62XX	Load DISP into Index Register 2
63XX	Load DISP into Index Register 3
6400XXXX	Load Addr into the Instruction Register
6500XXXX	Load Addr into Index Register 1
6600XXXX	Load Addr into Index Register 2
6700XXXX	Load Addr into Index Register 3
6480XXXX	Load contents of CSL at Addr into the Instruction Register
6580XXXX	Load contents of CSL at Addr into Index Register 1
6680XXXX	Load contents of CSL at Addr into Index Register 2
6780XXXX	Load contents of CSL at Addr into Index Register 3
	Store Index (STX) 01101
68XX	Store I in CSL at EA (I+DISP)
69XX	Store XR1 in CSL at EA (I + DISP)
6AXX	Store XR2 in CSL at EA (I + DISP)
6BXX	Store XR3 in CSL at EA (I + DISP)
6C00XXXX	Store I in CSL at EA (Addr)
6D00XXXX	Store XR1 in CSL at EA (Addr)
6E00XXXX	Store XR2 in CSL at EA (Addr)
6F00XXXX	Store XR3 in CSL at EA (Addr)
6C80XXXX	Store I in CSL at EA (V in CSL at Addr)
6D80XXXX	Store XR1 in CSL at EA (V in CSL at Addr)
6E80XXXX	Store XR2 in CSL at EA (V in CSL at Addr)
6F80XXXX	Store XR3 in CSL at EA (V in CSL at Addr)
	Store Status (STS) 00101
28XX	Store status of indicators in CSL at EA (I+DISP)
29XX	Store status of indicators in CSL at EA (XR1+DISP)
2AXX	Store status of indicators in CSL at EA (XR2+DISP)
2BXX	Store status of indicators in CSL at EA (XR3+DISP)
2C00XXXX	Store status of indicators in CSL at EA (Addr)
2D00XXXX	Store status of indicators in CSL at EA (Addr+XR1)
2E00XXXX	Store status of indicators in CSL at EA (Addr+XR2)
2F00XXXX	Store status of indicators in CSL at EA (Addr+XR3)
2C80XXXX	Store status of indicators in CSL at EA (V in CSL at Addr)
2D80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr+XR1")
2E80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr+XR2")
2F80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr+XR3")
	Load Status (LDS) 00100
2000	Set CARRY and OVERFLOW indicators OFF
2001	Set OVERFLOW ON and CARRY OFF
2002	Set OVERFLOW OFF and CARRY ON
2003	Set CARRY and OVERFLOW indicator ON

Key to Symbols Used in the Instruction Set

Symbol	Meaning	Symbol	Meaning
A	Accumulator (ACC)	I	Contents of the instruction register (IAR)
Q	Accumulator Extension (EXT)		
Addr	Contents of the address portion of a two-word instruction	V	Value
		XR1	Contents of Index Register 1
CSL	Core Storage location	XR2	Contents of Index Register 2
DISP	Contents of the displacement portion of a one-word instruction	XR3	Contents of Index Register 3
		X	Hexadecimal value can be 0–F
		*	Hexadecimal values that have limits
EA	Effective address		
EA+1	Next higher address from EA		

Instruction Set

Hexadecimal	Arithmetic Instructions
	Add (A) 10000
80XX	Add contents of CSL at EA (I+DISP) to A
81XX	Add contents of CSL at EA (XR1+DISP) to A
82XX	Add contents of CSL at EA (XR2+DISP) to A
83XX	Add contents of CSL at EA (XR3+DISP) to A
8400XXXX	Add contents of CSL at EA (Addr) to A
8500XXXX	Add contents of CSL at EA (Addr +XR1) to A
8600XXXX	Add contents of CSL at EA (Addr +XR2) to A
8700XXXX	Add contents of CSL at EA (Addr +XR3) to A
8480XXXX	Add contents of CSL at EA (V in CSL at Addr) to A
8580XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") to A
8680XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") to A
8780XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") to A
	Add Double (AD) 10001
88XX	Add contents of CSL at EA (I+DISP) and EA+1 to A and Q
89XX	Add contents of CSL at EA (XR1+DISP) and EA+1 to A and Q
8AXX	Add contents of CSL at EA (XR2+DISP) and EA+1 to A and Q
8BXX	Add contents of CSL at EA (XR3+DISP) and EA+1 to A and Q
8C00XXXX	Add contents of CSL at EA (Addr) and EA+1 to A and Q
8D00XXXX	Add contents of CSL at EA (Addr+XR1) and EA+1 to A and Q
8E00XXXX	Add contents of CSL at EA (Addr+XR2) and EA+1 to A and Q
8F00XXXX	Add contents of CSL at EA (Addr+XR3) and EA+1 to A and Q
8C80XXXX	Add contents of CSL at EA (V in CSL at Addr) and EA+1 to A and Q
8D80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 to A and Q
8E80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 to A and Q
8F80XXXX	Add contents of CSL at EA(V in CSL at "Addr+XR3")and EA+1 to A and Q
	Subtract (S) 10010
90XX	Subtract contents of CSL at EA (I+DISP) from A
91XX	Subtract contents of CSL at EA (XR1+DISP) from A
92XX	Subtract contents of CSL at EA (XR2+DISP) from A
93XX	Subtract contents of CSL at EA (XR3+DISP) from A
9400XXXX	Subtract contents of CSL at EA (Addr) from A
9500XXXX	Subtract contents of CSL at EA (Addr+XR1) from A
9600XXXX	Subtract contents of CSL at EA (Addr+XR2) from A
9700XXXX	Subtract contents of CSL at EA (Addr+XR3) from A
9480XXXX	Subtract contents of CSL at EA (V in CSL at Addr) from A
9580XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") from A
9680XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") from A
9780XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") from A
	Subtract Double (SD) 10011
98XX	Subtract contents of CSL at EA (I+DISP) and EA+1 from A and Q
99XX	Subtract contents of CSL at EA (XR1+DISP) and EA+1 from A and Q
9AXX	Subtract contents of CSL at EA (XR2+DISP) and EA+1 from A and Q
9BXX	Subtract contents of CSL at EA (XR3+DISP) and EA+1 from A and Q
9C00XXXX	Subtract contents of CSL at EA (Addr) and EA+1 from A and Q
9D00XXXX	Subtract contents of CSL at EA (Addr+XR1) and EA+1 from A and Q
9E00XXXX	Subtract contents of CSL at EA (Addr+XR2) and EA+1 from A and Q
9F00XXXX	Subtract contents of CSL at EA (Addr+XR3) and EA+1 from A and Q
9C80XXXX	Subtract contents of CSL at EA (V in CSL at Addr) and EA+1 from A and Q
9D80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 from A and Q
9E80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 from A and Q
9F80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 from A and Q
	Multiply (M) 10100
A0XX	Multiply contents of CSL at EA (I+DISP) by A
A1XX	Multiply contents of CSL at EA (XR1+DISP) by A

Instruction Set

Hexadecimal	Arithmetic Instructions
A2XX	Multiply contents of CSL at EA (XR2+DISP) by A
A3XX	Multiply contents of CSL at EA (XR3+DISP) by A
A400XXXX	Multiply contents of CSL at EA (Addr) by A
A500XXXX	Multiply contents of CSL at EA (Addr+XR1) by A
A600XXXX	Multiply contents of CSL at EA (Addr+XR2) by A
A700XXXX	Multiply contents of CSL at EA (Addr+XR3) by A
A480XXXX	Multiply contents of CSL at EA (V in CSL at Addr) by A
A580XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A
A680XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A
A780XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
	Divide (D) 10101
A8XX	Divide A and Q by contents of CSL at EA (I+DISP)
A9XX	Divide A and Q by contents of CSL at EA (XR1+DISP)
AAXX	Divide A and Q by contents of CSL at EA (XR2+DISP)
ABXX	Divide A and Q by contents of CSL at EA (XR3+DISP)
AC00XXXX	Divide A and Q by contents of CSL at EA (Addr)
AD00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR1)
AE00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR2)
AF00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR3)
AC80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at Addr)
AD80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1")
AE80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2")
AF80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3")
	Logical And (AND) 11100
E0XX	AND contents of CSL at EA (I+DISP) with A
E1XX	AND contents of CSL at EA (XR1+DISP) with A
E2XX	AND contents of CSL at EA (XR2+DISP) with A
E3XX	AND contents of CSL at EA (XR3+DISP) with A
E400XXXX	AND contents of CSL at EA (Addr) with A
E500XXXX	AND contents of CSL at EA (Addr+XR1) with A
E600XXXX	AND contents of CSL at EA (Addr+XR2) with A
E700XXXX	AND contents of CSL at EA (Addr+XR3) with A
E480XXXX	AND contents of CSL at EA (V in CSL at Addr) with A
E580XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A
E680XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR2") with A
E780XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Or (OR) 11101
E8XX	OR contents of CSL at EA (I+DISP) with A
E9XX	OR contents of CSL at EA (XR1+DISP) with A
EAXX	OR contents of CSL at EA (XR2+DISP) with A
EBXX	OR contents of CSL at EA (XR3+DISP) with A
EC00XXXX	OR contents of CSL at EA (Addr) with A
ED00XXXX	OR contents of CSL at EA (Addr+XR1) with A
EE00XXXX	OR contents of CSL at EA (Addr+XR2) with A
EF00XXXX	OR contents of CSL at EA (Addr+XR3) with A
EC80XXXX	OR contents of CSL at EA (V in CSL at Addr) with A
ED80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR1") with A
EE80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR2") with A
EF80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Exclusive Or (EOR) 11110
F0XX	EOR contents of CSL at EA (I+DISP) with A
F1XX	EOR contents of CSL at EA (XR1+DISP) with A
F2XX	EOR contents of CSL at EA (XR2+DISP) with A
F3XX	EOR contents of CSL at EA (XR3+DISP) with A
F400XXXX	EOR contents of CSL at EA (Addr) with A
F500XXXX	EOR contents of CSL at EA (Addr+XR1) with A
F600XXXX	EOR contents of CSL at EA (Addr+XR2) with A
F700XXXX	EOR contents of CSL at EA (Addr+XR3) with A
F480XXXX	EOR contents of CSL at EA (V in CSL at Addr) with A
F580XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A
F680XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A
F780XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A

Instruction Set

Hexadecimal	Shift Instructions
	Shift Left Accumulator (SLA) 00010
10*X	Contents of A shift left the number of shift counts in DISP
1100	Contents of A shift left the number of shift counts in XR1
1200	Contents of A shift left the number of shift counts in XR2
1300	Contents of A shift left the number of shift counts in XR3
	Shift Left Accumulator and Extension (SLT) 00010
10*X	Contents of A and Q shift left the number of shift counts in DISP
1180	Contents of A and Q shift left the number of shift counts in XR1
1280	Contents of A and Q shift left the number of shift counts in XR2
1380	Contents of A and Q shift left the number of shift counts in XR3
	Shift Left and Count Accumulator (SLCA) 00010
10*X	Contents of A shift left the number of shift counts in DISP
1140	Contents of A shift left the number of shift counts in XR1
1240	Contents of A shift left the number of shift counts in XR2
1380	Contents of A shift left the number of shift counts in XR3
	Shift Left and Count Accumulator and Extension (SLC) 00010
10*X	Contents of A and Q shift left the number of shift counts in DISP
11C0	Contents of A and Q shift left the number of shift counts in XR1
12C0	Contents of A and Q shift left the number of shift counts in XR2
13C0	Contents of A and Q shift left the number of shift counts in XR3
	Shift Right Accumulator (SRA) 00011
18*X	Contents of A shift right the number of shift counts in DISP
1900	Contents of A shift right the number of shift counts in XR1
1A00	Contents of A shift right the number of shift counts in XR2
1B00	Contents of A shift right the number of shift counts in XR3
	Shift Right Accumulator and Extension (SRT) 00011
18*X	Contents of A and Q shift right the number of shift counts in DISP
1980	Contents of A and Q shift right the number of shift counts in XR1
1A80	Contents of A and Q shift right the number os shift counts in XR2
1B80	Contents of A and Q shift right the number of shift counts in XR3
	Rotate Right Accumulator and Extension (RTE) 00011
18*X	Contents of A and Q rotate right the number of counts in DISP
19C0	Contents of A and Q rotate right the number of counts in XR1
1AC0	Contents of A and Q rotate right the number of counts in XR2
1BC0	Contents of A and Q rotate right the number of counts in XR3

Instruction Set

Hexadecimal	I/O Instructions
	Execute I/O (XIO) 00001
08XX	Execute IOCC in CSL at EA (I+DISP) and EA+1
09XX	Execute IOCC in CSL at EA (XR1+DISP) and EA+1
0AXX	Execute IOCC in CSL at EA (XR2+DISP) and EA+1
0BXX	Execute IOCC in CSL at EA (XR3+DISP) and EA+1
0C00XXXX	Execute IOCC in CSL at EA (Addr) and EA+1
0D00XXXX	Execute IOCC in CSL at EA (Addr+XR1) and EA+1
0E00XXXX	Execute IOCC in CSL at EA (Addr+XR2) and EA+1
0F00XXXX	Execute IOCC in CSL at EA (Addr+XR3) and EA+1
0C80XXXX	Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1
0D80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1
0E80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1
0F80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1

Instruction Set

Hexadecimal	Branch Instructions
	Branch Or Skip On Condition (BSC or BOSC) 01001
48*X	Skip the next one-word instruction if ANY condition is sensed
4C*XXXXX	Branch to CSL at EA (Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (Addr+XR1) on NO condition
4E*XXXXX	Branch to CSL at EA (Addr+XR2) on NO condition
4F*XXXXX	Branch to CSL at EA (Addr+XR3) on NO condition
4C*XXXXX	Branch to CSL at EA (V in CSL at Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition
4E*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition
4F*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition
	Branch And Store Instruction Register (BSI) 01000
40XX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1
41XX	Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1
42XX	Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1
43XX	Store next sequential address in CSL at EA (XR3+DiSP) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1
47*XXXXX	If NO condition is true, store nextsequential address in CSL at EA (Addr+XR3) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and Branch to EA+1
	Modify Index and Skip (MDX) 01110
70XX	Add expanded DISP to I (no skip can occur)
71XX	Add expanded DISP to XR1
72XX	Add expanded DISP to XR2
73XX	Add expanded DISP to XR3
74XXXXXX	Add expanded positive DISP to CSL at Addr (Add to memory)
7500XXXX	Add Addr to XR1
7600XXXX	Add Addr to XR2
7700XXXX	Add Addr to XR3
74XXXXXX	Add expanded negative DISP to CSL at Addr (Add to Memory)
7580XXXX	Add V in CSL at Addr to XR1
7680XXXX	Add V in CSL at Addr to XR2
7780XXXX	Add V in CSL at Addr to XR3
	Wait (WAIT) 00110
3000	WAIT until manual start or until completion of an interrupt subroutine

STR 4 of 8 Line Transmission Code

Graphic	4 of 8 Code N X O R 8 4 2 1	Hex	Graphic	4 of 8 Code N X O R 8 4 2 1	Hex
blank	1 1 1 1 0 0 0 0 ①	F0	F	0 1 1 0 0 1 1 0	66
¢	0 1 1 0 1 0 1 0	6A	G	1 0 0 0 0 1 1 1	87
.	1 0 0 0 1 0 1 1	8B	H	0 1 1 1 1 0 0 0	78
<	0 1 1 0 1 1 0 0	6C	I	0 1 1 0 1 0 0 1	69
(	0 1 0 1 0 1 1 0	56	J	1 1 0 1 0 0 0 1	D1
+	0 0 1 1 0 1 1 0	36	K	1 1 0 1 0 0 1 0	D2
¦ ②	1 0 0 0 1 1 0 1	8D	L	1 1 0 0 0 0 1 1	C3
&	1 0 0 0 1 1 1 0	8E	M	1 1 0 1 0 1 0 0	D4
!	1 1 0 0 1 0 1 0	CA	N	1 1 0 0 0 1 0 1	C5
$	0 1 0 0 1 0 1 1	4B	O	1 1 0 0 0 1 1 0	C6
*	1 1 0 0 1 1 0 0	CC	P	0 1 0 0 0 1 1 1	47
)	0 1 0 1 1 1 0 0	5C	Q	1 1 0 1 1 0 0 0	D8
;	0 0 1 1 1 1 0 0	3C	R	1 1 0 0 1 0 0 1	C9
¬	0 1 0 0 1 1 0 1	4D	none ③	1 0 1 0 1 0 1 0	AA
-	0 1 0 0 1 1 1 0	4E	S	1 0 1 1 0 0 1 0	B2
/	1 0 1 1 0 0 0 1	B1	T	1 0 1 0 0 0 1 1	A3
,	0 0 1 0 1 0 1 1	2B	U	1 0 1 1 0 1 0 0	B4
%	1 0 1 0 1 1 0 0	AC	V	1 0 1 0 0 1 0 1	A5
—	0 1 0 1 1 0 1 0	5A	W	1 0 1 0 0 1 1 0	A6
>	0 0 1 1 1 0 1 0	3A	X	0 0 1 0 0 1 1 1	27
?	0 0 1 0 1 1 0 1	2D	Y	1 0 1 1 1 0 0 0	B8
:	0 0 1 0 1 1 1 0 ①	2E	Z	1 0 1 0 1 0 0 1	A9
#	0 0 0 1 1 0 1 1	1B	0	1 0 0 1 1 0 1 0	9A
@	1 0 0 1 1 1 0 0	9C	1	1 1 1 0 0 0 0 1	E1
'	0 0 0 0 1 1 1 1	0F	2	1 1 1 0 0 0 1 0	E2
=	0 0 0 1 1 1 1 0	1E	3	1 0 0 1 0 0 1 1	93
"	0 0 0 1 1 1 0 1	1D	4	1 1 1 0 0 1 0 0	E4
A	0 1 1 1 0 0 0 1	71	5	1 0 0 1 0 1 0 1	95
B	0 1 1 1 0 0 1 0	72	6	1 0 0 1 0 1 1 0	96
C	0 1 1 0 0 0 1 1	63	7	0 0 0 1 0 1 1 1	17
D	0 1 1 1 0 1 0 0	74	8	1 1 1 0 1 0 0 0	E8
E	0 1 1 0 0 1 0 1	65	9	1 0 0 1 1 0 0 1	99

①This is correct for System/360 Programs, but is not consistent with certain other STR devices. See the specific device manual.

②Group Mark

③Record Mark

1627 Pen Movement Code

Code	Pen Movement	Code	Pen Movement
000001	Raise Pen	010010	+X +Y
000010	+Y	010100	+X -Y
000100	-Y	001100	-X -Y
001000	-X	001010	-X +Y
010000	+X	100000	Lower Pen

Character Codes

Ref. No. ①	EBCDIC Binary	EBCDIC Hex	IBM Card Code Rows	IBM Card Code Hex ④	Graphics and Control Names	Console Printer Hex	PTTC/8 Hex ②	1132 Hex ③	1403 Hex
0	00000000	00	12,0,9,8,1	B030	NUL				
1	0001	01	12,9,1	9010	SOH				
2	0010	02	12,9,2	8810	STX				
3	0011	03	12,9,3	8410	ETX				
4	0100	04	12,9,4	8210	PF Punch Off				
5*	0101	05	12,9,5	8110	HT Horiz Tab	41 ⑤	6D(U/L)		
6*	0110	06	12,9,6	8090	LC Lower Case		6E(U/L)		
7*	0111	07	12,9,7	8050	DEL Delete		7F(U/L)		
8	1000	08	12,9,8	8030					
9	1001	09	12,9,8,1	9030					
10	1010	0A	12,9,8,2	8830	SMM				
11	1011	0B	12,9,8,3	8430	VT				
12	1100	0C	12,9,8,4	8230	FF				
13	1101	0D	12,9,8,5	8130	CR				
14	1110	0E	12,9,8,6	8080	SO				
15	1111	0F	12,9,8,7	8070	SI				
16	00010000	10	12,11,9,8,1	D030	DLE				
17	0001	11	11,9,1	5010	DC1				
18	0010	12	11,9,2	4810	DC2				
19	0011	13	11,9,3	4410	DC3				
20*	0100	14	11,9,4	4210	RES Restore	05 ⑥	4C(U/L)		
21*	0101	15	11,9,5	4110	NL New Line	81 ⑦	DD(U/L)		
22*	0110	16	11,9,6	4090	BS Backspace	11	5E(U/L)		
23	0111	17	11,9,7	4050	IDL Idle				
24	1000	18	11,9,8	4030	CAN				
25	1001	19	11,9,8,1	5030	EM				
26	1010	1A	11,9,8,2	4830	CC				
27	1011	1B	11,9,8,3	4430	CU1				
28	1100	1C	11,9,8,4	4230	FLS				
29	1101	1D	11,9,8,5	4130	GS				
30	1110	1E	11,9,8,6	4080	RDS				
31	1111	1F	11,9,8,7	4070	US				
32	00100000	20	11,0,9,8,1	7030	DS				
33	0001	21	0,9,1	3010	SOS				
34	0010	22	0,9,2	2810	FS				
35	0011	23	0,9,3	2410					
36	0100	24	0,9,4	2210	BYP Bypass				
37*	0101	25	0,9,5	2110	LF Line Feed	03	3D(U/L)		
38*	0110	26	0,9,6	2090	EOB End of Block		3E(U/L)		
39	0111	27	0,9,7	2050	PRE Prefix				
40	1000	28	0,9,8	2030					
41	1001	29	0,9,8,1	3030					
42	1010	2A	0,9,8,2	2830	SM				
43	1011	2B	0,9,8,3	2430	CU2				
44	1100	2C	0,9,8,4	2230					
45	1101	2D	0,9,8,5	2130	ENQ				
46	1110	2E	0,9,8,6	2080	ACK				
47	1111	2F	0,9,8,7	2070	BEL				
48	00110000	30	12,11,0,9,8,1	F030					
49	0001	31	9,1	1010					
50	0010	32	9,2	0810	SYN				
51	0011	33	9,3	0410					
52	0100	34	9,4	0210	PN Punch On				
53*	0101	35	9,5	0110	RS Reader Stop	09 ⑧	0D(U/L)		
54*	0110	36	9,6	0090	UC Upper Case		0E(U/L)		
55	0111	37	9,7	0050	EOT End of Trans				
56	1000	38	9,8	0030					
57	1001	39	9,8,1	1030					
58	1010	3A	9,8,2	0830					
59	1011	3B	9,8,3	0430	CU3				
60	1100	3C	9,8,4	0230	DCA				
61	1101	3D	9,8,5	0130	NAK				
62	1110	3E	9,8,6	0080					
63	1111	3F	9,8,7	0070	SUB				

① Codes identified by * are recognized by all Monitor System conversion subroutines. Codes that are not asterisked are recognized only by the SPEED subroutine.

② U = Upper Case, L = Lower Case; ③ EBCDIC subset

④ Hexadecimal codes identified by ④ can also be entered from the console keyboard.

Console Printer Codes: ⑤ Tabulate, ⑥ Shift to Black, ⑦ Carrier Return

⑧ Shift to Red

Character Codes

Ref. No. ①	EBCDIC Binary	EBCDIC Hex	IBM Card Code Rows	IBM Card Code Hex ④	Graphics and Control Names	Console Printer Hex	PTTC/8 Hex ②	1132 Hex ③	1403 Hex
64*	01000000	40	No Punches	0000④	blank (space)	21	10(U/L)	≠	7F
65	0001	41	12,0,9,1	B010					
66	0010	42	12,0,9,2	A810					
67	0011	43	12,0,9,3	A410					
68	0100	44	12,0,9,4	A210					
69	0101	45	12,0.9,5	A110					
70	0110	46	12,0,9,6	A090					
71	0111	47	12,0,9,7	A050					
72	1000	48	12,0,9,8	A030					
73	1001	49	12,8,1	9020					
74*	1010	4A	12,8,2	8820④	¢	02	20(U)		
75*	1011	4B	12,8,3	8420④	. (period)	00	6B(L)	4B	6E
76*	1100	4C	12,8,4	8220④	<	DE	02(U)		
77*	1101	4D	12,8,5	8120④	(	FE	19(U)	4D	57
78*	1110	4E	12,8,6	80A0④	+	DA	70(U)	4E	6D
79*	1111	4F	12,8,7	8060④	¦(logical OR)	C6	3B(U)		
80*	01010000	50	12	8000④	&	44	70(L)	50	15
81	0001	51	12,11,9,1	D010					
82	0010	52	12,11,9,2	C810					
83	0011	53	12,11,9,3	C410					
84	0100	54	12,11,9,4	C210					
85	0101	55	12,11,9,5	C110					
86	0110	56	12,11,9,6	C090					
87	0111	57	12,11,9,7	C050					
88	1000	58	12,11,9,8	C030					
89	1001	59	11,8,1	5020					
90*	1010	5A	11,8,2	4820④	!	42	5B(U)		
91*	1011	5B	11,8,3	4420④	$	40	5B(L)	5B	62
92*	1100	5C	11,8,4	4220④	*	D6	08(U)	5C	23
93*	1101	5D	11,8,5	4120④	)	F6	1A(U)	5D	2F
94*	1110	5E	11,8,6	40A0④	;	D2	13(U)		
95*	1111	5F	11,8,7	4060④	¬(logical NOT)	F2	6B(U)		
96*	01100000	60	11	4000④	- (dash)	84	40(L)	60	61
97*	0001	61	0,1	3000④	/	BC	31(L)	61	4C
98	0010	62	11,0,9,2	6810					
99	0011	63	11,0,9,3	6410					
100	0100	64	11,0,9,4	6210					
101	0101	65	11,0,9,5	6110					
102	0110	66	11,0,9,6	6090					
103	0111	67	11,0,9,7	6050					
104	1000	68	11,0,9,8	6030					
105	1001	69	0,8,1	3020					
106	1010	6A	12,11	C000					
107*	1011	6B	0,8,3	2420④	, (comma)	80	3B(L)	6B	16
108*	1100	6C	0,8,4	2220④	%	06	15(U)		
109*	1101	6D	0,8,5	2120④	_ (underscore)	BE	40(U)		
110*	1110	6E	0,8,6	20A0④	>	46	07(U)		
111*	1111	6F	0,8,7	2060④	?	86	31(U)		
112	01110000	70	12,11,0	E000					
113	0001	71	12,11,0,9,1	F010					
114	0010	72	12,11,0,9,2	E810					
115	0011	73	12,11,0,9,3	E410					
116	0100	74	12,11,0,9,4	E210					
117	0101	75	12,11,0,9,5	E110					
118	0110	76	12,11,0,9,6	E090					
119	0111	77	12,11,0,9,7	E050					
120	1000	78	12,11,0,9,8	E030					
121	1001	79	8,1	1020					
122*	1010	7A	8,2	0820④	:	82	04(U)		
123*	1011	7B	8,3	0420④	#	C0	0B(L)		
124*	1100	7C	8,4	0220④	@	04	20(L)		
125*	1101	7D	8,5	0120④	' (apostrophe)	E6	16(U)	7D	0B
126*	1110	7E	8,6	00A0④	=	C2	01(U)	7E	4A
127*	1111	7F	8,7	0060④	"	E2	0B(U)		

‡ Any code other than those defined for the 1132 will be interpreted by the PRNT 1 subroutine as a blank.

STR Control Characters

Control Characters	4 of 8 Code N	X	O	R	8	4	2	1	Hex
Idle	0	0	1	1	1	0	0	1	39
Start of Record 1 or Acknowledge 1 (SOR 1 or ACK 1)	0	1	0	1	0	0	1	1	53
Start of Record 2 or Acknowledge 2 (SOR 2 or ACK 2)	0	0	1	1	0	0	1	1	33
Transmit Leader (TL)	0	0	1	1	0	1	0	1	35
Control Leader (CL)	0	1	0	1	0	1	0	1	55
End of Transmission (EOT)*	0	1	0	1	1	0	1	0	5A
Inquiry or Error (INQ or ERR)	0	1	0	1	1	0	0	1	59
Telephone*	0	1	0	1	1	1	0	0	5C
Group Mark	1	0	0	0	1	1	0	1	8D
Longitudinal Redundancy Check (LRC)**	-	-	-	-	-	-	-	-	--

* Also used as a data character

** This character has a 0 bit in each bit position that contained an even number of 1 bits for that bit position in the data record. If that bit position in the record had an odd number of 1 bits the LRC character ranges from all 0s to all 1s and thus, is not in the 4 of 8 code.

BSC Control Characters

Character	Bit Configuration 0 1 2 3 4 5 6 7	Hex	Meaning
SYN	0 0 1 1 0 0 1 0	32	Synchronous Idle
DLE	0 0 0 1 0 0 0 0	10	Data Link Escape
ENQ	0 0 1 0 1 1 0 1	2D	Enquiry
SOH	0 0 0 0 0 0 0 1	01	Start of Heading
STX	0 0 0 0 0 0 1 0	02	Start of Text
ETB	0 0 1 0 0 1 1 0	26	End of Transmission Block
ETX	0 0 0 0 0 0 1 1	03	End of Text
EOT	0 0 1 1 0 1 1 1	37	End of Transmission
NAK	0 0 1 1 1 1 0 1	3D	Negative Acknowledgement
*ACK 0	0 1 1 1 0 0 0 0	70	Positive Acknowledgement (even record)
*ACK 1	0 1 1 0 0 0 0 1	61	Positive Acknowledgement (odd record)

* Control characters when preceded by DLE

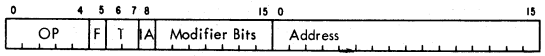
Character Codes

Ref. No. ①	EBCDIC Binary	Hex	IBM Card Code Rows	Hex ④	Graphics and Control Names	Console Printer Hex	PTTC/8 Hex ②	1132 Hex ③	1403 Hex
128	10000000	80	12,0,8,1	B020					
129	0001	81	12,0,1	B000	a				
130	0010	82	12,0,2	A800	b				
131	0011	83	12,0,3	A400	c				
132	0100	84	12,0,4	A200	d				
133	0101	85	12,0,5	A100	e				
134	0110	86	12,0,6	A080	f				
135	0111	87	12,0,7	A040	g				
136	1000	88	12,0,8	A020	h				
137	1001	89	12,0,9	A010	i				
138	1010	8A	12,0,8,2	A820					
139	1011	8B	12,0,8,3	A420	[				
140	1100	8C	12,0,8,4	A220					
141	1101	8D	12,0,8,5	A120					
142	1110	8E	12,0,8,6	A0A0					
143	1111	8F	12,0,8,7	A060					
144	10010000	90	12,11,8,1	D020					
145	0001	91	12,11,1	D000	j				
146	0010	92	12,11,2	C800	k				
147	0011	93	12,11,3	C400	l				
148	0100	94	12,11,4	C200	m				
149	0101	95	12,11,5	C100	n				
150	0110	96	12,11,6	C080	o				
151	0111	97	12,11,7	C040	p				
152	1000	98	12,11,8	C020	q				
153	1001	99	12,11,9	C010	r				
154	1010	9A	12,11,8,2	C820					
155	1011	9B	12,11,8,3	C420	]				
156	1100	9C	12,11,8,4	C220					
157	1101	9D	12,11,8,5	C120					
158	1110	9E	12,11,8,6	C0A0					
159	1111	9F	12,11,8,7	C060					
160	10100000	A0	11,0,8,1	7020					
161	0001	A1	11,0,1	7000					
162	0010	A2	11,0,2	6800	s				
163	0011	A3	11,0,3	6400	t				
164	0100	A4	11,0,4	6200	u				
165	0101	A5	11,0,5	6100	v				
166	0110	A6	11,0,6	6080	w				
167	0111	A7	11,0,7	6040	x				
168	1000	A8	11,0,8	6020	y				
169	1001	A9	11,0,9	6010	z				
170	1010	AA	11,0,8,2	6820					
171	1011	AB	11,0,8,3	6420					
172	1100	AC	11,0,8,4	6220					
173	1101	AD	11,0,8,5	6120	]				
174	1110	AE	11,0,8,6	60A0					
175	1111	AF	11,0,8,7	6060					
176	10110000	B0	12,11,0,8,1	F020					
177	0001	B1	12,11,0,1	F000					
178	0010	B2	12,11,0,2	E800					
179	0011	B3	12,11,0,3	E400					
180	0100	B4	12,11,0,4	E200					
181	0101	B5	12,11,0,5	E100					
182	0110	B6	12,11,0,6	E080					
183	0111	B7	12,11,0,7	E040					
184	1000	B8	12,11,0,8	E020					
185	1001	B9	12,11,0,9	E010					
186	1010	BA	12,11,0,8,2	E820					
187	1011	BB	12,11,0,8,3	E420					
188	1100	BC	12,11,0,8,4	E220					
189	1101	BD	12,11,0,8,5	E120	]				
190	1110	BE	12,11,0,8,6	E0A0					
191	1111	BF	12,11,0,8,7	E060					

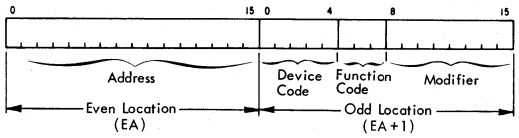
Character Codes

Ref. No. ①	EBCDIC Binary	Hex	IBM Card Code Rows	Hex ④	Graphics and Control Names	Console Printer Hex	PTTC/8 Hex ②	1132 Hex ③	1403 Hex
192	11000000	C0	12,0	A000	(+ zero)				
193*	0001	C1	12,1	9000 ④	A	3C/3E	61(U)	C1	64
194*	0010	C2	12,2	8800 ④	B	18/1A	62(U)	C2	25
195*	0011	C3	12,3	8400 ④	C	1C/1E	73(U)	C3	26
196*	0100	C4	12,4	8200 ④	D	30/32	64(U)	C4	67
197*	0101	C5	12,5	8100 ④	E	34/36	75(U)	C5	68
198*	0110	C6	12,6	8080 ④	F	10/12	76(U)	C6	29
199*	0111	C7	12,7	8040 ④	G	14/16	67(U)	C7	2A
200*	1000	C8	12,8	8020 ④	H	24/26	68(U)	C8	6B
201*	1001	C9	12,9	8010 ④	I	20/22	79(U)	C9	2C
202	1010	CA	12,0,9,8,2	A830					
203	1011	CB	12,0,9,8,3	A430					
204	1100	CC	12,0,9,8,4	A230					
205	1101	CD	12,0,9,8,5	A130					
206	1110	CE	12,0,9,8,6	A0B0					
207	1111	CF	12,0,9,8,7	A070					
208	11010000	D0	11,0	6000	(- zero)				
209*	0001	D1	11,1	5000 ④	J	7C/7E	51(U)	D1	58
210*	0010	D2	11,2	4800 ④	K	58/5A	52(U)	D2	19
211*	0011	D3	11,3	4400 ④	L	5C/5E	43(U)	D3	1A
212*	0100	D4	11,4	4200 ④	M	70/72	54(U)	D4	5B
213*	0101	D5	11,5	4100 ④	N	74/76	45(U)	D5	1C
214*	0110	D6	11,6	4080 ④	O	50/52	46(U)	D6	5D
215*	0111	D7	11,7	4040 ④	P	54/56	57(U)	D7	5E
216*	1000	D8	11,8	4020 ④	Q	64/66	58(U)	D8	1F
217*	1001	D9	11,9	4010 ④	R	60/62	49(U)	D9	20
218	1010	DA	12,11,9,8,2	C830					
219	1011	DB	12,11,9,8,3	C430					
220	1100	DC	12,11,9,8,4	C230					
221	1101	DD	12,11,9,8,5	C130					
222	1110	DE	12,11,9,8,6	C0B0					
223	1111	DF	12,11,9,8,7	C070					
224	11100000	E0	0,8,2	2820					
225	0001	E1	11,0,9,1	7010					
226*	0010	E2	0,2	2800 ④	S	98/9A	32(U)	E2	0D
227*	0011	E3	0,3	2400 ④	T	9C/9E	23(U)	E3	0E
228*	0100	E4	0,4	2200 ④	U	B0/B2	34(U)	E4	4F
229*	0101	E5	0,5	2100 ④	V	B4/B6	25(U)	E5	10
230*	0110	E6	0,6	2080 ④	W	90/92	26(U)	E6	51
231*	0111	E7	0,7	2040 ④	X	94/96	37(U)	E7	52
232*	1000	E8	0,8	2020 ④	Y	A4/A6	38(U)	E8	13
233*	1001	E9	0,9	2010 ④	Z	A0/A2	29(U)	E9	54
234	1010	EA	11,0,9,8,2	6830					
235	1011	EB	11,0,9,8,3	6430					
236	1100	EC	11,0,9,8,4	6230					
237	1101	ED	11,0,9,8,5	6130					
238	1110	EE	11,0,9,8,6	60B0					
239	1111	EF	11,0,9,8,7	6070					
240*	11110000	F0	0	2000 ④	0	C4	1A(L)	F0	49
241*	0001	F1	1	1000 ④	1	FC	01(L)	F1	40
242*	0010	F2	2	0800 ④	2	D8	02(L)	F2	01
243*	0011	F3	3	0400 ④	3	DC	13(L)	F3	02
244*	0100	F4	4	0200 ④	4	F0	04(L)	F4	43
245*	0101	F5	5	0100 ④	5	F4	15(L)	F5	04
246*	0110	F6	6	0080 ④	6	D0	16(L)	F6	45
247*	0111	F7	7	0040 ④	7	D4	07(L)	F7	46
248*	1000	F8	8	0020 ④	8	E4	08(L)	F8	07
249*	1001	F9	9	0010 ④	9	E0	19(L)	F9	08
250	1010	FA	12,11,0,9,8,2	E830					
251	1011	FB	12,11,0,9,8,3	E430					
252	1100	FC	12,11,0,9,8,4	E230					
253	1101	FD	12,11,0,9,8,5	E130					
254	1110	FE	12,11,0,9,8,6	E0B0					
255	1111	FF	12,11,0,9,8,7	E070					

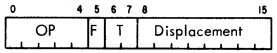
Long Instruction Format



Input/Output Control Command



Short Instruction Format



Cycle Steal Priority

Cycle-Steal Priority		
Priority	Cycle Steal Level	Device
1	0	Single Disk Storage
2	1	SAC (or 2250)
	Mpx 0	2310 Drive 1
	Mpx 1	2310 Drive 2
	Mpx 2	2310 Drive 3
	Mpx 3	2310 Drive 4
	Mpx 4	Reserved
	Mpx 5	Reserved
	Mpx 6	SAC II (or 2250)
	Mpx 7	1403
	Mpx 8	Reserved
	Mpx 9	Reserved
	Mpx 10	Reserved
	Mpx 11	Reserved
3	2	1132
4	3	2501

Reserved Core Storage Locations

Tag Bits	Core Storage Address(Decimal)	Description
00	--	Displacement
01	00001	Index Register 1
10	00002	Index Register 2
11	00003	Index Register 3
--	00008 - 00013	Interrupt Vectors
--	00032 - 00039	1132 Scan Field

Tag Bit Codes

Instructions	Tag Bits	Register/Operation
Load Index and Store Index	00	IAR
	01	XR 1
	10	XR 2
	11	XR 3
Shift Left and Shift Right	00	Disp
	01	XR 1
	10	XR 2
	11	XR 3
Modify Index and Skip		
F = 0	00	Disp Added to IAR
	01	Disp Added to XR 1
	10	Disp Added to XR 2
	11	Disp Added to XR 3
F = 1; IA = 0	00	Disp Added to C
	01	Add added to XR 1
	10	Add added to XR 2
	11	Add added to XR 3
F = 1; IA = 1	00	Disp added to C
	01	C added to XR 1
	10	C added to XR 2
	11	C added to XR 3

Disp = Contents of the displacement field of the instruction
Add = Contents of the address field of the Instruction
C = Contents of the location specified by the address (Add)

AND OR, EOR Operations

Core (B Reg) → Acc →	Results in Acc		
	AND	OR	EOR
0 → 0 →	0	0	0
0 → 1 →	0	1	1
1 → 0 →	0	1	1
1 → 1 →	1	1	0

BSC Condition Codes

Bit Position	Condition	
10	ACC zero	(Z)
11	ACC negative	(-)
12	ACC positive, not zero	(+)
13	ACC even	(E)
14	Carry Indicator OFF	(C)
15	Overflow Indicator OFF	(O)

Short Instruction
Skip if any one condition is true.
No-Op if all bits are zero.

Long Instruction
Branch if none of the conditions are true.
Unconditional branch if all bits are zero.

Decimal/Hexadecimal Conversion

16-Bit Word							
Bits 0,1,2, and 3		Bits 4,5,6, and 7		Bits 8,9,10, and 11		Bits 12,13,14, and 15	
Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal
0	0	0	0	0	0	0	0
1	4,096	1	256	1	16	1	1
2	8,192	2	512	2	32	2	2
3	12,288	3	768	3	48	3	3
4	16,384	4	1,024	4	64	4	4
5	20,480	5	1,280	5	80	5	5
6	24,576	6	1,536	6	96	6	6
7	28,672	7	1,792	7	112	7	7
8	32,768	8	2,048	8	128	8	8
9	36,864	9	2,304	9	144	9	9
A	40,960	A	2,560	A	160	A	10
B	45,056	B	2,816	B	176	B	11
C	49,152	C	3,072	C	192	C	12
D	53,248	D	3,328	D	208	D	13
E	57,344	E	3,584	E	224	E	14
F	61,440	F	3,840	F	240	F	15

To find the decimal equivalent of a hexadecimal number, locate the hexadecimal number and its decimal equivalent for each hexadecimal position (four bits). Add the four decimal equivalents to obtain the decimal number. For example, the decimal equivalent of hexadecimal number FCCE is 64,718 (61,440 + 3,072 + 192 + 14).

To find the hexadecimal equivalent of a decimal number, locate the next lower decimal number in the chart. The corresponding hexadecimal digit is the first significant hexadecimal digit (any higher order hexadecimal digits are zero). Subtract the first decimal number used (in the chart) from the original decimal number. Use the difference obtained to determine the next hexadecimal digit. Subtract the second decimal number used (in the chart) from the first difference. Use the second difference to determine the next hexadecimal digit. Repeat this procedure until the complete hexadecimal number is determined. For example, the hexadecimal equivalent of decimal number 2,914 is 0B62 (high order = 0; 2,816 = B; 96 = 6; 2 = 2).

The maximum value shown on the chart is 65,535 (hexadecimal FFFF).

Data Word Binary/Decimal Values

Bit Position	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Binary Value	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
Decimal Value	Sign	16,384	8,192	4,096	2,048	1,024	512	256	128	64	32	16	8	4	2	1

Effective Address Computation

Tag Bits	F=0 (Direct Addressing)	F=1, IA=0 (Direct Addressing)	F=1, IA=1 (Indirect Addressing)
T=00	EA=Disp+IAR	EA=Add	EA=C/Add
T=01	EA=Disp+XR1	EA=Add+XR1	EA=C/(Add+XR1)
T=10	EA=Disp+XR2	EA=Add+XR2	EA=C/(Add+XR2)
T=11	EA=Disp+XR3	EA=Add+XR3	EA=C/(Add+XR3)

Disp = Contents of Displacement field of instruction.
Add = Contents of Address field of instruction.
C = Contents of Location specified by Add or Add+XR.

Note: For BSI add 1. This table does not apply to the MDX, LDX, STX, LDS, Shift or Wait instructions.

BSC Control Sequences

Characters	Meaning
ENQ	Enquiry
SOH	Start of Heading
STX	Start of Text
DLE STX	Start of Transparent Text
ETB CRC-16 *	End of Block
DLE ETB CRC-16	End of Transparent Block
ETX CRC-16	End of Text
DLE ETX CRC-16	End of Transparent Text
DLE ACK 1	Acknowledgement of Odd Record
DLE ACK 0	Acknowledgement of Even Record
NAK	Negative Acknowledgement
EOT	End of Transmission
DLE EOT	Disconnect Signal
SYN SYN	Synchronous Idle (Normal)
DLE SYN	Synchronous Idle (Transparent Text)

* CRC-16 is a 16-bit cyclic check character accumulated from text and heading data.

STR Control Sequences

Control Sequence	Control Character Sequence	
	Leader Character	Trailer Character
End of IDLE (EOI)*	CL	1 IDLE
Inquiry (Synchronized ?)*	TL	INQ
Acknowledge (Synchronized)	CL	ACK 2
Telephone Sequence *	CL	TEL
Acknowledge Telephone *	CL	TEL
Start of Record 1 (SOR 1) 1st or odd numbered record	TL	SOR 1
Start of Record 2 (SOR 2) 2nd or even numbered record	TL	SOR 2
End of Transmittal Record (EOTR)	TL	LRC
Acknowledge Record 1	CL	ACK 1
Acknowledge Record 2	CL	ACK 2
Repeat Last Record (ERROR)	CL	ERR
Intermediate LRC**	GM	LRC
End of Transmission (EOT)*	CL	EOT
Acknowledge EOT *	CL	EOT

*These sequences are always preceded by a 1.25 second transmission of IDLE characters.
** This sequence may be required on some terminals e.g. 1013, 7701, 7702

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