HP 13220

PROCESSOR MODULE

Manual Part No. 13220-91088

REVISED

AUG-14-81

DATA TERMINAL
TECHNICAL INFORMATION
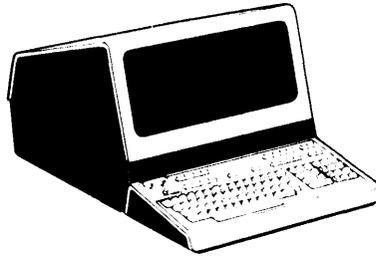
HEWLETT **hp** *PACKARD*

1.0   INTRODUCTION

The 02620-60088 Processor PCA performs the terminal logic functions for the 2623A terminal. Its operation is based on the Z80A microprocessor, National Semiconductor 8367 CRT Controller (CRTC), and a prom based microsequenced graphics controller.

The control and I/O section of the Processor PCA provides control signals, input/output and data processing functions. The memory section provides 16K bytes of dynamic RAM for character display memory, scratch pad memory, data buffers and space for up to six 4K or 8K byte ROMs of which 40K are used for complete terminal operation (4K of ROM optional with integral printer). The Graphics memory subsystem contains 16K words (16K X 16) of vector display memory. The Graphics subsystem is responsible for both write and display refresh of the graphics memory. The video control section provides timing signals for driving the sweep circuitry and video logic as well as performing direct memory access (DMA) of display data. A detailed description of the operation of each of these sections follows in section 3.0.

2.0   OPERATING PARAMETERS.

A summary of operating parameters for the Processor Module is contained in tables 1.0 through 4.0

Table 1.0   Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.1 Inches	Weight (Pounds)
02620-60088	Processor PCA	12.3 x 10.9 x 0.5	1.4

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NOTE: This document is part of the 262XX DATA TERMINAL product
        series Technical Information Package (HP 13220).

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Table 2.0 Reliability and Environmental Information

```
==================================================================================
|                                                                                |
|                                                                                |
|  Environmental:   HP Class B                                                   |
|                                                                                |
|                                                                                |
|  Restrictions:    Type tested at product level                                 |
|                                                                                |
|                                                                                |
|                                                                                |
|==============================================================================|
|                                                                                |
|            Failure Rate:   3.71    (percent per 1000 hours)                    |
|                                                                                |
==================================================================================
```

Table 3.0 Power Supply Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+16 Volt Supply	+12 Volt Supply	+5 Volt Supply	-12 Volt Supply
@ 0 mA	@ 475 mA	@ 5.0 A	@ 77 mA
NOT APPLICABLE			
115 volts ac		220 volts ac	
@ A		@ A	
NOT APPLICABLE		NOT APPLICABLE	

Table 4.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
J1		** PRINTER **
Pin -1	PRINTER	Negative True, Printer Strobe
-2	PWR ON/FAIL	Negative True, Power On/Failing
-3	WRITE	Negative True, Write signal
-4	A1	Negative True, Select bit 1
-5		N/C
-6	DATA 0	LSB - Negative True, Data
-7	DATA 1	-
-8	DATA 2	-
-9	DATA 3	-
-10	DATA 4	-
-11	DATA 5	-
-12	DATA 6	-
-13	DATA 7	MSB - Negative True, Data
-14	GND	Set printer contrast
-16	PINT	Negative True, Printer Interrupt
-17	A0	Negative True, Select bit 0
-18	+5V	Vcc Power
-19	+5V	.
-20	+5V	.
-21	+5V	.
-22	GND	Power Return
-23	GND	.
-24	GND	.
-25	GND	.
-26	GND	.

Table 4.0 Connector Information (Cont'd)

Connector and Pin No.	Signal Name	Signal Description
J2		** POWER SUPPLY **
Pin -1	+5V	+5V Power
-2		N/C
-3	+5V	+5V Power
-4	+12V	+12V Power
-5	GND	Return for Power
-6	GND	Return for Power
-7	PWR ON/FAIL	Negative True, Power On/Failing
-8	-12V	-12V Power
-9	BATTERY	Positive Battery Terminal
-10	BATRET	Negative Battery Terminal
J3		** SWEEP **
Pin -1	HLFBRT	Negative true, Half Bright Video
-2		N/C
-3	RETURN	Return for half bright twisted pair
-4	FULLBRT	Negative true, Full Bright Video
-5	RETURN	Return for Video twisted pair
-6	RETURN	Return for Drive signals
-7	VERDR	Negative True, Vertical Drive
-8	HORDR	Horizontal Drive
J4		** KEYBOARD **
Pin -1	KEY0	Key Data (LSB)
-2	KEY1	Key Data
-3	KEY2	Key Data
-4	KEY3	Key Data
-5	KEY4	Key Data
-6		N/C
-7	KEY5	Key Data
-8	KEY6	Key Data (MSB)
-9	KEYACT	Key Active (Status, key selected)
-10	GND	Power Return
-11	BELL	Bell Line
-12	+5v	+5v Power
-13	+12v	+12v Power
-14	-12v	-12v Power

Table 4.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
J5		** EXTERNAL PRINTER PORT **
Pin -1	SHIELD	Shield ground
-2	SD	Transmitted Data
-3	RD	Received Data
-4	RS	Request to Send
-5	CS	Clear to Send
-6	DM	Data Set Ready
-7	GROUND	Signal Ground
-8		N/C
-9		N/C
-10		N/C
-11		N/C
-12	OCR2	Secondary Receive Ready
-13		N/C
-14		N/C
-16		N/C
-17		N/C
-18		N/C
-19	OCD2	Secondary Request to Send
-20		N/C
-21		N/C
-22		N/C
-23		N/C
-24		N/C
-25		N/C
-26		N/C

Table 4.0 Connector Information (Cont'd)

Connector and pin No.	Signal Name	Signal Description
J6		** DATA COMM **
Pin -1		N/C
-2	+5V	+5V Pod Power
-3	+5V	+5V Pod Power
-4	GND	Power Return
-5	GND	Power Return
-6	GND	Power Return
-7	OCD1	Rate Select (23)
-8		N/C
-9	RD	Received Data (3)
-10		N/C
-11	CS	Clear To Send (5)
-12	DM	Data Set Ready (6)
-13		N/C
-14		N/C
-15	SG	Signal Ground (7)
-16		N/C
-17		N/C
-18	OCR1	Ring Indicator (22)
-19	+12V	+12V Pod Power
-20	-12V	-12V Pod Power
-21	SD	Transmitted Data (2)
-22	RS	Request To Send (4)
-23	TR	Ready (20)
-24		N/C
-25		N/C
-26		N/C
-27		N/C
-28		N/C
-29		N/C
-30		N/C
-31		N/C
-32	GND	Return
-33	SHIELD	Shield Ground (1)
-34		N/C

Notes: (n) denotes the RS-232 pin number

3.0   FUNCTIONAL DESCRIPTION

         Refer to block diagrams (figs. 1-3), schematic diagrams (figs.
         21,22,23,24), timing diagrams (figs. 4-14), component layout diagram
         (fig. 20), and parts list (fig. 25) located in the appendix. The
         following describes the operation of the five major sections of the
         Processor PCA; control and I/O, terminal character memory, character
         video control, graphics controller, and graphics display control and
         memory.

3.1   CONTROL AND I/O SECTION

3.1.1   Clock

         A 25.7715 MHz crystal is attached to the CRTC which oscillates at the
         video dot frequency. This is buffered by the CRTC and again by a
         74LS244 (U423) to become DRCX, buffered dot rate clock. This clock is
         then divided by seven by the 74S163 (U323) to produce 3.6816 MHz, which
         is shaped by Q4 and its associated circuitry to produce a symmetrical
         clock for the Z80A, which has a zero level < 0.45V and a one level >
         4.4V. This clock is also divided by two to produce a 1.8408 MHz clock
         which the datacomm chip (U424) uses to produce baud rates.

3.1.2   Z80A
         The Z80A microprocessor performs the major control and data
         manipulation functions of the processor PCA. It provides addresses and
         control signals to read and write data from and to both memory and I/O
         ports. It also responds to two externally generated interrupts, NNMI
         and NINT, which, when enabled, interrupt current execution and cause
         the Z80A to branch to its interrupt service routine. The Z80A also
         responds to a bus request signal, NBUSREQ, allowing the CRTC control of
         the system buses.

         At power up (or reset) the Z80A begins executing instructions from
         program memory beginning at address 0000H. A routine is executed which
         initializes variables and devices according to information contained in
         non-volatile memory (CMOS) and performs a self test of ROM and RAM. If
         an error is detected a series of beeps are issued to the keyboard which
         indicate the failing ROM or RAM. After inintialization the program
         enters a major loop responding to inputs from the keyboard and datacomm
         ports.

Three 74LS244's (U714,U811,U814) buffer the address and control lines
from the Z80A. The 1 of 8 decoder, U911, is used to seperate program
memory into six blocks, each 8K bytes long. The addressed ROM is
enabled during a memory read by the TNRD and TNMREQ signals or during
an instruction fetch by the NM1 signal. Since the time to read the
data in an instruction fetch is less than that for a memory read, the
NM1 signal was used to provide an early enable of the ROM allowing it
to respond within the required time. ROMs with access times of 350 ns
from address or 300 ns from enable are required to run the system at
full speed. EPROMs or ROMs with 450 ns access times from address may
be used by installing jumper W6 and removing jumper W5, which causes
the Z80A to wait one cycle longer during instruction fetches. The quad
latch U617 and associated gating provides the required wait signal to
the Z80A.

3.1.3   I/O Ports

CMOS

The Z80A is capable of addressing 256 different input/output ports.
I/O addresses from the Z80A appear on address bits A0-A7 and the
accumulator contents appear on bits A8-A15. I/O addresses 0-7FH are
used to access locations in the nonvolatile CMOS RAM, U921, where
configuration data is stored. Since the CMOS RAM is not fast enough to
respond within the I/O cycle time a wait state is generated (by U617)
each time the CMOS RAM is accessed. Diodes CR4-CR6 ensure that around
5 volts is always on the CMOS supply pin. Emmitter follower circuit,
Q5, makes sure that during a power off the CMOS is always disabled
before the Z80A buses become undefined and remains so until buses
become defined at power on. During power off the battery maintains
CMOS contents. If power on configuration is to be fixed, the COMS RAM
may be replaced by an HM7611 PROM (however it must be realized that the
standard read/complement/write test for the CMOS self test would show a
CMOS error since the prom cannot be written).

DATACOMM

The SY6551 Asynchronous Communications Interface Adapter performs the
parallel to serial conversion, error detection and baud rate generation
functions required for serial data communication. It appears to the
Z80A as four read only and four write only ports with address bit TA2
selecting the read/write function. This is done to compensate for the
unique timing of the 6500 series devices. The SY6551 is selected by
the rising edge of SELDC1 which is inverted from U512, the 1 of 8
decoder. The addresses of the SY6551 (U722) are A0-A7H.

The status inputs of the SY6551 produce undesirable results and
therefore are forced to their active low states while the necessary
status signals are routed through another port. RS-232 line driver,
U623, and receiver, U624, are used to convert from TTL levels to RS-232
levels (+-12V) and vice versa. Transmitted signals are: send data
(SD), terminal ready (TR), request to send (RS) and optional control
driver 1 (OCD1). Received signals are: receive data (RD), data mode
(DM), optional control receiver 1 (OCR1), and clear to send (CS).

The datacomm subsystem operates in an asynchronous, full-duplex, point-
to-point environment. Characters may be transmitted and received
simultaneously (full-duplex) with

character flow occurring over random time intervals (asynchronous). To
achieve hardware synchronization each character is framed by a start
bit and a stop bit (2 stop bits at 110 baud). The addition of the
framing bits for transmitted characters and the detection of framing
bits for the received characters are done by the SY6551. The parity
(for error detection) of the character is selectable (in the datacomm
configuration menu) and is also generated and detected by the SY6551
which reports errors (parity, framing, and overrun) to the Z80A by
means of a status register in the SY6551 which is read when a character
is received. The data transmission and reception rates are set by the
Z80A in an internal register within the SY6551. Rates are selectable
(in the datacomm configuration menu) from 110 to 9600 baud.

The datacomm status inputs and outputs provide the necessary control
lines to connect the terminal to a host computer via a modem, or to
provide direct hardware handshaking between the terminal and host. At
power-on the TR and RS lines are activated to indicate that the
terminal is ready. Upon receipt of a modem disconnect escape sequence
(esc f) the TR line is brought inactive for about two seconds to
disconnect the modem. The presence of a modem connection is detected
by DM which causes the indicator "LED" (an asterisk '*') to be
displayed on the bottom center of the display. The CS signal from the
host when active allows the terminal to transmit data and goes inactive
to halt transmission (the terminal may ignore CS depending on datacomm
configuration). The state of OCD1 is controlled by a configuration
strap with its default state being low (inactive). This line selects
the modem rate for dual speed modems. OCR1 is monitored in datacomm
self test to detect the presence of the loopback test hood. All modem
status lines are active high (+12V).

Upon receipt of a character from datacomm the SY6551 generates an
interrupt signal (NINT) to the Z80A. This causes the Z80A to branch to
the datacomm interrupt service routine which reads the SY6551 status,
clearing the interrupt , and if no errors are present, inputs the
character and places it into the datacomm buffer in RAM. Characters
for which errors (parity, framing or overrun) are present cause a
delete character to be placed in the buffer.

EXTERNAL PRINTER PORT

The SY6551 ACIA which is used for datacomm also performs the parallel
to serial conversion, error detection, and baud rate generation
functions required for the external printer communication. It appears
to the Z80A as four read only and four write only ports with address
bit TA2 selecting the read/write function. This is done to compensate
for the unique timing of the 6500 series devices. The SY6551 is
selected by the rising edge of SELDC2 which is inverted from U512, the
1 of 8 decoder. The addresses of the SY6551 (U721) are B0-B7H.

The status inputs of the SY6551 produce undesirable results and
therefore are forced to their active low states while the necessary
status signals are routed through another port. RS-232 line driver,
U622, and receiver, U621, are used to convert from TTL levels to RS-232
levels (+-12V) and vice versa. Transmitted signals are: send data
(SD), terminal ready (TR), request to send (RS) and optional control
driver 2 (OCD2). Received signals are: receive data (RD), data mode
(DM), optional control receiver 2 (OCR2), and clear to send (CS).

Although we use the same 6551, the terminal uses it as an output device
only. The hardware is set up much like the datacomm. The difference
is the external printer port must be poled for internal status while
the datacomm drives an interupt line to the Z80A processor telling it
status of the internal receive register has changed.

OCR2 and OCD2 are used as a secondary receive ready and a secondary
request to send on the external printer port. All other transmit and
receive signals are handled similar to that of the datacomm.

TBUS PORTS

The remaining I/O ports are buffered to the Z80A data bus by the
bidirectional bus driver, U616. This was done because of data bus
loading. The signal TNRD selects the direction of the driver which is
enabled for all I/O accesses except CMOS RAM and datacomm.

U516 forms the keystatus port located at address 80H. The keystatus
port returns the status of 8 keys at a time, which keys are determined
by the keyboard/display port (U416). Four bits of the key address
(column address) are supplied by U416 (located at address B8H) and
three more from the CRTC scan line outputs (row address). As the row
address (scan line count) from the CRTC change, keystates are clocked
into the keystatus shift register (a high bit indicating key active)
from which they are later read. The column address is incremented
(during an NMI) for each of the first sixteen display rows thereby
scanning the entire range of keyboard addresses.

The keyboard/display port also enables a counter (U224) which counts horizontal sync pulses down to a bell frequency. The bell signal is then shaped by Q2 and its associated circuit. The remaining bits of the keyboard/ display port determine whether enhancements will be enabled and latches the signal which determines the blinkrate of blinking characters.

The NNMI (non-maskable interrupt) signal to the Z80A is masked externally by a D flip-flop (half of U425). Port addresses 88H to 8FH select the NENNMI signal of the port decoder, clocking the latch while address bit TA0 is the data input. This means that a write to port 88H clears the latch, disabling NMI, while a write to port 89H sets the latch enabling NMI.

The system status port, U515 and U423, at address 90H allows the Z80A to read the vertical blank signal (VBLANK) for synchronizing the software with the hardware. It also provides the inputs for the datacomm status signals discussed above and also monitors the integral printer status.

The integral printer port at address 98H buffers data continuously to the printer bus, the data being latched in the printer when the NPRINTER signal is active. The processor writes data and commands to the printer via U315 and half of U314. Printer control is specified by performing a write operation to the printer with address lines TA0 and TA1 and data lines TD0-TD7 selecting the particular function. Printer status is read back from the printer on the upper half of U15 which is enabled for read operations from the printer port. The presence of the printer is detected by reading status from the printer and checking data bit TD1. TD1 will be low if the printer is not connected due to the pullup resistor R1. When the printer is connected to the processor J1 pin 11 is pulled low by the printer therby indicating connection.

Each character in the printer is formed by 30 bytes of dot data, each pair of bytes being made up of the dot data needed to form the character if the character cell is scanned horizontally. The first byte in the pair indicates the state of every other dot while seven bits of the following byte indicate the state of the interstitial dots for the same horizontal scan. Thus fifteen pairs of bytes correspond to fifteen horizontal scans of the character. In this way any character font in a 15 by 15 cell may be created. The printer buffers the data and translates the horizontal dot information into vertical dots for printing. Each 30 bytes of dot data are followed by a print command to print the character. The printer is also able to print in expanded and compressed modes.

The TBUS port located at A8H latches two signals to the video section and two for the datacomm section. The NMODEM signal is inverted to provide the clock for the latch (U415).

GRAPHICS SUBSYSTEM

The Graphics Controller occupies address port locations C0 to FF
completing the full range of addressable I/O. The Z80A processes the
necessary vector parameters needed for the graphics controller. The
Z80A downloads to the graphics arithmetic logic unit (ALU) registers
these parameters. After the vector has been described by the Z80A, it
tells the graphics controller to calculate and draw the described
vector into graphics memory. The graphics hardware supports set,
clear, compliment and jam pattern drawing modes. See section 3.4 and
3.5 for a full technical report of the graphics subsystem.

3.2   MEMORY SECTION

The Z80A is capable of addressing 65536 (64K) bytes of memory data.
The memory map for this processor is shown in the table below.

TABLE 5.0 Terminal Memory Map

Address	Contents		Size
0000H	Initialization, NMI Routine, Main Scan Loop, Range Tables, Support Routines, Block Mode Tear Aparts, Datacomm, Test Routines.	U912	8K
2000H	User Soft Keys Routine, Configuration Menus, Keyboard Mapper, Translator Routines, Language Tables.	U913	16K
4000H	Graphics Routines.	U915	24K
6000H	Integral and External Printer Routines.	U916	32K
8000H	Video Intrinsics (CRTC map)	U918	40K
A000H	Character Dot Information for the Printer. (lower 4K used, upper 4K is empty) (CRTC map)	U919	48K

C000H	Dynamic RAM
	   - buffers
	   - display memory
	   - stack
	   - system variables
	
	ZD0 : ZD1 : ZD2 : ZD3 : ZD4 : ZD5 : ZD6 : ZD7
	U820 :U819 :U818 :U817 :U720 :U719 :U718 :U717
			64K

3.2.1   Read-only-memory

As can be seen from the memory map 48 K of address space has been
allocated for read-only-memory (ROM).   This memory contains the Z80A
programs which controls the terminal operation.   The ROM space is
decoded into six 8K byte blocks by the 74LS138 decoder U911.

During an instruction (opcode) fetch the Z80A activates the NM1 signal
to indicate that an instruction fetch cycle is in process. This signal
is used to provide an early enable of the ROM being addressed during an
opcode fetch therby allowing the use of ROMs with an access time on 350
ns from address or 300 ns from enable (note that an opcode fetch is one
clock cycle shorter than a memory read operation) without wait states.
During a memory read from ROM the

TNMREQ and TNRD signals go active enabling the addressed ROM.   Data is
required valid approximately 470 ns from address, therefore no wait
states are required for memory reads even when using 450 ns EPROMs.
Note that data is placed directly on the Z80A data bus without
buffering.

3.2.2   Random-access-memory

The RAM subsystem has been designed around the MK4116-2 (or equivalent)
16K x 1 bit dynamic RAMs.   The MK4116-2 has a minimum access time of
150 ns and minimum cycle time of 320 ns.   U820-817 and U720-717 supply
data bits ZD0-ZD7 respectively to provide the 16K bytes of RAM data
storage.

The RAMs are accessed in three ways: by the Z80A for memory read or
write accesses, by the Z80A during a refresh cycle and by the CRTC
during a DMA (direct-memory-access) cycle.   Each of the three is
discussed below.   Refer to figure 6.0 for RAM timing.

Z80A READ/WRITE

A Z80A access to RAM is initiated by lowering the TNMREQ signal at an
address location between C000H and FFFFH (RAM address range). Prior to
TNMREQ going low the output of U613 would be high causing 1's to be
shifted through the shift register, U514, by DRCX. As TNMREQ goes low
(TNRFSH is high) the output of U613 goes low also.   As the clock
occurs, 0's are shifted through the shift register causing outputs QA-
QD to go low in turn.   This produces the RAM timing sequence as
follows: NRAS-strobes in row address, MUX-changes RAM address inputs
to column address, NCAS-strobes in column address and activates
internal RAM circuitry to access the addressed cell.   Data ouput on
MD0-MD7 is vaild 100 ns from NCAS. When the Z80A is finished accessing
the RAM the TNMREQ signal goes high and 1's are shifted through the
shift register completing the RAM cycle.

If the Z80A is performing a read operation the TNRD line is lowered
along with TNMREQ (TNWR remains high).   The TNRD signal is gated with
the output of U613 to enable the transparent latch, U618, during the
read operation. When the NMUX signal goes high (as MUX goes low) the
transparent latch becomes transparent, that is, the outputs follow the
inputs, placing the RAM outputs on the Z80A data bus.   The latch
outputs are enabled until TNRD and TNMREQ go high again.

For a write operation, the Z80A lowers TNMREQ and places the output
data on the data bus. Approximately one Z80A clock later the TNWR line
goes low strobing the data into the internal data latch in the RAM.
The TNRD signal will be high disabling the transparent latch so RAM
outputs will never be on the Z80A data bus.   The cycle proceeds as for
a read operation with TNMREQ going high, shifting 1's through the shift
register to complete the cycle.

Z80A REFRESH

The nature of dynamic RAMs requires that each row must be accessed
every two milliseconds to guarantee the contents of that row are held.
The Z80A has a built-in refresh function to provide signals which
perform dynamic RAM refresh without requiring extra processor overhead.
The Z80A maintains a 7 bit memory refresh counter which is incremented
following each instruction fetch.   While the instruction is being
decoded and executed the refresh counter is output on address bits TA0-
TA7 while the TNRFSH and TNMREQ signals are brought low, initiating the
RAS-MUX-CAS sequence, refreshing that row.   Since the TNRD and TNWR
signals remain high during the refresh cycle, the memory contents are
unaltered and the transparent latch is not enabled so that the accessed
byte does not appear on the bus. CRTC DMA

Twice per video row, on scan lines 6 and 14 (if starting to count from
0), the NBUSREQ signal to the Z80A is activated to allow the CRTC to
perform DMA of enhancement and character data (see section 3.3 for more
information on the CRTC).   The Z80A responds to NBUSREQ at the end of
the current machine cycle by tristating its address and control lines
and activating the NBUSAK line signalling that the bus is available and
will remain so until NBUSREQ is raised.   The NBUSAK signal is inverted
and buffered by U711 to provide both TBUSAK (active high) and TNBUSAK
(active low, buffered).   These signals are used to tristate the address
and control buffers U814, U714 and U811 and enable the video subsystem
for DMA action.   TBUSAK enables the CRTC to place the lower 12 bits of
the DMA address on the bus and enables the output of the transparent
latch, U618, as well as enable the load signal to the shift register,
U514. TNBUSAK enables the upper four bits of the DMA address from U515
onto the bus and takes the recirculating line buffer, U619, out of the
recirculate mode (see section 3.3 for more information on DMA
addressing).

Approximately four character times before the start of the video row
the line rate clock (NLRC) output of the CRTC goes high enabling the
load signal to the shift register through the OR gate U614.   The load
signal is derived from the character rate clock, LCGAX, which is
delayed three dot times through U414 in order to synchronize the RAM
access to the video timing and guarantee sufficient address set up time
to the RAMs. The load signal causes RAS-CAS shift register , U514, to
be parallel loaded on the next rising edge of DRCX (dot rate clock).
Upon loading, the shift register output QD is high and QA is low. THis
condition forces the output of U613 to go low, causing 0's to be
shifted through the shift register.   The next three occurances of DRCX
produce the NRASMUX-NCAS sequence, accessing the addressed byte. Data
is available 100 ns from NCAS, and, since NMUX is high, is placed
directly on the Z80A data bus (U618 is in transparent mode), and
therefore on the line buffer inputs.   As the shift register output QD
goes low the output of U613 is forced high and 1's are shifted through
the shift register completing the RAM cycle.   As MUX goes high again,
NMUX goes low causing the data out from the RAM to be latched in the
transparent latch, U618, where it is held until the next memory access.
As LBCDEL (delayed line buffer clock) goes low the data is clocked into
the line buffer U619.   The CRTC increments the address and the next
load signal occurs 9 dot times from the first, repeating the DMA cycle.
In this way 80 sequential bytes of data are fetched from the RAM and
loaded into the line buffer during the 80 active video character times
of the display.

   Note: Although the shift register load signal is enabled four
   character times before active video, the CRTC holds the starting
   address until active video and then increments it during active
   video.   In addition, the data is not clocked into the line buffer
   until the line buffer clock transitions low during active video.

On the last scan line of a character row, scan line 14, the CRTC lowers
the LBRE (line buffer recirculate enable) output, taking line buffers
U620 and U518 out of the recirculate mode (where the output is shifted
back into the input) thereby allowing data to be clocked into the
inputs. During the DMA cycle of scan line 14, as characters are being
output from line buffer U518 to the display, characters for the next
row are fetched from memory and loaded into line buffer U518.   At the
same time, as enhancement data is shifted out from U620, the data which
was previously stored in the temporary line buffer U619 (during the DMA
cycle of scan line 6) is shifted into U620.   In this way the display
data for the next row of characters is loaded into the line buffers
during the last scan line of the previous row as it is being displayed
on the screen.

3.3   VIDEO CONTROL SECTION

3.3.1   Overview

The video control section generates the timing signals required to fetch character and enhancement data from memory and drive the analog sweep circuitry to display that information on the CRT.

The display is divided into 26 rows of 80 character cells each. Each character cell is a rectangle, 15 dots vertical by nine dots horizontal. Any character to be displayed is produced by selectively lighting the dots of the character cell which shape that character, leaving the others blank. Dots are left blank on either side and on the top and bottom of the character cell to provide horizontal and vertical separation between normal characters. This is not true of characters which are continuous across the character boundary, such as line drawing characters (used to display forms).

The analog sweep circuitry sweeps the electron beam from left to right and from top to bottom across the display. As the beam is swept horizontally it is turned on to produce a lighted dot and off to blank a dot position. As the beam reaches the end of its scan a horizontal sync signal is sent to the sweep causing the beam to retrace horizontally and begin sweeping again. During this time the beam is also being swept vertically. The combination of these two produces the display raster. As the beam reaches the bottom of the display a vertical sync signal is sent to the sweep causing the beam to retrace from the bottom right to the top left corner. In this manner the CRT display is written 60 times per second (when configured at 60 Hz) or optionally 50 times per second (configured at 50 Hz).

HORIZONTAL TIMING

After the 80th character position of a scan line the beam is turned off (blanked) and remains so as the horizontal retrace takes place. The beam is enabled again as it reaches the position for the first character of the next scan. This blanking interval is called "horizontal blanking". This blanking allows time for the beam to retrace, settle at the left side and begin tracing again. The portion of the scan where the beam is enabled is known as "active video". The horizontal scan time consists of the 80 character times of active video plus 35 character times of horizontal blanking for a total of 115 character times per scan (1 character time = 349 ns). This produces a horizontal scan frequency of 24.9 KHz.

The horizontal sync signal is activated 16 character times before the
last video character of the scan and is active for 7 character times.
It is produced in advance of the last character to compensate for the
delay in the sweep horizontal centering circuit.

VERTICAL TIMING

The 26 active video rows of the display each require 15 horizontal
scans for a total of 390 active video scans. After the last scan line
of the last row is displayed, a vertical blank signal is activated
which disables the electron beam during the vertical retrace time. The
beam is enabled again on the first scan line of the first row. The
duration of the vertical blank interval depends upon the occurance of
the vertical sync signal which triggers the vertical retrace. This
vertical sync timing depends in turn on the frequency with which the
frame (one entire display) is refreshed. This frame rate may be
configured to either 50 or 60 Hz corresponding to the AC line
frequencies in foreign countries or the U.S. to eliminate display
interference between the power supply and CRT. The following table
describes the timing relationships between the vertical blank and
vertical sync signals and the frame rate.

TABLE 6.0 Frame Timing

	Frame Rate	
	60 Hz	50 Hz
Delay after v. blank to v. sync (# scan lines)	0	38
v. sync width (# scan lines)	19	64
v. blank duration (# scan lines)	25	108
Total # scan lines per frame	415	498

3.3.2   Display memory addressing

Section 3.2.2 describes how the CRTC performs DMA to load the line
buffers with character and enhancement data for display. Before it
performs DMA, the CRTC must be loaded with a starting address (called
the row-start address). Each time the CRTC is enabled it fetches 80
consecutive bytes of data starting from the row start address and
places it into one of the recirculating line buffers.

The Z80A maintains a table of 24 row start addresses in memory
indicating the addresses of the first byte of character data for each
of the character rows being displayed. Rows 25 and 26 contain the soft
key labels and are always accessed from fixed locations. This table is
actually a subset of a larger table which contains row-start addresses
for all 48 display rows. The address of the first enhancement byte of
a row is the first character byte address offset by 80.

Two scan lines prior to the NBUSREQ signal being activated a non-
maskable interrupt (NMI) is generated which causes the Z80A to branch
to the NMI service routine after completing the current instruction.
Part of this service routine writes the row-start address for the next
DMA into the rowstart register of the CRTC.   The row-start address is
written into the CRTC via the address bus itself.   At the same time,
bits TA13 and TA12 are written into the 74LS175 U615, which provides
the upper bits of the RAM address for DMA.   The Z80A reads the row
start address from the table, adds the 80 byte offset for enhancement
data DMA, masks bits TA15 and TA14 to a 1 and 0 respectively and then
writes a 02H to this address. By masking bits TA15 and TA14 the
address corresponds to a ROM location, which of course can't be
written.   These bits are decoded by part of U517 and U417, along with
TNMREQ and TNWR to generate the register load signal (U421 pin 38)
which latches the address into the CRTC and U75 for use during the next
DMA cycle. The data bits ZD0 and ZD1 select the register to be written
to, in this case, the row-start register.   The NMI service routine
keeps count of the next row to be displayed in order to determine which
row start address to send to the CRTC next.   Since NMI can be disabled
for an indefinate period (for example during a RAM test) it is
resynchronized every frame by reading the VBLANK signal through the
system status port.

3.3.3   Character display

At any given time the characters for the current row being displayed
are held in the recirculating line buffer U518.   The character codes
output from this line buffer are resynchronized to the character clock
through the octal latch, U418, from which they are sent to the
character ROM, U419.   This ROM contains the dot pattern for each scan
line of each each possible character code.   The standard character set
uses the ASCII character code to represent the 128 possible characters
in the set.   The first 32 characters of the set are the control
characters (escape, line feed, carriage return, etc.)   while those
remaining are the alphanumeric and punctuation characters.   These 128
characters are represented in bits X0-X6 with X7 being a 0.   These bits
along with the scan line count become addresses for the dot data from
the character ROM.   Therefore, 11 address bits are required, meaning
that a 2K byte ROM may be used to contain the dot data for the standard
character set.   Bit X7 will then serve as an active low chip select.

By using a 4K byte character ROM, two complete character sets may be
displayed.   In this case bit X7 selects between the two character sets.
Likewise an 8K byte ROM can store four complete, 128 character,
character sets.   The schematic shows a signal from the enhancement data
latch, U520 pin 15, which is inverted by U218, and sent to U419 pin 21.
This signal is used to address the 8K byte character ROM on 4K
boundaries.   This combined with bit X7 from the character data latch
allows selection of any of the four character sets.   This uppermost
address bit becomes a chip select for 2K or 4K character ROMs.

As the character code and scan line count is issued to the character
ROM an   access   time delay is encountered before   the   dot data is
available at the outputs.   The character ROM has an access time of 300
ns, therefore one full character time (349 ns) delay is introduced.

As the dot data becomes available out of the character ROM the LVSRX
(load video shift register, buffered) signal is brought low which, on
the rising edge of DRCX, parallel loads the data from the character ROM
into the character shift registers U319 and U320 (and U324 as explained
later).   Since only seven dots per scan line are required for standard
characters, seven dots are loaded from the character ROM (low output
means dot is lit) into the shift registers. The MSB (most significant
bit) output from the character ROM is latched by U222 (on LCGAX clock)
and is used to enable the half-shift function (described below).   The
MSB output of U319 is connected to the serial input of U320 essentially
forming an 8 bit shift register.   At the same time that the seven dots
are loaded into the shift register a 1 is loaded into the MSB.

The QD output of U320 goes to the character multiplexor, U124.   This
multiplexor selects one of several inputs to gate to the dot stream.
For a normal scan (not half-shift) the multiplexor select inputs will
be 101 (C input is most significant) selecting the D5 input.   As the
dots are loaded into the shift register the first dot (which is high)
appears on the D5 input of the multiplexor and is gated to the dot
stream.   On each of the next 8 dot rate clocks (DRCX) dot data is
shifted one bit position in the shift register and therefore to the D5
multiplexor input and to the dot stream.   Since the serial input of
U319 is tied high, a 1 (blank dot) is shifted into the shift register
as the dot data is shifted out.   Therefore at the end of the 9 dot
clocks comprising the horizontal scan for a standard character, the
first and last dots are blanked (1's) with the 7 dots from the
character ROM in between.

HALF-SHIFT

To avoid the "stairstep" appearance of characters with long diagonals,
a feature known as "half-shift" is implemented which allows and scan
line of a character to be delayed by half a dot time. This half-
shifted scan line, placed between two normal scan lines, fills in the
diagonal as shown below.

```
    X              normal          X
    X           half-shifted        X
      X            normal            X
      X         half-shifted          X
        X          normal             X
        X       half-shifted            X
```

(no half-shift)   (with half-shift)
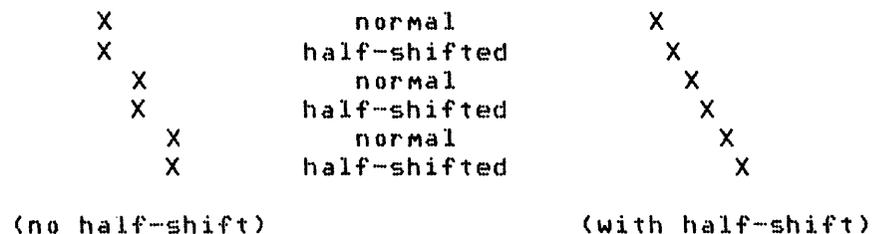
In the standard character set the MSB output of the character ROM
indicates that a scan line is to be halfshifted. This output is
latched (by LCGAX) into U18 where it is held for the 9 dots of the
character time. The output of U222 is fed to the character multiplexor
select input A which, for half-shifted scan lines, selects the D4 input
(U124 pin 15). The QD output of the dot shift register, U320, is sent
to the JK flip-flop, U221, clocked on the falling edge of DRCX, which
performs the half-shift of the dot data. The output of this flip-flop
goes to the D4 input of the character multiplexor. The half-shift
flip-flop is preset by LVSRX at the time new dots are loaded into the
shift registers.

COPY BIT

Some alternate character sets such as line drawing set or large
character set require all nine dots an a scan line to be active. This
allows for continuous dots across a character boundary as required for
drawing forms, etc. on the display. In order to get nine dots out of
eight outputs from the character ROM, a copy bit circuit is activated
which copies the MSB output into the first two dots while the remaining
seven ROM outputs form the remaining seven dots.

The seven least significant ouputs from the character ROM are loaded
into shift registers U319 and U320 as for standard characters. The
most significant output is loaded into both the A and B inputs of shift
register U324 at the same time as the least significant seven bits.
Thus, the MSB is "copied" in shift register U324. The remaining dots
are brought from the QC output of U320 into the serial inputs of U324
thereby forming a nine bit shift register with U319, U319, and U320.
The QB output from U324 is then fed to the D7 and D6 inputs of the
character multiplexor which are selected when the select inputs are
11X. Note that the select A input is a don't care since half-shift
cannot be used in these character sets.

The copy bit circuit is activated whenever the X7 output of of the
character latch U418 is active. Remember that this bit is activated to
select the second character set in a 4K character ROM or the second and
fourth sets in an 8K character ROM.   The first 32 character of any of
the four posible character sets are reserved for control characters and
therefore copy bit is deactivated when these positions are accessed.
This condition is decoded by bits X5 or X6 being gated with X7 (U123
and U724) to enable copy bit only for the upper 96 characters of the
set.   The result of this decoding is latched in the D flip-flop, U425,
which allows for the access time of the character ROM.   The flip-flop
is clocked by the combination of LVSRX and DRCX which are gated
together by U525.   The output of the copy bit enable latch is then used
to select the copy bit shift register output and gate it to the dot
stream.

CURSOR

The generation of the cursor for the display is performed by a
combination of hardware and software.   The CRTC activates its cursor
output when the address of the character being fetched during a DMA
cycle matches the contents of its internal cursor address register.
This output is active for all scan lines.   The software maintains and
updates this register in the CRTC corresponding to the position of the
cursor on the display.   In order to make the cursor blink the software
alternately writes a valid cursor address and then an invlaid one.

The cursor signal, CUR, output from the CRTC is gated with another
signal, ULTIME, to produce a cursor signal, NCUR, which is active on
the 13th scan line.   ULTIME is decoded from the scan line count by U316
and U317.   This signal also enables the underline enhancement during
the 13th scan line.

In the normal situation, where the cursor does not lie in an underline
field,   the NCUR signal is propogated thru U614 to become NCURSOR which
is fed to the select C input of the character multiplexor.   This input
goes low to activate the cursor which for normal characters (not copy
bit) selects the D0 or D1 inputs which are tied low.   This causes the
dot stream to be active for the 13 scan line of the character position
in which the cursor lies.   In effect this OR's the cursor with the
character in the cell (a non-destructive cursor).   If the copy bit
circuit is active however, the D2 of D3 inputs of the character
multiplexor are selected.   These inputs provide the inverted series of
dots from the copy bit shift register.   In essence this inverts the
13th scan line of the character when the cursor is active.   This is
necessary rather than the OR'd cursor used above due to the fact that
some of the characters may have all dots of the 13th scan line lit and
the cursor would never be seen.

DOT STRETCH

The dots are inverted by U124, the character multiplexor, to provide an active high dot stream output. This dot stream is then passed through Q3 and its associated circuitry which performs a "dot stretch" function. This dot stretch is used to provide an elongated active dot which has a more pleasant appearance when displayed. It essentially "fattens up" the dots composing a character. The switching time of the transistor from saturation to cutoff is dependent upon the parasitic collector to base capacitance and the external capacitor C14. This capacitance limits the switching speed, essentially stretching the amount of time the transistor is active (in saturation). Capacitor C17 is included to compensate for parasitic base to emitter capacitance. Note that an inversion is introduced by this dot stretch circuit.

After being stretched, the dot stream is gated through U122 where it picks up the underline enhancement and then is sent to the enhancement multiplexor where graphics video and the remaining enhancements are added before sending the information to the analog sweep circuitry.

3.3.4   Enhancement Display

A one-to-one correspondence exists between each byte of character data and each byte of enhancement data held in recirculating line buffers U518 and U620 respectively. As a byte of character data is sent to the character ROM its corresponding enhancement byte is sent to the enhancement section where it is decoded and recombined with the dot stream in the enhancement multiplexor, U120.

Of the eight available bits in the enhancement byte, only seven are used. Four of these, EN0-EN3, select the blink, inverse, underline and halfbright attributes which may be selected in any combination. Bit EN4 is the set enhancement bit which, when high, causes the current enhancement to be latched and held until another enhancement is set or until the end of the current row. Bit EN5 is the end-of-line bit which causes the display to be from the current character to the end of the row. In this way, to clear the display, end-of-line is set in the first character postion of each row.   Bit EN6 as described above forms the most significant address bit for an 8K byte character ROM.

As a character is latched into U418, six of the seven enhancement bits are latched into the hex latch, U520. The set enhancement bit is latched at the same time (by LCGAX) into U222. At this time EN6 is fed to the character ROM to provide the character ROM address selection for its corresponding character. The attribute bits, EN0-EN3, output from U520 are then sent to the 74LS163, U519. In this mode, with the count enable inputs P and T grounded, it acts as a latch with a synchronous load and clear.   This latch provides the additional character time delay to compensate for the character ROM access time.   If the set enhancement bit, EN4, is set, the output, U222 pin 3, will go low as the bit is latched.   This activates the load input of U519 causing the attributes to be loaded on the next character clock (when the character ROM outputs are loaded into the shift register).

VIDEO ATTRIBUTES

The blink attribute output (U519 pin 14) is gated with the blinkrate
signal from the I/O section, which alternates high and low to produce
the active low NBLINK signal. When active the NBLINK signal allows
only the cursor to be displayed, blanking the character. In this way,
the blinking characters are alternately displayed and blanked. The
inverse bit simply selects the inverted dot stream (ALPHA) or cursor
signals.

The underline signal, ULINE, under normal conditions (when cursor is
not active) simply causes the dot stream to be turned on during scan
line 13. This is accomplished by gating the ULINE signal with ULTIME
and using the results to force U122 pin 3 high, thereby activating the
dot stream. A problem exists, however, when we want to position the
cursor at a character position where underline is active. We can no
longer merely "OR" in the cursor into the dot stream because it lies on
the same scan line as the underline and therefore would never be seen.
What is done instead is that when both are active (NCUR is low and
ULINE is high), neither the cursor nor underline appear on the display.
This essentially disables the underline at the cursor position on the
display producing a blinking hole in the underline. The NCUR signal is
sent into U611 pin 9 which, when active, prevents the underline signal
from being gated into the dot stream. At the same time the ULINE
signal is sent into U614 pin 9 disabling the NCURSOR signal which
normally generates the cursor. Thus, both are disabled.

The last attribute, halfbright, selects which of the video inputs on
the analog sweep board will receive the dot information. When the
halfbright attribute is activated the dot information is inhibited from
the NFULLBRT output (which gives full intensity characters), U218 pin
11, by pulling U218 pin 13 low, and is enabled through U218 pin 8 which
sends the active low dot information on NHALFBRT to the sweep.

END-OF-LINE

The remaining enhancement bit, EN5, performs the end-of-line function.
When set, this bit causes the display to be blanked from the current
character position to the end of the row. This eliminates the need to
clear both character and enhancement data in order to clear the
display. After being latched in U520 the end-of-line signal is gated
through U218 and U525 to lower the clear input of U519 (pin 1). This
causes the enhancements to be cleared at the next character clock (when
character ROM outputs are loaded into the shift registers). At the
same time that U519 is cleared, the endof-line signal is latched into
U321. The Q' output (U321 pin 8) is sent back to the preset input to
hold the flip-flop in the cleared state for the rest of the scan line.
At the end of the scan line the NLRCX (inverted line rate clock) clears
the flip-flop (clear overrides preset). At the same time the Q'
output, NEOLDEL, is gated through U122 to activate the BLANK signal.

This signal blanks the display by deselecting the alpha input, only
allowing the cursor signal to be gated to the sweep.   The cursor signal
is allowed since it is necessary to be able to position the cursor even
in a blanked field.   The Q NOT output, U321 pin 8, is gated to the
clear input of U519 in order to hold the enhancement latch in the
cleared state.

The horizontal blank signal causes the dot stream to be disabled
(blanked) after the 80th character of a row and holds it in the blanked
state until the first character of the next row.   This signal is
obtained by latching the LBCX (line buffer clock) signal in U222 pin 13
and adding a one character delay in U222 pin 5.   The LBCX signal is
active high at the rising edge of LCGAX during the 80 active video
characters.   HBLANK is then gated through U517 to activate BLANK and
disable NCUR.   VBLANK and DISPOFF also blank the display in a similar
fashion.

The last part of the video section to consider is the enhancement off
circuit which allows the enhancement latches to be disabled.   The Z80A
sets the ENHOFF signal, output from U416, which is latched by the
RECIRC signal into U321.   The Q output (U321 pin 5) is gated through
U525 to clear U519 while the Q' output (U321 pin 6) clears U520.   The
RECIRC signal goes low to take the line buffers out of the recirculate
mode as they are loaded during scan line 14.   This means that the
ENHOFF bit is always latched at the start of a new row.   The software
can then change ENHOFF during an NMI service routine to disable
enhancement display on the next row.

3.4   GRAPHICS SUBSYSTEM

The Graphics Subsystem is a complete entity apart from the
alphanumerics portion of the terminal.   The Z80A sees the the graphics
hardware as a read and write I/O port.   The hardware consists of a
graphics controller, ALU, write and read display circuitry, and 16K
Words (16K X 16) display of memory.   Graphics video is multiplexed with
the character video just before the sweep circuitry sees it.   To draw a
vector, the Z80A download vector parameters describing the point to
point location in which the vector is to be drawn.   From there the
graphics controller takes over and calculates the addresses of each dot
position which makes up the line path of the vector.   Each dot is
stored into the graphics memory one dot at a time.   After a vector has
been drawn the graphics controller set a status flag at a port location
telling the Z80A the controller is done drawing.   At this point the
Z80A can go ahead and download vector paramemeters of another line to
be drawn.

3.4.1   Vector Algorithym

If we use Cartisian coordinates in the positive right half plane, we
can define an algorithym that will give us a incremented line path:

                    Delta X = X old - X new
                    Delta Y = Y old - Y new

The unconditional direction is the direction in which the position is
aways incremented.   If Delta X was greater than Delta Y it would make
sense to increment the X direction for every iteration and let the Y be
incremented if it is needed.   This makes the Y direction conditional
because it is dependant on the X position for it's incrementation.

The following algorithym assumes:

Delta X is greater than or equal to Delta Y is greater than or equal to
0.

This says that the X direction is always the unconditional direction
and the Y direction is the conditional.

The conditional direction is the direction that is dependent on an
error term "e" which checks if the conditional direction has exceeded
the unconditional directions unit length.   If it has, it is then
incremented and the error checking is repeated until the path of the
vector length is completed.

The error term is described as follows:
        e = (Delta Y / Delta X) - 0.5

By following the preceeding algorithym we can determine when to
increment the unconditional and conditional directions.

```
START)   is e > 0            (checks to see if the conditional
                             direction should be incremented)

         if not true -> go to COND


         Y = Y + 1           (increment the conditional
                             direction)

         e = e - 1           (reinitialize the error term)

         X = X + 1           (increment the unconditional
                             direction)

         go to START

COND)    X = X + 1           (increment the unconditional
                             direction)

         e = e + (Delta Y / Delta X)

                             (add slope differential to error
                              term as an increment for uncon-
                              ditional unit length detection)
         go to START

         end
```

This algorithym has two problems, it has a divide in it's operation
which can be slow or hard for our microprocessor to do and it only
describes a line from 0 to 45 degrees.

To get rid of the divive function, we multipling the error term by a
constant, 2 Delta X. We can do the same algorithym but now with adds,
subtracts and multiply by 2's which is easy for a microprocessor to do
by shifting one bit space.

To be able to draw in all the quadrants we must define three more
variables.   By being able to specify the X and Y increment as positive
and or negative, we can draw a vector in any four quadrants from 0 to
45 degrees with respect to the specified quadrant.   The third variable
needed is a check to see which direction is unconditional .   This
determines which octant in a given quadrant to draw in.

         Octant flag = abs|Delta X| - abs|Delta Y|

If the sign of the results is negative, we know the Y direction is
greater so it is the unconditional direction.

The vector length or the number of dots to be drawn is determined by
the unconditional direction's value.   Since it is this direction that
is incremented every iteration, the integer value of the Delta will be
it's length.

The resulting algorithym is the one that is used.   Please refer to the
flow chart figure 3.0.

Note: The error terms are now called discriminants.

START) is OCTANT FLAG < 0
          yes, then increment Y with Yinc
          no , then increment X with Xinc

       is DISCRIMINANT < 0
          yes, then increment DISCRIMINANT WITH D1
               GO TO START
          no , then increment DISCRIMINANT with D2
               and increment the conditional direction
               with it's increment
               GO TO START

D1 and D2 are incremental discriminants used for slope detection and
error term reinitialization, respectively.
  Initial Discriminant = -| Delta X | + 2 | Delta Y |
                  D1 = 2 | Delta Y |
                  D2 = 2 | Delta Y | - 2 | Delta X |

3.4.2   Graphics I/O allocations

I/O PORT ADDRESS (HEX)	DESCRIPTION
C0	Write to static ram- Y starting address (LSB)
C1	Write to static ram- Y starting address (MSN)
C2	Write to static ram- X starting address (LSB)
C3	Write to static ram- X starting address (MSN)
C4	Write to static ram- Dot count (LSB)
C5	Write to static ram- Dot count (MSN)
C6	Write to static ram- Initial Descriminant (LSB)
C7	Write to static ram- Initial Descriminant (MSN)
C8	Write to static ram- Increment D1 (LSB)
C9	Write to static ram- Increment D1 (MSN)
CA	Write to static ram- Increment D2 (LSB)
CB	Write to static ram- Increment D2 (MSN)
CC	Write to static ram- Yinc (LSB)
CD	Write to static ram- Yinc (MSN)

I/O PORT ADDRESS (HEX)	DESCRIPTION
CE	Write to static ram- Xinc (LSB)
CF	Write to static ram- Xinc (MSN)
D0	Write to static ram- not used
D1	Write to static ram- Octant Flag (MSN)
DA	Write to static ram- 00H Test constant (LSB)
DB	Write to static ram- XEH Test constant (MSN)
DC	Write to static ram- 01H Test increment (LSB)
DD	Write to static ram- X0H Test increment (MSN)
DE	Write to static ram- 00H Copy constant (LSB)
DF	Write to static ram- X0H Copy constant (MSN)

E1	Write register- Modes and Prescale
	
	` ‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾ `
	`  I 7 I 6 I 5 I 4 I 3 I 2 I 1 I 0 I `
	` ‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾‾ `
	`  MSB                        LSB `
	
	Bits 0-3 > Prescale 1's compliment
	Bits 4 and 5 > Mode
	          00B clear mode
	          01B set mode
	          10B compliment mode
	          11B jam mode
	Bit 6 > set to Blank Video
	Bit 7 > set to inhibit 1'st dot write

I/O PORT ADDRESS (HEX)	DESCRIPTION
E2	Read Status- Graphics controller status Bit 7 > Busy Flag Bit 0 > Vertical Blank time (write to clear)
E4	Write to Pattern Register- writes 8 bit pattern to the pattern register and also sets scale of the pattern.
E8	Write Drawing Flags- Bit 7 > set to Draw Vector Bit 1 > low to set or clear memory Bit 0 > low to inhibit pattern
F0	Read Vector Data-reads MSB of specified Graphics Word
F1	Read Vector Data-reads LSB of specified Graphics Word

3.4.3   Graphics Controller and ALU

The Graphics Controller and ALU are responsible for receiving and executing vector parameters downloaded by the Z80A. Before a vector can be written into graphics memory, the Z80A, knowing X and Y start and end points, must calculate the dot count, descriminants, mode and etc. which describes the vector fully. These parameter are then downloaded through the graphics bus transceiver, U410, to the proper address locations in ram (U21, U33, and U53). The address of these rams are multiplexed by U52 and selects between the Z80A addresses or the graphics controller addresses .   When the graphics controller is not busy it allow the Z80A the address the rams.   The port decoding is done with U82 and U71 monitoring addresses C0 thru FF and the NIO request signal to enable the various ports in the graphics I/O.

After downloading the vector parameters to the ram (address locations C0 through DF), the Z80A writes to port E1 to set the mode and scale. Port E1 is decoded by U94 pin 8 and the data is latched by U49.   See Graphics I/O allocation for bit assignment of this port.

If the vector is to be drawn with pattern, a write to port E4 will load
pattern and scale (previously defined at port E1) into the shift
register U48.

While all the parameter are being set up by the Z80A, the Prom Based
Microsequenced Graphics Controller is in a wait loop waiting for the
Z80A to set the draw bit telling it to go ahead and draw the vector.

The internal bus is 16 bits wide of which the lower byte ROR7-ROR0,
contains ALU ram addresses or program jump locations and the upper byte
ROR15-ROR8, containing the ALU intructions. The instructions are
decoded by U41 into simple add, store and jump signals.

This architecture is basically pipelined having the program counters
U31 and U32 address the two program proms U42 and U22 clocking the
instructions and address locations to two octal latches U23 and U43.

After the Z80A done sending vector parameters it writes to port E8
which consists of three d flip-flops U51, and U61, setting the draw bit
to a 1.

The controller is monitoring this bit through the demux U62, while it
is in it's wait loop. Upon receiving this bit the program counters,
U31 and U32, begin to step through the micro code of the proms. The
prom code then executes the vector algorithym described in section
3.4.1.

The proms, U22 and U42, are 32 X 8 bits and contain the following micro-code:

	PROGRAM ADDRESS	INSTRUCTION CODE (U42)	ADDRESS (U22)	OPERATION
PON	00H	60H	00H	Power On, Flag resets controller into wait
WAIT	01H	02H	01H	Jump NOT BUSY, to WAIT
	02H	84H	00H	load YaddrB > YaddrA
	03H	84H	11H	load XaddrB > XaddrA
	04H	84H	22H	load DotC B > DotC A
	05H	84H	33H	load InDiscB > InDiscA
	06H	84H	88H	load OctFgB > OctFgA
DLOOP	07H	88H	D1H	Test Carry Xaddr, Ovflo
	08H	03H	0DH	Jump on Carry to DOTC
	09H	88H	D0H	Test Carry Yaddr, Ovflo
	0AH	03H	0DH	Jump on Carry to DOTC
	0BH	20H	01H	Store X address
	0CH	40H	00H	Store Y address
DOTC	0DH	80H	E2H	Add to DotC, increment
	0EH	03H	00H	Jump on Carry to PON
	0FH	88H	F8H	Test sign of OctFg

continued.....

	PROGRAM ADDRESS	INSTRUCTION CODE (U42)	ADDRESS (U22)	OPERATION
	10H	01H	13H	Jump Sign neg. to YUNC
	11H	80H	71H	Add to Xaddr, Xinc
	12H	00H	14H	Uncond Jump to DOD
YUNC	13H	80H	60H	Add to Yaddr, Yinc
DOD	14H	88H	F3H	Test Descriminant < 0
	15H	01H	1DH	Jump Sign neg. to DOD1
	16H	80H	53H	Add to Descriminant, D2
	17H	88H	F8H	Test sign of OctFg
	18H	01H	1BH	Jump sign neg. to YUNC2
	19H	80H	60H	Add to Yaddr, Yinc
	1AH	00H	07H	Uncond Jump to DLOOP
YUNC2	1BH	80H	71H	Add Xaddr, Xinc
	1CH	00H	07H	Uncond Jump to DLOOP
DOD1	1DH	80H	43H	Add to Descriminant, D1
	1EH	00H	07H	Uncond Jump to DLOOP
	1FH	XXH	XXH	not used

The Graphics controller steps through the micro-code and uses the ALU to check for Carry and Sign Bit for conditional jumps. Referencing the micro-code the first operation done is to download the starting Y address, starting X address, Dot Count, Initial Descriminant, and the Octant Flag. This is copied to the same address locations from register B (U21, U33, U53) to register A (U64, U44, U24). By doing this we can use register A as the update register, and register B for the incremental value to be added to register A.

The next step is to check to see if both the X and Y starting addresses are within the write address range of ther graphics memory. This is done by addressing the X or Y address from register A and adding it to the overflow constant E00H from register B. Remember that the ALU only has 12 bit resolution and we are checking to see if the X or Y value is larger than 512B (9 bits). By adding E00H to it and getting a carry, we know it is out of the addresable space of the memory. The additions are done through 3 4-bit full adders (U54, U34, U14) and are latched by 3 4-bit latches (U55, U35, U15) using the inverted outputs. This is done because the ram outputs and operation of the ALU is complimented. The Carry and Sign bits are latched by U63, a D flip-flop.

The controller then increments the dot count and checks to see if it is done drawing the vector. In this algorithym the dot count determines the vector length.

The next step is to test the Octant Flag to see which direction is unconditional.

The unconditional direction is then incremented and then the Descriminant is checked for sign. If negative, the program jumps to an instruction to add the incremental Descriminant D1 to the exsisting Descriminant then jumps back to the X and Y overflow check at the begining and starts the algorithym all over again. If the sign is positive then it knows to increment the conditional direction. The addition of the incremental Descriminant D2, to the exsisting Descriminant is done. An unconditional jump back to the overflow check is then executed.

All jumps, conditional or unconditional, is done by preloading the program address counters U31 and U32 with the jump location if the conditions are met. If a jump occurs, the instruction decoder must be inhibited from executing a false instruction (this is because it take two clocks to execute an instruction). U51 inhibits an instruction cycle by monitoring U62 pin 7 for a jump load signal.

After each iteration through the program loop, if the X and Y addresses
are valid, they will be stored in temporary registers U25, U45, and
U65. Both the X and the Y addresses are 9 bits in length. Upon
storage of the Y address a dot request flag is set in hardware to tell
the write state machine a valid dot address was caculated. U67 sets
this dot request. The state machine U75, is responsible for getting
the dot written into the display memory at the address specified by the
dot address of the ALU. The ALU addresses the display memory as
follows:

```
     X addr (U25+U65)                Y addr (U45+U65)
     ========================        ========================
S>  I0I1I2I3I4I5I6I7I8I       S>  I0I1I2I3I4I5I6I7I8I
     ------------------------        ------------------------
     I--**---I----word address of bit location-----I
```

     ** = bit in the word location to be written to.

Note: Each word is 16 bits so the lower 4 bits of the ALU X address is
      used to select the coresponding bit in that word.

      The Word address is then multiplexed and used to address all 16
      dynamic ram in the display memory of the specific word location
      in which one of it's 16 bit is to be written to.

The multiplexors U26 and U46 multiplex the word address of the ALU.

This completes the description of the primary functions of the Graphics
Controller and ALU.

4.5   GRAPHICS DISPLAY AND MEMORY

      The display circuitry is responsible for the accessing of graphics
      memory for raster scan video imformation. The display hardware
      consists of a RAS, MUX, and CAS generator for the graphics ram, display
      counters, display memory (16K X 16), and display related hardware sync
      circuitry.

4.5.1   Graphics Dot Clock Syncronization

      The display resolution of the graphics is 512 X 390. If we use the
      same dot frequency of the alphanumerics (25.77 MHz), the graphics
      display would occupy a small portion of active video. Also the scaler
      aspect ratio would be off. By dividing the 25.77 MHz clock down 1.5
      times, we will have a 17.181 Mhz graphics clock.

For every three alpha dots in the X direction, you will have two dots
of graphics.   This also made it posible to have a correct aspect ratio
with respect to the dot resolution.

By using two time shifted divive by three 16.66% duty cycle clocks
(U97, U89, U87, U98) we can "or" the two together and form a 17.181 MHz
33.33% duty cycle graphics clock. U88 "or's" these two signal together
and forms G Clk.

The 2/3 clock or 1 1/2 divider is created in hardware by a D flip-flop
(U89) and 4 bit syncronous counter (U97).

Reference figure 12.0 Graphics Dot Syncronization.

On the first NLCGAX signal, the counter U97 loads a binary 7 into it
registers on the positive edge of DRCX, the 25.77 MHz dot clock.   On
the next negative edge of DRCX U89 is Clocked. What is clocked through
is the signal on U97.14 which is a 0, which makes U89.6 a "1" since the
output is off of Q NOT.   This set up U87 for the next rising edge of
DRCX when U87 will output a 1 for the 19.4 nS high time of DRCX.   On

the next negative edge of DRCX, U89.6 is clocked low disabling U87
until the 4 clock edges where this is repeated.   This is on of the two
1/3 dividers.   On the following positive edge after U89.6 goes low,
U97.11 goes low enabling U98 for the next negative edge of DRCX when
another 19.4 nS high time from U98.1 will occur.   On the next rising
edge U97.11 goes high disabling U98.   U98 generate the second 1/3
divider only time shifted by 38.8 nS (one DRCX time). These two clocks
are then "or'd" by U88 to form the graphics dot rate clock G CLK.

4.5.2   Graphics Display

The display memory is bit-mapped and is accessed 16 bits at a time
(words). Each sixteen bits constitutes a graphics word. Therefore the
display raster consists of 32 words by 390 lines of graphics dot
imformation.   (32 words X 16 bits = 512 dots in the X direction.)

```
         |---------------------- 512 dots -----------------------|
Line     ---------------------------------------------------------
 0       | word 0  |.............................| word 32  |
 1       |                                                   |
 .       |                                                   |
 .       |                                                   |
 .       |                                                   |
 .       |                                                   |
 .       |                                                   |
 .       |                                                   |
 .       |                                                   |
389      | word 0  |.............................| word 32  |
         ---------------------------------------------------------
```

The display counter U17, U57, U56, U37, and U47 are used for addressing
the graphics ram for every word access. At Start of Frame when all the
counters are reset signifing the top of screen scan for the first line
of video, a ram access of the first word of the first line of video is
done.

The word address is incremented for the next word address of the first
scan line which another word   access is done for shifting out
continuously with the previous word as video graphics data.

The counters are clocked and another word access is done.   This is
repeated for every scan line until the hardware receives another Start
of Frame signal which occurs every frame time.

Addressing consist of 14 bits in which the lower 5 bits are the Word
count and the remaining 9 bits are the line count.   As in the ALU
addressing, this is mutiplexed by U36 and U16 for display accesses.
Since the address counters are syncronously incremented, each address
tells which word is being fetched.

Line 0 |word 0 |word 1 |.....word 32 |
address   00000000000000 00000000000001   000000000011111

Line 1 |word 0 |word 1 |.....word 32 |
address   00000000100000 00000000100001   000000001111111

The reference clock called DIS CYC is a clock divided by 16 from the G
CLK (graphics dot clock 17.181 MHz). This clock is from U76.11.

U76, U77, U78, U79 control the ras, mux and cas signals for display
writes or reads into graphics memory.

Reference figure 11.0 for display memory timing.

When the DIS CYC clock is low for 8 G CLK cycles the display hardware
allows a ras, mux and cas for a display word fetch at the address on
the display counters U17, U57, U56, U37 and U47.

The signal DLOD from U710.6 loads the two 8 bit shiftregister (U19,
U29) of the word accessed.   On the next G CLK the first bit of that
word is shifted out as serial graphics video to the video multiplexor.

Display Counters

The Row and Column address control is done by using a 4 bit counter U76
as a reference.   After a Start of frame, U76, which is clocked by G
CLK, starts to up count.   The lower three bit are used to select the
demultiplexor U77 which controls the D flip-flops U78 and U79 which
create the GNRAS, GMUX, and GCAS.

The fourth bit is the divide by 16 signal that is referenced as DIS
CYC.   So for every 16 G CLK's, or dot times, we can have two ras and
cas cycles of graphics memory. Since one display word fetch is 16 bits
long and it only takes 8 dot times to access and latch the word, the
remaining 8 dot times for which another ras and cas cycle can be done
is allocated for memory writes, since during this time we are still
shifting out the 16 bits as video imformation.

At the end of the count (16) the carry bit U76.15 enables the word
counters U17 and U57 which is clocked to the next word address of that
display scan line.   There is only one ras and cas cycle per 16 dot
times for display accesses and only one ras and cas cycle per 16 dot
times for memory writes during one DIS CYC period.   The memory cycle
for writes is controled by the Write State Machine which enables the
ras and cas generator U77 during the second 8 dot times of the DIS CYC
signal.

See Write State Machine section 4.5.7.

After every 16 dot times or G CLK's the Word counters are clocked.   At
word 31 (the 32'nd Word) U56 the J-K flip-flop toggles and a binary 21
(for word 21) is preloaded into the word counters U17 and U57.   This
will count to word 31 again for horizontal retrace time which is 11
word times.   A two dot time delay is needed to sync with the analog
sweep frequency. This is implemented by U66 a 4bit shift register. It
delays U76 from counting for two dot times at the end of every line.
Also during retrace the ras and cas for display addressing is inhibited
by U88.1,2 being both low at this time.   At the end of Word 31 of
retrace, U56.5 toggles high and clocks the line counters U37, U47 and
U56 to the next line address.

The signal GBLANK goes active high during retrace and inhibits loading
of the video shift registers.   This is repeated every scan line until
another Start of Frame signal comes again.

4.5.3   Start of Frame

The Start of Frame (SOF) signal is responsible for syncing the graphics
display to the character display of the terminal. It's two main
functions are reseting the display counter when the scan line is at the
top of the screen and to start the graphics video sixteen graphics dot
times before start of character video.   Since the graphics dot time is
2/3 that of the character dot time, 480 graphics dots will occupy 720
character dots on the same line of video.

(720 character dots X 2/3 = 480 graphics dots)

If we have 512 graphics dots per scan line, there will be a 32 graphics
dot overlap on top of the character display.   To symmetrically center
the two, the SOF must tell the display circuitry to start the graphics
video 16 graphics dot times (or one word time) before character data
appears on the screen.   This will leave 16 graphics dots after the
character data has ended making the graphics centered with the
character display.

```
 ----------------------------------------------------------------------
| |     |                                                   |    |    |
| |     |                                                   |    |    |
| |     |                                                   |    |    |
| |     |-----------Character Display----------------------|    |    |
| |     |         (720 dots @ 25.77 MHz)                    |    |    |
| |     |                                                   |    |    |
|-----|-----------Graphics Display------------------------|----|
| |     |         (512 dots @ 17.181 MHz)                   |    |    |
| |     |                                                   |    |    |
| |     |                                                   |    |    |
| |     |                                                   |    |    |
| |     |                                                   |    |    |
| |     |                                                   |    |    |
| |     |                                                   |    |    |
 ----------------------------------------------------------------------
```

The operation of SOF is explained as follows: In both 50 and 60 Hz
operation, Vsync goes active low during vertical retrace and goes
inactive high 6 scan lines before the first line of video (7th line).

Counter U810 is the SOF line counter which is clocked by LRCX, line
rate clock. As NVSYNC goes low line counter U810 preloads 9H into it's
registers.   When 9H preloads on the nexted clock from LRCX, Qd
(U810.11) is set to a 1.   As NVSYNC goes high the P and T inputs to
U810 are enabled by U87.6 going high. The counter then counts the next
6 LRCX clocks which on the 6th a carry wiil appear on U810.15. This is
an enable signal to the character counter U89 and U99.   The character
counters are held off until horizontal retrace time.   This is when
NLRCX is high.   To start the graphics video at the right time, SOFC
(U99.15) must occur two character dot times into the -5 character
position of the first line of video.

Reference figure 13.0 Start of Frame Timing.

After U89 and U99 count 30 character times in retrace on the 30th clock
SOFC (U99.15) goes active. U89 and U99 are clocked by NLCGAX which is
the the character rate clock.   SOFC signal is clocked through to U79.8
as SOF by the SOF CLK (U91.12).   SOF resets not only the display
counters but also the the SOF circuitry itself.   When SOF occurs U810
is asyncronously reseted causing U810.11 low which disables the P and T
inputs of U810.

This disables the carry (U810.15) which disables the T input to U99
which in turn disables the SOFC signal.   This all occurs before the
next SOF CLK so on the preceeding SOF CLK the SOF signal will go
inactive.   The graphics hardware takes 10 graphics dot times to fetch
and load the video shift registers (U19, U29) before the the first
video bit is shifted out.   This puts the graphics video bit 24
character dot times before the first character or 16 graphics dot times
(24 X 2/3 = 16 graphics dot times).

Since each graphics line is syncronous with each character line, SOF
only occur at each frame interval.

4.5.4   Graphics Drawing Modes

There are for drawing modes implimented in the hardware.   They are:

              CLEAR MODE: Writes 0's into memory along
                           the vector path.

                SET MODE: Writes 1's into memory along
                           the vector path.

         COMPLIMENT MODE: Compliments the memory along
                           the vector path.

        JAM-PATTERN MODE: Writes the pattern data into
                           memory along the vector path.

The bits MODE0 and MODE1 from the latch U49 select what mode in which
the vector is to be drawn.   The graphics ram data demultiplexor U510,
selects what is to be written into the graphics ram from what these two
control bits are set to.

MODE1	MODE0	Mode
0	0	CLEAR
0	1	SET
1	0	COMPLIMENT
1	1	JAM-PATTERN

4.5.5   Scaled and Pattern Drawing

The scale register (U59) and pattern register (U48) controls the way
all data is written into graphics memory in all four modes.   In the
first three modes, clear, set and compliment, the pattern register is
used as a write mask by controling the WRITE CONTROL signal with the
pattern data through U58. When it is in jam-pattern mode, the pattern
register is used as the actaul data to be written into the graphics
ram.

The scale register (U59) controls when the data in the pattern register
is clocked out.   A small example on how this works can be shown as
follows:

Let's define, as the Z80A would, a scale of 2, and a pattern of 55H.
Upon writting 55H to port E4 the pattern register, the scale value is
also preloaded into U59. For a scale of 2, a 1110 binary would be
preloaded.

         SCALE = 1's compliment of (scale - 1)

In this example scale = 2-1 = 1, the 1's compliment of 1 in four bits
is 1110B. If it was 4, scale = 4-1 = 3, 1's compliment is 1100B.

The Write State Machine, explained in section 4.5.7, clocks the scale
and pattern registers on every dot memory cycle. With the scale set at
2, and the pattern set with 55H, the first dot written into ram will be
a "1" since in the pattern 55H the first bit is a "1".

             pattern register

         | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |)data shifted
         -- out

The Write State Machine will clock the scale register but not the
pattern register because the carry bit from U59.15 not being set keeps
the pattern register from clocking. Now the carry bit U59.15 is set to
a "1" from the incremented preloaded count of 1110B to 1111B.

On the next dot write the pattern register still has a "1" on the
output and this will be written again into the graphics ram. The scale
register now allows the pattern register to clock to the next data bit
which is a "0". The previous "1" is recirculated back into the last
bit position. At the same time the pattern register is clocked, the
scale is again preloaded back into the scale register U59 and this is
repeated until the vector path drawn is completed.

By having a scale of 2, we delay the shifting of the pattern register
by 2 dot write into memory making the pattern drawn twice per bit
giving the effect of making the pattern twice as large.

Remember this is used both as a write mask and data depending on which
mode you are in.

4.5.6   Display Write State Machine

The primary function of the Write State Machine   (U75) is to execute,
upon receiving a DOT REQ, a write sequence into graphics memory the
correct dot data of the vector that is currently being drawn.   It is
also responsible for the current scale and pattern data of that vector.

Reference figures 9.0 and 11.0.

Upon receiving a DOT REQ from the ALU the Write State Machine, which is
clocked by DIS CYC, clocks the request through on the first negative
edge of DIS CYC.   A this time a display word fetch for screen refresh
is executed and takes up the next 8 graphics dot times.   On the rising
edge of DIS CYC, M DOT goes low (U85.3) since the DOT REQ was clocked
through to U75.5. M DOT is the signal that enables the GNRAS and GNCAS
signals during a memory read-write time   (a memory read-write time is
when the DIS CYC clock is high for 8 graphics dot times) and uses the
ALU adresses to read or write dot imformation of the graphics ram.   M
DOT enable a ram access by allowing U86.3 to be high and enabling U77
to do a GNRAS and GNCAS when the DIS CYC signal is high.

A word access is then done using the dot address of the ALU.   When the
word becomes valid, all 16 bits of that word is latched into to 8 bit
latches U28 and U18 by the signal NALOD.

By latching the word location in which the actual dot address is at we
can now modify it, in the case of compliment mode, by addressing the
actual bit we are looking at.   This is done by using the lower 4 bit of
the ALU X address DBIT0-DBIT3.   Using   a demultiplexor with a
complimented output (U39),   the bit that is to be complimented is
selected and feed back to U510 the graphics ram data demultiplexor as
the complimented data to be written back into the graphics ram at the
same ALU address location on the next memory cycle.

NOTE: This reading and latching of the word at the ALU dot address is
      not necessary for clear, set, or jam-pattern modes since the dot
      data is or has been predefined. The hardware does it anyway.

This complete the first part of two memory cycles that occur for every
DOT REQ form the ALU.

After the memory read cycle is done, DIS CYC goes low and a display
memory word fetch for the next display word on the current scan line is
executed. What also occurs is the clocking of the Write State Machine.
This makes GNWRITE (U75.7) go low which disables the clocking of the
word latches (U18, U28) through U83 and enables the graphics ram write
selector U310.   U610.8 which is low, because DIS CYC is low, will
enable U310 when DIS CYC goes high again for the memory write cycle
time.

When this occurs U310 selects 1 of the 8 write lines to both banks of
graphics ram.   DBIT0-DBIT2 select which one of 8 rams are written to,
and DBIT3 controls which bank of 8 (U110-U117 or U210-U217) gets the
GNRAS and GNCAS strobe signals.   This allows only one bit of the word
address specified by the ALU address to be written too.   The ram data
could have been 0 (clear),   1 (set) complimented (data latched and
complimented through U39.6), or pattern from the pattern shift register
U48.

The negative edge of the current DIS CYC signal will clear the Write
State Machine and leave it idle until another DOT REQ comes.   Also the
pattern register (U48) (if allowed) and the scale counter (59) is
clocked. This sets up the hardware for the next DOT REQ.

The Write State Machine after receiving a DOT REQ executes a read and
write cycle faster than the ALU can calculate a new dot address.
Therefore there is no handshaking with the ALU.

Also occuring at the end of the write cycle is a signal generated from
U77.7 that goes through U83.6 to create a signal called DOT CLR.   This
clears the DOT REQ latch U67.

4.5.7   1's Dot Inhibit

The purpose of this hardware feature is to inhibit the first memory
write of the vector being drawn.   Since the first dot address of the
current vector is the last address written to from the previous vector
makes the first pixel position has already been written.

As an example, if we were in compliment mode, the first bit of every
vector in a chain would be recomplimented. By inhibiting the first dot
write, the first bit in every vector would only be complimented once.

The 1's Dot Inhibit bit is latched from a Z80A port write to U67.
After the Write State Machine (U75) completes the first read and write
cycle the signal DOT CLR is generated.   This clears the 1's Dot Inhibit
latch so the remaining dot writes are not inhibited.

4.5.8   Graphics Raster Dump

The Z80A can indirectly access the graphics memory to retreive video
word imformation to dump to the internal dot printer.   To accomplish
this without disturbing the existing memory we use the 1's Dot Inhibit
feature.

By writing a 1 dot vector to any 16 dots of the word location wanted
and setting the 1's Dot Inhibit on the ALU gives only one DOT REQ at
the specified address but is inhibited by the hardware 1's Dot Inhibit
leaving the graphics memory unchanged.   What we accomplished was to
latch the word in U18 and U28 which can be read back by the Z80A
through port assignments F0 and F1 (hex).

The Z80A reads 15 words in the Y direction and sends 15 bytes of the
word to the printer after buffering the remaining 15 bytes.   Then this
is sent to the printer to be printed.   The X direction is incremented
16 and 15 more words in the Y direction are read.   This is continued
until all display words are read and printed.   This is all done by
writing 1 dot vectors then reading them back from the graphics
hardware.

5.0   Glossary of Signal Names

           This section lists the signal names used on the schematic drawings,
           figures 21.0 to 24.0, along with a brief description of their use.
           Note: an 'N' prefix generally indicates an active low signal,
           otherwise the signal is active high; a 'T' prefix or an 'X' suffix
           indicate that the signal is buffered.

           1.84 MHZ   —   The 1.84 MHz datacomm chip clock

           3.68 MHZ   —   The 3.68 MHz Z80A clock

           60 HZ   —   Sets the video frame rate, low = 50 Hz

           ADD   —   signal used to latched output of adder in the
                                  graphics ALU

           ADDR COUNT   —   enables the word counters in the graphics
                                  display circuitry.
           ALPHA   —   video dot stream after dot stretch

           BATT+ or BATT-   —   connection to the battery + (or -) terminal for CMOS
                                  backup during power off

           BELL   —   output signal to drive the keyboard bell

           BIA 0-3   —   buffered internal ALU address to the
                                  ALU static ram.

           BLANK   —   inhibits the ALPHA dot stream from being
                                  sent to the sweep circuitry

           BLINKRATE   —   alternates at the blinkrate for blinking
                                  character attribute
           CARRY   —   carry bit in the ALU graphics hardware
                                  used for overflow checks

           CE   —   detects presence of loopback hood

           CLRSTMEM   —   clear or set graphics memory by
                                  setting low a write to all graphics
                                  occurs.

           CS   —   clear-to-send from host computer

           CTR CLK   —   A 4.2 MHz clock dirived from dividing
                                  the 17.181 MHz G CLK by 4 to run the
                                  graphics controler

CTS	—	TTL level clear-to-send
CUR	—	cursor output from CRTC
DBIT0-DBIT17	—	ALU addressing bits after being latched
DISBRQ	—	inhibit DMA
DIS CYC	—	A divide by 16 reference from G CLK for display timing purposes
DISD	—	the inverse of the DIS CYC clock
DLOD	—	display load signal to the graphics video shift registers
DOT CLR	—	clears the DOT REQ after a memory cycle of the graphics ram is completed
DOT INH	—	1's dot inhibit signal set in hardware
DOT REQ	—	dot request from the ALU telling the hardware a valid dot address is ready
DISPOFF	—	blank entire display
DM	—	detect modem connection
DRCX	—	dot rate clock
DSR	—	TTL level detect modem connection
EN0-EN7	—	enhancement data bits from line buffer
ENHOFF	—	inhibit enhancements
ENNMI	—	clock for NMI mask latch
EOL	—	graphics end of line
FLAG	—	signal to reset graphics controler
GBLANK	—	graphics horizontal blank signal
G CLK	—	17.181 MHz graphics dot clock
GMUX	—	select signal to change from row to column address of the graphics ram
GNCAS	—	graphics column address strobe

GNRAS   —   graphics row address strobe

GNWRITE   —   graphics clock for scale and pattern
                   registers

GVIDEO   —   graphics serial video data

GWRITE   —   pre-enables the graphics write decoder

HBLANK   —   horizontal blank signal

ICH   —   TTL level detect datacomm test hood

ID0-ID7   —   interal data bus for graphics subsystem

INVERSE   —   select inverse video attribute

JUMP   —   ALU hardware signal for a jump instruc-
                   tion to another address location

KEY0-KEY6   —   keyboard row/column scan outputs

LBCDEL   —   delayed line buffer clock

LBCX   —   line buffer clock

LCGADEL   —   delayed latch character generator address

LCGAX   —   latch character generator address

LD0-LD7   —   latched graphics video data

LOAD C   —   data for graphics word counters

LVSRX   —   load video shift register

MD0-MD7   —   RAM data outputs

MEM0-MEM6   —   graphics ram address lines

MODE0-MODE1   —   graphics mode select bits
MUX   —   selects between row and cloumn address
                   for dynamic RAM

NBLINK   —   select blink attribute

NBUSREQ   —   request bus control for DMA

NCAS   —   column address strobe for RAM

NCMOSREQ   — enable CMOS for read/write

NCUR   — one line cursor signal

NDCLK   — two graphics dot clock delay signal

NURSOR   — cursor active without underline

NENNMI   — select NMI latch

NEOLDEL   — end-of-line signal

NFULLBRT   — normal intensity video output

NHALFBRT   — half-intensity video output

NHSYNC   — horizontal synchronization

NINT   — datacomm interrupt

NIOG   — I/O enable for the graphics subsystem

NKEYACT   — key active (depressed) on keyboard

NKEYDISP   — select (clock) keyboard/display latch

NKEYSTAT   — enable keystatus port

NLRCX   — line rate clock

NLSB   — graphics port decode to write into
                   the LSB of the ALU static ram

NM1   — opcode fetch machine cycle

NMODEM   — select (clock) modem/display latch

NMSN   — graphics port decode to write into
                   the MSN of the ALU static ram

NMUX   — clock RAM output latch

NNMI   — non-maskable interrupt (video)

NPFAIL   — power fail signal from power supply

NPRINTER	—	printer select signal
NRAS	—	row address strobe for dynamic RAMs
NRESETA	—	power-on reset, driver A
NRESETB	—	power-on reset, driver B
NRVD	—	graphics port decode for reading of graphics video data
NSELDC	—	datacomm port select
NSF	—	graphics port decode to set flags
NSP	—	graphics port decode for scale preset
NSR	—	graphics port decode for status read
NSYSSTAT	—	system status port select
OCD1	—	optional control driver 1, datacomm
OCR1	—	optional control receiver 1, datacomm
PAT INH	—	inhibit the pattern register in graphics
PINT	—	printer interrupt status
PULLUP	—	common pullup resistor
RD	—	receive data, datacomm
RECIRC	—	line buffer recirculate enable
RESET	—	printer reset signal
RETRACE LOAD	—	loads signal for graphics word display
ROR0-ROR15	—	graphics controler address lines
RS	—	request to send, datacomm
S0-S11	—	ALU added data
SCL0-SCL3	—	scale bits for the graphics hardware
SD	—	send data, datacomm
SELDC	—	datacomm chip select

SIGN	–	ALU signal to check sign of the addition
SG	–	signal ground, datacomm
SHIELD	–	shield (earth) ground, datacomm
SMEM0-SMEM5	–	ROM0-ROM5 chip enable
SOF	–	graphics start of frame
SOFC	–	carry bit that initates SOF
STORE X	–	graphics instruction to store the X address
STORE Y	–	graphics instruction to store the Y address
TA0-TA15	–	address bits 0-15
TBUSAK	–	bus acknowledge, Z80A tristate
TD0-TD7	–	buffered data bus
TNBUSAK	–	active low bus acknowledge
TNMREQ	–	Z80A memory request
TNRD	–	memory or I/O read select
TNRFSH	–	dynamic RAM refresh active
TNWR	–	memory or I/O write select
TR	–	terminal ready, datacomm
ULINE	–	select underline attribute
ULTIME	–	active on scan line 13, indicates scan line for underline or cursor display
VBLANK	–	vertical blank signal
VSYNC	–	vertical synchronization signal
WRITE CONTROL	–	enables write decoder of the graphics ram
WRITE ENABLE	–	enable the write decoder to the graphics ram
X0-X7	–	character code address to character ROM
ZBLANK	–	hardware flag set by the Z80A to stop graphics video from being displayed
ZD0-ZD7	–	Z80A data bus
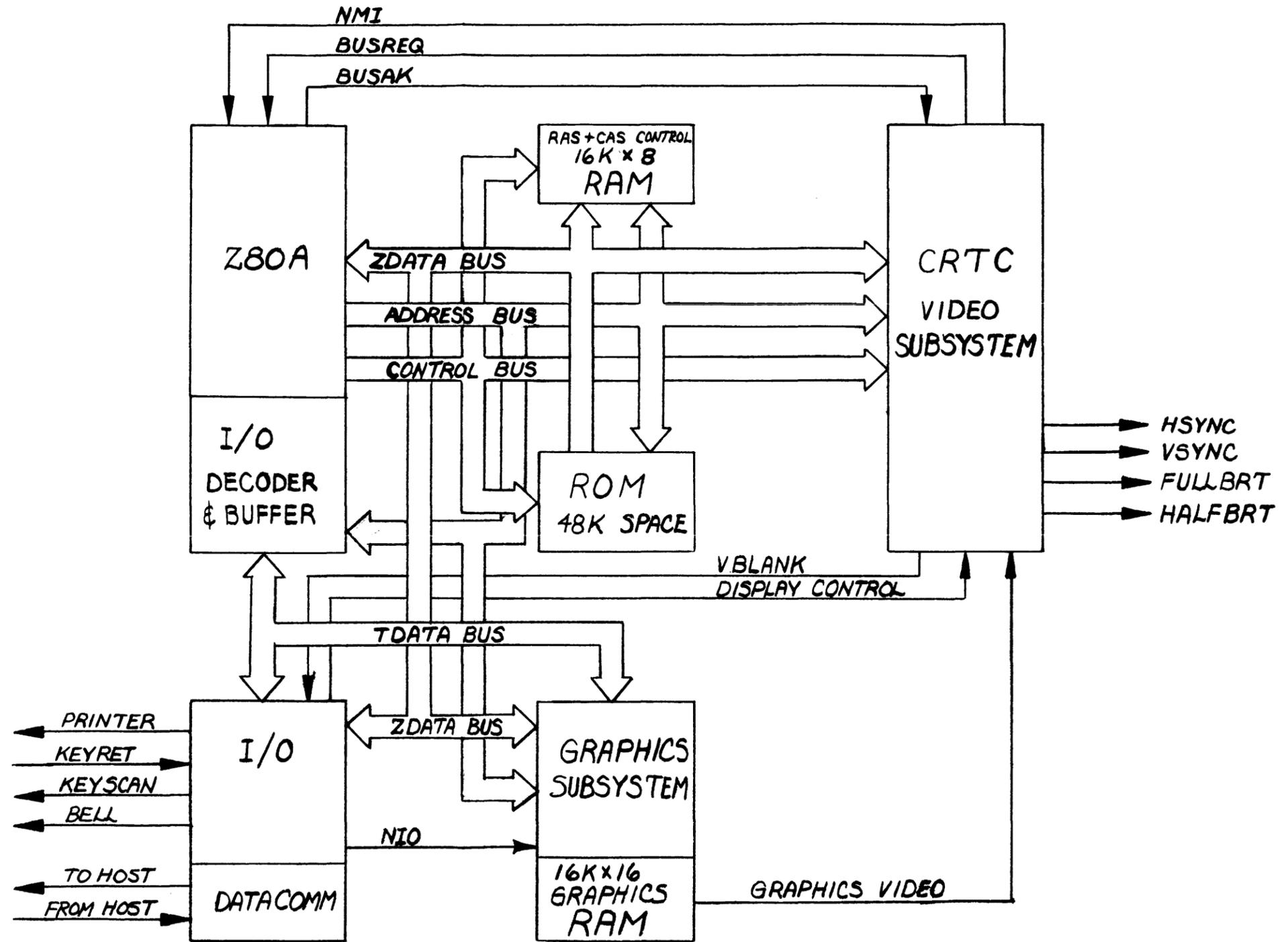
FIGURE 1.0   PROCESSOR BLOCK DIAGRAM
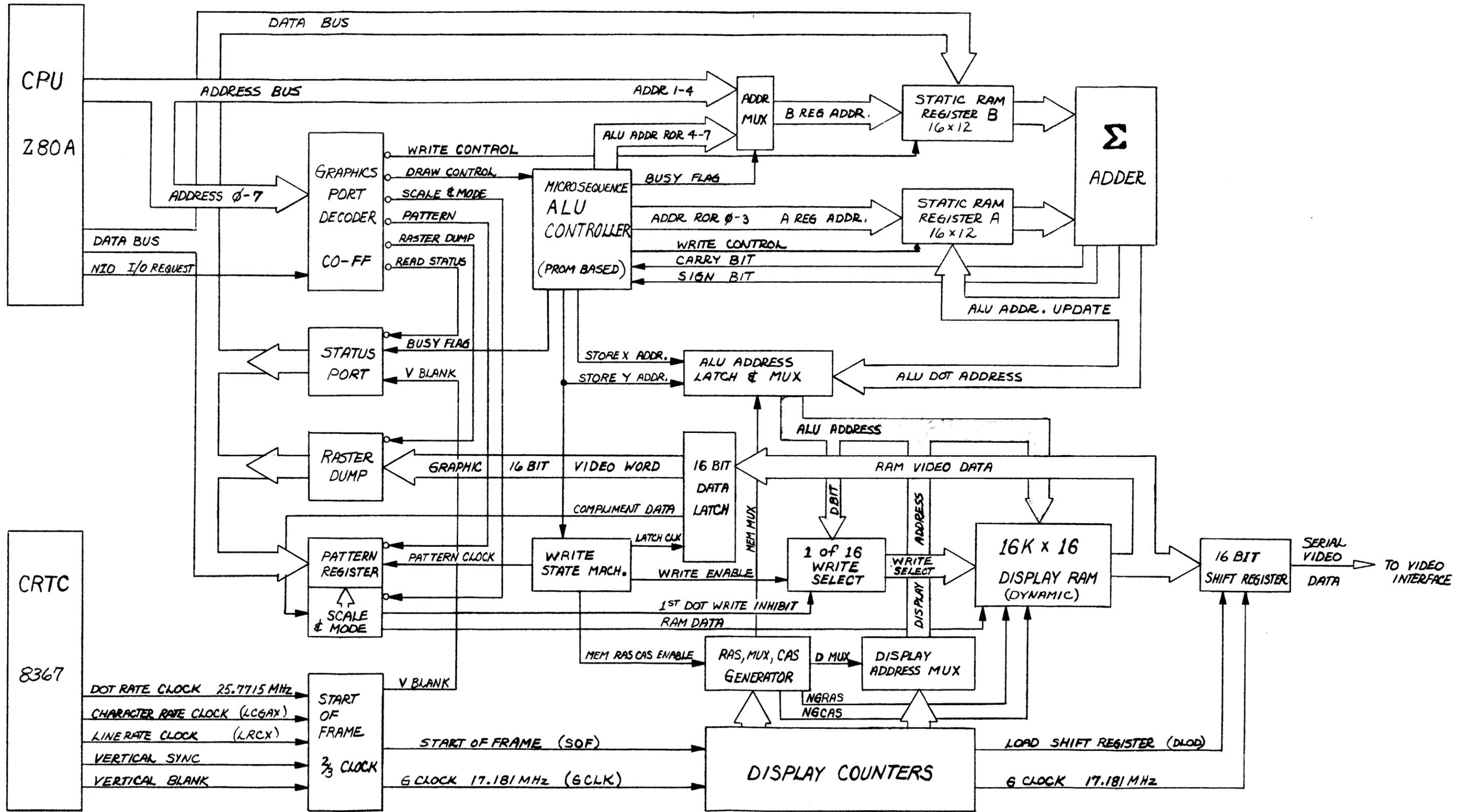
FIGURE 2.0 GRAPHICS SUBSYSTEM BLOCK DIAGRAM

Figure 2
Graphics Block Diagram
AUG-14-81   13220-91088
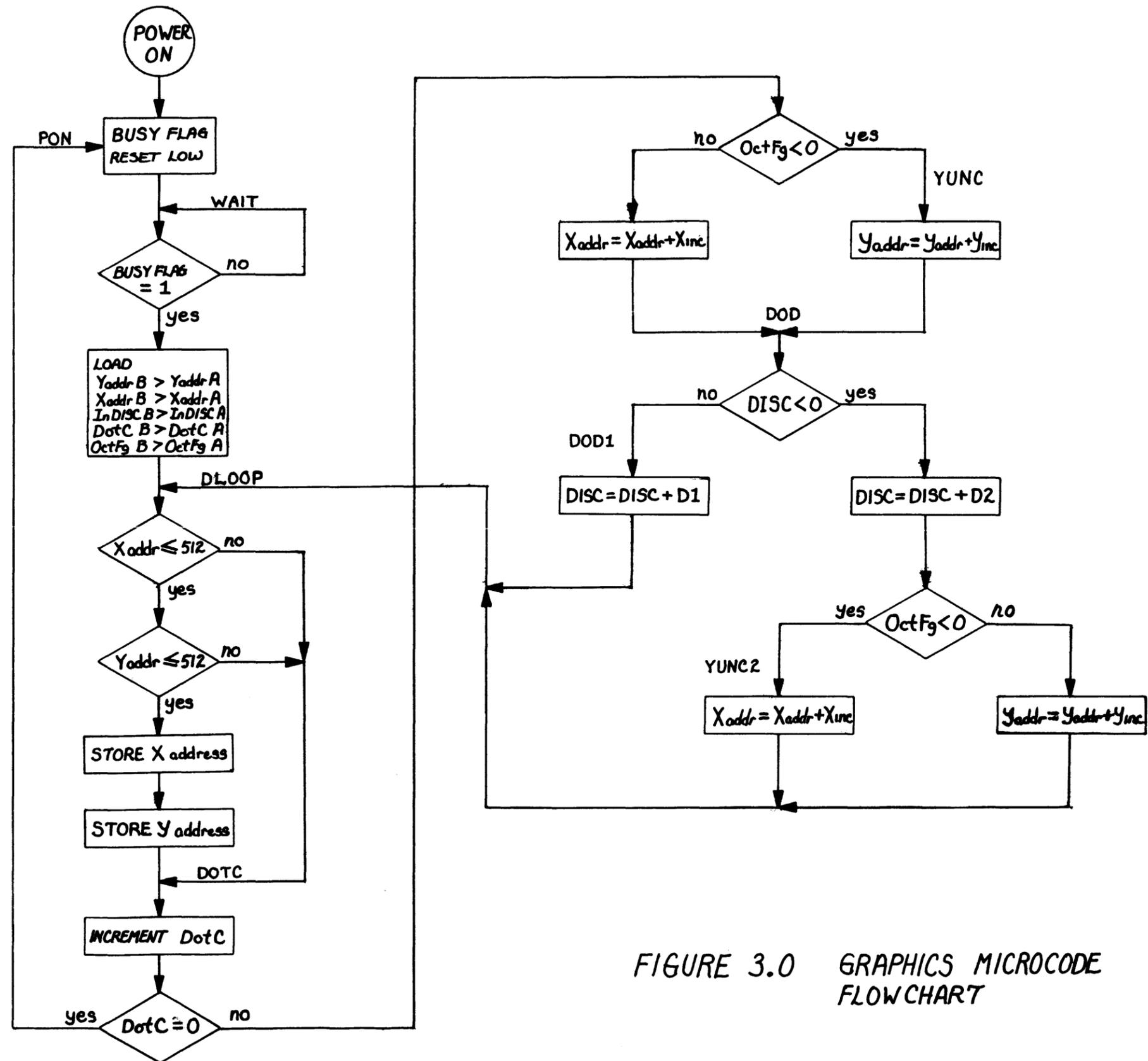
FIGURE 3.0   GRAPHICS MICROCODE
            FLOW CHART

FIGURE 4.0   Z80A I/O TIMING

* AUTOMATICALLY INSERTED WAIT STATE
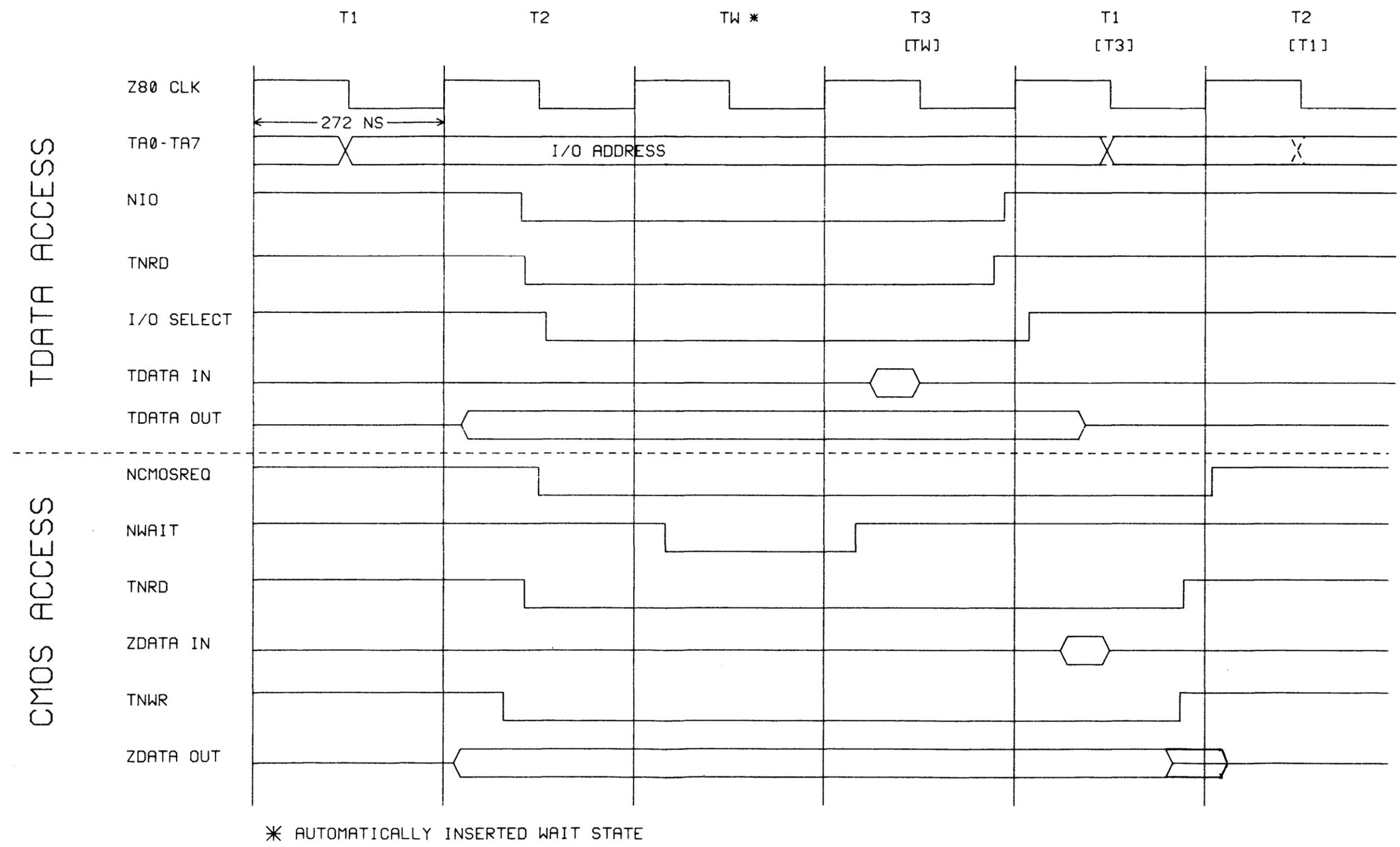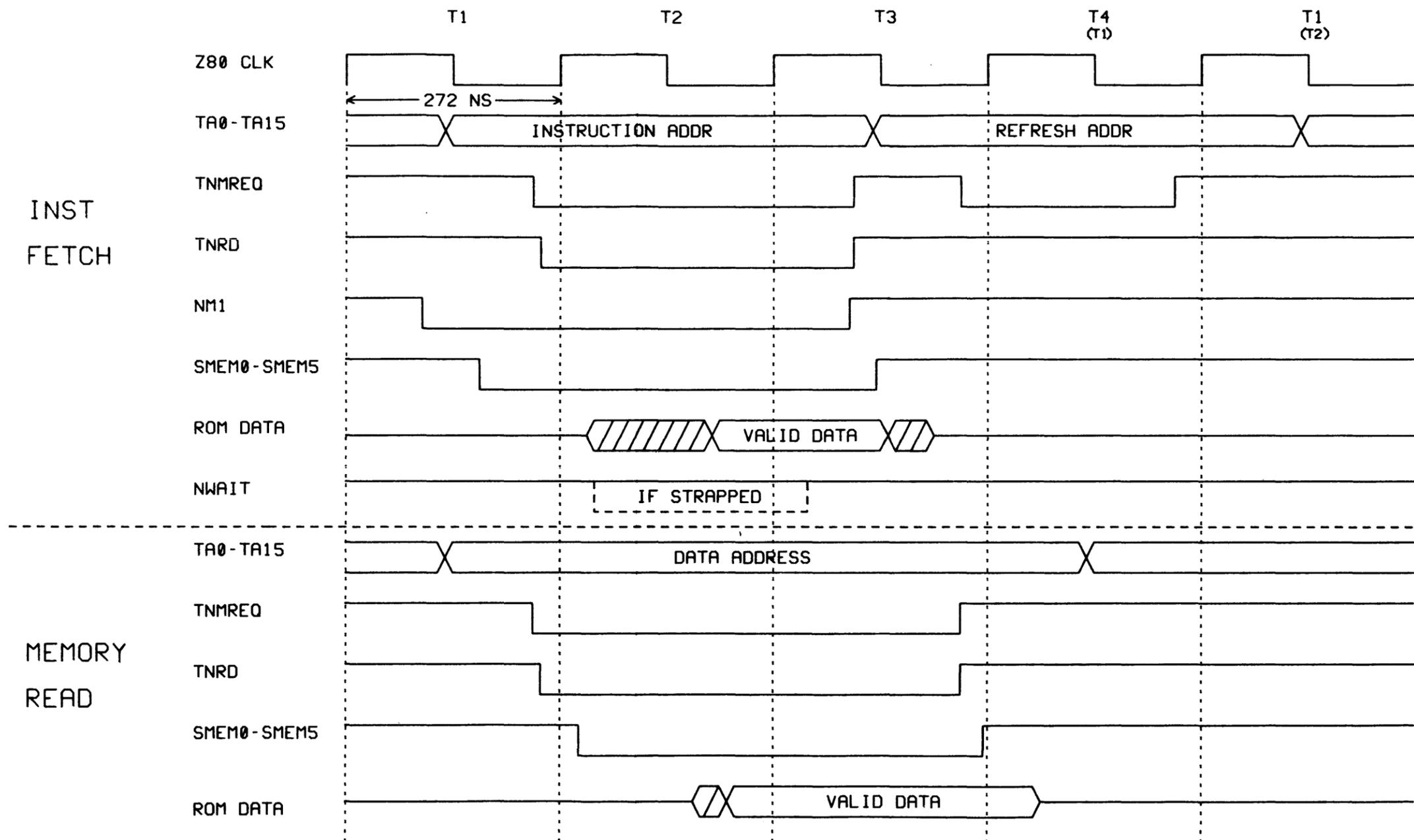
FIGURE 5.0 Z80A ROM TIMING
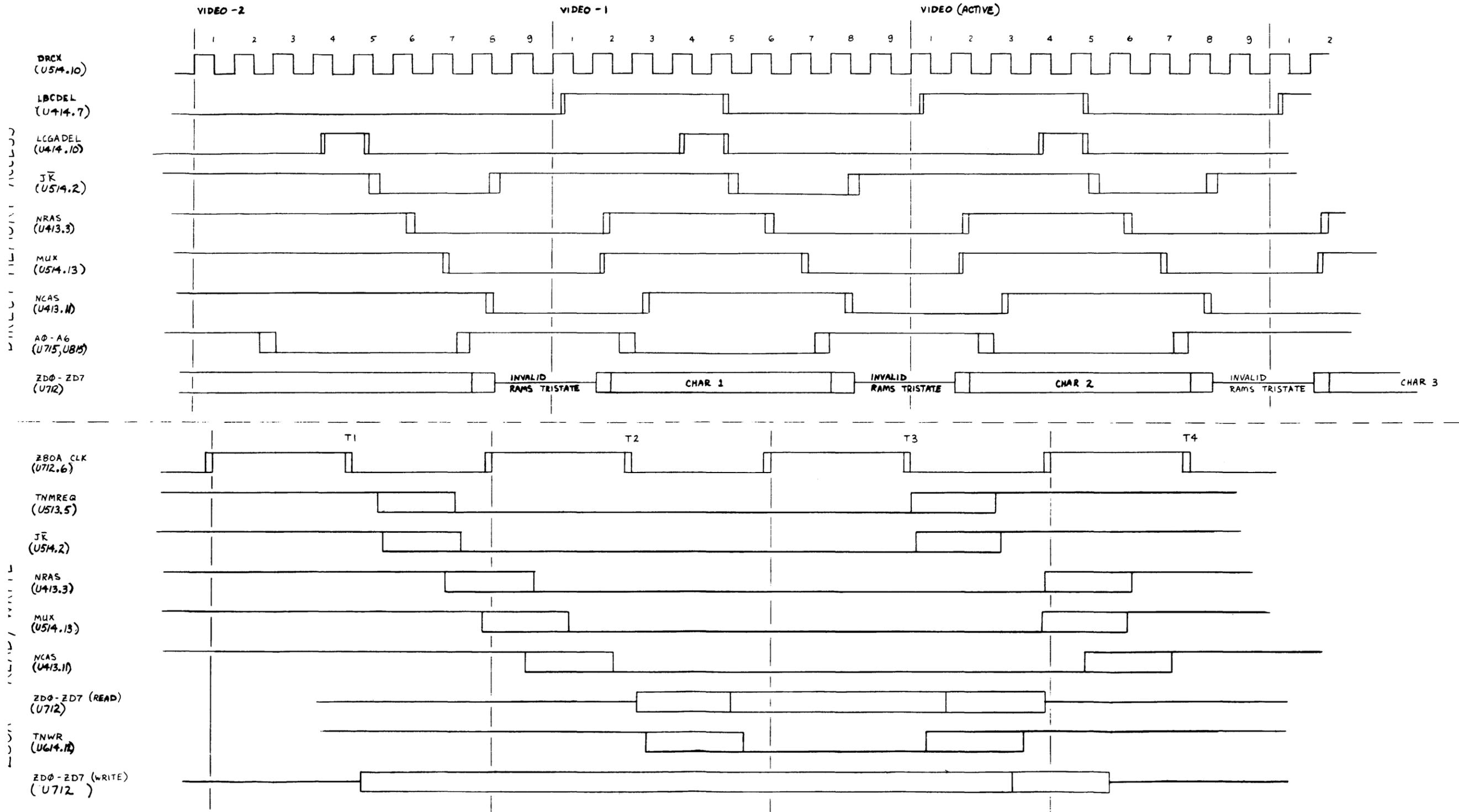
FIGURE 6.0 RAM TIMING
(ALPHA)

Figure 6
RAM Timing Diagram
AUG-14-81   13220-91088
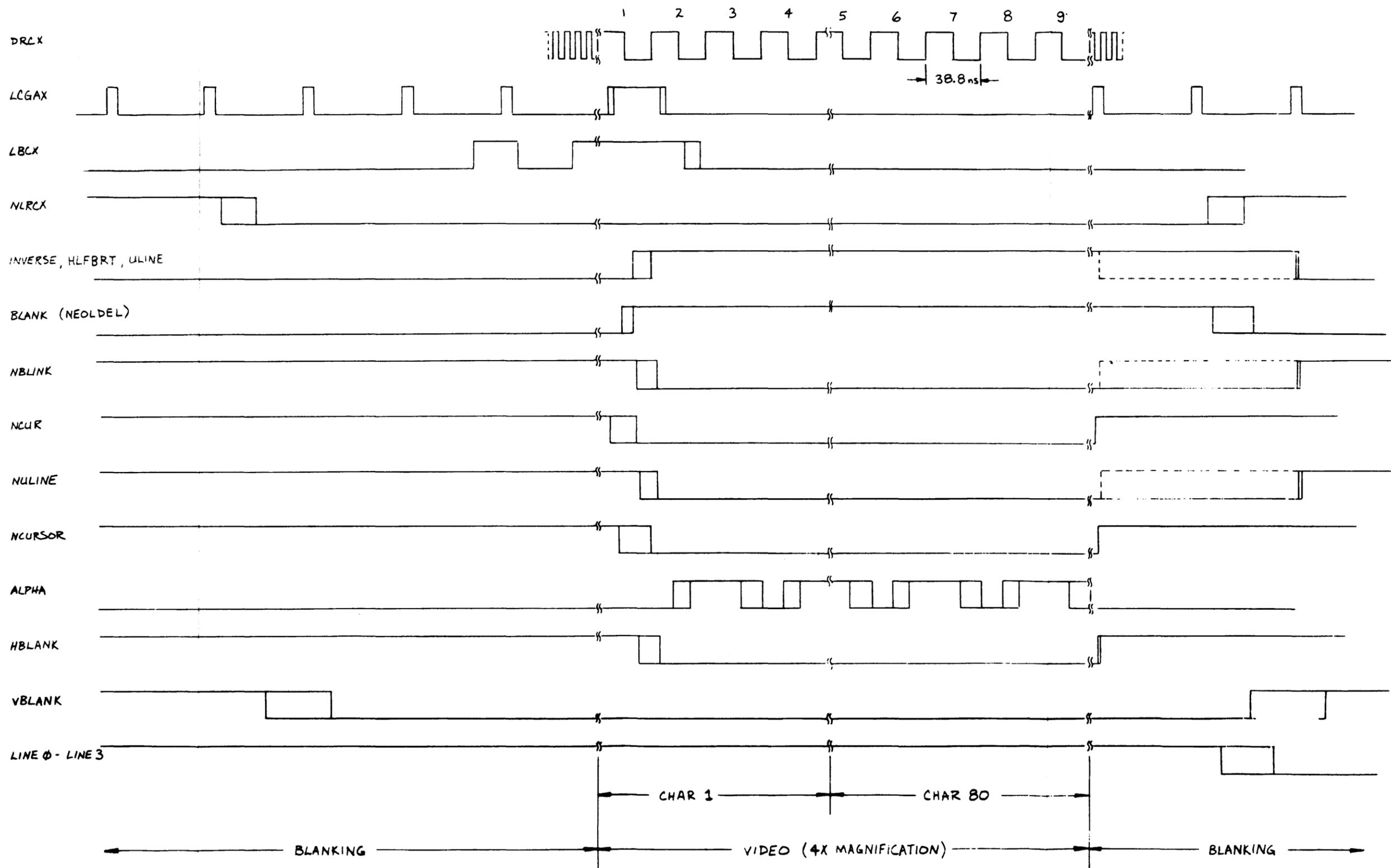
FIGURE 7.0 VIDEO LINE RATE
TIMING (ALPHA)

Figure 7
Video Line Rate Timing Diagram
AUG-14-81   13220-91088
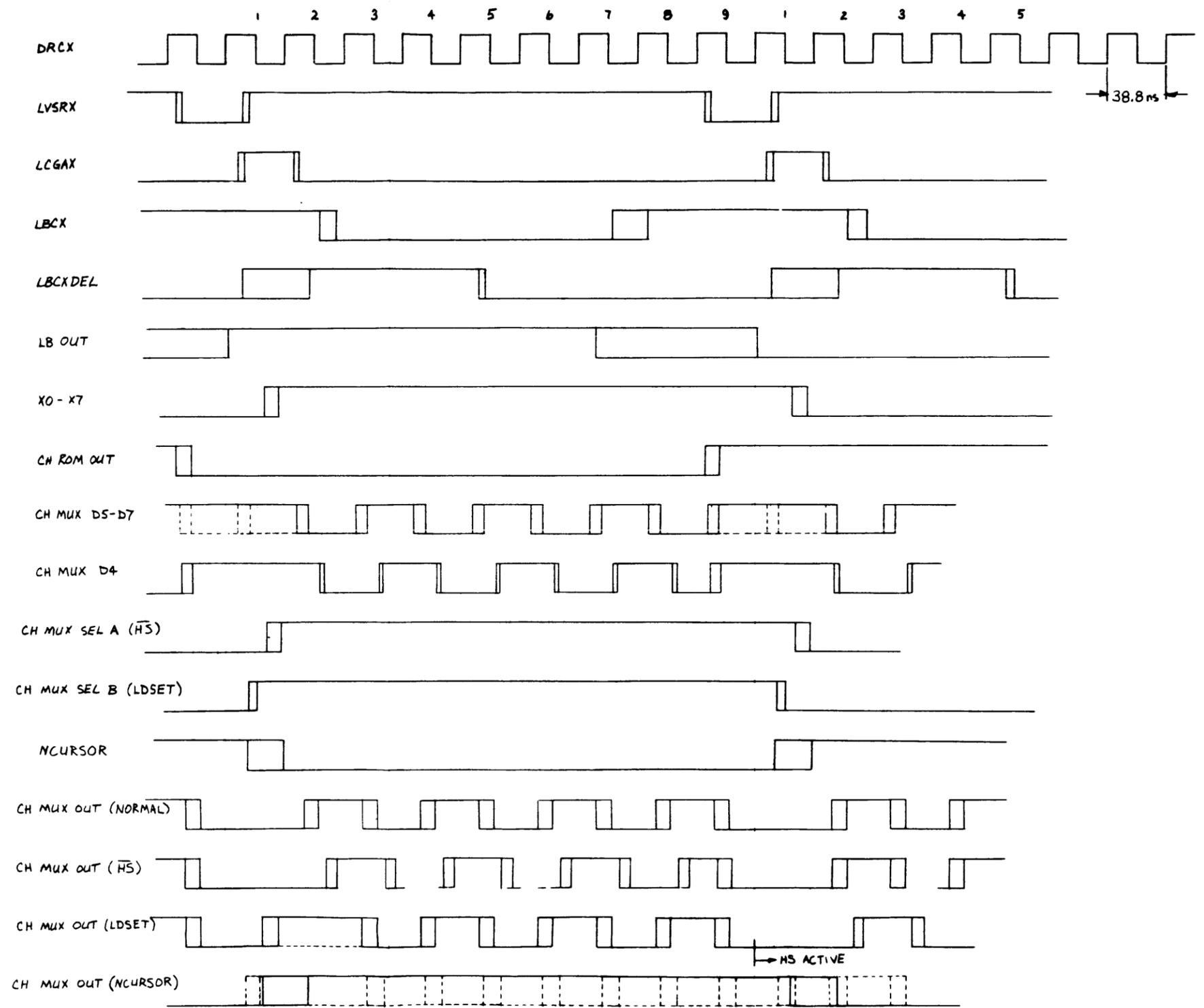
FIGURE 8.0 VIDEO CHARACTER TIMING
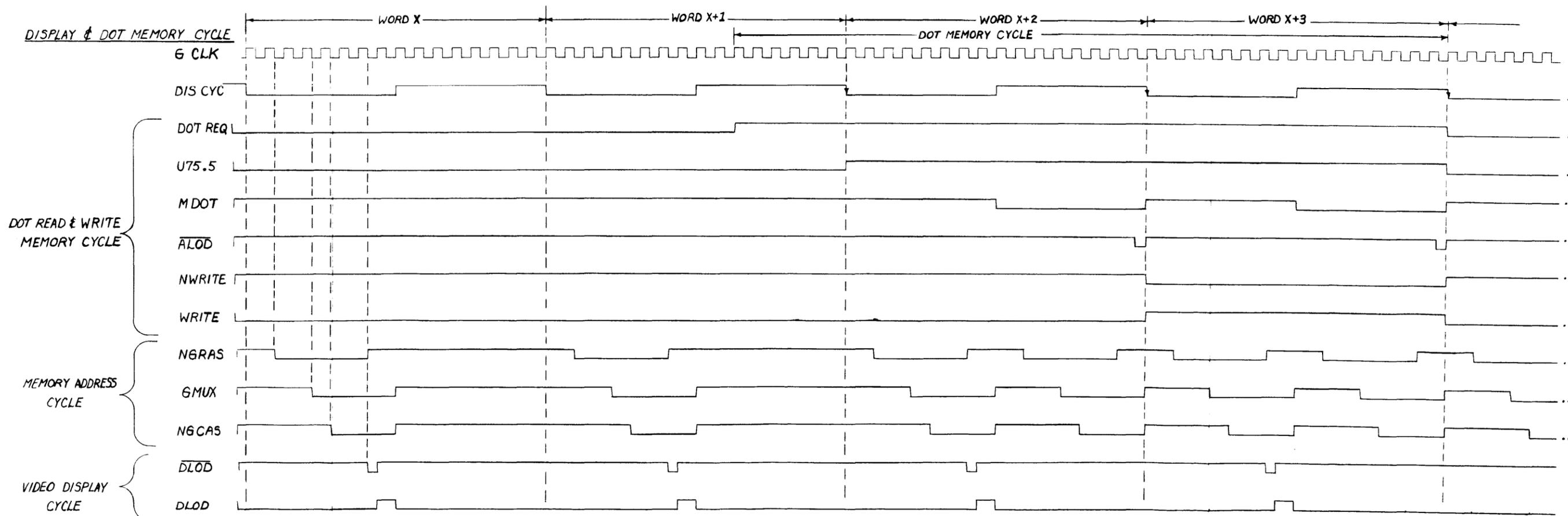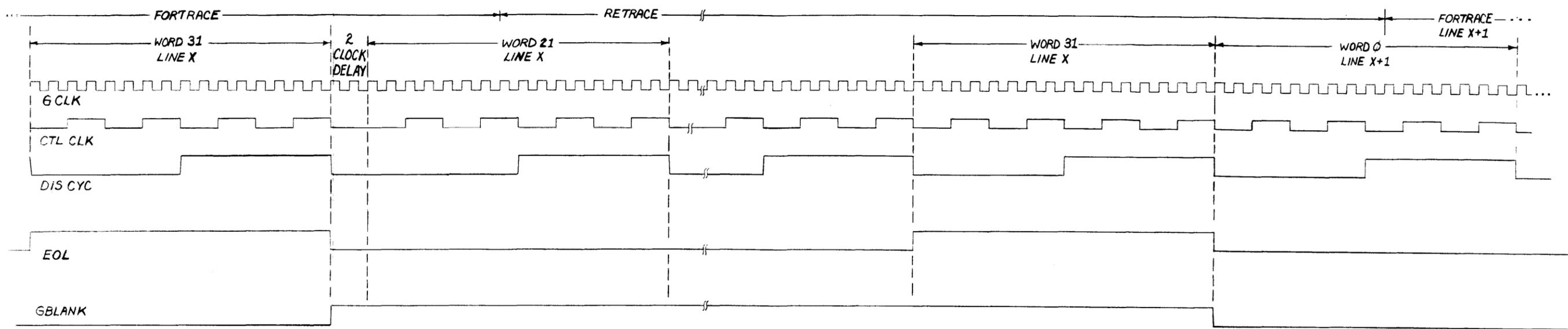
FIGURE 9.0 GRAPHICS MAJOR TIMING

Figure 9
Graphics Major Timing Diagram
AUG-14-81   13220-91088
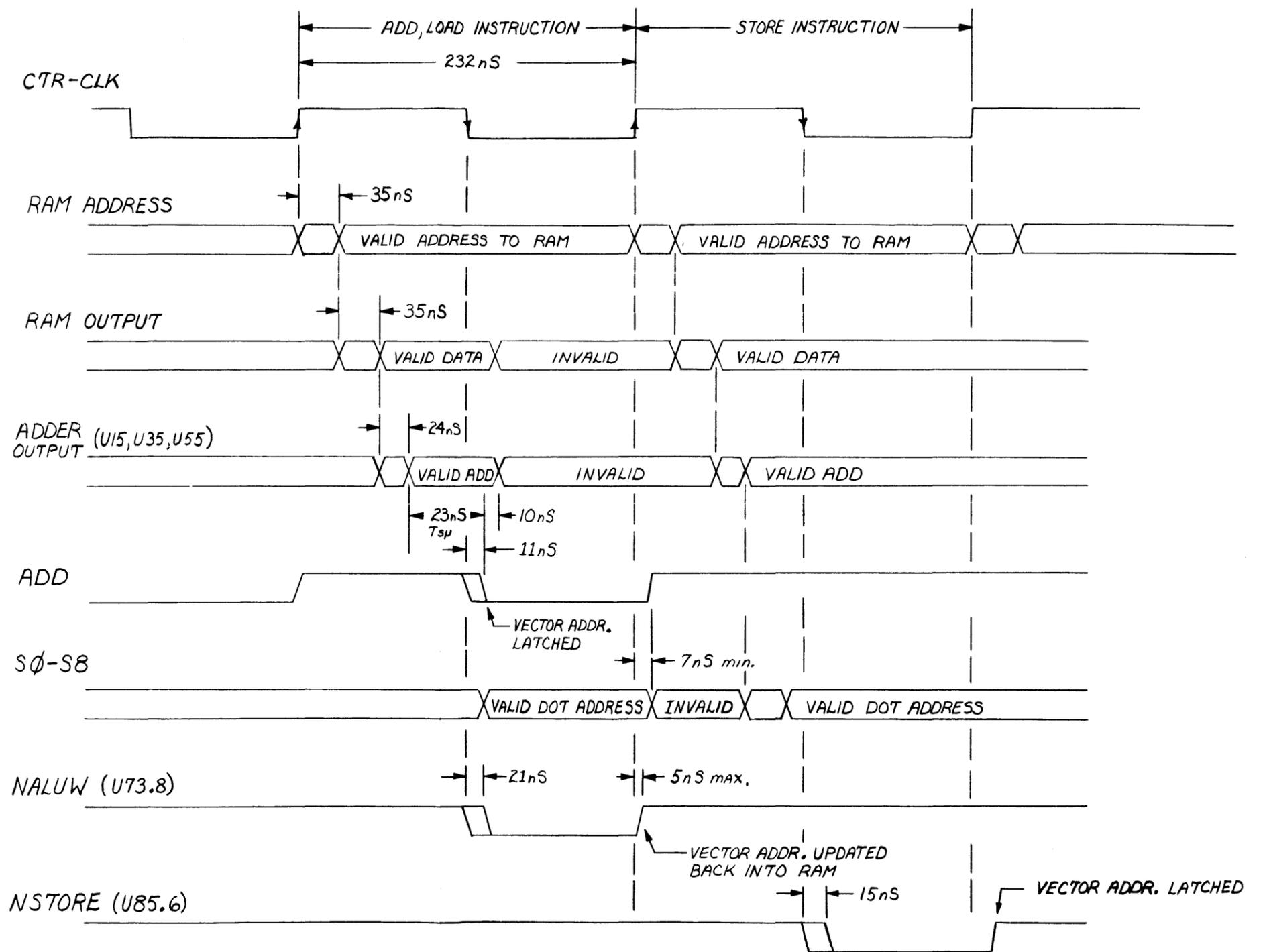
FIGURE 10.0 GRAPHICS ALU TIMING
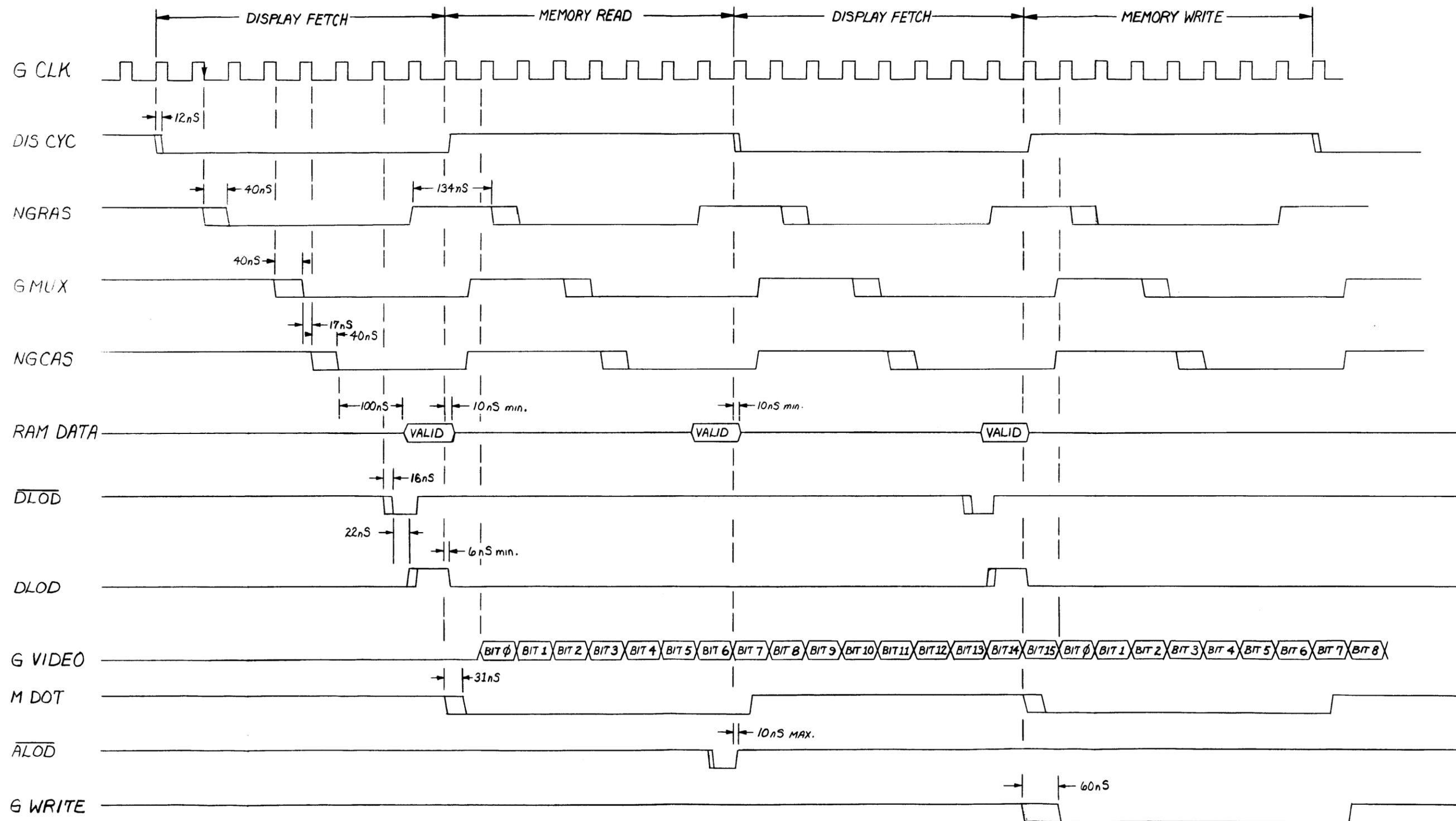
FIGURE 11.0 GRAPHICS VIDEO DISPLAY AND MEMORY WRITE TIMING

Figure 11
Graphics Display and Memory Timing
AUG-14-81   13220-91088

GRAPHICS DOT SYNCHRONIZATION

DOT RATE
DRCX

15nS

NLCGAX
(U98.13)

4.4nS
Set up
to U89

U97.14   UNKNOWN

U97.11   UNKNOWN

14nS

U89.6

U87.8 (DRCX·U89.6)

U98.1 ($\overline{U97.11 + DRCX}$)

19.4nS   38.8nS

G CLK
U88.6 (U87.8 + U98.1)

FIGURE 12.0   GRAPHICS DOT SYNCRONIZATION TIMING
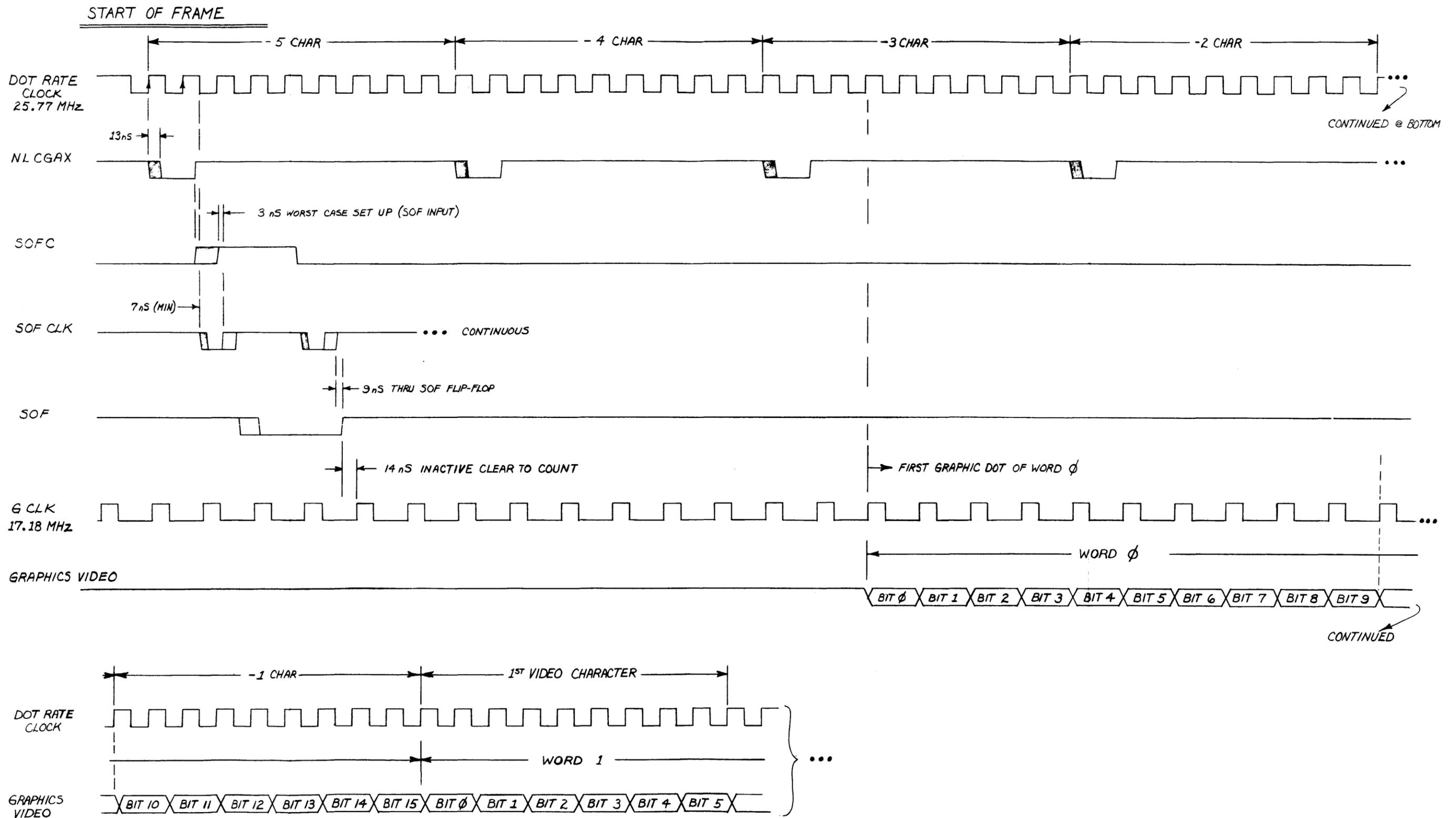
START OF FRAME

FIGURE 13.0 START OF FRAME FOR GRAPHICS VIDEO TIMING
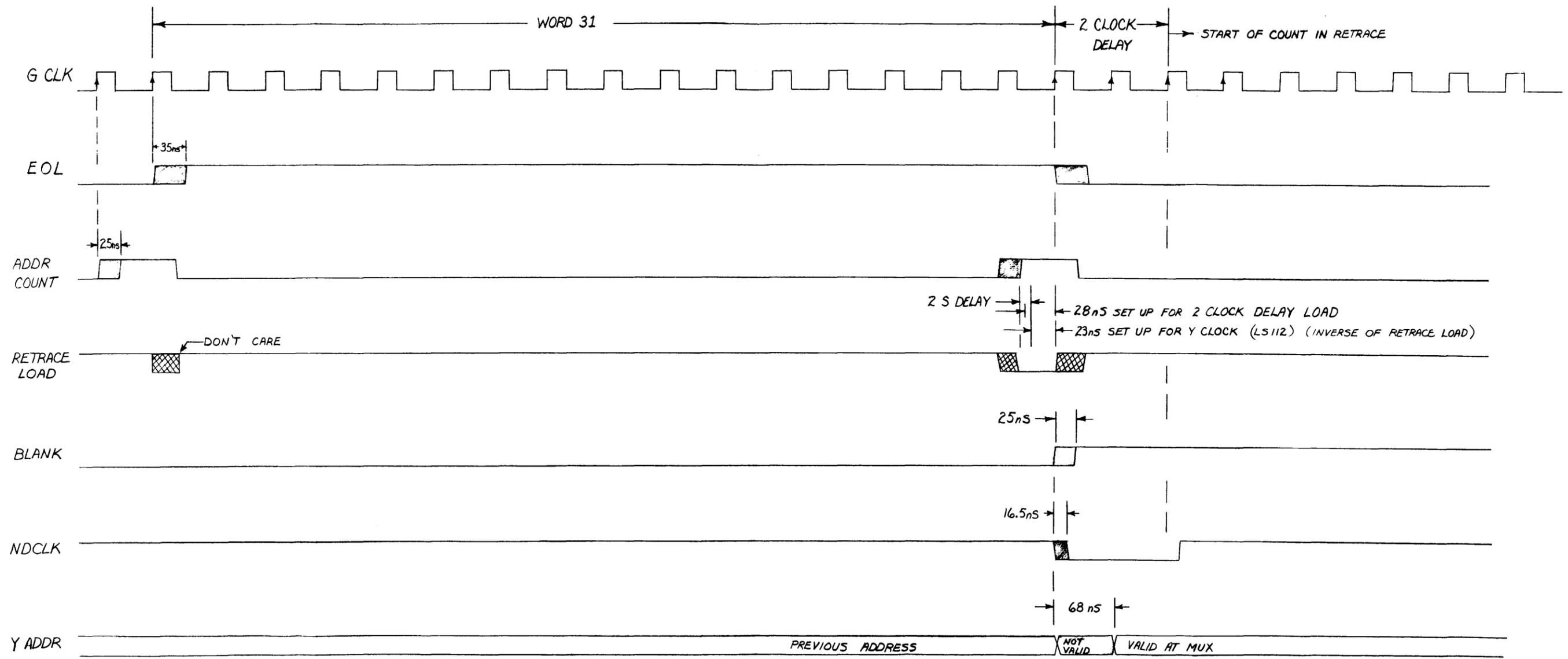
FIGURE 14.0   GRAPHICS END OF LINE TIMING

DISTANCE BETWEEN TARGET
REGISTRATION HOLES 393.7±.076 MM
15.500±.003
INCHES
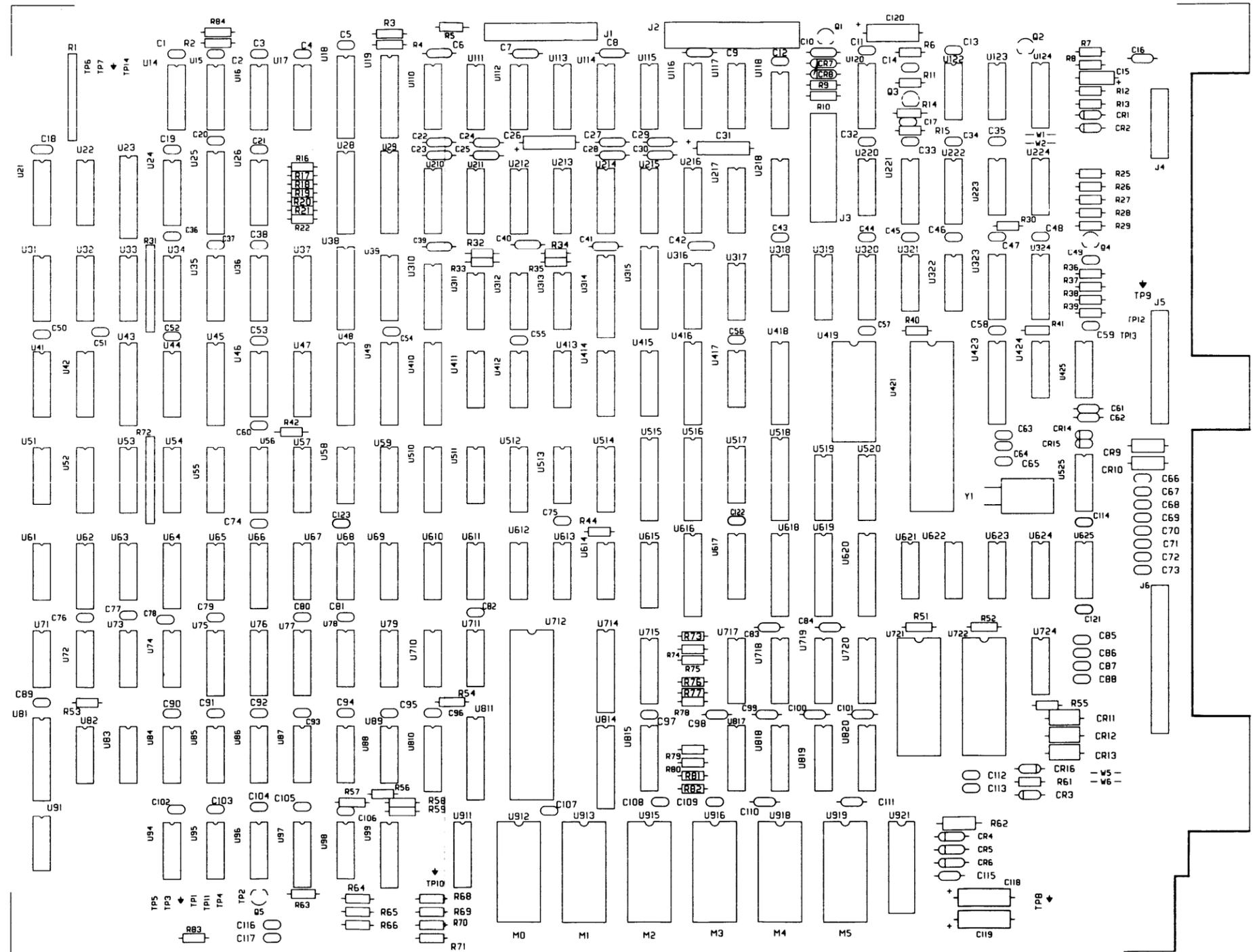
FIGURE 15.0   COMPONENT LAYOUT

SILKSCREEN

02620-80088

10-22-81

HEWLETT PACKARD
LAYER 12
AZT-OSM
7-6-81

Figure 15
Component Layout Sheet
AUG-14-81   13220-91088

Figure 16
Z80 and Ports Schematic
AUG-14-81   13220-91088
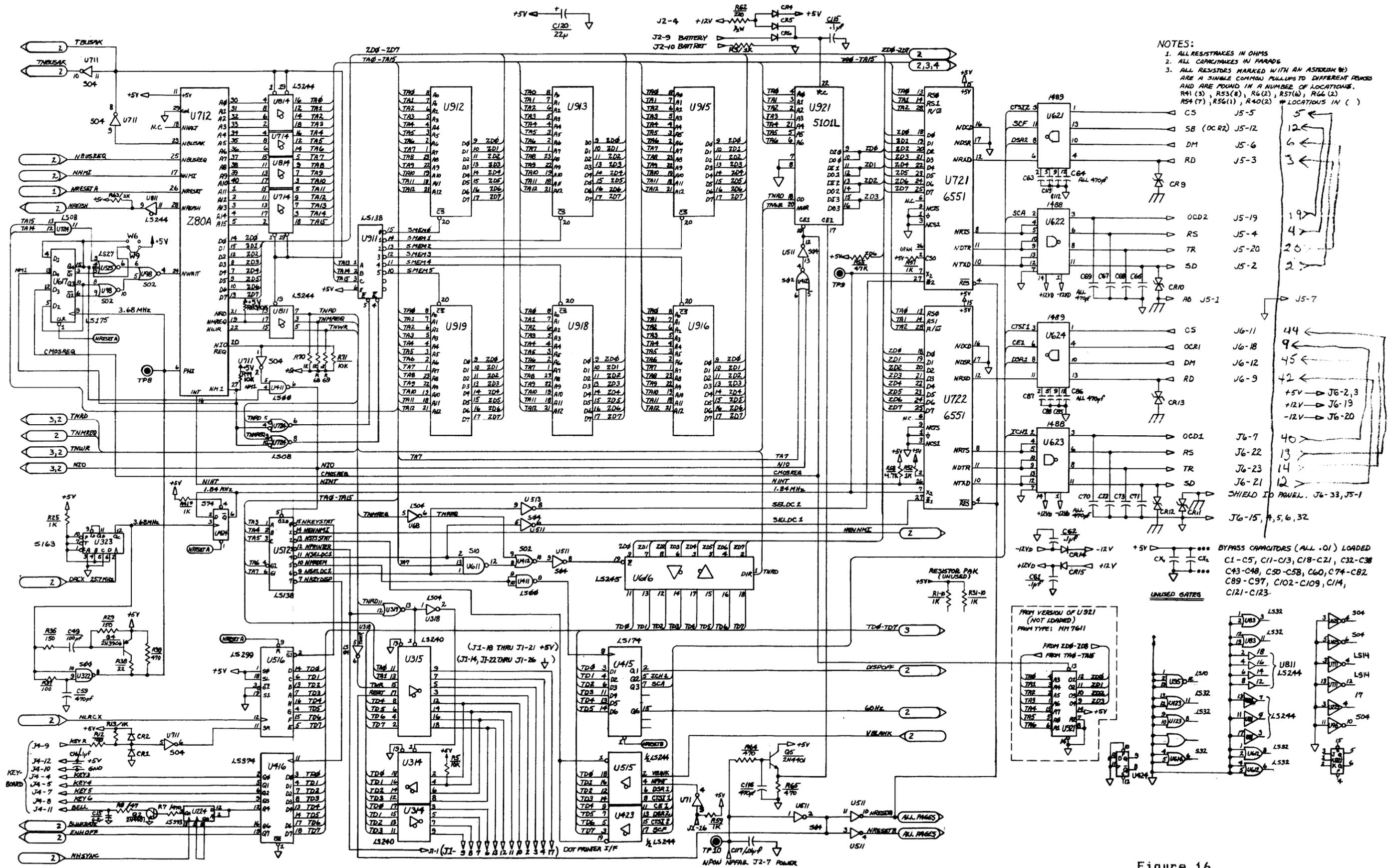
NOTES:
1. ALL RESISTANCES IN OHMS
2. ALL CAPACITANCES IN FARADS
3. ALL RESISTORS MARKED WITH AN ASTERISK (*) ARE A SINGLE COMMON PULLUPS TO DIFFERENT POWERS AND ARE FOUND IN A NUMBER OF LOCATIONS. R41 (5), R53 (8), R6 (2), R57 (6), R66 (2), R54 (7), R56 (1), R40 (2) # LOCATIONS IN ( )
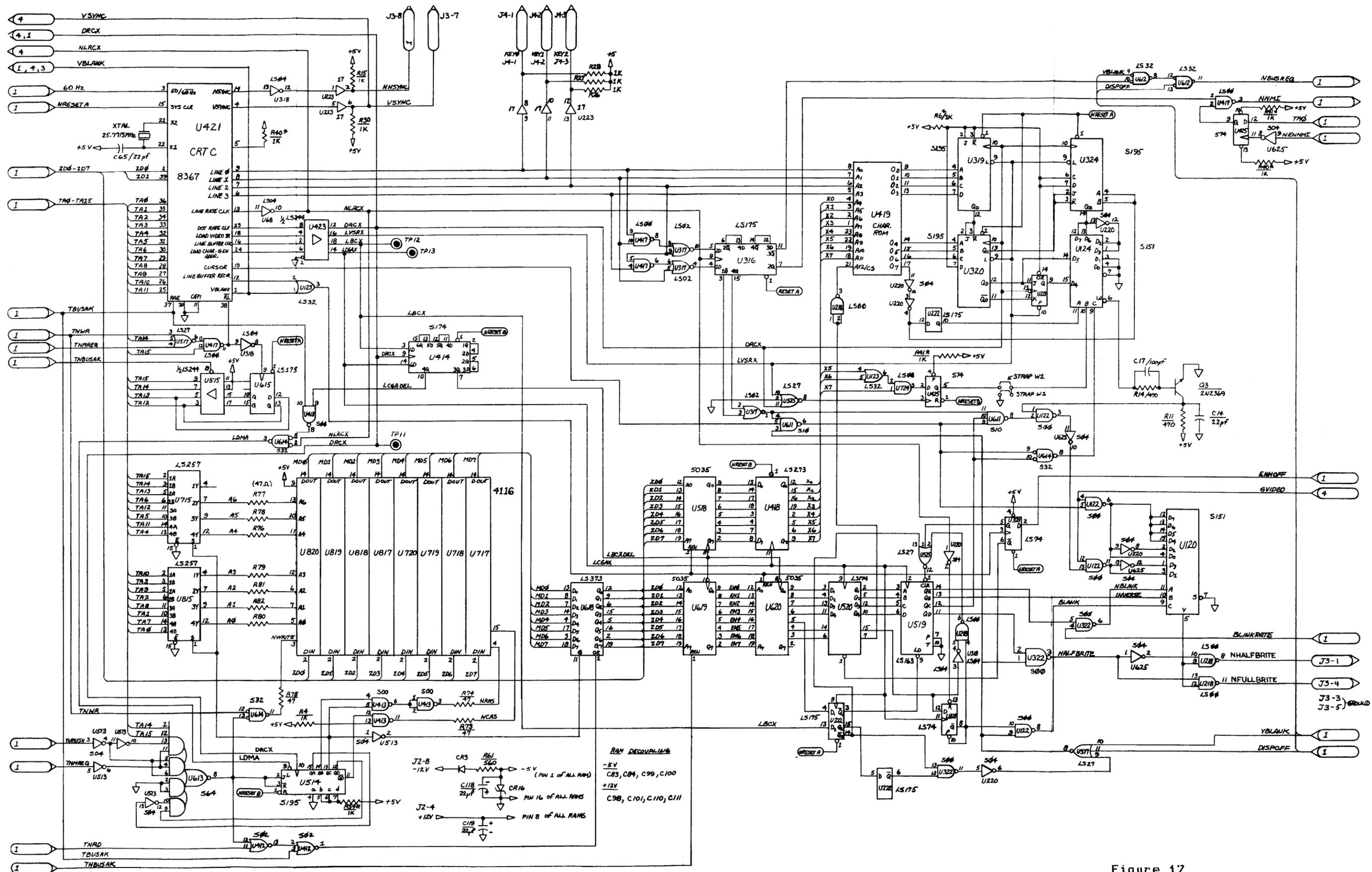
Figure 17
Video and Display Memory Schematic
AUG-14-81   13220-91088

Figure 18
Vector Graphics ALU Schematic
AUG-14-81   13220-91088
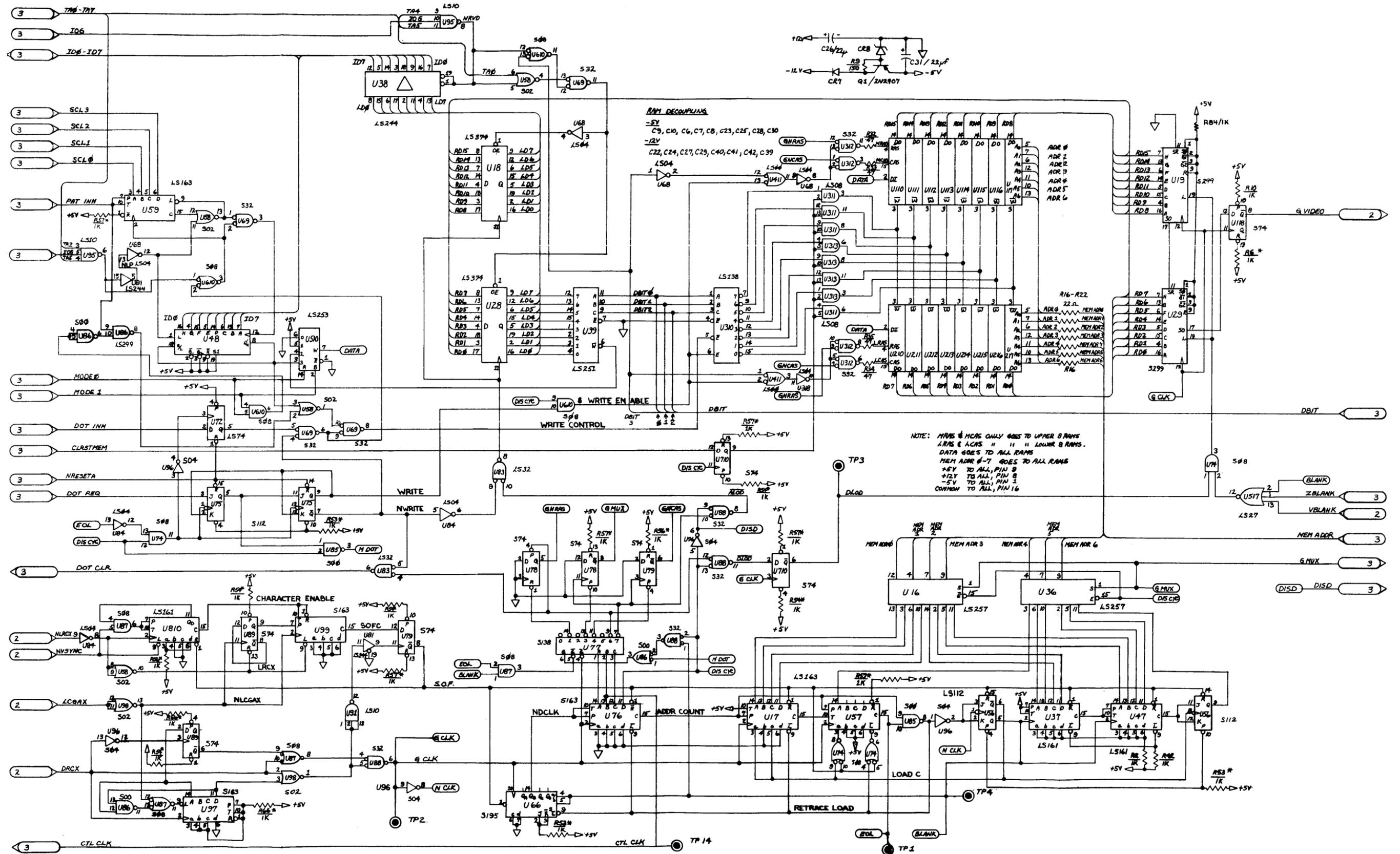
Figure 19
Vector Graphics Display Schematic
AUG-14-81   13220-91088

Replaceable Parts

| Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02620-60088	0	1	PROCESSOR-PCA 2623A	28480	02620-60088
C1	0160-4554	7	66	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C2	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C4	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C5	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C6	0160-4557	0	29	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C7	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C8	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C9	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C10	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C12	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C14	0160-4787	8	2	CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30	28480	0160-4787
C15	0180-1701	2	1	CAPACITOR-FXD 6.8UF+-20% 6VDC TA	56289	150D685X0006A2
C16	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C17	0160-4801	7	2	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C19	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C22	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C23	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C24	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C25	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C26	0180-2879	7	5	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C27	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C28	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C29	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C30	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C31	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C32	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C33	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C34	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C35	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C36	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C37	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C38	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C39	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C40	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C41	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C42	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C43	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C44	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C45	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C46	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C47	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C48	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C49	0160-4801	7		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C50	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C51	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C52	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C53	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C54	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C55	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C56	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C57	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C58	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C59	0160-3335	0	18	CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C60	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C61	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C62	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C63	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C64	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C65	0160-4787	8		CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30	28480	0160-4787
C66	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C67	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C68	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C69	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C70	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
C71	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C72	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C73	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C74	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C75	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C76	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C77	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C78	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C79	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C80	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C81	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C82	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C83	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C84	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C85	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C86	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C87	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C88	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C89	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C90	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C91	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C92	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C93	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C94	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C95	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C96	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C97	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C98	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C99	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C100	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C101	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C102	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C103	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C104	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C105	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C106	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C107	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C108	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C109	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C110	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C111	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C112	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C113	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C114	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C115	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C116	0160-3335	0		CAPACITOR-FXD 470PF +-10% 100VDC CER	28480	0160-3335
C117	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C118	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C119	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C120	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C121	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C122	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C123	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
CR1	1901-0050	3	9	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR8	1902-0952	6	1	DIODE-ZNR 5.6V 5% DO-35 PD=.4W TC=+.046%	28480	1902-0952
CR9	1902-0976	4	5	DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR10	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR11	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR12	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR13	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR14	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR15	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR16	1902-0041	4	1	DIODE-ZNR 5.11V 5% DO-35 PD=.4W	28480	1902-0041
J1	1251-5500	9	2	CONNECTOR 26-PIN M POST TYPE	28480	1251-5500
J2	1251-5521	4	1	CONNECTOR 9-PIN M POST TYPE	28480	1251-5521
J3	1251-5520	3	1	CONNECTOR 7-PIN M POST TYPE	28480	1251-5520
J4	1251-5499	5	1	CONNECTOR 16-PIN M POST TYPE	28480	1251-5499
J5	1251-5500	9		CONNECTOR 26-PIN M POST TYPE	28480	1251-5500

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
J6	1251-5546	3	1	CONNECTOR 34-PIN M POST TYPE	28480	1251-5546
Q1	1853-0281	9	1	TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
Q2	1854-0467	5	2	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q3	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q4	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
Q5	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
R1	1810-0275	1	3	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R2	0683-1025	9	28	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R3	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R4	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R5	0683-1035	1	4	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R6	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R7	0683-4715	0	6	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R8	0683-4705	8	15	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R9	0683-1515	2	3	RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R10	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R11	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R12	0683-1015	7	2	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R13	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R14	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R15	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R16	0683-2205	9	8	RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R17	0683-2205	9		RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R18	0683-2205	9		RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R19	0683-2205	9		RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R20	0683-2205	9		RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R21	0683-2205	9		RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R22	0683-2205	9		RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R25	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R26	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R27	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R28	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R29	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R30	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R31	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R32	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R33	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R34	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R35	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R36	0683-1515	2		RESISTOR 150 5% .25W FC TC=-400/+600	01121	CB1515
R37	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R38	0683-2205	9		RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R39	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R40	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R41	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R42	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R44	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R51	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R52	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R53	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R54	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R55	0683-4735	4	1	RESISTOR 47K 5% .25W FC TC=-400/+800	01121	CB4735
R56	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R57	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R58	0683-4725	2	1	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R59	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R61	0683-5615	1	1	RESISTOR 560 5% .25W FC TC=-400/+600	01121	CB5615
R62	0686-2215	7	1	RESISTOR 220 5% .5W CC TC=0+529	01121	EB2215
R63	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R64	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R65	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R66	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R68	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R69	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R70	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R71	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R72	1810-0275	1		NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
R73	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R74	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R75	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R76	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R77	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R78	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R79	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R80	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R81	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R82	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R83	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R84	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
TP1-						
TP19	0360-0124	3	19	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
U14	1820-1441	6	3	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U15	1820-1445	0	3	IC LCH TTL LS 4-BIT	01295	SN74LS375N
U16	1820-1438	1	7	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U17	1820-1432	5	6	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U18	1820-1997	7	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U19	1820-1457	4	2	IC SHF-RGTR TTL S D-TYPE PRL-IN PRL-OUT	01295	SN74S299N
U21	1816-0724	7	6	IC TTL S 64-BIT STAT RAM 35-NS 3-S	01295	SN74S189N
U22	1816-1472	4	1	IC TTL S 256-BIT ROM 50-NS 3-S	34371	HM3-7603-5 PROGRAMMED
U23	1820-1858	9	5	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U24	1816-0724	7		IC TTL S 64-BIT STAT RAM 35-NS 3-S	01295	SN74S189N
U25	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U26	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U28	1820-1112	8	7	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U28	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U29	1820-1457	4		IC SHF-RGTR TTL S D-TYPE PRL-IN PRL-OUT	01295	SN74S299N
U31	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U32	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U33	1816-0724	7		IC TTL S 64-BIT STAT RAM 35-NS 3-S	01295	SN74S189N
U34	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U35	1820-1445	0		IC LCH TTL LS 4-BIT	01295	SN74LS375N
U36	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U37	1820-1430	3	3	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U38	1820-2024	3	7	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U39	1820-1298	1	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS251N
U41	1820-1240	3	2	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U42	1816-1471	3	1	IC TTL S 256-BIT ROM 50-NS 3-S	34371	HM3-7603-5 PROGRAMMED
U43	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U44	1816-0724	7		IC TTL S 64-BIT STAT RAM 35-NS 3-S	01295	SN74S189N
U45	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U46	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U47	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U48	1820-1987	5	2	IC SHF-RGTR TTL LS COM CLEAR STOR 8-BIT	01295	SN74LS299N
U49	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U51	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U52	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U53	1816-0724	7		IC TTL S 64-BIT STAT RAM 35-NS 3-S	01295	SN74S189N
U54	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U55	1820-1445	0		IC LCH TTL LS 4-BIT	01295	SN74LS375N
U57	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U58	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U59	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U61	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U62	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U63	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U64	1816-0724	7		IC TTL S 64-BIT STAT RAM 35-NS 3-S	01295	SN74S189N
U65	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U66	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
U66	1820-1303	9	5	IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U67	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U68	1820-1199	1	4	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U69	1820-1449	4	5	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U71	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U73	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U74	1820-1367	5	3	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U75	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U76	1820-1453	0	4	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U77	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U78	1820-0693	8	7	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U79	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U81	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U82	1820-1201	6	4	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U83	1820-1208	3	3	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U84	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U85	1820-0681	4	5	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U86	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U87	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U88	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U89	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U91	1820-1202	7	3	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U94	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U95	1820-1202	7	5	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U96	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U97	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U98	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U99	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U110	5081-2705	3	24	16K RAM	28480	5081-2705
U111	5081-2705	3		16K RAM	28480	5081-2705
U112	5081-2705	3		16K RAM	28480	5081-2705
U113	5081-2705	3		16K RAM	28480	5081-2705
U114	5081-2705	3		16K RAM	28480	5081-2705
U115	5081-2705	3		16K RAM	28480	5081-2705
U116	5081-2705	3		16K RAM	28480	5081-2705
U117	5081-2705	3		16K RAM	28480	5081-2705
U118	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U120	1820-1319	7	2	IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S151N
U122	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U123	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U124	1820-1319	7		IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S151N
U210	5081-2705	3		16K RAM	28480	5081-2705
U211	5081-2705	3		16K RAM	28480	5081-2705
U212	5081-2705	3		16K RAM	28480	5081-2705
U213	5081-2705	3		16K RAM	28480	5081-2705
U214	5081-2705	3		16K RAM	28480	5081-2705
U215	5081-2705	3		16K RAM	28480	5081-2705
U216	5081-2705	3		16K RAM	28480	5081-2705
U217	5081-2705	3		16K RAM	28480	5081-2705
U218	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U220	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U221	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U222	1820-1195	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U223	1820-0618	7	1	IC BFR TTL NON-INV HEX	01295	SN7417N
U224	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U310	1820-1216	3	3	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U311	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U312	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U313	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U314	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U315	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U316	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U317	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U318	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U319	1820-1303	9		IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U320	1820-1303	9		IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U321	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U322	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U323	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U324	1820-1303	9		IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U410	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U411	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U412	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U413	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U414	1820-1076	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG CLEAR	01295	SN74S174N
U415	1820-1196	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U416	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U417	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U418	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U421	1820-2373	5	1	IC-NAT 8367 CRT C	28480	1820-2373
U423	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U424	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U425	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U510	1820-1238	9	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U511	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U512	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U513	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U514	1820-1303	9		IC SHF-RGTR TTL S R-S PRL-IN PRL-OUT	01295	SN74S195N
U515	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U516	1820-1987	5		IC SHF-RGTR TTL LS COM CLEAR STOR 8-BIT	01295	SN74LS299N
U517	1820-1206	1	2	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U518	1820-2416	7	3	IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U519	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U520	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U525	1820-1206	1		IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U610	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U611	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U612	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U613	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U614	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U615	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U616	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U617	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U618	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U619	1820-2416	7		IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U620	1820-2416	7		IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U621	1820-0990	8	2	IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U622	1820-0509	5	2	IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U623	1820-0509	5		IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U624	1820-0990	8		IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U625	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U710	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U711	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U712	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298
U714	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U715	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U717	5081-2705	3		16K RAM	28480	5081-2705
U718	5081-2705	3		16K RAM	28480	5081-2705
U719	5081-2705	3		16K RAM	28480	5081-2705
U720	5081-2705	3		16K RAM	28480	5081-2705
U721	1820-2577	1	2	IC-SYP 6551 ACIA	28480	1820-2577
U722	1820-2577	1		IC-SYP 6551 ACIA	28480	1820-2577
U724	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U810	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U811	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U814	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U815	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U817	5081-2705	3		16K RAM	28480	5081-2705
U818	5081-2705	3		16K RAM	28480	5081-2705
U819	5081-2705	3		16K RAM	28480	5081-2705
U820	5081-2705	3		16K RAM	28480	5081-2705
U911	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U921	1818-0708	1	1	IC CMOS 1024 (1K) STAT RAM 650-NS 3-S	S0545	UPD5101LC
W2	8159-0005	0	2	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W5	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
XU22	1200-0607	0	26	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU42	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU110	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU111	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU112	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU113	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU114	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU115	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU116	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU117	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU210	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU211	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU212	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU213	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU214	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU215	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU216	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU217	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU419	1200-0541	1	7	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU421	1200-0654	7	2	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU518	1200-0639	8	3	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU619	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU620	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU621	1200-0638	7	4	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
XU622	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
XU623	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
XU624	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
XU712	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU717	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU718	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU719	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU720	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU721	1200-0567	1	2	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
XU722	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
XU817	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU818	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU819	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU820	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU912	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU912	1200-0612	7	1	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
XU913	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU915	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU916	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU918	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU919	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
Y1	0410-1224	3	1	CRYSTAL-QUARTZ 25.7715 MHZ HC-25/U-HLDR	28480	0410-1224
	1200-0546	6	1	SOCKET-XTAL 2-CONT HC-25/U DIP-SLDR	28480	1200-0546
	1390-0104	3	4	FASTENER-SNAP-IN GROM PANEL THKNS	28480	1390-0104
	1390-0281	7	4	FASTENER-SNAP-IN PLGR PANEL THKNS	28480	1390-0281

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
S0545	NIPPON ELECTRIC CO	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
03508	GE CO SEMICONDUCTOR PROD DEPT	AUBURN	NY	13201
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11961	SEMICON INC	BURLINGTON	MA	01803
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH	NC	27604
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34371	HARRIS SEMICON DIV HARRIS-INTERTYPE	MELBOURNE	FL	32901
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247