HEWLETT PACKARD

SPECIFICATION CONTROL DRAWING

This page provides a consequential record of changes for a multi-page drawing. Each "Revision Description" shall also include the appropriate page number(s). The change on the numbered page(s) shall be indicated with the new revision letter enclosed in a delta symbol, e.g., △B. (The term, "Extensive Changes" may be entered if the loss of history is acceptable). All pages of this drawing shall carry the same revision letter as shown on this page.

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HEWLETT PACKARD

SYSTEM DEVICE CONTROLLER

MICROPROCESSOR FIRMWARE

THEORY OF OPERATION

FOR

PART NUMBER

1820-4784

REVISION B

This is from the file INTEL.ERS.TEXT

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See Pg. 1 for Revs

1.1 INTRODUCTION

This document describes the operation and usage of the 8042 which implements the functions of the HP-HIL interface, the battery backed real time clock, system timers, user timers and the sound generator.

1.2 REVISIONS

This document is for Intel code 1820-4784 Rev B. The change in code from Rev A to Rev B consisted of a two instruction line change where the configuration register (R11) is set to 30 h during the reconfiguration process. Nothing else changed.

1.3 CAPABILITIES

The HP-HIL interface, real time clock, battery backed clock, system timers, user timers and sound generator are controlled by the same processor, an Intel 8042. A brief description of the overall capabilities is listed below:

1.4 THE HP-HIL INTERFACE

The HP-HIL (HP- Human Interface Loop) is used to connect up to 7 peripheral devices generally associated with the human interface to the host computer.

Usually the system keyboard and graphics locater will be connected thru this interface. There is code in the 8042 which controls the loop and makes an ITF keyboard compatible with old boot ROMs etc. The HIL Nimitz keyboard has been added to this version of the code.

1.5 REAL TIME CLOCK

The real time clock keeps real time in milliseconds since midnight and days since January 1. All functions of the real time clock have 10 msec. resolution and an accuracy of 12 msec.

1.6 THE BATTERY BACKED CLOCK

A communications interface to the battery backed real time clock (BBRTC) is provided thru the 8042 to reduce the hardware requirements for this feature. All communications to the BBRTC are controlled by the host processor with the 8042 acting as a "buffer".

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1.7 SYSTEM TIMERS

There are three system timer functions provided. They are listed below:

10 mS PERIODIC INTERRUPT - This is a maskable timer intended for system timing functions.

FAST HANDSHAKE DELAY TIMER - This is a a programmable delay which generates an interrupt on on level 7 (NMI). It is intended for the implementation of system time-out functions.

HP-HIL TIMEOUT INDICATION - This timer is used when the system sends data or commands to the HP-HIL interface for loop error detection.

1.8 USER TIMERS

There are three special purpose timers that the user can program to generate an interrupt. These timer functions are:

MATCH TIMER - Generates an interrupt if the match time setup matches the real time mS field (does not match on days).

DELAY TIMER - Generates an interrupt after a programmable delay of up to 1.94 days with 10 mS resolution (3 bytes).

CYCLE TIMER - Generates a programmable periodic interrupt with a maximum interval of 1.94 days and 10 mS resolution.

1.9 THE BEEPER

The beeper has been enhanced to include four independent voices three of which have programmable tone, the fourth is a noise generator. Each of the voices have programmable volume and duration. In addition to the aformentioned timers there are 5 timers associated with the beeper.

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2.1 INTERRUPT ADDRESS LOCATION

The 8042 will normally interrupt on level 1. When an interrupt occurs, the status register should be read. **The data buffer must be read even if the status register indicates that it contains no useful data.** The 8042 status is accessed by reading memory location 428003. The data buffer is accessed by reading memory location 428001. Data is sent to the 8042 by writing to memory location 428001 and a command is sent by writing to memory location 428003.

2.2 INTERRUPT STATUS REGISTER

When an interrupt is requested by the 8042 the most significant four bits of the status register are used to define the type of interrupt. The following defines the status register contents:

0000XXXX - Not used.

0001XXXX - The interrupt is a 10 msec. periodic interrupt.

0010XXXX - The interrupt is from one of the special purpose timers.

0011XXXX - There is both a special purpose timer interrupt and a 10 msec. periodic interrupt.

0100XXXX - The data buffer contains a byte of data that the 68000 has requested.

0101XXXX - The data buffer contains a STATUS CODE associated with the HP-HIL interface.

0110XXXX - The data buffer contains a byte of DATA associated with the HP-HIL interface.

0111XXXX - Power-up reset and selftest was completed successfully.

1000XXXX - The data buffer contains a key (both shift and control).

1001XXXX - The data buffer contains a key (only control).

1010XXXX - The data buffer contains a key (only shift).

1011XXXX - The data buffer contains a key (no shift or control).

1100XXXX - The data buffer contains an RPG count (both shift and

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control).

1101XXXX - The data buffer contains an RPG count (only control).

1110XXXX - The data buffer contains an RPG count (only shift).

1111XXXX - The data buffer contains and RPG count (no shift or control).

2.3 NMI INTERRUPTS

In the case of an NMI (level 7 interrupt), the 8042 status register must be read to determine the type of NMI; the following is the definition of the status register:

xxxxx1xx - The NMI is a fast-handshake interrupt.

xxxxx0xx - The NMI was generated to indicate that the reset key was pressed.

It is possible to tell if the 8042 pulled on NMI by reading location 478005 and checking bit 1. If this bit is a one the 8042 has pulled on NMI. For real time interrupts the data buffer is defined as:

Bit 7 - If set, an on time match interrupt occurred.

Bit 6 - If set, a delay interrupt occurred.

Bit 5 - If set, a cycle interrupt occurred.

Bits 4:0 - If non-zero, an error occurred. This contains the binary number representing the number of cycle interrupts that were missed. (Any combination of bits 5, 6, or 7 can be set.)

2.4 INTERRUPT COMMUNCIATION

The 8042 may be used as a polled device rather than an interrupting device by checking bit zero of the status register. When this bit is one it means that the 8042 is interrupting.

Before a command or data can be written to the 8042 the status register must be read to determine if the IBF flag, bit 1, is zero. If bit 1 is one, the transfer cannot take place. When data is asked for an interrupt will occur. This interrupt cannot be masked.

When a command is sent to the 8042 it cannot be considered carried out until the input buffer full flag (bit 1 of the status register) has been cleared.

by reading status then data

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3.1 POWER UP RESET

There are two types of RESET recognized by the 8042, the power up reset and the "hard" reset. The following occurs at power up:

A selftest is performed to verify operation of the 8042.

The output FIFO is cleared.

All voices of the sound generator are turned off.

All timers are disabled.

The real time clock is cleared. ? what about the time ?

The repeat rate is set to infinite

The interrupt mask is set to 1FH.

The HP-HIL interface is configured.

The LPCTRL register is set to 17H.

The first keyboard is identified.

The language and configuration registers are setup.

The poll fault and reconfiguration counters are cleared.

The selftest result byte is output to the host.

If the HP-HIL interface does not configure, or no keyboard is found, the configuration code register will contain 30H indicating no keyboard present, the language register will contain 1F (ASCII). LPSTAT may be read to determine the integrity of the interface. The time between the power up reset and the selftest result being returned to the system may be as long as 300 ms. This time is determined by the maximum selftest time for a device on the HP-HIL interface (200 mS).

3.2 HARD RESET

A "hard" reset of the 8042 will result in the following:

The output FIFO is cleared.

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All voices of the sound generator are turned off.

All timers are disabled.

The interrupt mask is set to 1FH.

The LPCTRL register is set to 17H.

The selftest result byte is output to the host.

3.3 RESET COMMUNICATIONS

The 8042 decides if the reset is a result of power up or not depending on the contents of a few registers. If any one of these registers contains an incorrect code the complete power up sequence is executed. This may be forced by writing a zero to the "selftest result byte" listed above (cmnd EFH data 0) and then pulling down the reset line. Note this will clear the real time. Do not try to do this if bit 5 of the configuration register is 0.

In order to be sure that the 8042 does not lose real time when the 68000 does a reset command, the following must be done.

Send command 31 to the 8042. As usual do not send the command until the IBF flag is clear.

Wait for the command to be taken by checking the IBF flag (bit 1 of the status register must be zero).

Do the reset command within 100 micro-seconds.

When the 8042 is reset it will pull on interrupt level 1 and will continue to pull on it until about 20 micro-seconds after reset is released. This interrupt should not be serviced. Level 1 interrupts should not be enabled during a reset command and for 20 micro-seconds after the reset command. The status register will not indicate that the 8042 is interrupting at this time.

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4.1 INTRODUCTION

The 8042 command set can be divided into five major groups; load timer output buffer commands, data request commands, set-up commands (for data input), trigger commands (to initiate actions), and an interrupt mask command.

4.2 LOAD TIMER OUTPUT BUFFER COMMANDS

The timer output buffer commands are five commands that the 68000 can use to read the current values of the cycle interrupt timer, the fast handshake timer, and the real time clock. The output buffer is a bank of five registers that the 8042 uses to temporarily store the data that the 68000 has asked for. A list and description of the timer output buffer commands will now be presented.

Buffer order / contents
0 LSByte time
1
2 MSByte time
3 LSByte "day"
4
5 MSByte "day"

31 - Load the timer output buffer with the real time. The first three bytes will contain the number of 10 milliseconds since midnight. The next two bytes contain the number of days since time was set. The least significant byte of the time will be in the first location of the buffer and the most significant will be in the third location. The least significant byte of the day will be in the fourth byte of the buffer and the most significant in the fifth byte. Both the days and and the 10 msec. are given as positive true binary numbers.

36 - Load the timer output buffer with the fast handshake time. The first two bytes of the timer output buffer will contain the current value of the fast handshake timer. The least significant byte will be in the first buffer location and the most significant byte in the second location.

38 - Load the timer output buffer with the on time match value. The first three bytes of the timer output buffer will contain the match value. The least significant byte will be in the first buffer location and the most significant byte in the third location.

3B - Load the timer output buffer with the delay interrupt time. The first three bytes of the timer output buffer will contain the current value of the delay timer. The least significant byte will be in the first buffer location and the most significant byte in the third location.

3E - Load the timer output buffer with the cycle interrupt time. The first three bytes of the timer output buffer will contain the

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current value of the cycle timer. The least significant byte will be in the first buffer location and the most significant byte in the third location.

4.3 DATA REQUEST COMMANDS

The data request commands are used by the 68000 to access a byte of data from the 8042. These commands read data from the 8042. The following is a list and description of each of the data request commands.

00 - Load the data buffer with the current byte of 8042 RAM data and increment the RAM location counter. (for debugging) This will cause an interrupt.

04 - Load the data buffer with the interrupt mask. This will cause an interrupt.

11 - Load the data buffer with the configuration code. This will cause an interrupt.

12 - Load the data buffer with the language code. This will cause an interrupt.

13 - Load the data buffer with the first byte of the timer output buffer. This will cause an interrupt.

14 - Load the data buffer with the second byte of the timer output buffer. This will cause an interrupt.

15 - Load the data buffer with the third byte of the timer output buffer. This will cause an interrupt.

16 - Load the data buffer with the fourth byte of the timer out- put buffer. This will cause an interrupt.

17 - Load the data buffer with the fifth byte of the timer output buffer. This will cause an interrupt.

FX - Request a byte of data from any one of the top 16 registers in the 8042 RAM space. (more on this later)

4.4 SET-UP COMMANDS

The set-up commands are a group of commands that are used by the 68000 to initialize or set-up the 8042. These commands are as follows:

A0 - Set up to input the delay to start repeating. This command is followed by sending the delay. The number sent is the 2's complement representation of the required delay.

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A2 - Set up to input the repeat rate. This command is followed by sending the repeat rate to the 8042. The number sent is the 2's complement representation of the number of 10 msec. for the repeat rate. Sending zero means do not repeat.

A3 - Set up to input bell information. This command is followed by sending the duration (2's complement representation of of the number 10 msec.) and then sending the frequency f=(approx)81.38*number sent). The upper two bits of the frequency must be zero. If a beep.command is sent while an old beep is still going, the new beep will cancel the old beep. The old beep will continue until both data bytes are received for the new beep. A beep command can also interfere with a voice #3 tone in progress and visa versa. (shared hardware)

A6 - Set up to input the rate at which the RPG can interrupt. This command is followed by sending the rate. The number sent is the number of 10 msec. This is essentially a NOP as far as this part is concerned because all locaters return raw caravan information with a 20 mS rate.

AD - Set up to input the 10 msec. real time. This command is followed by three data bytes; which are sent least significant byte first and is the number of 10 ms since midnight. Time is counted from the time this command is received. The day count may be sent following the time data without sending the AF command.

AF - Set up to input the days real time. This command is followed by two data bytes that are sent least significant byte first.

B2 - Set up to input a fast handshake delay. This command is followed by two bytes, least significant byte first, that is the 2's complement representation of the number of 10 msec. to wait until interrupting. This interrupt will be on the NMI line. If this command is not followed by 2 bytes of data the first handshake interrupt will be cancelled.

B4 - Set up to input a real time match interrupt. This command is followed by three bytes, least significant byte first, that is the number 10 msec. since midnight to match on. If this command is not followed by three bytes of data the real time match interrupt will be cancelled. Any real time match interrupt should be cancelled when the real time is about to be changed. If half way thru changing the real time it matches, an interrupt will occur.

B7 - Set up to input a delay interrupt. This command is followed by three bytes, least significant first, which is the 2's complement representation of the number of 10 msec. to wait until interrupting. Time is counted after the last data byte is received. If this command is not followed by three bytes of data, the interrupt will be cancelled.

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BA - Set up to input a cycle interrupt. This command is followed by three bytes, least significant byte first, that is the 2's complement of the cycle time. Time is counted after the third byte is received. If this command is not followed by three bytes of data, the interrupt will be cancelled.

C1 - Reset the RAM data output pointer associated with the 00 command. (for debugging)

E0 - Setup to input data for the TI beeper, BBRTC, or host to HP-HIL data transfers.

EX - Setup to write one of the top 16 registers in the 8042 RAM space. (more on this later)

4.5 TRIGGER COMMANDS

The trigger commands initiate some action, an interrupt may or may not be generated as a result (command specific). The trigger commands are listed below:

C2 - WRITE BBRTC; Trigger command to transfer data from a buffer to the BBRTC.

C3 - READ BBRTC; Trigger command to read data from the BBRTC.

C4 - Trigger command to transfer data from a buffer to the beeper IC and initiate a "new" beep from one of the voices.

C5 - Trigger command to transfer data from a buffer to the HP-HIL interface. (Host to loop transfers).

4.6 SET INTERRUPT MASK COMMAND

The interrupt mask command is used to set the internal interrupt mask for the functions provided by the 8042. The following is a description of the interrupt mask command.

01xxxxxx - When the upper two bits of the command are 01 the lower five are the interrupt mask. Presently bit 5 is not defined but should be sent as a 0. The lower five bits are described below. (Masked means that the interrupt is disabled.) A one means to disable the interrupt, and a zero means to enable the interrupt.

Bit 0 - Mask the KEYBOARD, RPG, and HPHIL.

Bit 1 - Mask the RESET key.

Bit 2 - Mask the timer interrupt.

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Bit 3 - Mask the periodic system interrupt.

Bit 4 - Mask the fast handshake interrupt.

Bit 5 - Reserved, set to 0.

Dec 12 17:29:34 PST 1989

Read data
- 03
- 01
- 02
- 01
- 00
- 09
↓ 1 sec
- 09 - why?

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5.1 INTRODUCTION

This section describes communication with the HP-HIL interface and other functions provided by the 8042 peripheral processor in series 200/300 products. For the most part the interface was changed as little as possible from the previous series 200 definition. In fact the interface to the timers, real time clock and beeper have not changed at all. (excluding enhancements). The interface to the keyboard (on power up) is also nearly identical to the old definition with the only exceptions being changes in the keycodes returned. This is a result of the new (ITF) keyboard layout. The following is primarily a description of the enhancements added to handle the HP-HIL interface. This interface is capable supporting up to seven devices, such as graphics input, system ID roms, beepers, and other peripherals generally related to human input, as well as the system keyboard. For a complete description of the HP-HIL interface and data protocol refer to the documents listed in the "Reference documents" chapter at the end of this ERS. Enhancements to the software interface have also been added to accomodate the BBRTC and a tone generator having four independent voices capable of producing chromatic scales with independent volume control.

5.2 SERIES 300 ENHANCEMENTS

Two new status codes have been implemented to handle data transfers from HP-HIL devices to the system. Also new commands have been added to handle data transfers from the system to HP-HIL devices. These will be described below. The 8042 takes care of configuring the HP-HIL interface and error detection as well as some error correction. The 42 will generally have control of the loop and will be doing the required polling for data. The transfers from the 42 to the system will, in general, be on an interrupt basis. When data is returned from the loop in response to a poll, all of the data is read from Cerberus and put in an internal fifo before the host system is interrupted. Data transfers from this fifo to the host take approximately 150 uS per byte (50 for the host to respond to the interrupt and 100 for the 8042 to get the next data byte out).

5.3 INTERRUPT STATUS CODE 5X

When the 42 generates an interrupt with a status code of 5X the associated data byte will contain information describing what type of data is to follow (with status code 6X) and, if appropriate, the device address of the originator of the data to follow. The bits in this data byte are defined below:

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If BIT 7 is clear then:

BITS 0:2 - Contain the address to be associated with the data to follow.

BIT 3 - When set indicates that the data to follow is the command which caused the previous data bytes (if any) to be returned. This bit may be used as a data packet termination indicator.

BIT 4 - Indicates that the data to follow was returned in response to a poll command initiated by the 42 in auto-poll mode.

BITS 5:6 - Undefined.

If BIT 7 is set then:

there is some type of exception or error. The remainder of the byte should be interpreted as an "error code" defined as follows:

80H - Indicates that the loop has reconfigured successfully. (reconfiguration is complete).

81H - Indicates that there was a parity error, framing error or fifo overflow in response to a system initiated data or command transfer to the HP-HIL interface. No data will follow.

82H - Indicates that there was a loop timeout in response to a system initiated data or command transfer to the HP-HIL interface with a timeout interval setup. No data will follow.

84H - Indicates that the loop is being reconfigured. No data will follow.

5.4 STATUS CODE 6X

When the 42 generates an interrupt with a status code of 6X the associated data byte will contain data received (in sequence) directly from the HP-HIL interface. This data is to be associated with the most recently received info byte which was returned with status code 5X.

The HP-HIL info byte will be sent at the beginning and end of each data packet as well as whenever the data within a packet is to be associated with a new device address. The data packets are of variable length as defined by the HP-HIL interface protocol.

Whenever poll data (from a raw mode device) is received from the HP-HIL interface, the 8042 will interrupt the host and send the data packet. No commands are required from the host for this transfer. A data stream for a typical packet is shown below. This packet is the result of a mouse at loop address 2 sending X,Y data and a raw-mode keyboard at loop address 4 sending key data, both in the same poll interval.

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(STATUS and DATA are in HEX)

STATUS	DATA	MEANING
5X	12	Poll data from device 2
6X	02	Header, two coordinates returned
6X	00	X delta (0)
6X	FF	Y delta (-1)
5X	14	Poll data from device 4
6X	40	Header, keycodes, no coordinate data
6X	5A	The "A" key went down
5X	18	Packet terminator
6X	15	Poll command (5 bytes returned)

5.5 LOOP RECONFIGURATION

The HP-HIL interface may be reconfigured (automatically) for several reasons, most of which are listed below:

An uncorrectable loop error is detected, such as the loss of a poll command or a double parity fault. The most probable cause for this might be Electro Static Discharges to loop devices.

A device is removed from the loop by the user.

A device is added to the loop by the user.

The host system requests a loop reconfiguration.

The result of a loop reconfiguration is as follows:

The language code of the first keyboard found is put in the language code register.

The KBDSADR and NIMSADR registers are updated to indicate the current location of all keyboards on the loop.

Any auto-repeat in process is cancelled.

The shift and control keys are assumed up.

The LPSTAT register is updated.

The reconfigure counter is incremented.

If enabled (if bit 2 of the LPCTRL reg is set) the 8042 will inform the system of the loop reconfiguration.

If no keyboards are found the language code and configuration code registers are changed to their default values. Earlier versions of the system controller did not update the language and configuration

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codes to default values.

5.6 HOST TO HP-HIL DATA TRANSFERS

The HP-HIL protocol does not allow more than one command on the loop at a time, as a result data transfers from the host to the loop must adhere to a strict handshake protocol. There is a "Loop BUSY bit" (bit 2 of R2) which indicates to the host that the 8042 has a command on the loop. Data must not be transferred from the host to the loop when this bit is set. Also because the 8042 will put a poll command out every 20 mS when in auto-poll mode either auto-polling must be disabled or one must be certain of the timing of the data transfer out to the loop so as not to interfere with the polling. When auto-polling is disabled and error reporting is turned on the host has complete control of the HP-HIL interface.

Data is transferred to the loop by writing three bytes to a data buffer and sending a trigger. The first byte sent to the buffer will be written to R1 of Cerberus, The second byte sent will be written to R0 of Cerberus. The third byte will be used to initialize a timeout interval (timed by the 8042) so that the host may recognize a loop timeout. If this last byte is a 0 the timeout interval will be infinite otherwise the timeout interval will be the twos compliment of the number sent in 10's of milliseconds. (ie FE will yield a 20 ms timeout)

Sequence for transferring data from the host to the HP-HIL:

Disable auto-polling by clearing bit 0 of the LPCTRL register.

Enable error reporting if desired.

Wait for bit 2 (loop busy) of register 2 to clear.

Send the command E0 to point the data input pointer to the data buffer.

Send three bytes of data, the data input pointer automatically increments.

Send the trigger command C5 to cause data to be transferred to Cerberus and initiate the timeout.

If data from the loop is expected, wait for a status 5 interrupt indicating data from the loop is available or the loop timed out.

Do whatever.

Re-Enable auto-polling.

If the host to loop data transfers complete within 20 ms no polls will be missed. If not, the next poll will be delayed and may cause the loss of a keystroke or some other data supplied by an

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unbuffered peripheral.

5.7 DATA REQUESTS FROM WITHIN AN ISR

Care should be taken when requesting data from the 8042, particularly from within an ISR, as only one data request can be processed at a time. This can be a problem if a foreground program requests a data byte from the 42 and an interrupt driven background process initiates a request for data before the foreground process receives the data it requested. Data from one request must be accepted before another request is initiated. If a second data request is made before data from the first is accepted one of the requests may not receive data or (more likely) the data returned may be received out of order.

Care should also be taken when transferring data to the 8042. Data transfers to the 8042 all use the same data input pointer. All data to be transferred must be sent before a new command (which changes the data input pointer) can be sent. If, for instance, a foreground process began a multi byte transfer of data to the 8042 which was interrupted by a background process which also transfers data to the 42, the pointer would be modified by the interrupt process and any further data sent to the 42 by the foreground process would not go to the correct register. Be very careful here as the results are unpredictable.

5.8 KEYCODES

HP-HIL ITF and Nimitz keyboards return both up-stroke and down-stroke keycodes for up to 128 keys. To minimize changes in the operating systems and boot ROM the keyboard controller has the capability of mapping the only the HP-HIL ITF keycodes into the keycodes and protocol expected by the series 200 operating systems. At power up the default is to map all keyboards on the loop thru this protocol conversion algorithm. This protocol conversion (keyboard "cooking") can be selectively or collectively enabled or disabled for any or all keyboards on the loop. The functions provided by the protocol conversion are:

Map the ITF down-stroke keycodes into series 200 standard keycodes.

Block all ITF up-stroke keycodes (except for a few special keys).

Maintain the status of the Shift and Control keys and return the state of these keys with the mapped keycodes.

Implement the Auto Repeat function with programmable delay and repeat rate.

Implement the level 7 interrupt Reset function (Shift + Break).

The ITF number pad is recognized as a keyboard so that a standard ITF

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keyboard (with no number pad) and a separate number pad will act the same as the extended keyboard (which has a built in number pad). As a side effect inputs from all keyboard are "ORED" together and are indistinguishable by the system software. If an application requires the separation of data from keyboards at different HP-HIL addresses the keyboards must be enabled for "RAW mode" (HP-HIL protocol) data transfers which include the addressing information.

In the table below the keycodes returned for a mapped keyboard are listed in the two left most columns in both hex and decimal. The next column indicates if the key exists only on the ITF keyboard (I), only on the old style series 200 keyboard (N), or both (IN). The next column (IC) is the ITF keycode returned for keyboards in RAW mode (hex). The following column (NC) is the HIL Nimitz keycode for the down stroke, the up stroke is the same keycode with the LSB set. The next column is the keycap label. For a RAW mode keyboard the keycode listed is for the down-stroke, the up-stroke is the same keycode with the LSB set. Hence down-strokes are even and up-strokes are odd.

HEX	DEC	IN	IC	NC	KEY-LABEL	HEX	DEC	IN	IC	NC	KEY-LABEL
00	0				UNUSED	40	64	IN	20	80	np 1
01	1	I	7E		~ ,	41	65	IN	24	82	np 2
02	2	I	CA		| \	42	66	IN	28	84	np 3
03	3	I	3E		esc / del	43	67	IN	2E	86	np -
04	4				UNUSED	44	68	IN	10	88	np 4
05	5	I	0E		BREAK / RESET	45	69	IN	14	8A	np 5
06	6	I	9C		STOP	46	70	IN	18	8C	np 6
07	7	I	EA		SELECT	47	71	IN	2A	8E	np *
08	8	I	1E		np ENTER	48	72	IN	1A	90	np 7
09	9	I	4C		np TAB	49	73	IN	12	92	np 8
0A	10	I	4A		np K0 (BLANK1)	4A	74	IN	16	94	np 9
0B	11	I	42		np K1 (BLANK2)	4B	75	IN	22	96	np /
0C	12	I	46		np K2 (BLANK3)	4C	76	N		98	np E
0D	13	I	4E		np K3 (BLANK4)	4D	77	N		9A	np (
0E	14	I	DC		home ARROW	4E	78	N		9C	np)
0F	15	I	DE		PREV	4F	79	N		9E	np ^
10	16	I	EE		NEXT	50	80	IN	7C	A0	1
11	17	I	9E		ENTER / PRINT	51	81	IN	7A	A2	2
12	18	I	06		EXTEND (LEFT)	52	82	IN	78	A4	3
13	19	I	04		EXTEND (RIGHT)	53	83	IN	76	A6	4
14	20	I	A0		SYSTEM / USER	54	84	IN	74	A8	5
15	21	I	90		MENU	55	85	IN	72	AA	6
16	22	I	AC		CLR LINE	56	86	IN	70	AC	7
17	23	I	AE		CLR DISP	57	87	IN	B0	AE	8
18	24	IN	5E	30	CAPS LOCK	58	88	IN	B2	B0	9
19	25	IN	6E	32	TAB	59	89	IN	B4	B2	0
1A	26	N		34	K0	5A	90	IN	B6	B4	-
1B	27	IN	98	36	K1 (f1)	5B	91	IN	B8	B6	=
1C	28	IN	96	38	K2 (f2)	5C	92	IN	C6	B8	[
1D	29	IN	A2	3A	K5 (f5)	5D	93	IN	C8	BA	]
1E	30	IN	A4	3C	K6 (f6)	5E	94	IN	D6	BC	;
1F	31	IN	A6	3E	K7 (f7)	5F	95	IN	D8	BE	'
20	32	IN	94	40	K3 (f3)	60	96	IN	E2	C0	,

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21	33	IN	92	42	K4 (f4)	61	97	IN	E4	C2	.
22	34	IN	FA	44	DOWN ARROW	62	98	IN	E6	C4	/
23	35	IN	FC	46	UP ARROW	63	99	IN	F2	C6	SPACE
24	36	IN	A8	48	K8 (f8)	64	100	IN	C2	C8	O
25	37	N		4A	K9	65	101	IN	C4	CA	P
26	38	IN	F8	4C	LEFT ARROW	66	102	IN	D2	CC	K
27	39	IN	FE	4E	RIGHT ARROW	67	103	IN	D4	CE	L
28	40	IN	BC	50	INSERT LINE	68	104	IN	6C	D0	Q
29	41	IN	BE	52	DELETE LINE	69	105	IN	6A	D2	W
2A	42	N		54	RECALL	6A	106	IN	68	D4	E
2B	43	IN	CC	56	INSERT CHAR	6B	107	IN	66	D6	R
2C	44	IN	CE	58	DELETE CHAR	6C	108	IN	64	D8	T
2D	45	N		5A	CLEAR -> END	6D	109	IN	62	DA	Y
2E	46	IN	BA	5C	BACK SPACE	6E	110	IN	60	DC	U
2F	47	N		5E	RUN	6F	111	IN	C0	DE	I
30	48	N		60	EDIT / DISP FCTNS	70	112	IN	5A	E0	A
31	49	N		62	ALPHA / DUMP ALPHA	71	113	IN	58	E2	S
32	50	N		64	GRAPHICS / DUMP GRAPH	72	114	IN	56	E4	D
33	51	N		66	STEP / ANY CHAR	73	115	IN	54	E6	F
34	52	N		68	CLEAR LINE / CLEAR SCR	74	116	IN	52	E8	G
35	53	N		6A	RESULT / SET TAB	75	117	IN	50	EA	H
36	54	N		6C	PRT ALL / CLR TAB	76	118	IN	D0	EC	J
37	55	N		6E	CLR I/O / STOP	77	119	IN	E0	EE	M
38	56	N		70	PAUSE / RESET(*)	78	120	IN	38	F0	Z
39	57	IN	DA	72	ENTER (RETURN)	79	121	IN	36	F2	X
3A	58	N		74	CONTINUE	7A	122	IN	34	F4	C
3B	59	N		76	EXECUTE	7B	123	IN	32	F6	V
3C	60	IN	2C	78	np 0	7C	124	IN	30	F8	B
3D	61	IN	48	7A	np .	7D	125	IN	F0	FA	N
3E	62	IN	1C	7C	np ,	7E	126	I	3A		META (LEFT)
3F	63	IN	26	7E	np +	7F	127	I	F6		META (RIGHT)

RESET(*): Reset on the HIL Nimitz will return 70h when down by itself, but will return 0Eh when either shift key is down (and 71 on the up stroke). The 0E is trapped by the Intel processor and turned into an NMI to the main processor. Control Shift and Reset down keys will generate a HIL command System Hard Reset (FBh) in addition to transmitting a poll response for each key.

Keycodes with the MSB set were not used in the previous series 200 implementation. Some of these codes have now been defined for special keys and keys unique to the ITF and HIL Nimitz keyboard. These new keycodes are listed below:

HEX	DEC	IN	IC	NC	KEY-LABEL
--	--	I	0C	0C	CTRL
--	--	I	0A	0A	SHIFT (RIGHT)
--	--	I	08	0A	SHIFT (LEFT)
92	146	I	07		EXTEND CHAR (RIGHT) UP

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93	147	I	09	EXTEND CHAR (LEFT) UP
FE	254	I	3B	META (LEFT) UP
FF	255	I	F7	META (RIGHT) UP

The following keys are unique to the "compressed" ITF keyboard.

81	129	I	44	3 / PREV
82	130	I	00	5 / +CHAR
83	131	I	40	6 / -CHAR
84	132	I	9A	8 / +LINE
85	133	I	AA	9 / -LINE
86	134	I	F4	. / NEXT

The following keys do not presently exist on any ITF or Nimitz keyboards. The ITF has matrix locations defined.

A9	169	I	5C	NOT NAMED
AA	170	I	E8	NOT NAMED
AB	171	I	EC	NOT NAMED
B0	176	I	80	BUTTON 0
B1	177	I	82	BUTTON 1
B2	178	I	84	BUTTON 2
B3	179	I	86	BUTTON 3
B4	180	I	88	BUTTON 4
B5	181	I	8A	BUTTON 5
B6	182	I	8C	BUTTON 6
B7	183	I	8E	PROXIMITY

The RAW mode BUTTON codes are the same as the codes returned for buttons on a locater device such as the mouse or a tablet.

If a keyboard contains a locater device such as a KNOB or a Joystick the positioner information will be returned as for a raw mode positioner, independent of whether the keyboard is in cooked or raw mode. The associated address will, of course, be that of the keyboard.

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6.1 INTRODUCTION

A CMOS RTC chip MSM-58321 sourced by OKI (or EPSON) is connected thru the 8042 to the host processor. The 8042 interface to this part allows (indirect) RTC register read and write operations. The existence of the battery backed real time clock (BBRTC) is indicated by a bit in the 8042 extended configuration register. Normally the battery backed time will be used only to initialize the standard real time clock implemented in the 8042. System software is required to do the format conversion from the way data is stored in the battery backed clock to the way data is stored in the 8042.

6.2 SOFTWARE INTERFACE

Data is sent to the BBRTC by first writing it to a buffer register (at address 70, command E0) in the 8042 and then sending a trigger command (C2) to the 8042 to cause the data to be transferred to the BBRTC. The RTC chip has 16 registers and accepts 4 bit data. The data byte sent to the buffer in the 8042 must contain the register address of the RTC chip in the lower nibble and the data to be transferred in the upper nibble. The write may be considered complete when the input buffer full bit of the 8042 clears after the trigger command is sent.

Data is read from the BBRTC by first writing the address of the BBRTC register to be accessed to the buffer register (same as above) and then sending a trigger command (C3) to the 8042 to cause a read of the BBRTC. The address must be in the lower nibble, with the upper nibble 0. The data will be returned to the system via the standard interrupt mechanism of the 8042 with a status code of 4X (data requested).

The buffer register address in the 8042 is 70H (same buffer is used for beeper data and HPHIL data transfers). The command used to address this buffer register for a write operation is E0.

Remember that all of the uninteruptable sequence business for multi byte data transfers to the 8042 applies here and must be observed.

6.3 REGISTER DEFINITIONS

The time data is stored in the RTC chip in 16 four bit registers as Hour, Min, Sec, Month, Day, Year. The register layout and definitions are shown in the table below:

RTC REGISTER DEFINITIONS

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FUNCTION	ADDRESS	RANGE	NOTES
SEC LSD	0	0..9	WHEN MSD OF HOURS IS SET:
SEC MSD	1	0..5	D3 = 1 FOR 24 HOUR FORMAT
MIN LSD	2	0..9	D2 = 0 FOR AM, OR 24 HOUR MODE
MIN MSD	3	0..5	
HR LSD	4	0..9	
HR MSD	5	0..2	
DOW	6	0..6	DAY OF THE WEEK
DAY LSD	7	0..9	
DAY MSD	8	0..3	WHEN MSD OF DAY IS SET D3 & D2
MO LSD	9	0..9	DEFINE THE LEAP YEAR SELECTION
MO MSD	A	0..1	D3 | D2 | YEAR/4 REMAINDER
YR LSD	B	0..9	---|----|----------
YR MSD	C	0..9	0 | 0 | 0 (WESTERN)
RST PS	D		0 | 1 | 3 (JAPANESE)
RESERVED	E		1 | 0 | 2
RESERVED	F		1 | 1 | 1

It is not possible to "stop" the counters in the RTC for a read operation and the part contains no capture buffer. The result of this is that a counter overflow may occur during a read causing incorrect data to be returned. The solution to this problem is to read the data twice and compare for equivalence. If the same data is read twice in a row it is guaranteed to be correct. Note all registers in a complete time string must be compared as an overflow between register reads may cause an error.

To avoid this problem when the part is written the following sequence should be observed: First write register D of the OKI part to reset the prescaler in the BBRTC, this insures that no register overflow will occur for at least 1 second. All registers must be written within this interval. It may be desirable to check the data after the write to insure the data integrity.

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7.1 INTRODUCTION

The sound generator electronics include a TI SN76494 four voice sound generator IC and linear amplifier. Three of the four independent voices produce square wave tone outputs. The fourth voice is a semi-programmable noise source. Each voice has an independent volume control with 30 db of dynamic range (in 2 db increments), and an independent duration timer (implemented in the 8042) which allows for timed durations of up to 2.5 seconds in 10 mS increments.

The interface thru the 8042 to the SN76494 is essentially a pass thru to the device except for the duration timers which exist in the 8042. Data is transferred to the 76494 by writing four bytes to a data buffer and sending a trigger. When the trigger is received the first three bytes sent to the buffer will be written directly to the 76494 in sequence. The fourth byte sent to the buffer is used to initialize a duration timer for the appropriate voice. To write to the data buffer the data input pointer must be set up by sending the command E0 (hex). The beep trigger command is C4 (hex). Note that the data buffer is the same as the one used to transfer data out to the HP-HIL interface. The same precautions about sending the data bytes associated with a command in an uninterruptable sequence applies here.

The data format required is rather complicated because it includes the addressing information required by the 76494 for register and voice identification. The first two bytes define the frequency of the tone (10 bits) and the third byte determines the attenuation of the tone (four bits). The duration timer number (voice association) is determined from the addressing information supplied in the attenuation byte. The frequency of a tone may be calculated from the function F=83333/N where N is the 10 bit number sent in the combination of the two frequency bytes. (83333 Hz is the rate of the clock supplied to the part).

7.2 CONTROL REGISTERS

The SN76494 has 8 internal registers which are used to control the 3 tone generators and the noise source. During all data transfers to the part the first byte contains a three bit field which determines the destination control register. The register address codes are shown below:

R2	R1	R0	DESTINATION CONTROL REGISTER
0	0	0	Tone 1 Frequency
0	0	1	Tone 1 Attenuation

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0	1	0	Tone 2 Frequency
0	1	1	Tone 2 Attenuation
1	0	0	Tone 3 Frequency
1	0	1	Tone 3 Attenuation
1	1	0	Noise Control
1	1	1	Noise Attenuation

7.3 DATA FORMAT

In the table below the four bytes required to initiate a tone from one of the voices are detailed. There are four fields defined by the bit designators R0-R2, F0-F9, A0-A3, and D0-D3.

R0-R3 - Is the register address field. As described above.

F0-F9 - Is the frequency determination field. (F0 = LSB)

A0-A3 - Is the attenuation determination field. (A0 = LSB)

D0-D7 - Is the duration field. (D0 = LSB)

A 1 or 0 in a bit position indicates a mandatory bit value.

Byte 1:	(Frequency 1)	MSB-	1	R2	R1	R0	F3	F2	F1	F0 -LSB
Byte 2:	(Frequency 2)	MSB-	0	0	F9	F8	F7	F6	F5	F4 -LSB
Byte 3:	(Attenuator)	MSB-	1	R2	R1	R0	A3	A2	A1	A0 -LSB
Byte 4:	(Duration)	MSB-	D7	D6	D5	D4	D3	D2	D1	D0 -LSB

Note that there is no register identification in byte 2, the register used depends on the address field of byte 1.

If the attenuation field is 0 the resultant tone will have maximum volume. As the attenuation value is increased the volume decreases by approximately 2 db per count. A value of F (hex) in the attenuation field turns the tone off.

The duration of a tone is the value of the duration byte multiplied by 10 mS. Hence tones may be automatically timed from 10 mS to 2.55 Seconds in duration. A value of 0 for the duration byte turns the tone on indefinitely (it must then be terminated by the system). The system can determine if any voice has timed out by reading the contents of the voice timer registers. The timers count down from the initial value to 0. A value of 0 indicates the time interval has expired and the voice has been turned off. The commands to read the voice timer registers associated with each voice number are listed below.

F4 - Read voice #1 timer.

F5 - Read voice #2 timer.

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F6 - Read voice #3 timer.

F7 - Read voice #4 timer.

Using the noise source (voice 4):

Only one byte is required by the 76494 to setup the noise generator, however the interface thru the 8042 will send two (bytes one and two). Therefore when data is written to the noise control register it should be duplicated in both byte on and byte two of the data input buffer. The noise source also has associated attenuation and duration bytes which are controlled exactly as for the other voices.

The noise source is a shift register with an exclusive OR feedback network. Whenever the noise control register is changed, the shift register is cleared. The shift register will shift at one of four rates as determined by the two NF bits (described below). The fixed shift rates are derived from the clock input.

The noise control byte has the following layout.

MSB- 1 R2 R1 R0 0 FB NF1 NF0 -LSB

R2, R1, and R0 must of course be 1,1,0 respectively to select the noise control register. The other three bits control the characteristics of the noise generated as follows:

If FB is a 0 periodic noise is generated.
If FB is a 1 white noise is generated.

The two bits NF1 and NF0 control the noise generator shift rate as described in the table below:

NF1	NF0	SHIFT RATE
0	0	M/64
0	1	M/128
1	0	M/256
1	1	Uses tone generator 3 output

7.4 OLD BEEPER COMPATIBILITIES

For reverse compatibility the old beep command (A3) works just as in the other keyboard controller IC's used in series 200 products. This command causes a tone of the correct frequency and duration to be generated using voice #3 at maximum amplitude. The frequency of the old beep was given by F=81.38*n where n was a five bit number sent by the host system. The new frequencies available are given by F=83333/N where N is a 10 bit number. This means that the new tone generator is capable of a more chromatic scale with a greater dynamic

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range than the old beeper, but is not capable of producing exactly the same frequencies for a given beep command as those which were produced by the old hardware. The frequency generated is the one which is closest to the old beep frequency as possible given 10 bits of control.

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8.1 INTRODUCTION

These registers give the system information about the configruation of the system devices. The main two registers are the Configuration Register (R11) and Language Register (R12). There are additional registers refered to as high registers which were added in later versions of the system device controller that contain additional operating information. Refer to the next chapter for these registers.

8.2 CONFIGURATION REGISTER, R11

The configuration code registers may be read by the host at any time, but it is updated from the keyboard only at power up or after loop reconfiguration.

The bits of the configuration register are defined as indicated below:

Bit 0 - Keyboard code (see next section)

Bit 1 - Keyboard code (see next section)

Bit 2 - Reserved, always 0

Bit 3 - When set, N key rollover is implemented.

Bit 4 - Keyboard not present, reflects logic of J7. (0 = keyboard present).

Bit 5 - HP-HIL interface and extended configuration register present.

Bit 6 - 804X code revision identification bit.

Bit 7 - A one indicates there is an IDPROM present, accessable thru the keyboard controller. (always a zero for this part)

8.3 HP-HIL IDENTIFICATION

Operating system should read R11, bit 5 to determine if the controller supports HP-HIL or the non-HIL versions of the Series 200. If bit 5 is set, then HP-HIL is supported. If HP-HIL is supported, then the keyboard code can be interperted as listed in the next section. If bit 5 is cleared, then a different set of keyboard codes are supported for different keyboards.

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8.4 KEYBOARD IDENTIFICATION CODES

At present there are only two HIL keyboards which this processor recognizes and supports. They are identified by the following bit assignments. If there is not a keyboard connected at the time of configuration, then the default is 000 which is the ITF keyboard.

Bit 2	Bit 1	Bit 0	Description
0	0	0	ITF
0	0	1	reserved
0	1	0	98203C
0	1	1	reserved

8.5 REVISION IDENTIFICATION CODE

Six code revisions of 804X peripheral processors now exist for series 200/300 products. Since earlier versions of the System Controller did not have a REVID code, a read of the configuration register (Cmnd=11H) is required to identify the type of system controller. In this data byte bits 5 and 6 indicate the part revision. The six part types, their usage and identification is as follows: (part number, bit 6, bit 5, usage).

1820-2564 (00) Used in the 9826 and 9836 mainframes.

1820-3087 (00) Used in the 9816.

1820-3300 (10) Used in the 9816 and on the 34 board for the 9920.

1820-3712 (01) Used in the 9817 (Marbox) and on the '35 board for the 9920.

1820-4379 (01) Used in Bobcat, extended ID indicates BBRTC support.

1820-4784 (01) Used for all HPHIL series 200/300, includes HIL Nimitz.

The first two parts are identical in operation and no external distinctions need be made. If bit 5 is set there is an Extended Identification register (R7E) which can be read (command FE) to extract more information about implemented features. For the part described in this document it is sufficient to note that bit 5 being set indicates an HP-HIL type of interface.

8.6 LANGUAGE REGISTER (R12)

The language codes for the ITF keyboards are different than those for the Nimitz keyboard which are also for keyboards previously available on the series 200 machines. A table showing the available keyboard language options for the ITF and Nimitz keyboards and the the

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associated codes returned in the language register is given below. The Nimitz only support six language configurations.

NATIONALITY	LANGUAGE CODE (hex) ITF	NIMITZ
United States (USASCII)	1F	00
German	0F	02
United Kingdom	17	
French	1B	01
Katakana	1D	05
Latin Spanish	1E	04
Canadian English	07	
Italian	0B	
Dutch	0D	
Swedish	0E	03
European Spanish	13	04
Belgian (Flemish)	15	
Finnish	16	03
Swiss German	19	
Norwegian	1A	
Danish	1C	
Swiss French	03	
Canadian French	18	

If more than one keyboard is installed the language register will contain the language code for the first keyboard on the loop (lowest address).

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9.1 INTRODUCTIONS

There are many different types of registers available to the operating system. Many of them are accessable by specific commands while others are accessable by the command to read and write the top 16 registers in memory. This chapter deals only with the top 16 registers refered to as the high registers.

9.2 HIGH REGISTER LOCATIONS

New commands have been added to allow the host to directly read or write the TOP 16 bytes of R/W memory in the 8042. This space contains registers for control and status of the HP-HIL interface as well as buffer space for data transfers. The layout of the space is shown below:

ADDRESS	FUNCTION
(7) 0-3	General purpose data buffer. (four bytes)
4-7	Timers for the four voices of the sound generator
8	NIMSADR - Bit per address of HIL Nimitz keyboard
9	KBDSADR - Bit per address of "cooked" keyboards
A	LPSTAT - HP-HIL interface status
B	LPCTRL - HP-HIL interface control
C	Reserved (for testing)
D	Reconfigure counter
E	Extended Configuration Registere
F	Selftest result byte

9.3 REGISTER COMMUNICATION

The command to read one of the top 16 bytes in the 8042 is FX where X is the byte address (0 to F). An interrupt with status code 4X will be generated indicating the data byte is available. The command to write one of these locations is EX followed by a write to the data register with the data byte. The address for data input to the 8042 is automatically incremented after a data byte is received, so a buffer may be loaded by sequentially sending data after the initial address setup command. Of course the normal handshaking procedure must be observed throughout all the transfers from the host to the 8042.

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9.4 NIMSADR REGISTER

This register was added to identify only the HIL Nimitz keyboards, while KBDSADR will identify all HIL keyboards. The identification of the keyboard is simular to the KBDSADR register in that the bit position identified the device address of the keyboard. Clearing a bit in this register will cause the system to think that the keyboard is an ITF keyboard, assuming the associated bit in the KBDSADR register was not cleared. Clearing the Nimitz location bit in the KBDSADR register will place the keyboard in the "raw" mode as it will for the ITF keyboard.

9.5 KBDSADR REGISTER

Each bit in this register is associated with keyboards (or number pads) at specific addresses on the loop. If bit 0 is set there is a keyboard at address 1, if bit 6 is set there is a keyboard at address 7 etc. This register is used by the 8042 to determine which keyboards get data mapped and which have data passed straight thru as "raw mode" HP-HIL devices. At power up or any time the loop is reconfigured all keyboards on the loop are identified. The KBDSADR register is setup to reflect this configuration. The host system can clear bits in this register to allow "raw mode" access to individual keyboards. Note however that a reconfiguration of the loop for any reason will rewrite the register with current configuration information. Because of this if a system is using some keyboards in mapped mode and some in raw mode the reconfiguration information transfers should be enabled and the host must take appropriate action upon loop reconfiguration. The bit in LPCTRL which converts ALL keyboards on the loop to "raw mode" is not changed if the loop is reconfigured.

9.6 LPSTAT REGISTER

The register LPSTAT is used to determine the status of the HP-HIL interface and is layed out as follows:

BITS 0:2 - Contain a count of the number of devices on the loop.

BIT 3 - When set indicates that the loop has been successfully configured. This bit is set to 0 at the start of loop configuration.

BITS 4:6 - UNUSED

BIT 7 - When set indicates that reconfiguration was attempted but not accomplished. Reconfiguration attempts will continue indefinitely until the loop configures (At least one device must be found).

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9.7 LPCTRL REGISTER

The register LPCTRL is used to control the operation of the HP-HIL interface and is layed out as follows:

BIT 0 - AUTO-POLL

When one the 8042 will automatically poll the loop. Data will be returned to the host only if a device on the loop returns data in response to a poll. The host may disable auto-polling by setting this bit to a zero. The auto-poll rate is fixed at 50 Hz (20 mS intervals).

BIT 1 - DON'T REPORT LOOP ERRORS

When set the 8042 will not inform the host of parity, framing, fifo overflow or loop timeout errors discovered after a host initiated data transfer. This bit should normally be set the same as the auto-poll bit so the 8042 will handle errors while in auto-poll mode. If the 42 is not in auto-poll mode and this bit is a one any error discovered will result in a reconfiguration of the loop. In general the host should handle loop errors if the 42 is not in auto-poll mode.

BIT 2 - DON'T REPORT LOOP RECONFIGURATION

When set the 8042 will not inform the host if the loop is, for some reason, reconfigured. The loop will be reconfigured if an unrecoverable error is discovered while the 8042 is handling loop errors. If this bit is a zero the "loop being reconfigured code" (status 5X data 84) and "loop reconfigured code" (status 5X data 80) will be sent to the host at the beginning and end of loop configuration respectively.

BIT 3 - UNUSED

BIT 4 - COOK KEYBOARDS

When set, data from selected keyboards on the loop will be intercepted and translated to emulate the "old" series 200 keyboard keycodes and data transfer mechanism. If this bit is set to 0 data from all devices on the loop will be returned without modification (RAW mode).

BIT 5 - UNUSED

BIT 6 - UNUSED

BIT 7 - RECONFIGURE THE LOOP

The system can cause the loop to be reconfigured by setting this bit. The 8042 will reset the bit and proceed to

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reconfigure the HP-HIL interface loop. Note: In this case the "loop reconfigured" codes will not be sent.

9.8 LOOP RECONFIGURATION REGISTER

This register is incremented everytime the HIL is reconfigured. Refer to the section on loop reconfiguration in the chapter on HP-HIL Interface.

9.9 EXTENDED CONFIGURATION REGISTER

The bit pattern in this register can be considered to be an extension of the configuration register (at address 11H). It can be read by the command FE as described previously.

The Extended ID register (R7E) has the following bit definitions: Do not try to read this register if bit 5 of the configuration register is 0.

BITS 0-2 - Code revision ID (001 = 1820-3712, 010 = 1820-4379) (011 = 1820-4784)

BIT 3 - Four voice TI SN76494 beeper available. (when set)

BIT 4 - Reserved (defaults to 1).

BIT 5 - OKI battery backed real time clock (BBRTC) present. (when set)

BITS 6-7 - Reserved (default to 0).

9.10 SELFTEST RESULT REGISTER

The selftest was removed in the 1820-4784 version of the system device controller because of shortage of space. The expected results of a successful pass of the selftest (value 55H) are placed in the register. Refer to the chapter on controller reset for more information.

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10.1 REGISTER MAP

The following is a list and description of all of the registers in the 8042. Most of these registers are not accessable by the operation system. These definitions may change in later versions.

'R0' Scratch and pointer register.

'R1' Scratch and pointer register.

'R2' In use register, with each bit has the following meaning:

'Bit 0' When one, loop is in reset mode configuration process.

'Bit 1' Internal "loop busy" bit.

'Bit 2' External "loop busy" bit.

'Bit 3' When one, the fast handshake timer is being used.

'Bit 4' When one, the cycle timer is being used.

'Bit 5' When one, the delay timer is being used.

'Bit 6' When one, the match timer is being used.

'Bit 7' When one, the bell is on.

'R3' Scratch.

'R4' Mask register with each bit described below:

'Bit 0' When one, the keyboard and HP-HIL interface interrupts are masked.

'Bit 1' When one, the reset key is masked.

'Bit 2' When one, the user timer interrupts are masked.

'Bit 3' When one, the PSI is masked.

'Bit 4' When one, the fast handshake interrupt is masked.

'Bit 5' When one, it is time to auto-repeat the current output key.

'Bit 6' When one, the first time repeat delay has elapsed.

'Bit 7' When one, indicates current output key has repeated at

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least once.

'R5' Interrupt request register with the following bit assignments:

'Bit 0' State of the shift keys; 0=either shift key pressed, 1=not pressed.

'Bit 1' State of the control key; 0=pressed, 1=not pressed.

'Bit 2' When one, it is time to do a PSI.

'Bit 3' When one, it is time to do a user timer interrupt.

'Bit 4' State of left shift key. 0=pressed.

'Bit 5' When one, it is time to send the 68000 something it asked for.

'Bit 6' State of right shift key. 0=pressed.

'Bit 7' When one, it is time to do a fast handshake interrupt.

'R6' FIFO control and misc.

'Bit 0' When one, poll delay has elapsed.

'Bit 1' When one, Cerberus has data.

'Bit 2' When one, loop is in configuration mode.

'Bit 3' When one, loop is in fault detected mode.

'Bit 4' When one, a poll was sent as the last loop command.

'Bit 5' When one, indicates FIFO is NOT empty.

'Bit 6' When one, indicates FIFO is full

'Bit 7' When one, the loop timed out.

'R7' Keycode of the current output key. (0 if no key is down)

'R8' The 8042 stack.

'R9' The 8042 stack.

'RA' The 8042 stack.

'RB' The 8042 stack.

'RC' The 8042 stack.

'RD' The 8042 stack.

'RE' The 8042 stack.

See Pg. 1 for Revs

'RF' The 8042 stack.

'R10' Reset debounce counter.

'R11' Configuration jumper code.

'R12' Language jumper code.

'R13' Timer output buffer.

'R14' Timer output buffer.

'R15' Timer output buffer.

'R16' Timer output buffer.

'R17' Timer output buffer.

'R18' Scratch and pointer.

'R19' Scratch and pointer.

'R1A' Scratch, accumulator storage during interrupts etc.

'R1B' User timer output word (the bits are listed below).

'Bits 0-4 ' The number of cycle interrupts missed.

'Bit 5' When one, a cycle is up.

'Bit 6' When one, a delay is up.

'Bit 7' When one, there is a real time match.

'R1C' The current RPG count.

'R1D' The pointer register to store data sent by the 68000.

'R1E' The pointer register for data sent to the 68000.

'R1F' Six counter for 8042 timer interrupt.

'R20' Auto-repeat delay.

'R21' Auto-repeat timer.

'R22' Auto-repeat rate.

'R23' (old) Beep frequency.

'R24' Beep timer (counts up to zero).

'R25' RPG timer.

See Pg. 1 for Revs

'R26' RPG interrupt rate.

'R27' Bit 6 indicates that a timer interrupt occurred.

'R28' Not used.

'R29' Not used.

'R2A' Not used.

'R2B' Not used.

'R2C' Not used.

'R2D' LSB of time of day.

'R2E' Second byte of time of day.

'R2F' Third byte of time of day.

'R30' LSB of days.

'R31' Second byte of days.

'R32' LSB of fast handshake timer.

'R33' Second byte of fast handshake timer.

'R34' LSB of real time match.

'R35' Second byte of days.

'R36' Third byte of days.

'R37' LSB of delay timer.

'R38' Second byte of delay timer.

'R39' Third byte of delay timer.

'R3A' LSB of cycle timer.

'R3B' Second byte of cycle timer.

'R3C' Third byte of cycle timer.

'R3D' LSB of cycle timer save.

'R3E' Second byte of cycle timer save.

'R3F' Third byte of cycle timer save.

'R40 to R67' These bytes are used as a FIFO buffer. 40 bytes

See Pg. 1 for Revs

'R68' FIFO read pointer. 'R69' FIFO write pointer.

'R6A' Loop timeout counter.

'R6B' State counter for configuration state machine.

'R6C' Temp storage.

'R6D' Loop watchdog timer.

'R6E' Temp storage.

'R6F' AA if selftest completed.

'R70' Four byte buffer used for the TI beeper, OKI clock, & HP-HIL.

'R71' Four byte buffer used for the TI beeper, OKI clock, & HP-HIL.

'R72' Four byte buffer used for the TI beeper, OKI clock, & HP-HIL.

'R73' Four byte buffer used for the TI beeper, OKI clock, & HP-HIL.

'R74' Four bytes used for voice (beep) timers, Voice #1.

'R75' Four bytes used for voice (beep) timers.

'R76' Four bytes used for voice (beep) timers.

'R77' Four bytes used for voice (beep) timers.

'R78' NIMSADR Nimitz address map.

'R79' KBDSADR keyboard address map.

'R7A' LPSTAT HP-HIL interface loop status byte.

'R7B' LPCTRL HP-HIL interface loop control byte.

'R7C' Loop poll fault counter.

'R7D' loop reconfiguration counter.

'R7E' Extended configuration/ID register.

'R7F' 55 if selftest completed.

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11.1 HP-HIL DOCUMENTATION

Several documents are available which describe the protocol and capabilities of the HP-HIL interface. These documents should be referenced in regard to the processing of information from general HP-HIL devices. Of primary importance is:

HP-HIL Technical Reference Manual, Product No. 45918A

11.2 KEYBOARDS

The theory of operation documents for each of the other keyboard controllers which have been used in the series 200 and 300 may also be useful.

11.3 SOUND GENERATOR

More information about the sound generator IC may be obtained by referencing the TI data sheet for the SN76494N. Application notes for this part (published by TI) also exist. The title for one report is "A GUIDE TO USING THE TEXAS INSTRUMENTS SN76489A SOUND GENERATOR" notice the part number is different but the report is also applicable to the 76494.

11.4 BATTERY BACKED CLOCK

More information about the battery backed real time clock may be obtained from the data sheets published by OKI, EPSON, or STATEK for the RTC-58321 IC.

11.5 SOURCE CODE

This document, in a machine readable form, the source and object code for the bits in the 8042, and several other programs used for development of the 8042 software exists in specs on a 3.25" disc (S-1820-4784-1).

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